Impact of V_{th} Instability of Schottky-Type p-GaN Gate HEMTs on Switching Behaviors

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***Abstract*—Schottky-type p-GaN gate gallium nitride high electron mobility transistors suffer from threshold voltage (V_{th}) instability phenomenon. Both positive and negative V_{th} shifts are reported when device undertakes the voltage bias, but the impact of this V_{th} instability phenomenon on device switching behaviors is less investigated. In this study, the drain-source voltage (V_{ds}) induced bidirectional V_{th} shift in hard-switching condition is characterized and decoupled by an H-bridge based double-pulse test. Subsequently, the influence of V_{th} shift on switching behaviors is theoretically analyzed and demonstrated through SPICE simulation and experiment, showing how a positive shifted V_{th} can reduce the device turn-ON commutation speed and increase the switching losses, and vice versa. The results suggest that the V_{th} instability phenomenon should be considered in accurate switching modeling.**

***Index Terms*—Neural networks, power semiconductor devices, semiconductor device modeling, switching loss, threshold voltage.**

I. Introduction

GALLIUM nitride high electron mobility transistors (GaN-HEMTs) have been playing an increasing significant role in electrical energy conversion due to the low power losses and fast switching speed that is beneficial to high-efficiency and high power density converter design [1]. However, the GaN-HEMTs suffer from instability phenomena when undertaking drain to source voltage (V_{ds}) or gate to source voltage (V_{gs}) biases, mainly expressed as dynamic ON-state resistance (R_{ds}^{on}), current collapse, and threshold voltage (V_{th}) instability [2], [3], [4].

Among different gate technologies to achieving enhancement mode devices, p-GaN gate technology provides a good tradeoff between cost and reliability [5]. Ohmic- and Schottky-type p-GaN gate HEMTs are two kinds of commercialized power transistors. The stabilities of Ohmic-type devices are widely reported for both R_{ds}^{on} [6], [7], [8] and V_{th} [9], [10]. However, their stabilities come at the cost of current driving and high gate leakage current in mA level, which requires relative complicated gate circuit design and causes higher driving losses [6], [8], [11]. On the other hand, Schottky-type devices exhibit voltage driving characteristics and significantly suppressed gate leakage current, resulting in convenient application and low driving losses [8], [9], [10]. Therefore, Schottky-type GaN-HEMTs show considerable potential in high-efficiency power converter applications.

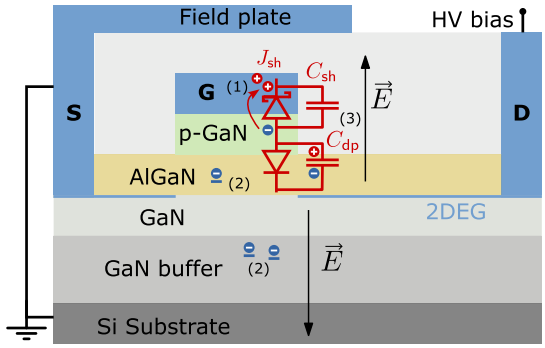

Fig. 1. Structure of Schottky-type p-GaN gate HEMTs under OFF-state high V_{ds} voltage bias and main mechanisms of V_{th} instability: (1) Holes emitted from p-GaN layer. (2) Trapped electrons in AlGaN or GaN buffer layer. (3) p-GaN potential is elevated by V_{ds} due to the in series C_{sh} and C_{dp}.

However, the Schottky-type devices suffer from V_{th} instability phenomenon that is mainly attributed to its "back-to-back" diode structure in gate stack, composed by the Schottky junction (gate metal/p-GaN) and PIN junction (p-GaN/AlGaN/GaN), as shown in Fig. 1. Here, three main mechanisms could be responsible for the V_{th} instability under high V_{ds} bias.

1) The PIN junction is in reverse bias, electrons in p-GaN are accumulated at the interface of p-GaN/AlGaN. Simultaneously, holes in p-GaN are emitted to gate electrode, but these holes cannot be recovered immediately after removing the V_{ds} bias, as the Schottky junction (J_{sh}) is in reverse bias. These unrestored holes cause hole-deficiency of p-GaN layer, leading to positive V_{th} shift [12], [13], [14].
2) Material growth defect or doping introduced acceptor-like traps in AlGaN and GaN buffer can capture electrons under high V_{ds} bias, leaving negative charged states. And these states can lead to positive V_{th} shift [15], [16].

Manuscript received 29 January 2024; revised 22 April 2024; accepted 19 May 2024. Date of publication 24 May 2024; date of current version 16 July 2024. This work was supported in part by the University of Lille, France, and in part by Coventry University, U.K. Recommended for publication by Associate Editor Y. Zhang. *(Corresponding author: Xuyang Lu.)*

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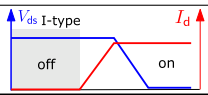
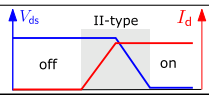
Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3405320.

Digital Object Identifier 10.1109/TPEL.2024.3405320

TABLE I
TWO TYPES OF V_{ds} BIAS RELATED V_{th} INSTABILITY

V_{ds} bias	I-type V_{ds} bias	II-type V_{ds} bias
V_{th} shift	positive [13], [14], [15], [16], [19], [20], [21]	negative [17], [18], [22], [23]
Mechanisms	(1) Hole-deficiency in p-GaN layer [12], [13], [14]; (2) Electron trapping in AlGaN layer and GaN buffer [15], [16]	(3) p-GaN potential is elevated by V_{ds} [17], [18]
Device state	off-state	switching commutation
Switching waveforms		

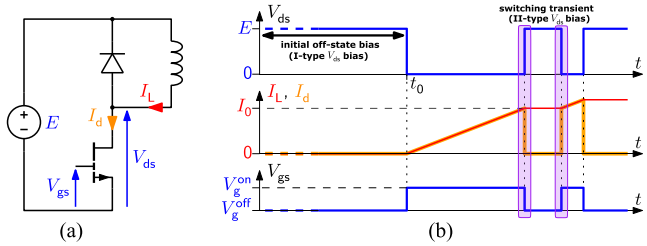


Fig. 2. Conventional DPT (a) schematic and (b) corresponding switching waveforms including the two types of V_{ds} bias.

3) The equivalent capacitors of the Schottky junction (C_{sh}) and PIN junction (C_{dp}) are in series. Here, the p-GaN potential can be elevated by a V_{ds} bias, reducing the energy barrier of the channel under the gate and resulting in a negative V_{th} shift [17], [18].

When using the device, it is crucial to consider when these mechanisms will occur, and whether the shifted V_{th} can impact device turn-ON and turn-OFF switching behaviors. The V_{ds} bias induced positive shift are reported when device is in OFF-state [13], [14], [15], [16], [19], [20], [21], and they could be explained by the aforementioned mechanisms (1) and (2). However, the device also undertakes high V_{ds} bias during the switching commutation transient in hard-switching, as depicted in the waveform diagram in Table I. During the turn-ON transient, the current rising stage is under high V_{ds}, and this voltage bias could cause negative V_{th} shift based on mechanism (3). This negative V_{th} shift is observed during the resistance load hard-switching transient in [22], and the negative V_{th} induced false turn-ON phenomenon is discussed in [23]. For conciseness, the OFF-state V_{ds} bias is defined as I-type V_{ds} bias, and the V_{ds} bias during switching commutation is defined as II-type V_{ds} bias in this study, as summarized in Table I. Consequently, the hard switching commutation transient could be influenced by these two types of V_{ds} bias induced reverse directional V_{th} shift.

In [14], [19], [20], and [21], the decreased dV_{ds}/dt and dI_d/dt in turn-ON switching transient are reported and attributed to the I-type V_{ds} bias induced positive V_{th} shift, but lacking of theoretical explanation. Moreover, the influence of II-type V_{ds} bias induced negative V_{th} shift on switching behavior are not sufficiently discussed in literature. Neglecting the V_{th} shift may lead to inaccurate evaluation of device switching losses and electromagnetic interference.

This study aims to investigate the influence of these two types of V_{ds} bias induced bidirectional V_{th} shift on device switching behaviors. The commercial GS66502B GaN-HEMTs are adopted as the research object [24]. The methodologies are given as follows.

1) To characterize the bidirectional V_{th} shift in hard-switching, the double-pulse test (DPT) is adopted. The schematics and switching waveforms of device under test (DUT) in conventional DPT are shown in Fig. 2. Both types of V_{ds} bias can be observed in the typical switching waveforms of DPT in Fig. 2(b). Furthermore, an H-bridge based DPT is implemented to control the I-type V_{ds} bias induced positive V_{th} shift by eliminating the initial OFF-state V_{ds} bias (before t_0). In this way, the switching waveforms and the corresponding I–V characteristics with and without the influence of I-type V_{ds} bias induced positive V_{th} shift can be obtained. Moreover, both of the extracted I–V characteristics include the II-type V_{ds} bias induced negative V_{th} shift, since they are extracted from the hard-switching transient under high V_{ds}.
2) To demonstrate the impact of V_{th} instability on switching behaviors, the relationship between dV_{ds}/dt, dI_d/dt, and V_{th} is deducted. Afterward, the obtained I–V characteristics including V_{th} instability are modeled and imported to SPICE device models. By comparing the simulation results and experiments with and without initial I-type V_{ds} bias, the influence of positive V_{th} shift can be verified. The impact of II-type V_{ds} bias induced negative V_{th} shift can be observed by comparing the simulation results under different V_{ds}.

It should be clarified that a 1 kΩ turn-ON gate resistor (R_g^{on}) is used to slow down the turn-ON switching transient for extracting the I–V characteristics, which is not a typical application case for GaN-HEMTs. The device V_{th} in this slowed hard-switching transient might be different with fast switching, due to the higher possibility of hot electrons trapping [25] and impact ionization [26]. Moreover, the dynamic R_{ds}^{on} phenomenon of the device might become serious due to this slowed down switching transient [25], [27], which could increase the conduction losses of the device. However, the objective of this work is purely to demonstrate the impact of V_{th} instability on switching behaviors. In fast switching, circuit parasitic inductance [28] and probe impedance [29] will all make it impossible to draw the conclusion if any difference observed, which will be investigated in future work.

The rest of this article is organized as follows. Section II theoretically analyses the influence of V_{th} shift on switching behaviors. In Section III, the I–V characteristics are constructed, where two types of V_{ds} bias induced V_{th} instability are considered. Afterward, SPICE models considering the obtained I–V characteristics are proposed to verify the impact of V_{th} instability on switching behaviors. Finally, Section IV concludes this article.

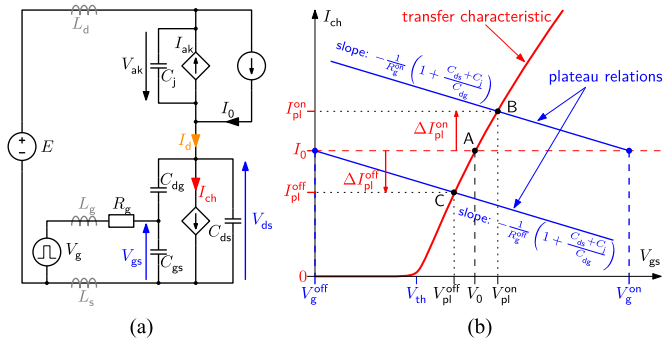


Fig. 3. Simplified analysis based on (a) switching cell model and (b) plateau voltage determination.

II. Impact of V_{th} Instability on the Turn-On and Turn-Off Switching Behaviors of Transistors

A simple model of the switching cell is depicted in Fig. 3(a) for analysing the typical hard switching transition, where the switched voltage and current are E and I_0, respectively. The diode is modeled as a voltage-controlled current source I_{ak} and a junction capacitance C_j, and the transistor is modeled as a channel current source I_{ch} and three interelectrode capacitances C_{gs}, C_{ds}, and C_{dg}. It is driven by a control voltage V_g and a gate resistance R_g. The ON/OFFgate control voltages are named V_g^{off} and V_g^{on}, respectively.

To simplify the analysis, parasitic drain, gate, and common source inductances are neglected and the interelectrode capacitances are assumed linear. Two situations depending on the existence of Miller plateau are analyzed at first in Sections II-A and II-B, which respectively corresponds to the slow and fast switching commutation cases. The expected impact of V_{th} instability on switching commutations is then analyzed in a more general case in Section II-C. The analysis in this section notably aims at highlighting the different impact of V_{th} instability between turn-ON and turn-OFF transitions.

A. Case I: With Miller Plateau Voltage

With the aforementioned hypotheses, Fig. 4 presents typical power transistor switching waveforms with Miller plateau (gate voltage V_{pl}^{on} and V_{pl}^{off} at turn-ON and turn-OFF, respectively) occurring during the V_{ds} transition. Since the commutation mostly occurs in the current saturation region of the output characteristics, it can be conveniently analysed in the I_{ch}–V_{gs} plane of transfer characteristics under high V_{ds} shown in Fig. 3(b), where the operating point moves along the device characteristics during the commutation process.

1) At turn-ON, current transition starts with V_{gs} rising until the (V_{gs}, I_{ch}) operating point reaches point A (V_0, I_0), corresponding to time t_2^{on} in Fig. 4(a). Then, the diode gets blocked (zero I_{ak}) and the plateau voltage is reached between t_2^{on} and t_3^{on}, corresponding to point B in Fig. 3(b), where V_{ds} drops due to $I_{ch} > I_0$ discharging of the DUT output capacitance $(C_{ds} + C_{dg})$ and charging of the diode junction capacitance C_j. Finally, the device conducts with low V_{ds} and the transfer characteristic is no longer relevant.

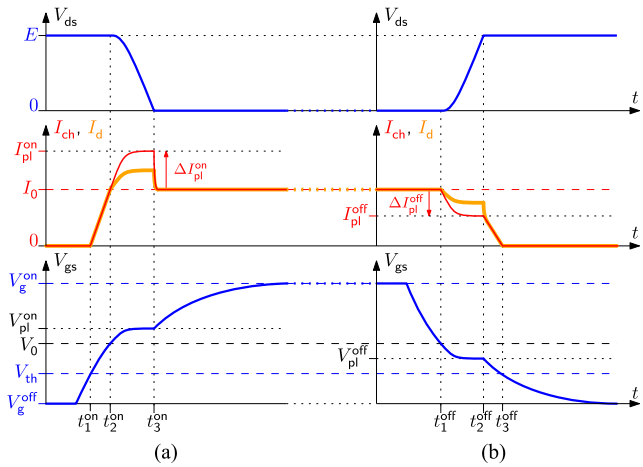


Fig. 4. Simplified commutation waveforms with Miller plateau (a) turn-ON (b) turn-OFF.

2) At turn-OFF, voltage transition starts around point A when the channel current gets smaller than I_0, so that the DUT output capacitance gets charged. The corresponding plateau voltage is reached at point C between t_1^{off} and t_2^{off} in Fig. 4(b). Once the diode becomes conducting at t_2^{off}, transistor current drops to zero with decreasing V_{gs}.

The current transition is obviously linked to the transfer characteristics according to the basic model

$$I_{ch} = g_m(V_{gs} - V_{th}) \quad , \quad V_{gs} > V_{th}. \tag{1}$$

The voltage transition, however, requires more analysis focusing on the plateau voltage. At the plateau, constant V_{gs} implies that V_{dg} and V_{ds} have the same time derivatives, such that

$$\frac{V_g - V_{gs}}{R_g} = -C_{dg}\frac{dV_{ds}}{dt}. \tag{2}$$

In addition, voltage variations are linked to the charge or discharge of the output C_{dg} and C_{ds} capacitances by $I_{ch} - I_d$, where I_d is the drain current

$$\frac{dV_{ds}}{dt} = \frac{I_d - I_{ch}}{C_{dg} + C_{ds}}. \tag{3}$$

Since parasitic inductances to the dc source E are omitted, V_{ds} and V_{ak} also have the same time derivatives, which yields

$$I_d = I_0 - C_j\frac{dV_{ak}}{dt} = I_0 - C_j\frac{dV_{ds}}{dt}. \tag{4}$$

Combining (2) to (4), I_{ch} and V_{gs} are linked by

$$I_{ch} = I_0 - \frac{V_{gs} - V_g}{R_g}\left(1 + \frac{C_{ds} + C_j}{C_{dg}}\right). \tag{5}$$

This "plateau relation" is plotted as straight lines in Fig. 3(b), passing through points (V_g^{on}, I_0) at turn-ON (respectively, (V_g^{off}, I_0) at turn-OFF) with a negative slope that depends on the gate resistance (R_g^{on} or R_g^{off}, respectively, if different) and power devices interelectrode capacitances. Note that C_j equals $C_{ds} + C_{dg}$, if an identical reverse-conducting GaN-HEMT is used as the diode. Thus, the operating point at the plateau (point

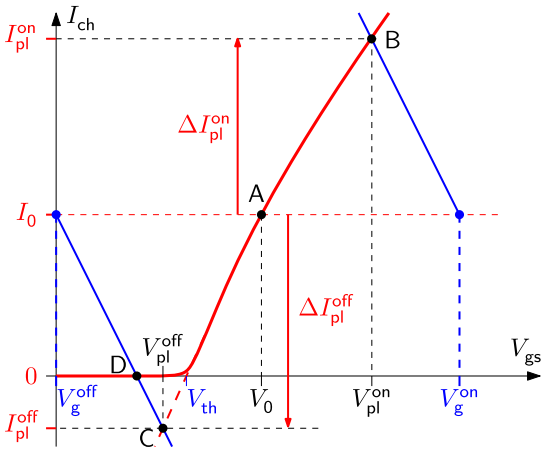


Fig. 5. I_{ch}–V_{gs} significant points for device commutation.

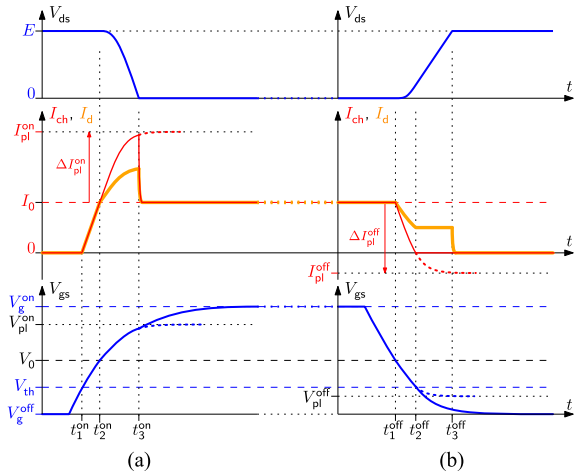


Fig. 6. Commutation waveforms without Miller plateau (a) turn-ON (b) turn-OFF.

B (V_{pl}^{on}, I_{pl}^{on}) at turn-ON and C (V_{pl}^{off}, I_{pl}^{off}) at turn-OFF) is obtained at the intersection of the the plateau relation with the DUT transfer characteristics.

Furthermore, the difference ΔI_{ch} between channel and load currents is a key parameter for voltage transition speed since (3) and (4) yield

$$\frac{dV_{ds}}{dt} = \frac{I_0 - I_{ch}}{C_{dg} + C_{ds} + C_j} = \frac{-\Delta I_{ch}}{C_{dg} + C_{ds} + C_j}. \tag{6}$$

Its value at points B and C is represented in Fig. 3(b) as ΔI_{pl}^{on} and ΔI_{pl}^{off}, respectively. Calculating the intersection of the plateau relation line with the transfer characteristic using (1), the voltage transition at the plateau can then be expressed as a function of V_{th}

$$-\frac{dV_{ds}}{dt} = \frac{g_m(V_g - V_{th}) - I_0}{g_m R_g C_{dg} + C_{ds} + C_{dg} + C_j} = f(V_{th}). \tag{7}$$

This equation shows how the V_{th} instability influences the voltage transition. Interestingly, it is easily verified that turn-on transition gets slower due to negative $^{df}/_{dV_{th}}$.

Finally, drain current is related to channel current from (4) and (6) by

$$\frac{I_d - I_0}{\Delta I_{ch}} = \frac{C_j}{C_{dg} + C_{ds} + C_j} \tag{8}$$

which equals $1/2$ if the diode is actually an identical GaN-HEMT (still considering linear capacitances). For this reason, the I_d curve in Fig. 4 has half the deviation of I_{ch} to I_0 during the voltage transitions.

B. Case II: Without Miller Plateau Voltage

The preceding analysis should be completed by considering that plateau voltages may actually not have time to be attained, due to the fast switching speed of GaN-HEMTs [30]. Indeed, with high C_{ds}/C_{dg} ratio and small R_g values, the slopes of the plateau relation lines in Fig. 3(b) increase so that the resulting crossing points move away as shown in Fig. 5.

At turn-ON, both current and voltage transitions are similar to the previous section, except that the "target" ΔI_{pl}^{on} is now much larger at point B. Consequently, as I_{ch} keeps increasing a lot beyond point A, V_{ds} voltage falls more and more rapidly and eventually reaches its final ON-state value before the pseudosteady state is reached. Thus, point B is not fully attained and the waveforms in Fig. 6(a) do not have time to stabilize in the $[t_2^{on}, t_3^{on}]$ interval (dotted lines after t_3^{on} show how they would have stabilized otherwise).

The turn-OFF transition is more impacted by the new slopes in Fig. 5, because the crossing point with the transfer characteristics is now at point D with zero channel current. Should the transconductance curve remain straight below V_{th} gate voltage, extending to negative I_{ch}, then the "target" pseudosteady state for the voltage transition would be at point C with a large negative ΔI_{pl}^{off}. Consequently, when voltage transition starts, the channel current rapidly drops to zero in Fig. 6(b). Thus, current transition is already finished in the channel at time t_2^{off} in Fig. 6(b) (dotted lines after t_2^{off} show how V_{gs} and I_{ch} would stabilize if current could become negative at point C). However, t_2^{off} is only the beginning of the voltage transition: afterward drain voltage rises up to E in the $[t_2^{off}, t_3^{off}]$ interval, under $\Delta I_{ch} = -I_0$ in (6). Thus, the drain current alone is merely charging the DUT output capacitance, resulting in a turn-OFFvoltage rising speed that only depends on the load current I_0. Similar behavior has been reported for various transistor technologies [31], [32], usually associated with low current switching. It suggests that V_{th} instability would not influence the turn-OFF commutation once the channel stops conducting.

C. Influence of V_{th} Instability on Switching Behaviors

The analysis from Figs. 5 and 6 can be combined with the I-type V_{ds} bias induced positive V_{th} shift to illustrate its effect on switching waveforms. Fig. 7 presents simple piecewise linear transfer characteristics defined by device V_{th} and g_m according to (1). Two curves are considered as follows.

1) *Unbiased* means that the DUT is not affected by the initial I-type V_{ds} bias. The corresponding curve (solid line) would be obtained when the device has zero initial V_{ds} bias. Thus,

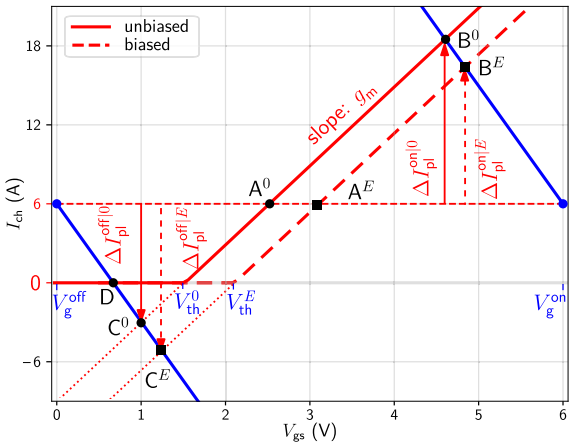


Fig. 7. Transfer characteristics in unbiased and biased modes.

TABLE II
PARAMETER VALUES FOR FIG. 7

$V_{th}^0 = 1.5\,\text{V}$	$V_g^{on} = 6\,\text{V}$	$I_0 = 6\,\text{A}$	$R_g = 15\,\Omega$	$C_j = 20.3\,\text{pF}$
$V_{th}^E = 2.1\,\text{V}$	$V_g^{off} = 0\,\text{V}$	$g_m = 6\,\text{S}$	$C_{dg} = 0.3\,\text{pF}$	$C_{ds} = 20\,\text{pF}$

the corresponding threshold voltage are identified with a "0" superscript: V_{th}^0.

2) *Biased* means that the DUT incurred initial I-type V_{ds} bias induced positive V_{th} shift, by voltage E before t_0 in the conventional DPT in Fig. 2. The corresponding curve (dashed line in Fig. 7) is determined by V_{th}^E, including the E bias superscript indication.

In addition, the plateau relation lines are also plotted, similar to Fig. 5, and the crossing points A^0, B^0, C^0 for the unbiased curve and A^E, B^E, C^E for the biased case are defined.

The parameters used for Fig. 7 are based on the GaN Systems device GS66502B, where the unbiased V_{th}^0 is approximated from the datasheet transfer characteristics, while the biased V_{th}^E is set in Table II. And the positive shifted value is consistent with orders of magnitude to our measurement and literature [13], [14], [15], [16], [20], [21]. For plotting the plateau relation lines, Table II also indicates the ON/OFF gate voltages, switched current, gate resistance (same for ON and OFF) and device capacitance values that are approximated from the datasheet at 200 V drain voltage.

At turn-ON, Fig. 7 shows that current transition should be slower in biased conditions because the V_{gs} rising span from $(V_{th}^E, 0)$ to point A^E is closer to its final value V_g^{on}, compared with the unbiased case from $(V_{th}^0, 0)$ to A^0. This means the current rising stage in biased condition is longer due to the RC charging characteristics of V_{gs}. Afterward, the voltage transition is linked to ΔI_{ch} as mentioned in (6). Fig. 7 reveals that its "target" values in biased ($\Delta I_{pl}^{on|E}$) and unbiased ($\Delta I_{pl}^{on|0}$) conditions are different, as V_{th} instability shifting the transfer characteristics. Thus, ΔI_{ch} rises slower in biased state (from A^E towards B^E) than in unbiased one (from A^0 toward B^0), resulting in slower voltage transition as well. Importantly, it can be expected that slower transitions in biased case increase switching power losses.

At turn-OFF, the previous section shows that voltage rise is first associated with a fast current transition in I_{ch} that quickly reaches zero when the operating point moves from point A toward point C in Fig. 5, bifurcating at $(V_{th}, 0)$ toward point D. Consequently, this transition is much less impacted by V_{th} shift as it was at turn-ON. Afterward, drain voltage keeps rising under the effect of drain current charging the DUT output capacitance, as discussed in Fig. 6(b). Since this transition is then independent on the transfer characteristics, it might be concluded that the V_{th} shift does not influence turn-OFF switching, which is subjected to low power losses anyway.

Overall, the I-type V_{ds} bias induced positive V_{th} shift can slow down the turn-ON switching commutation by decreasing the dV_{ds}/dt and dI_d/dt, while the turn-OFF switching transition is not influenced. Moreover, the device V_{th} is also depend on the II-type V_{ds} bias in hard-switching. And only the transfer characteristics under high V_{ds} can be used to predict the hard-switching transition, as the switching commutation mainly occurs in high V_{ds} saturation region.

To verify the two types of V_{ds} bias induced V_{th} instability on device switching behaviors, a method to obtain and modeling the transfer characteristics under different high V_{ds} is required.

III. HVHC I–V Characterization and Modeling Using the H-Bridge Based DPT

The conventional DPT based high-voltage and high-current (HVHC) I–V (equivalent to the transfer characteristics under different high V_{ds}) characterization methods are reported for SiC-MOSFETs in [28], [33]. The HVHC I–V characteristics can include the II-type V_{ds} bias related negative V_{th}, because they are extracted from hard-switching transition in different high V_{ds}. However, the HVHC I–V characterization method in [28] and [33] is undesirable for GaN-HEMTs, since the initial I-type V_{ds} bias in conventional DPT cannot be eliminated as shown in Fig. 2(b), and its impact on the I–V characteristics will be coupled with II-type V_{ds} bias. To reveal the bidirectional V_{th} shift and their impact on switching behaviors, theses two types of V_{ds} bias in conventional DPT should be decoupled. The whole HVHC I–V characterization and modeling process of this section is shown in Fig. 8.

A. H-Bridge Based I–V Characterization

To decouple these two types of V_{ds} bias induced V_{th} instability, the existence of I-type V_{ds} bias should be controlled. Hence, an H-bridge based DPT circuit is adopted, which is proposed in our previous research [34]. The schematic is shown in Fig. 9. The modified H-bridge DPT consists of two parts. The main board is a normal half-bridge for conventional DPT. The auxiliary board is used to control the I-type V_{ds} bias of DUT, where T_H and T_L operate complementarily. Two modes of DPT can be realized in this H-bridge. In unbiased mode, initially, the T_H is off and the V_{ds} of DUT is zero as V_{aux}. In this way, the initial V_{ds} bias before starting the DPT can be removed. After T_H is turned ON, the state of T_H and T_L will be latched, afterward the H-bridge behaves

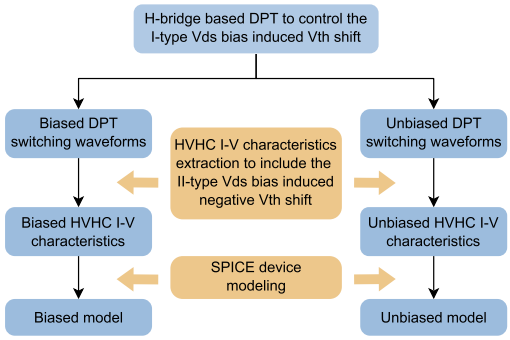


Fig. 8. Process of HVHC I-V characterization and modeling to decouple the two types of V_{ds} bias induced V_{th} instability.

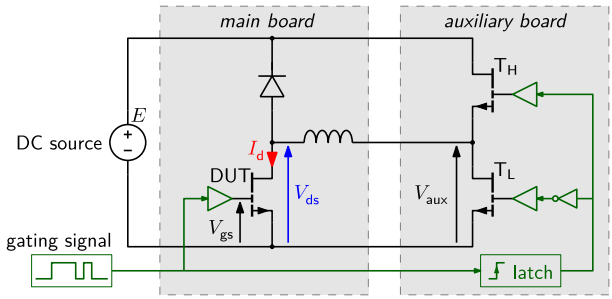


Fig. 9. Schematic of the H-bridge based DPT.

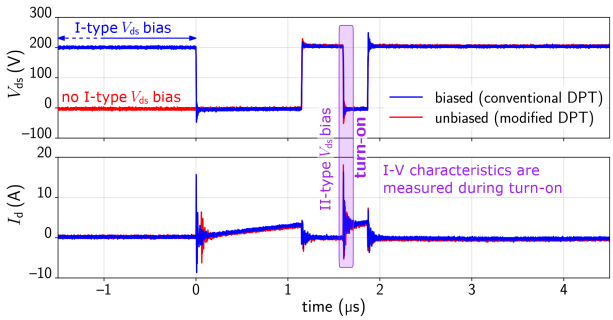


Fig. 10. Biased and unbiased switching waveforms from H-bridge based DPT.

as the conventional DPT. In the biased mode, the conventional DPT can be directly achieved by tuning ON and locking the T_H in advance. This H-bridge enables to control the dc source E caused I-type V_{ds} bias in conventional DPT. Therefore, the DPT with and without the influence of I-type V_{ds} bias can be implemented, labeled as biased and unbiased DPT, respectively, in this article. The switching waveforms of biased and unbiased DPT are displayed in Fig. 10.

The HVHC output characteristics can be obtained by interpolating a set of turn-ON switching waveforms from the H-bridge based DPT with various V_{gs} values, where the V_{ds} drops from 200 to 0 V and I_d increases from 0 A to various values, as shown in Fig. 11(a). For example, when V_{gs} is 1.8 V, the corresponding I_d and V_{ds} can be plotted as one curve of HVHC output characteristics, as shown in Fig. 11(b). By repeating this interpolation over a range of V_{gs}, the full HVHC output characteristics can be obtained. More delicate curves can be obtained if the numbers

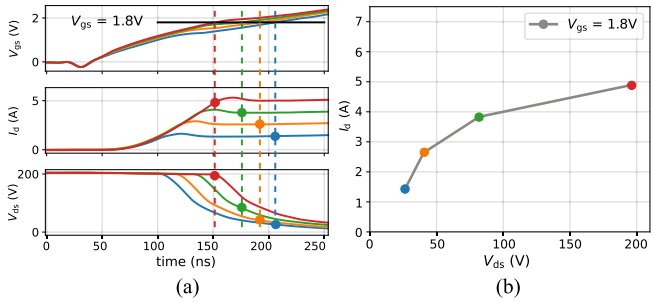


Fig. 11. HVHC output characteristics can be obtained by interpolating (a) a set of slowed down turn-ON switching waveforms with different load current (b) extracted HVHC output characteristics when $V_{gs} = 1.8$ V.

of the waveform at various currents are increased in Fig. 11(a). In the HVHC output characteristics, the complete relationship between V_{gs}, V_{ds} and I_d in device switching commutation can be obtained. And this method is reported in our previous work [35]. Though the turn-ON switching waveforms are slowed down by a large R_g^{on}, the voltage drop on device internal resistance and the displacement current through interelectrode capacitance of device are still compensated to get the channel current I_{ch} and voltage drop on C_{gs}. And the propagation delay between voltage and current probes are de-skewed based on the power-resistor based method in [36]. One minute of initial I-type V_{ds} bias is applied in biased mode DPT to produce a saturated positive V_{th} shift [15], [22], [37], as the V_{ds} induced V_{th} instability is time dependent.

The HVHC output characteristics of GS66502B are shown in Fig. 12(a). These characteristics are depicted as biased and unbiased HVHC output characteristics, represented by dashed and solid lines, respectively. This differentiation depends on whether the HVHC output characteristics are extracted from the biased mode DPT switching waveforms. Moreover, the transfer characteristics at different high V_{ds} can be obtained by interpolating at different V_{ds} values on the HVHC output characteristics as shown in Fig. 12(b). In this way, these two types of V_{ds} bias induced bidirectionally V_{th} shift can be clearly observed.

By comparing the solid and dashed curves in transfer characteristics, the I-type V_{ds} bias induced positive V_{th} shift can be observed, where the 0.5 V of ΔV_{th} is in the same order of magnitude as the literature [15], [37]. Moreover, all the transfer characteristics shift negatively with V_{ds} increasing from 50 to 200 V, which could be related to the II-type V_{ds} bias during turn-ON transient. And the mechanism may be attributed to the elevated potential of p-GaN layer under high V_{ds} bias as discussed in [17] and [18]. Note that this negative transfer characteristics shift are also reported for power SiC-MOSFETs [28], [38], but they are referred to the drain induced barrier lowering (DIBL) effect of vertical power MOSFETs.

To further investigate this negative V_{th} shift, the unbiased mode DPT is implemented under different dc voltage, where the initial I-type V_{ds} bias is eliminated. And the turn-ON time of DUT is set to 1 us to exclude the influence of varying V_{gs} bias time. The turn-ON switching waveforms are shown in Fig. 13(a). It is clear that I_d starts to rise earlier and faster under higher II-type

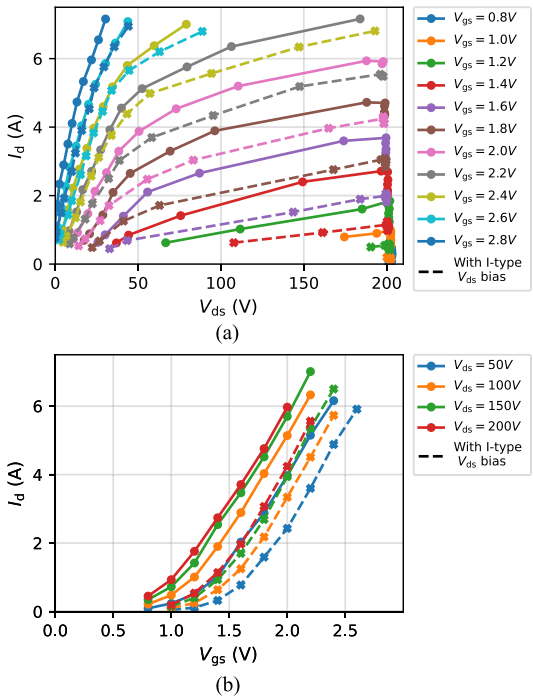


Fig. 12. HVHC I–V characteristics with (biased) and without (unbiased) the influence of I-type V_{ds} bias (a) output characteristics and (b) transfer characteristics under different V_{ds}. Here, the transfer characteristics are obtained by interpolating at different V_{ds} on the output characteristics. The I-type V_{ds} bias induced positive V_{th} shift can be obtained by comparing the dashed and solid curves. The II-type V_{ds} bias induced negative V_{th} shift are shown with V_{ds} increasing from 50 to 200 V in both types of curves.

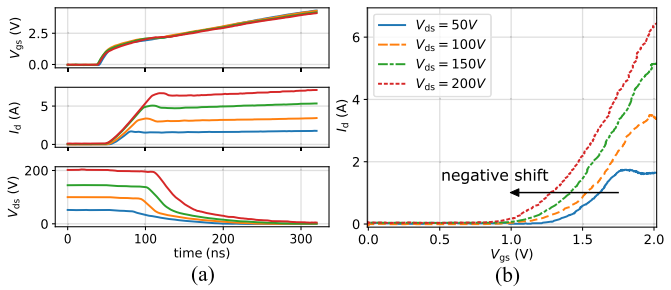


Fig. 13. Measured (a) turn-ON switching waveforms under different II-type V_{ds} bias from unbiased mode DPT and (b) negative V_{th} shift with the increase of II-type V_{ds} bias.

V_{ds} bias. Furthermore, the transfer characteristics under different V_{ds} are plotted using the I_d and V_{gs} switching waveforms in Fig. 13(a), as shown in Fig. 13(b). Noted that the influence of parasitic parameters are compensated, same as the HVHC I–V characteristics, to ensure that the I_d and V_{gs} can represent the channel current and voltage potential on the C_{gs}. Around -0.4 V of ΔV_{th} can be observed with V_{ds} increase from 50 to 200 V, which is agree with the negative ΔV_{th} in Fig. 12(b).

In this way, the V_{th} instability induced by the two types of V_{ds} bias are characterized. Note that both the biased and unbiased HVHC output characteristics in Fig. 12(a) include II-type V_{ds} bias induced negative V_{th}, since they both considers the complete relation between V_{ds}, V_{gs}, and I_d during high voltage hard-switching. While only the biased HVHC output characteristics include the I-type V_{ds} bias induced positive V_{th} shift. Theses biased and unbiased HVHC output characteristics can be further modeled to validate the impact of V_{th} instability on switching behaviors.

B. I–V Characteristics Modeling for SPICE Behavior Models

Behavior models considering the obtained HVHC I–V characteristics are constructed in this part. In conventional behavior modeling, empirical equations are adopted to fit measured I–V characteristics [28], [39], [40]. However, proposing appropriate equations and searching global solution for tens of optimized parameters are time-consuming and complicated in nonlinear regression. More importantly, most of the I–V characteristics models are proposed for HEMTs and MOSFETs, assuming I_d becoming saturated after V_{ds} above 5 or 10 V [24], [41], like manufacturer model [24], which means they do not include II-type V_{ds} bias induced V_{th} instability. But the power transistor mainly operates under hundred voltage of V_{ds} and the switching commutation happen in high V_{ds} region, such models may not be enough to accurately predict device switching behavior. Therefore, a neural network-based HVHC I–V characteristics model is proposed in this article, where the dedicated equations are not required and the training process is faster and more convenient compared to the conventional nonlinear regression [33], [42].

The multilayer perceptron neural network is adopted to model the HVHC I–V characteristics due to the compatibility of SPICE environment. A three-layer neural network with two neurons in the input layer, six neurons in the hidden layer, and one neuron output layer (for I_d) is employed, as expressed

$$I_d = \tanh(\mathbf{I} \times \mathbf{W_1}^\intercal + \mathbf{B_1}^\intercal) \times \mathbf{W_2} + \mathrm{b} \tag{9}$$

where the $\mathbf{I} = (V_{gs} \;\; V_{ds})$ is the input vector, b is a bias parameter, and other parameter matrices are display as follows:

$$\mathbf{W_1} = \begin{pmatrix} w_{11} & w_{21} \\ w_{12} & w_{22} \\ \vdots & \vdots \\ w_{16} & w_{26} \end{pmatrix}, \mathbf{B_1} = \begin{pmatrix} b_1 \\ b_2 \\ \vdots \\ b_6 \end{pmatrix}, \mathbf{W_2} = \begin{pmatrix} w_{31} \\ w_{32} \\ \vdots \\ w_{36} \end{pmatrix}. \tag{10}$$

As the above naming rules, the biased and unbiased neural network-based HVHC I–V characteristics models are created by feeding the data of measured turn-ON switching waveforms from biased and unbiased DPT. For cross reference, the I–V characteristics equations from high voltage adapted Angelov model in [43] are used to fit the measured HVHC I–V characteristics to get the corresponding Angelov models.

The HVHC I–V characteristics models constructed by neural network and Angelov equations are compared to the measurement results in Fig. 14. All models show good agreement with measured output characteristics. However, the Angelov model exhibits undesirable fitting result in high current region in biased conditions and this might be attributed to the limitation of model itself.

The device SPICE behavior models can be achieved by modifying the manufacturer model of GS66502B [24], in which

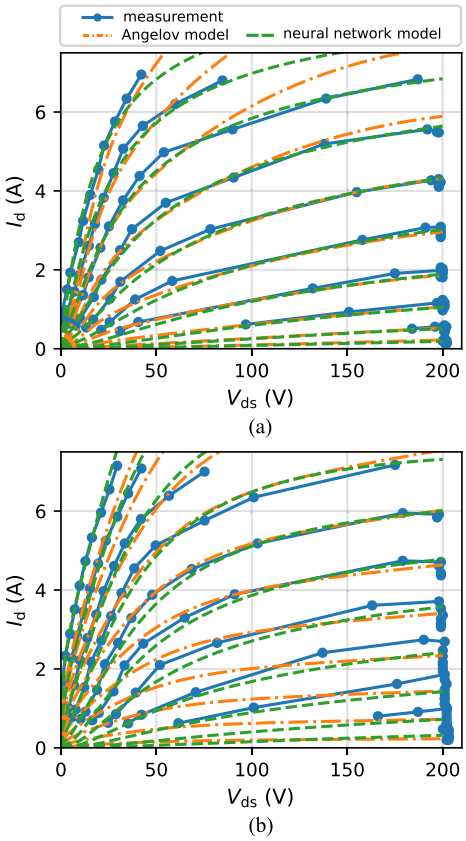


Fig. 14. Comparison of HVHC I–V characteristics between experiment measurement and constructed models (neural network and Angelov models) (a) with and (b) without the influence of I-type V_{ds} bias.

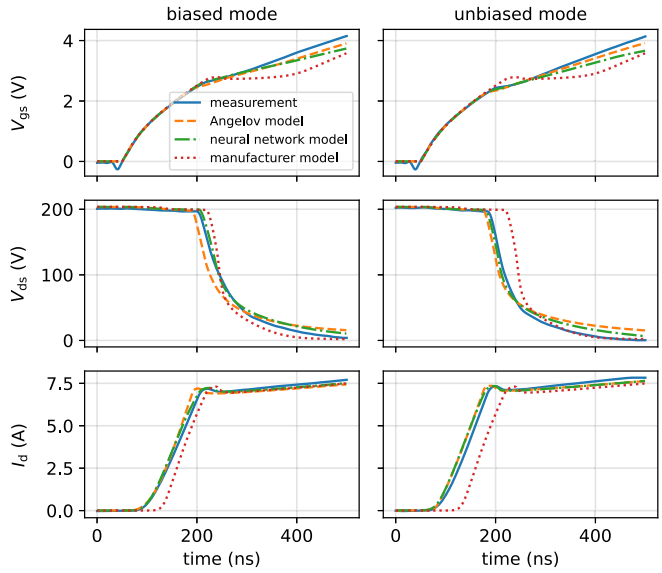


Fig. 15. Comparison of turn-ON switching waveforms (with 1 kΩ R_g^{on}) from biased and unbiased DPT with simulation results of biased and unbiased SPICE models.

the original I–V characteristics equations are replaced by our constructed HVHC I–V characteristics models in Fig. 14. As for other parts, such as, C–V characteristics, parasitics inductance inside the package remain unchanged, and the target is to exclude the influence of these parameters. This is why the SPICE model is adopted to demonstrate the influence of V_{th} instability on device switching behavior, as it is challenging to decouple the influence of I–V and C–V characteristics in experiments. Since the switching transition is also dependent on the device C–V characteristics, and the C–V characteristics may be also impacted by the V_{ds} bias-induced trapping effect in GaN buffer layer [44].

C. Model Validation and Switching Behavior Prediction

All SPICE behavior models are applied to the DPT simulation, with same schematic in Fig. 2(a), to replace the freewheeling diode and DUT. Their turn-ON simulation waveforms are compared to the biased and unbiased DPT measurement result at $I_d = 7$ A, which are depicted in Fig. 15. The result of manufacturer model is compared as a reference. Note that when using the split output gate driver (like LM5114) to drive GaN devices, the influence of output capacitance from gate driver MOSFETs should be considered to accurately model the switching waveform, especially in slow switching condition, the details are shown in our previous work [45]. As shown in Fig. 15, Miller plateau appears in V_{gs} waveforms as the large R_g^{on} is used, and it is tilted from the results of measurement and simulation models that the HVHC I–V is considered. This tilted Miller plateau could be attributed to the II-type V_{ds} bias induced negative V_{th} shift. Because transfer characteristics shift positively with V_{ds} decreasing as shown in Fig. 12(b), thus, a higher V_{gs} is required to maintain the same I_d in V_{ds} dropping stage. This can also be observed from Fig. 3(b), where shifted transfer characteristic would pull point B farther to the right, increasing plateau voltage. By contrast, flat Miller plateau is exhibited by the manufacturer model, as the transfer characteristics keep constant under different V_{ds} bias, meaning the II-type V_{ds} bias induced V_{th} instability is overlooked. This tilted Miller plateau is also observed in [38] for SiC-MOSFETs and in [14] for GaN-HEMTs. However, in Fig. 15, both neural network and Angelov model show slow voltage dropping speed when V_{ds} is under aroud 30 V, especially in unbiased models, which may be attributed to the undesirable fitting in low V_{ds} Ohmic region in HVHC I–V characteristics.

In addition, the $^{dV_{ds}}/_{dt}$, $^{dI_d}/_{dt}$ and turn-ON switching losses (E_{on}) of simulation and experiment waveforms in Fig. 15 are calculated in Table III. By comparing experimental results, the absolutely value of $^{dV_{ds}}/_{dt}$ and $^{dI_d}/_{dt}$ in biased mode are reduced, leading to 12.6 % higher switching losses, which is attributed to the I-type V_{ds} induced positive V_{th} shift and in accordance with the analysis in Section II-C. In simulation results, the neural network models can reproduce this trend, and the switching losses are increased 13.2 % from unbiased to biased model. However, the Angelov models could not show this phenomenon effectively, which could be ascribed to the undesirable fitting results in the high I_d and high V_{ds} region of HVHC I–V characteristics in Fig. 14(a). To further evaluate the performance of proposed models, the absolute difference of $^{dV_{ds}}/_{dt}$, $^{dI_d}/_{dt}$, and E_{on} between simulation and experiment results in Table III are compared in Table IV. The neural network models show the

TABLE III
dV_{ds}/dt, dI_d/dt AND SWITCHING LOSSES DURING TURN-ON TRANSITION FROM MEASUREMENT AND MODEL SIMULATION RESULTS IN FIG. 15

Turn-ON switching waveforms	dV_{ds}/dt (V/ns)	dI_d/dt (A/us)	E_{on} (uJ)
Measurement result biased	-1.40	63.64	142.88
Measurement result unbiased	-1.75	70.45	126.86
Neural network model biased	-1.24	65.02	159.71
Neural network model unbiased	-1.34	71.20	141.15
Angelov model biased	-1.15	73.54	139.36
Angelov model unbiased	-1.12	74.53	145.74
Manufacture model	-2.38	78.65	114.49

TABLE IV
COMPARISON OF THE ABSOLUTE DIFFERENCE OF dV_{ds}/dt, dI_d/dt AND E_{on} BETWEEN MODELS AND MEASUREMENT RESULTS IN TABLE III

| Model−Measurement |	dV_{ds}/dt (V/ns)	dI_d/dt (A/us)	E_{on} (uJ)
Neural network model biased	0.16	1.38	16.83
Neural network model unbiased	0.41	0.75	14.29
Angelov model biased	0.25	9.90	3.52
Angelov model unbiased	0.63	4.08	18.88
Manufacture model biased	0.98	15.01	28.39
Manufacture model unbiased	0.63	8.20	12.37

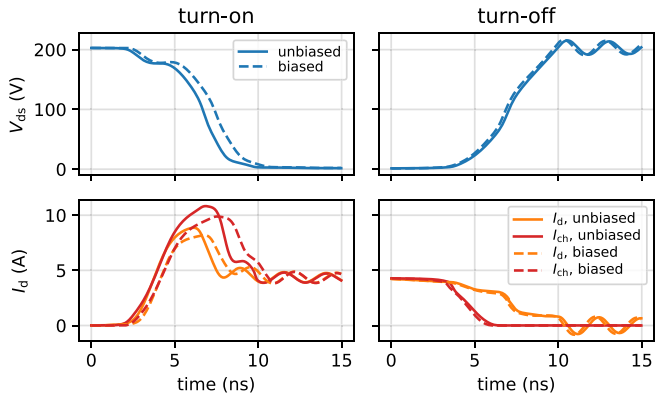


Fig. 16. Comparison of turn-ON and turn-OFF simulation switching waveforms of biased and unbiased neural network models. In turn-ON transient, the dV_{ds}/dt, dI_d/dt and current overshoot of biased model are decreased.

best agreement with measurement results in terms of dV_{ds}/dt and dI_d/dt. This also shows the potential advantage of neural network in nonlinear fitting.

The neural network models are employed to further verify the impact of V_{th} shift on device switching waveforms in fast switching conditions. In the simulation, 20 Ω of R_g^{on} and 2 Ω of R_g^{off} are adopted, and the 10 nH of L_g and 6 nH of L_d are included. The simulation waveforms of V_{ds}, I_d, and I_{ch} are shown in Fig. 16. At turn-ON, the absolute value of dV_{ds}/dt, dI_d/dt, and current overshoot toward ΔI_{pl}^{on} are larger in unbiased mode, as analyzed in Fig. 7. At turn-OFF, the commutation waveforms are almost identical in these two models. This is because I_{ch} drops to zero when V_{ds} starts to increase, meaning

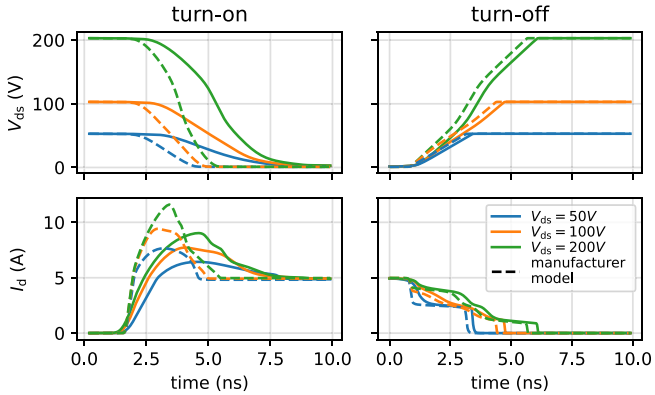


Fig. 17. Turn-ON and turn-OFF simulation waveforms at different V_{ds} from unbiased neural network models. In turn-ON transient, dI_d/dt and current overshoot of neural-network model are increased with V_{ds} voltage increasing.

the current transition is finished in the channel, afterward, the V_{ds} increasing process is independent of transfer characteristics. These results verify the hypothesis proposed in Section II-C that I-type of V_{ds} induced positive V_{th} shift can slow down the turn-ON commutation speed, while the turn-OFFprocess is not affected.

To evaluate the impact of II-type V_{ds} bias on switching waveforms, the unbiased neural network model is utilized for DPT simulation at different dc voltage, and the manufacture model is used as a reference. To clearly show the impact, the parasitic inductances are neglected. The simulation results are depicted in Fig. 17. At turn-ON, the I_d rises earlier and faster under higher V_{ds} bias, due to the negatively shifted transfer characteristics induced by the higher II-type V_{ds} bias. This trend is also observed in the measured turn-ON switching waveforms in Fig. 13(a). By contrast, the waveform of I_d from manufacturer model remains unchanged at different V_{ds} bias, due to its constant transfer characteristics. At turn-OFF, the I_d commutation speed is not affected by the shifted transfer characteristics, because I_{ch} drops to zero quickly as mentioned above. Both of the specific switching behaviors in turn-ON and turn-OFFagree with the analysis in Section II-C.

D. Experimental Verification in Fast Switching Commutation

The impact of V_{th} instability on device hard switching commutation is demonstrated by modeling and simulation above. And the decreased dV_{ds}/dt and dI_d/dt from slow experimental waveforms are quantified in Table III. However, the existence of this impact in a more practical switching condition deserve to be verified. Hence, the H-bridge DPT is implemented under 400 V dc bus voltage with 20 Ω of R_g^{on} and 2 Ω of R_g^{off} that is a typical application condition for the 650 V power transistors. The turn-ON and turn-OFF switching transition in biased and unbiased DPT are shown in Fig. 18. The V_{ds} and I_d in biased mode show the decreased dV_{ds}/dt (10.8 %) and dI_d/dt (13.2 %), leading to a 13.4 % increased E_{on}. And the switching waveforms show less peak overshoot compared to the unbiased mode in turn-ON transition. While, the turn-OFFcommutation does not show this variation. All of these experimental results show the

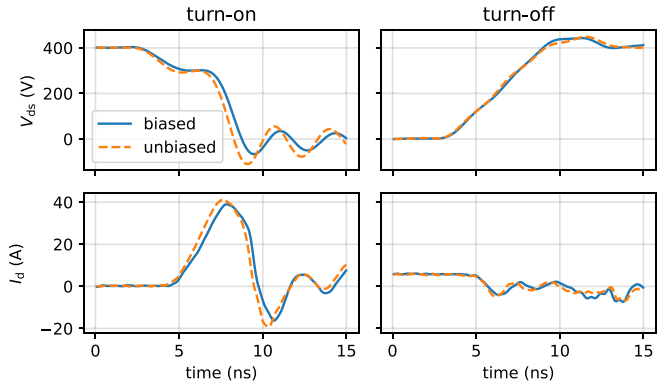


Fig. 18. Experimental turn-ON and turn-OFF switching waveforms from the H-bridge based DPT in fast switching condition with 400 V of V_{DC}.

consistency with the theoretical analysis and simulation. Similar effect in turn-ON switching waveforms is also reported in [20].

IV. Conclusion

In this work, we investigated two types of V_{ds} bias induced V_{th} instability in Schottky-type p-GaN gate HEMTs using the switching waveforms from the H-bridge based DPT. The results indicated that the OFF-state V_{ds} bias before turn-ON commutation (I-type V_{ds} bias) can cause positive V_{th} shift, while the V_{ds} bias during turn-ON transient (II-type V_{ds} bias) can lead to negative V_{th} shift. Based on the switching transient analysis, the positive V_{th} shift could reduce the turn-ON dV_{ds}/dt, dI_d/dt, increasing the switching losses. The reason is that the V_{gs} rising span from V_{th} to the plateau voltage is closer to V_g^{on} after positive V_{th} shift. As a result, the current commutation becomes longer due to the *RC* charging characteristics of V_{gs}. Moreover, the change in channel current ΔI_{ch} becomes smaller, which is positively related to dV_{ds}/dt based on our deduction in Section II. Meanwhile, the turn-OFFtransition remains essentially unchanged because the channel current drops to zero rapidly before the above mechanisms occur. The influence of negative V_{th} follows the same principle. Moreover, the tilted Miller plateau of GaN-HEMTs in slow switching condition can be attributed to the II-type V_{ds} bias induced negative V_{th} shift. The results suggest that the HVHC I–V characteristics that include the V_{th} instability phenomenon are indispensable for accurate turn-ON switching behavior modeling and losses estimation.

The actual I–V characteristics are influenced by various factors, including voltage biases, hot electrons, temperatures, etc., when the device operates in real power converters. Consequently, the characterization method to obtain the multiparameter coupled I–V characteristics is essential, which would improve the accuracy for switching behaviors modeling for GaN-HEMTs.

References

[1] T. Liu, C. Chen, K. Xu, Y. Zhang, and Y. Kang, "GaN-Based megahertz single-phase inverter with a hybrid TCM control method for high efficiency and high-power density," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6797–6813, Jun. 2021.

[2] J. P. Kozak et al., "Stability, reliability, and robustness of GaN power devices: A review," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8442–8471, Jul. 2023.

[3] S. Faramehr, K. Kalna, and P. Igić, "Drift-diffusion and hydrodynamic modeling of current collapse in GaN HEMTs for RF power application," *Semicond. Sci. Technol.*, vol. 29, no. 2, Jan. 2014, Art. no. 025007.

[4] M. Meneghini et al., "GaN-based power devices: Physics, reliability, and perspectives," *J. Appl. Phys.*, vol. 130, no. 18, 2021, Art. no. 181101, doi: 10.1063/5.0061354.

[5] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 96–106, 2018.

[6] S. Kaneko et al., "Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices IC's*, 2015, pp. 41–44.

[7] S. Yang, S. Han, K. Sheng, and K. J. Chen, "Dynamic on-resistance in GaN power devices: Mechanisms, characterizations, and modeling," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1425–1439, Sep. 2019.

[8] K. Zhong et al., "IG- and VGS-Dependent dynamic RON characterization of commercial high-voltage p-GaN gate power HEMTs," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8387–8395, Aug. 2022.

[9] J. O. Gonzalez, B. Etoz, and O. Alatise, "Characterizing threshold voltage shifts and recovery in Schottky gate and ohmic gate GaN HEMTs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 217–224.

[10] T. Oeder and M. Pfost, "Gate-induced threshold voltage instabilities in p-gate GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4322–4328, Sep. 2021.

[11] Y. Uemoto et al., "Gate injection transistor (GIT)–A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007.

[12] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold voltage instability in p-GaN gate AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, Jun. 2018.

[13] J. Wei et al., "Charge storage mechanism of drain induced dynamic threshold voltage shift in p -GaN gate HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 526–529, Apr. 2019.

[14] H. Xu, J. Wei, R. Xie, Z. Zheng, J. He, and K. J. Chen, "Incorporating the dynamic threshold voltage into the SPICE model of Schottky-type p-GaN gate power HEMTs," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5904–5914, May 2021.

[15] J. Chen et al., "OFF-State drain-voltage-stress-induced VTH instability in Schottky-type p-GaN gate HEMTs," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3686–3694, Jun. 2021.

[16] L. Efthymiou, K. Murukesan, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, "Understanding the threshold voltage instability during OFF-State stress in p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1253–1256, Aug. 2019.

[17] M. Nuo et al., "Gate/Drain coupled barrier lowering effect and negative threshold voltage shift in Schottky-type p-GaN gate HEMT," *IEEE Trans. Electron Devices*, vol. 69, no. 7, pp. 3630–3635, Jul. 2022.

[18] M. Nuo, Y. Wu, J. Yang, Y. Hao, M. Wang, and J. Wei, "Time-resolved extraction of negatively shifted threshold voltage in Schottky-type p-GaN gate HEMT biased at high VDS," *IEEE Trans. Electron Devices*, vol. 70, no. 7, pp. 3462–3467, Jul. 2023.

[19] K. Li, A. Videt, N. Idir, P. Evans, and M. Johnson, "Experimental investigation of GaN transistor current collapse on power converter efficiency for electrical vehicles," in *Proc. IEEE Veh. Power Propulsion Conf.*, 2019, pp. 1–6.

[20] F. Yang, C. Xu, and B. Akin, "Characterization of threshold voltage instability under off-state drain stress and its impact on p-GaN HEMT performance," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4026–4035, Aug. 2021.

[21] R. Xie et al., "Switching transient analysis for normally-off GaN transistor with p-GaN gate in a phase-leg circuit," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3711–3728, Apr. 2019.

[22] I. Hwang et al., "Extraction of dynamic threshold voltage in resistive load hard switching operation of Schottky-type p-GaN gate HEMT," *IEEE Electron Device Lett.*, vol. 43, no. 10, pp. 1720–1723, Oct. 2022.

[23] Z. Fan et al., "Analysis of drain-dependent threshold voltage and false turn-on of Schottky-type p-GaN gate HEMT in bridge-leg circuit," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 2351–2359, Feb. 2024.

[24] GS66502B Datasheet REV180420, "GaNsystems, 2018," 2018. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66502B-DS-Rev-180420.pdf

[25] N. Modolo et al., "Cumulative hot-electron trapping in GaN-Based power HEMTs observed by an ultra-fast (10 V/ns) on-wafer methodology," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5019–5026, Oct. 2022.
[26] H. Onodera, T. Kabemura, and K. Horio, "Numerical analysis of impact ionization effects on hard switching in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 70, no. 12, pp. 6217–6224, Dec. 2023.
[27] F. Yang, C. Xu, and B. Akin, "Experimental evaluation and analysis of switching transient's effect on dynamic on-resistance in GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10121–10135, Oct. 2019.
[28] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and H. Tanigawa, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sep. 2018.
[29] Z. Zeng, J. Wang, L. Wang, Y. Yu, and K. Ou, "Inaccurate switching loss measurement of SiC MOSFET caused by probes: Modelization, characterization, and validation," *IEEE Trans. Instrum. Meas.*, vol. 70, 2021, Art. no. 1002014.
[30] E. A. Jones, Z. Zhang, and F. Wang, "Analysis of the dv/dt transient of enhancement-mode GaN FETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2692–2699.
[31] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 3587–3594.
[32] K. Li, P. Evans, and M. Johnson, "SiC/GaN power semiconductor devices: A theoretical comparison and experimental evaluation under different switching conditions," *IET Elect. Syst. Transp.*, vol. 8, no. 1, pp. 3–11, 2018.
[33] P. Yang, W. Ming, J. Liang, I. Lüdtke, S. Berry, and K. Floros, "Hybrid data-driven modeling methodology for fast and accurate transient simulation of SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 440–451, Jan. 2022.
[34] A. Videt, K. Li, N. Idir, P. Evans, and M. Johnson, "Analysis of GaN converter circuit stability influenced by current collapse effect," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 2570–2576.
[35] X. Lu, A. Videt, K. Li, S. Faramehr, P. Igic, and N. Idir, "Influence of current collapse due to V_{ds} bias effect on GaN-HEMTs $I_d - V_{ds}$ characteristics in saturation region," in *Proc. 24th Eur. Conf. Power Electron. Appl.*, 2022, pp. P.1–P.9.
[36] H. Li, Z. Gao, R. Chen, and F. Wang, "Improved double pulse test for accurate dynamic characterization of medium voltage SiC devices," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1779–1790, Feb. 2023.
[37] K. Zhong, H. Xu, Z. Zheng, J. Chen, and K. J. Chen, "Characterization of dynamic threshold voltage in Schottky-type p-GaN gate HEMT under high-frequency switching," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 501–504, Apr. 2021.
[38] N. Wang, J. Zhang, and F. Deng, "Improved SiC MOSFET model considering channel dynamics of transfer characteristics," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 460–471, Jan. 2023.
[39] A. U. Rashid, M. M. Hossain, A. I. Emon, and H. A. Mantooth, "Datasheet-driven compact model of silicon carbide power MOSFET including third-quadrant behavior," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11748–11762, Oct. 2021.
[40] S. Faramehr and P. Igić, "Analysis of GaN HEMTs switching transients using compact model," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2900–2905, Jul. 2017.
[41] H. Li, X. Zhao, W. Su, K. Sun, X. You, and T. Q. Zheng, "Nonsegmented PSpice circuit model of GaN HEMT with simulation convergence consideration," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8992–9000, Nov. 2017.
[42] D. Chiozzi, M. Bernardoni, N. Delmonte, and P. Cova, "A neural network based approach to simulate electrothermal device interaction in SPICE environment," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4703–4710, May 2019.
[43] K. Li and S. Sen, "A fast and accurate GaN power transistor model and its application for electric vehicle," *IEEE Trans. Veh. Technol.*, vol. 73, no. 4, pp. 4541–4553, Apr. 2024.
[44] Q. Song, R. Zhang, Q. Li, and Y. Zhang, "Output capacitance loss of GaN HEMTs in steady-state switching," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5547–5557, May 2024.
[45] X. Lu, A. Videt, N. Idir, V. Marsic, P. Igic, and S. Faramehr, "Investigation on single and split output gate configurations influence on the GaN-HEMTs switching behaviours," in *Proc. 25th Eur. Conf. Power Electron. Appl.*, 2023, pp. 1–9.

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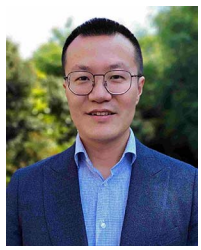

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