Design Optimization of Dual Active Bridge Converter for Supercapacitor Application

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***Abstract*—Supercapacitor (SC) is an energy storage suitable for meeting short-term requirements in power conversion systems. However, the low and variable terminal voltage of SC-based energy storage poses challenges to the design of its power electronic interface (PEI) to achieve a high round-trip efficiency and a rapid response of the energy storage system. The PEI design methodologies existing in the literature do not clearly tackle the mitigation of switching and conduction losses over the entire operating range of the SC. This article proposes a design strategy for an SC-interface dual active bridge (DAB) converter. The terminal characteristics of the SC are incorporated into an analytical design formulation aiming to maximize the DAB efficiency over the SC discharging cycle. The resulting optimization problem, addressing both conduction and switching losses, is solved numerically to obtain the optimal circuit parameters. The realization of the design objectives and the obtained efficiency is validated in circuit simulation and experiments on a 250 W laboratory prototype with a 125 V dc bus and a nominal SC voltage of 37.5 V, illustrating the improvement achieved over the conventional design approach.**

***Index Terms*—Design optimization, dual active bridge (DAB), gradient descent, supercapacitor (SC), zero voltage switching (ZVS).**

I. Introduction

POWER conversion systems increasingly employ supercapacitor (SC)-based storage to meet critical and short-term energy requirements [1]. The power and energy densities [2] and cycle life [3] of SCs make them suitable for supplying transient and backup power to complement a primary power source. The SC integration scheme is designed to tackle the challenges posed by the intrinsic properties of SC technology.

The terminal voltage of an SC, which varies with its state of charge, is interfaced to a constant-voltage dc bus using a power electronic interface (PEI). The low voltage ratings of commercially available SCs (∼3 V) are adapted to higher dc bus voltages (typically, a few hundred volts) through the series connection of SCs and the voltage gain of the PEI. In practice, the number of SCs in series is limited by cost/efficiency tradeoffs in voltage balancers [4], and by the severity of the dominant open-circuit failure mode in SCs [5]. The requisite voltage step-up is obtained from the PEI.

PEI topologies for SCs in the literature belong mainly to the single- or multiphase boost [6], [7], [8], [9] and the transformer-coupled dc/ac/dc [10], [11], [12], [13], [14], [15] categories; the low component count and the voltage step-up from the transformer are motivating factors in the respective cases. The choice of topology is influenced by application-specific considerations.

The speed of response of the power backup system is crucial in high-availability applications, such as data centers [16], necessitating a fast dynamic response of the PEI. In the case of the boost topology, the speed of response is limited by the right-half plane zero in the converter small-signal model [17]. Topologies such as the dual active bridge (DAB) [18] possess dynamics suited to this requirement. In addition, the scope of soft switching in the DAB permits operation at a high switching frequency, which facilitates a fast dynamic response.

The widely varying terminal voltage of SC storage is a significant consideration in the design of the PEI. The energy management [6], [7], [10] and control of the complete storage system [8] as well as the ancillary functions [9], [11] and the modulation and control of the PEI [13] are investigated in the literature. Efforts to optimize the PEI design for the SC application are limited [14], [15], [19]. In [14], an isolated multiport topology is designed for interfacing a battery and an SC. However, no clear justification is presented to support the choice of circuit parameters. The SC operating range is considered in the DAB design detailed in [15], where the turns ratio is selected to achieve zero voltage switching (ZVS) of both primary- and secondary-side full bridges over the entire operating range. The inductance parameter is chosen to operate the DAB at the power transfer limit, resulting in high rms currents. In [19], the selection of the transformer turns ratio to mitigate the rms current over the entire operating range of the SC is outlined. However, switching losses and the realization of ZVS over the operating range are not considered in the design. These gaps in the existing literature motivate a focused discussion of the design optimization of the SC-interface DAB.

The formulation of design optimization approaches for the DAB in the literature [20], [21] are not well-suited to direct adaptation for a PEI application. Since the PEI is an auxiliary

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component in an SC system, computationally simple control schemes favor low-cost implementations. This discourages the use of DAB optimization approaches, such as that in [21], employing computation-intensive modulation methods. The single phase-shift (SPS) modulation scheme is preferable from this perspective. In general, the variable SC voltage and the fixed dc bus voltage lead to unmatched voltages on the transformer primary and secondary sides, resulting in high rms currents in the DAB. A method to optimize the design of an SPS-modulated DAB over a range of voltages is presented in [20] for a battery charging application. However, the terminal characteristics of the SC, which constitute a key consideration in the PEI design optimization, are absent in this approach. Also, its computational cost leaves scope for improvement.

This article, which extends the work presented in [19], outlines a design optimization methodology for an SPS-modulated DAB in an SC interface application. The key contributions of this article are as follows.

1) Existing designs of the DAB aim to maximize the efficiency at a single worst-case operating condition or a set of operating points. In contrast, the optimization of efficiency over the entire operating interval, which is proposed in this article, is useful for minimizing the total energy loss for the SC application in particular and is also applicable to power converters in general.
2) A novel analytical formulation of the DAB rms current over the SC discharging interval is obtained using the slow temporal variation of the SC terminal voltage. This allows the analytical quantification and subsequent minimization of the conduction loss over the entire operating range, rather than at a single operating point as considered in conventional design approaches.
3) Current polarity-based ZVS relations of the SPS-modulated DAB, which are found in the literature, involve modulation-related quantities and are not directly utilizable within optimization algorithms. In this article, these relations are systematically derived only in terms of the DAB terminal operating quantities. Modulation-related variables are eliminated to obtain a design-oriented formulation which is especially useful for direct application to design optimization algorithms, such as that presented in this article.
4) The equivalent series resistance (ESR), which affects the SC voltage limits, is included in the design formulation.
5) A projected gradient-based design optimization procedure is introduced to minimize the rms current while satisfying ZVS constraints over the entire operating range. The physical significance of each design parameter is discussed and the optimization algorithm elaborated in a stepwise and general fashion. This general analytical description of the optimization process is of potential avail in the context of power converter design.
6) Although the DAB is widely employed for SC interfacing, a systematic design procedure for this application is not found in the literature. This gap is addressed by the proposed design flow, which also quantifies guidelines to select the switching frequency considering reduced-load operation.
7) The proposed design is validated in simulation and experiment, confirming the realization of the design objectives. The efficiency obtained through the proposed optimization is compared to the conventional approach.

The rest of this article is organized as follows. In Section II, the steady-state analysis of the DAB is combined with the SC terminal characteristics to obtain the rms current and ZVS expressions, which constitute, respectively, the objective function and the constraints for the design optimization. Physical insights into the design space and the gradient-based optimization algorithm are discussed in Section III, along with guidelines for switching frequency selection. The proposed optimization is illustrated using a design example in Section IV. Simulation and experimental results validating the design optimization procedure for this example design, and comparing it to a conventional design, are presented in Section V. Finally, Section VI concludes this article.

II. Design Formulation for SC Interfacing

The dynamic variation of SC terminal voltage between prescribed limits is a key detail to be captured in the design equations of the interface DAB. A normalized analysis and design procedure is adopted.

A. System Description and Normalization

Owing to their high capacitance, the energy density of SCs is higher than that of ordinary capacitors and allows them to be used as energy storage. However, SCs have an inherently high ESR that limits their power density; as a result, SCs occupy a power/energy niche complementary to both batteries and electrolytic capacitors. The construction and energy storage mechanisms of SCs differ from ordinary polarized capacitors, but their terminal characteristics are modeled most simply by representing the SC as a capacitance in series with a resistance. This representation is reported to suffice for efficiency-related studies, although higher-order models are proposed in the literature to accurately represent phenomena such as self-discharge. The interested reader is referred to [22] for a detailed survey of the characteristics of SCs. The characteristics of SCs significant to the present design problem are the low voltage of commercial SCs, and the capacitor-like terminal behavior, which makes a large variation in terminal voltage necessary to utilize the stored energy.

The schematic of an SC stack (C_{sc}) interfaced to a constant-voltage dc bus (V_{dc}) through a generic isolated PEI is shown in Fig. 1(a). During contingencies, the power requirement (P_b) at the dc bus is supported by the SC, which discharges in the process. This mode of operation continues until normal conditions resume, in case of short-term contingencies such as a voltage sag at the main power source [23]. Since SCs are suitable for short-term storage, longer contingencies are supported by auxiliary power sources; in such cases the SC supplies power during the intermediate start-up interval of the auxiliary

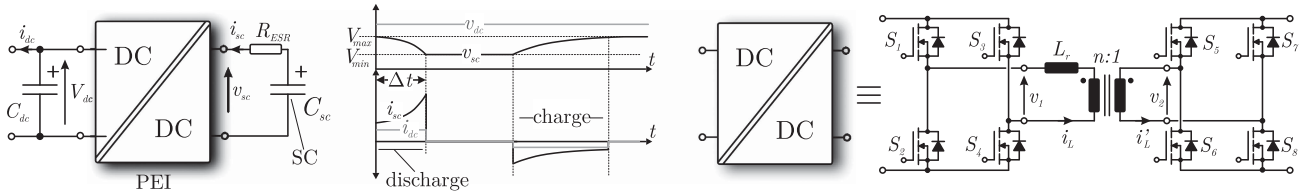


Fig. 1. (a) Schematic of an isolated PEI interfacing the SC to a DC bus. (b) Representative operating waveforms of the SC-PEI system showing charging and discharging operation at different constant powers. (c) The circuit schematic of the PEI realized as a DAB.

TABLE I
EXPRESSIONS FOR NORMALIZED CIRCUIT QUANTITIES OF THE SC INTERFACE DAB

Normalized quantity	Expression
Primary full bridge voltage, m_1	v_1/V_B
Secondary full bridge voltage, m_2	nv_2/V_B
Inductor current, j_L	$i_L Z_B/V_B$
SC voltage, m	$nv_{\rm sc}/V_B$
Output (SC) power, p	$P_b Z_B/V_B^2$

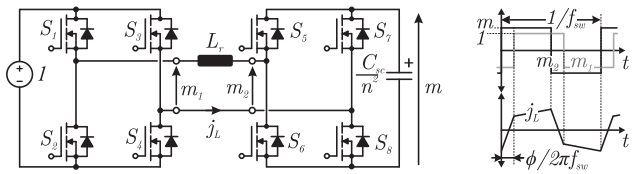


Fig. 2. Normalized (a) equivalent circuit of the SC-DAB system, and (b) representative operating waveforms of the DAB under SPS modulation, considering the discharging of the SC in the forward mode.

source [24]. The SC is then recharged suitably during normal operation. The rate of SC discharging is dictated by the power requirement (P_b), while the rate of charging is typically lower to improve the efficiency of SC charging [25] and relax the current stress on the voltage balancer [4]. Representative waveforms of SC voltage ($v_{\rm sc}$) and current ($i_{\rm sc}$), and dc bus voltage ($v_{\rm dc}$) and current ($i_{\rm dc}$) during charging and discharging are presented in Fig. 1(b). In this work, the power requirement at the dc bus is assumed constant over the duration of the contingency, and hence a constant-power discharge is assumed. The static upper ($V_{\rm max}$) and lower ($V_{\rm min}$) limits of $v_{\rm sc}$ are dictated by the design of the SC stack [24].

In the present context, the PEI is a DAB, as shown in Fig. 1(c). The topology allows bidirectional power transfer between the dc-side (S_1–S_4) and SC-side (S_5–S_8) MOSFET full bridges through a transformer with an $n:1$ turns ratio and an inductor (L_r). The circuit quantities are normalized considering the dc bus voltage ($V_{\rm dc}$) as the base voltage, V_B. The base impedance is equal to the impedance, Z_B, of the coupling inductor at the switching frequency ($f_{\rm sw}$) as (1).

$$Z_B = 2\pi f_{\rm sw} L_r \tag{1}$$

The quantities shown in Fig. 1(a) and 1(c) are referred to the transformer primary side and normalized using the base values mentioned. The normalized quantities are summarized in Table I and also indicated in the normalized equivalent circuit presented in Fig. 2(a).

B. Formulation of Design Objectives for SC Application

The efficiency of the DAB influences the required size of the SC stack for a given load power requirement. As discussed in Section II-A, the charging rate of the SC can be regulated in a way that achieves a high overall efficiency. During SC discharging, however, DAB operation is dictated by the load requirements and its efficiency is influenced solely by the design. Hence, the design procedure aims to improve the efficiency of the DAB over the SC discharging interval.

The efficient operation of the DAB requires the mitigation of conduction and switching loss. The conduction loss is reduced by minimizing the rms current over the operating interval. The individual operating conditions are combined to obtain an analytical expression for the rms current over the complete discharging interval. The evaluation of this overall rms current requires a consideration of the slow variation of the terminal voltage of the SC along with the DAB steady-state analysis; this analysis is presented in Section II-D.

The conduction loss in the SC ESR is significant [26]. However, the injection of high-frequency currents into an SC is not recommended due to an impact on its lifetime [27], and hence the SC current is considered to be purely dc when calculating the conduction loss in its ESR [26]. In practice, the high-frequency ripple current of the DAB is filtered out and the instantaneous SC current is dictated only by load requirements. Hence, the minimization of the DAB rms current during the discharging interval, as proposed above, has a negligible impact on the losses of the SC.

The conditions of ZVS of both SC- and dc-side bridges are imposed over the same operating interval to mitigate switching loss. Although ZVS conditions at a single DAB operating condition are available in the literature, analogous expressions to guarantee ZVS over an operating range are not clearly stated. Further, existing ZVS analysis is not performed in terms of DAB terminal quantities, complicating their use in analytical minimization procedures. The relations to gurantee ZVS over the complete SC discharging interval are obtained in terms of the application parameters and the design parameters, $\{n, Z_B\}$, in Section II-E.

C. ESR Modification to Limits of Normalized SC Voltage

The static voltage limits, $\{V_{\min}, V_{\max}\}$, apply to the SC stack only while the PEI is inactive. During operation, the SC terminal voltage limits differ from the corresponding static values by an amount equal to the voltage drop in the ESR. This effect is significant due to the relatively high SC current in the discharging interval, for which the design optimization is executed. The actual normalized SC voltage limits while discharging are obtained by subtracting the ESR drop from the static voltage limits, as (2) and (3).

$$m_{\max} = \frac{n}{V_B}\left(V_{\max} - \frac{P_b R_{\text{ESR}}}{V_{\max}}\right) \tag{2}$$

$$m_{\min} = \frac{n}{V_B}\left(V_{\min} - \frac{P_b R_{\text{ESR}}}{V_{\min}}\right) \tag{3}$$

D. Analysis of RMS Current Over the SC Discharging Interval

Representative waveforms of the normalized voltages, m_1 and m_2, and current, j_L, defined in Table I, are presented in Fig. 2(b) considering SC discharging. For SPS modulation, m_1 and m_2 have square waveforms with amplitudes of 1 and m, respectively, and are separated by a phase shift. The subsequent analysis uses a normalized phase shift, ϕ, which is equal to the phase shift expressed as a fraction of π. The normalized power flow relation is obtained from [20] as (4).

$$p = \frac{m}{\pi}\phi(1-\phi). \tag{4}$$

Using (4), the control variable, ϕ, is parametrized in terms of the terminal quantities, m and p, as (5).

$$\phi = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{4p}{m\pi}}\right) \tag{5}$$

The parametrization in (5) abstracts the control variable, ϕ, in favor of the design-dependent variables, m and p. The expression for ϕ, obtained in (5), is substituted into available rms current expressions for the DAB to obtain the normalized steady-state switching-cycle rms current ($j_{L,\text{rms}}$) as (6).

$$j_{L,\text{rms}} = \frac{\pi}{\sqrt{12}}\sqrt{m^2 + 1 - m\left(2 + \frac{4p}{\pi m}\right)\sqrt{1 - \frac{4p}{\pi m}}} \tag{6}$$

The quantity, $j_{L,\text{rms}}$, thus depends on the terminal voltage (m) and power (p). The terminal voltage of the SC, and hence, $j_{L,\text{rms}}$, varies during operation. The rms value of j_L over the entire discharge interval (Δt) affects the total conduction loss directly. This quantity, denoted by J_{rms}, is obtained as (7).

$$J_{\text{rms}} \triangleq \sqrt{\frac{1}{\Delta t}\int_0^{\Delta t} j_L^2 dt} = \sqrt{\frac{1}{\Delta t}\int_0^{\Delta t} j_{L,\text{rms}}^2 dt} \tag{7}$$

Equation (7) is a general expression for the rms current in a DAB over an operating interval. The use of this expression in subsequent design steps requires temporal information of the DAB operation. In the present case, the terminal voltage dynamics of the SC allow the following crucial simplification.

Neglecting losses, the voltage variation of the SC is related to the load power as (8).

$$P_b = v_{\text{sc}} i_{\text{sc}} = -v_{\text{sc}}\left(C_{\text{sc}}\frac{dv_{\text{sc}}}{dt}\right) \tag{8}$$

The normalized form of (8) is then obtained as (9).

$$p = -m\left(\frac{C_{\text{sc}} Z_B}{n^2}\frac{dm}{dt}\right) \tag{9}$$

The definition of the quantity, p, in Table I is substituted into (9). The resulting equation is rearranged to obtain as (10).

$$\frac{dm}{dt} = -\frac{P_b}{C_{\text{sc}} V_B^2}\frac{n^2}{m} \tag{10}$$

The substitution of (10) into the expression for J_{rms} in (7) yields

$$J_{\text{rms}} = \sqrt{\frac{C_{\text{sc}} V_B^2}{n^2 P_b \Delta t}\int_{m_{\min}}^{m_{\max}} j_{L,\text{rms}}^2\, m\, dm}. \tag{11}$$

The rms current on the secondary side (I_{rms}), which is significantly higher due to the lower SC voltage level [13], is selected as the quantity to be minimized. The expression in (11) is scaled by the secondary-side base current, nV_B/Z_B, to obtain the expression for I_{rms}, as (12).

$$I_{\text{rms}} = \sqrt{\frac{C_{sc} V_B^4}{Z_B^2 P_b \Delta t}\int_{m_{\min}}^{m_{\max}} j_{L,\text{rms}}^2(m, Z_B)\, m\, dm} \tag{12}$$

The expression in (12) is applicable to any modulation scheme. The expression for $j_{L,\text{rms}}$ depends on the specific modulation strategy. Considering SPS modulation, (6) is substituted into (12). The expression for I_{rms} thus obtained is presented as (13) and (14) in Table II and constitutes the objective function to be minimized in the design.

E. Analysis of ZVS Criteria Over the Entire Operating Range

The analytical criteria for ZVS over the entire SC operating interval are required for the design optimization presented in Section III. As an initial step, modulation-related variables are eliminated from the existing ZVS formulation [20], based on the current polarity condition. Conditions for ZVS are obtained in terms of the normalized terminal quantities, m and p, at a particular operating point as (15) and (16) for the dc- and SC-side full bridges, respectively.

$$m < \sqrt{\frac{m\pi}{m\pi - 4p}}, \text{ dc-side bridge} \tag{15}$$

$$\sqrt{\frac{m\pi - 4p}{m\pi}} < m, \text{ SC-side bridge.} \tag{16}$$

The conditions, (15) and (16), govern the realization of ZVS at a specific operating point. The analytical guarantee of ZVS over the complete SC operating range is derived next.

Squaring, rearranging, and solving (15) yields

$$m - \frac{2p}{\pi} - \sqrt{1 + \frac{4p^2}{\pi^2}} < 0. \tag{17}$$

TABLE II
EXPRESSIONS FOR THE RMS CURRENT IN THE DAB OVER THE SC DISCHARGING INTERVAL FOR SPS MODULATION

Equations
$I_{\rm rms}(n, Z_B) = \sqrt{\frac{\pi^2 C_{\rm sc} V_B^4}{12 Z_B^2 P_b \Delta t} \int_{m_{\rm min}}^{m_{\rm max}} \left[m^3 + m - \left(2m + \frac{4 P_b Z_B}{\pi V_B^2} \right) \sqrt{m^2 - \frac{4 P_b Z_B m}{\pi V_B^2}} \right] dm}$ (13)
$I_{\rm rms}(n, Z_B) = \sqrt{f(m_{\rm max}) - f(m_{\rm min})}$ (14)
$f(m) \triangleq \frac{\pi^2 C_{\rm sc} V_B^4}{12 Z_B^2 P_b \Delta t} \left(\frac{m^4}{4} + \frac{m^2}{2} - \frac{2}{3}(m^2 - 2mq)^{3/2} - 2q(m-q)\sqrt{m^2-2mq} + 2q^3 \log\left[(m-q) + \sqrt{m^2-2mq} \right] \right), \; q \triangleq \frac{2 P_b Z_B}{\pi V_B^2}$

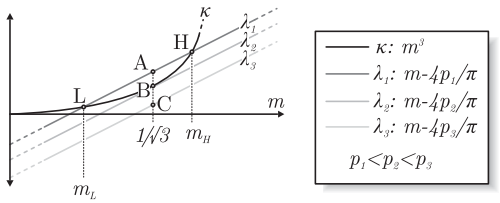


Fig. 3. Graphical illustration of (19) for normalized powers p_1, p_2, and p_3, with conditional ZVS (λ_1), edge-of-ZVS (λ_2), and guaranteed ZVS (λ_3) of the secondary-side full bridge, respectively.

The condition for ZVS of the dc-side bridge over the entire range of operation is obtained as (18) by substituting $m = m_{\rm max}$ in (17).

$$g_{\rm dc}(n, Z_B) \triangleq m_{\rm max} - \frac{2p}{\pi} - \sqrt{1 + \frac{4p^2}{\pi^2}} < 0 \quad \text{where} \quad p = P_b Z_B / V_B^2. \tag{18}$$

The SC-side ZVS constraint, (16), is squared and rearranged to obtain as (19).

$$m^3 > m - \frac{4p}{\pi} \tag{19}$$

Thus, the ZVS condition in (19) translates to a relation involving a cubic curve ($\kappa \equiv m^3$) and a straight line with unit slope ($\lambda \equiv m - 4p/\pi$). The curve, κ, is shown in Fig. 3 along with three lines, λ_1, λ_2, and λ_3, corresponding to three different designs. Based on the intersection between these curves, the ZVS condition is analyzed in two cases as follows.

1) *Case 1:* κ and λ do not intersect. This applies to all λ, e.g., λ_3, lying graphically below the tangential λ_2 in Fig. 3. The value of m at the point B is obtained as $1/\sqrt{3}$ from the condition of tangency of λ_2 and κ. Substituting $m = 1/\sqrt{3}$ into (19) yields the condition of SC-side ZVS for this case as (20).

$$p > \frac{\pi}{6\sqrt{3}} \tag{20}$$

2) *Case 2:* κ and λ intersect. This applies to all λ, e.g., λ_1, lying graphically above the tangential λ_2 as shown in Fig. 3. In Fig. 3, the points of intersection of λ_3 and κ are marked as H and L, at $m = m_H$ and $m = m_L$, respectively. Equation (19) is satisfied only if $m < m_L$ or $m > m_H$. Thus, to ensure SC-side ZVS, the range of m is designed for either $m_{\rm max} < m_L$ or $m_{\rm min} > m_H$. In the context of the design optimization, the rms current is reduced in the SPS modulation by matching the magnitudes of the transformer primary and secondary voltages. In an optimized design, these voltages are matched at some point within the operating range. This implies that $m = 1$ for some $m \in \{m_{\rm min}, m_{\rm max}\}$, and hence, $m_{\rm max} < m_L < 1/\sqrt{3}$ does not hold. Thus, the ZVS condition is satisfied if $m_{\rm min} > m_H$, as (21).

$$m_{\rm min} > m_H = \max\left\{ m : m^3 - m + \frac{4p}{\pi} = 0 \right\} \tag{21}$$

The value of m_H in (21) is obtained using standard methods for solving cubic equations [28].

The conditions (20) and (21) are combined to give the ZVS condition of the SC-side bridge, as (22).

$$g_{\rm sc}(n, Z_B) \triangleq \left\{ \begin{array}{ll} \frac{\pi}{6\sqrt{3}} - p, & \text{for } p > \frac{\pi}{6\sqrt{3}} \\ m_H - m_{\rm min}, & \text{otherwise.} \end{array} \right\} < 0$$
$$\text{where} \quad p = \frac{P_b Z_B}{V_B^2}, \; m_H = \max\left\{ m : m^3 - m + \frac{4p}{\pi} = 0 \right\} \tag{22}$$

In the rest of this article, a ZVS condition denotes the ZVS of all switches of the SC-side and dc-side bridges over the entire voltage range, i.e., (18) and (22) are simultaneously satisfied. Any other condition is denoted as loss of ZVS.

III. DESIGN OPTIMIZATION METHODOLOGY

The design optimization problem for the DAB targets the minimization of the rms current ($I_{\rm rms}$) expression, obtained as (14), subject to the ZVS constraints ($g_{\rm dc} < 0$ and $g_{\rm sc} < 0$), obtained as (18) and (22), respectively. These expressions are derived considering the entire SC discharging interval. The problem of obtaining the optimal design parameter set, $\{n^*, Z_B^*\}$, is stated formally as (23).

$$(n^*, Z_B^*) = \text{argmin}_{n, Z_B} I_{\rm rms}|_{g_{\rm sc}<0,\, g_{\rm dc}<0} \tag{23}$$

A. Motivation for Numerical Optimization

An SPS-modulated DAB can be optimized for a single operating point from qualitative considerations. The optimal turns

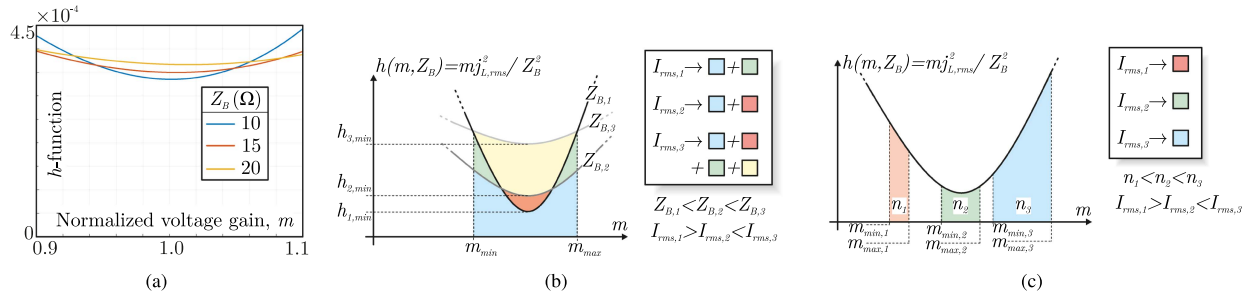


Fig. 4. (a) Plot showing the variation of the rms current function, h, with m for various values of Z_B and the ratings of Table IV. Representation of the rms current as the area under the curve, $h(m, Z_B)$, between normalized voltage limits (b) for three values of Z_B, and (c) for three values of n.

ratio is directly obtained considering voltage matching. Further, for a given operating point, the rms current in a voltage matching design of the DAB is an increasing function of Z_B. Hence, the rms current is minimized by selecting the minimum value of Z_B that satisfies ZVS constraints.

However, the same does not hold for the interface DAB over a range of SC voltages, since the transformer primary and secondary voltages are unmatched over most of the operating interval. Hence, an explicit step is required to solve the optimization problem in (23). The optimization algorithm is chosen based on a graphical analysis of the nature of the design space and the rms current objective function.

In (12), I_{rms} is given in terms of the integral of a function, h, defined as $h(m, Z_B) = mj^2_{L,\text{rms}}/Z^2_B$. The function, h, is plotted against m for three values of Z_B in Fig. 4(a).

The square of I_{rms} is proportional to the area under the curve h between the limits, $m_{\min} \leq m \leq m_{\max}$, as illustrated schematically in Fig. 4(b). As shown in Fig. 4(b), the area under the curve is the lowest for $Z_{B,2}$ although $Z_{B,3} > Z_{B,2} > Z_{B,1}$. Unlike a fixed-operating-point case, the rms current over the SC discharging interval does not necessarily increase with Z_B. Rather, the optimum occurs at a value of Z_B intermediate between the upper limit, imposed by power flow limitations, and the lower limit dictated by considerations of ZVS. The operation of the SC interface DAB involves both matched and unmatched transformer voltages. The optimal value of Z_B trades off the rms current at matched condition with the rms current at unmatched condition, as illustrated in Fig. 4(b). Thus, choosing the minimum possible Z_B, that minimizes rms current at the matched condition only, is not optimal.

The effect of the optimal turns ratio is also illustrated in terms of the area of the shaded region under the h-curve, in Fig. 4(c). The turns ratio affects the normalized voltage limits ($\{m_{\min}, m_{\max}\}$). As n is increased, the width of the base of the shaded region always increases, while the height changes according to h. Since the area depends approximately on the product of the height and the base, the rms current is not necessarily minimized at the minimum h corresponding to matched operation. Thus, the conventional approach to DAB optimization is unsuitable to optimize the SC-interface DAB.

B. Gradient-Based Optimization Algorithm

The graphical argument presented in Section III-A indicates a single optimum for Z_B for each choice of n, and vice-versa. This motivates the use of the projected gradient descent algorithm, described in [29], to optimize the parameters and minimize I_{rms}.

The design parameter vector ($\boldsymbol{x}^{(k)}$) at the k^{th} iteration step is formed from the turns ratio and the impedance as $\boldsymbol{x}^{(k)} = [n^{(k)}\ Z_B^{(k)}]^T$. An unconstrained gradient update term, $\boldsymbol{\Delta}^{(k)}$, is first subtracted from the parameter vector to obtain an intermediate vector, $\boldsymbol{x}^{(k+\frac{1}{2})}$, as (24).

$$\boldsymbol{x}^{(k+\frac{1}{2})} = \boldsymbol{x}^{(k)} - \boldsymbol{\Gamma}\boldsymbol{\Delta}^{(k)}$$
$$\text{where, } \boldsymbol{\Gamma} = \begin{bmatrix} \gamma_1 & 0 \\ 0 & \gamma_2 \end{bmatrix}, \boldsymbol{\Delta}^{(k)} = \left[\frac{\partial I_{\text{rms}}}{\partial n} \quad \frac{\partial I_{\text{rms}}}{\partial Z_B}\right]\Bigg|^T_{\boldsymbol{x}^{(k)}}. \quad (24)$$

The ZVS constraints are imposed next. This requires the computation of the vectors, $\boldsymbol{\lambda}_{\text{sc}}^{(k)}$ and $\boldsymbol{\lambda}_{\text{dc}}^{(k)}$, normal to the constraints, g_{sc} and g_{dc}, respectively.

$$\boldsymbol{\lambda}_{\text{sc}}{}^{(k)} = \left[\frac{\partial g_{\text{sc}}}{\partial n} \quad \frac{\partial g_{\text{sc}}}{\partial Z_B}\right]\Bigg|^T_{\boldsymbol{x}^{(k)}}, \boldsymbol{\lambda}_{\text{dc}}{}^{(k)} = \left[\frac{\partial g_{\text{dc}}}{\partial n} \quad \frac{\partial g_{\text{dc}}}{\partial Z_B}\right]\Bigg|^T_{\boldsymbol{x}^{(k)}}. \quad (25)$$

The analytical formulation proposed in Section II in terms of the design parameters is suitable to evaluate the derivatives in (24) and (25). The constrained gradient update term, $\boldsymbol{\Delta}^{(k+\frac{1}{2})}$, is obtained from $\boldsymbol{\Delta}^{(k)}$ by removing the update component that is orthogonal to the constraint boundary, as (26).

$$\boldsymbol{\Delta}^{(k+\frac{1}{2})} = \begin{cases} \boldsymbol{\Delta}^{(k)} - \frac{(\boldsymbol{\Delta}^{(k)} \cdot \boldsymbol{\lambda}_{\text{sc}}{}^{(k)})}{|\boldsymbol{\lambda}_{\text{sc}}{}^{(k)}|^2}\boldsymbol{\lambda}_{\text{sc}}{}^{(k)}, & \text{if } g_{\text{sc}}(\boldsymbol{x}^{(k+\frac{1}{2})}) \geq 0 \\ \boldsymbol{\Delta}^{(k)} - \frac{(\boldsymbol{\Delta}^{(k)} \cdot \boldsymbol{\lambda}_{\text{dc}}{}^{(k)})}{|\boldsymbol{\lambda}_{\text{dc}}{}^{(k)}|^2}\boldsymbol{\lambda}_{\text{dc}}{}^{(k)}, & \text{if } g_{\text{dc}}(\boldsymbol{x}^{(k+\frac{1}{2})}) \geq 0 \\ \boldsymbol{\Delta}^{(k)}, & \text{otherwise.} \end{cases} \quad (26)$$

The parameter vector is then updated as (27).

$$\boldsymbol{x}^{(k+1)} = \boldsymbol{x}^{(k)} - \boldsymbol{\Gamma}\boldsymbol{\Delta}^{(k+\frac{1}{2})}. \quad (27)$$

The initial guess for the turns ratio, $n^{(0)}$, is selected as per the conventional design approach such that the transformer primary and secondary voltages are matched at the nominal SC voltage. The initial guess for the base impedance, $Z_B^{(0)}$, is selected to obtain a worst-case phase shift of $\pi/4$. The initial parameter guess is summarized as (28).

$$\boldsymbol{x}^{(0)} = [n^{(0)}\ Z_B^{(0)}]^T = \left[\frac{V_B}{V_{\max}} \quad \frac{3\pi}{16}\frac{V_{\min}}{V_{\max}}\frac{V_B^2}{P_b}\right]^T \quad (28)$$

The gains, γ_1 and γ_2, are tuned by trial and error. The optimized design parameters, $\{n^*,\ Z_B^*\}$, are outputs of the

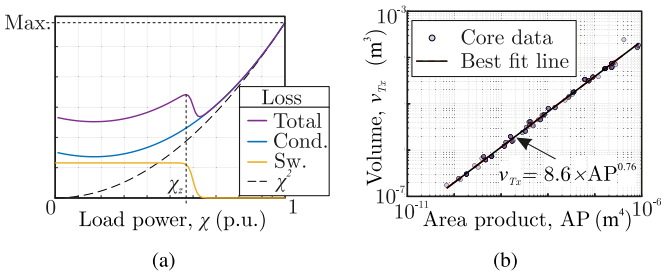


Fig. 5. (a) Variation of the power dissipation in a single device according to the rms current objective in (14) showing loss of ZVS at $\chi = \chi_z$. The capacitive turn-ON (Sw.) and conduction (cond.) components of the total loss are shown. A square function is also plotted to support the modeling of the conduction loss variation with power level presented in (29). (b) Variation of volume with area product for commercially available ferrite E-cores.

optimization. The rms current is fixed at this stage of the design, allowing the selection of the semiconductor devices.

C. Selection of Switching Frequency

The base impedance (Z_B) in (1) is a product of two parameters, namely, the coupling inductance (L_r) and the switching frequency (f_{sw}). The choice of switching frequency is constrained by considerations of switching loss at reduced power and also by the volume of magnetic components.

ZVS constraints in the design are imposed only at nominal power and ZVS is not guaranteed at lower power levels. At reduced power, even if one of the full bridges loses ZVS operation, the consequent rise of switching loss ($P_{l,\text{sw}}$) in the semiconductor devices is compensated by the reduction in the conduction loss in the devices ($P_{l,\text{con}}$). To ensure that device cooling arrangements are sufficient even at reduced load conditions, the switching frequency is selected such that the higher switching loss is completely offset by the lower conduction loss. The following discussion employs the subscripts, 1 and 2, for dc- and SC-side MOSFET full bridges.

The load condition is represented as a fraction, χ, of the nominal power. Since the terminal voltage range of the DAB is fixed, the rms current also scales in approximate proportion to χ. Thus, the conduction loss scales approximately as χ^2, illustrated by the dashed line in Fig. 5(a). If r_1 and r_2 are the respective device ON resistances of the dc- and SC-side MOSFETs, the dependence of the conduction loss on the power level is given by (29).

$$P_{l,\text{con},1} = (\chi I_{\text{rms}})^2 \frac{r_1}{n^2}, \quad P_{l,\text{con},2} = (\chi I_{\text{rms}})^2 r_2 \tag{29}$$

ZVS is lost at a reduced load condition, $\chi = \chi_z < 1$. The capacitive turn-ON loss, which is the significant component of the resulting increase in switching loss [30], is considered. The expression for this loss is given, in terms of the energy-equivalent device output capacitances, C_1 and C_2, as (30).

$$P_{l,\text{sw},1} = \frac{f_{\text{sw}} C_1 V_{\text{dc}}^2}{2}, \quad P_{l,\text{sw},2} = \frac{f_{\text{sw}} C_2 V_{\text{max}}^2}{2} \tag{30}$$

For each device, the total loss without ZVS must be less than the total loss at the nominal condition ($\chi = 1$). Hence, the higher switching loss at reduced load is fully offset by the lower conduction loss. This condition is expressed as (31).

$$P_{l,\text{con}}|_{\chi=1} - P_{l,\text{con}}|_{\chi=\chi_z} \geq P_{l,\text{sw}} \tag{31}$$

The upper limit on switching frequency is obtained as (32) by substituting the relations in (29) and (30) into (31).

$$f_{\text{sw}} \leq 2(1-\chi_z^2) I_{\text{rms}}^2 \min\left(\frac{r_1}{n^2 C_1 V_{\text{dc}}^2}, \frac{r_2}{C_2 V_{\text{max}}^2}\right) \tag{32}$$

The inclusion of the transformer leads to a larger volume of the DAB in comparison to nonisolated PEI topologies. The lower bound on the switching frequency is selected to limit the volume of the transformer (ν_{Tx}) to a fraction, y, of the volume of the SC stack (ν_{SC}), as (33).

$$\nu_{Tx} \leq y \nu_{\text{SC}}. \tag{33}$$

The volume of the transformer is estimated from the area product of its core (AP). The area product is inversely proportional to f_{sw} and depends on other design-specific quantities that are combined into a constant, K_{Tx}. The frequency dependence of the area product is thus expressed as (34).

$$\text{AP} = \frac{K_{\text{Tx}}}{f_{\text{sw}}}. \tag{34}$$

For commercially available ferrite E-cores, the dependence of the core volume on the area product is plotted in Fig. 5(b). A straight line is fit onto the log–log data to obtain the relation between the volume (ν_{Tx}) and the area product (AP), as (35).

$$\nu_{\text{Tx}}[\text{in m}^3] = 8.6\,(\text{AP}[\text{in m}^4])^{0.76} \tag{35}$$

The exponent, 0.76, is supported by dimensional analysis, since the volume and the area product are proportional to the third and fourth powers, respectively, of linear dimension. The transformer volume is designed to be a fraction of the SC stack volume. The relations (33), (34), and (35) are combined to obtain the lower switching frequency limit as (36).

$$K_{\text{Tx}} \left(\frac{8.6}{y \nu_{\text{SC}}}\right)^{1/0.76} \leq f_{\text{sw}} \tag{36}$$

The complete flow of the proposed design strategy is summarized in Fig. 6. The present work does not focus on the optimization of magnetic components; a detailed discussion on magnetics in a DAB application is presented in [31]. However, the selection and design of the inductor and the transformer are briefly outlined in Section IV-B.

D. Considerations of Core Losses in Magnetic Components

In the foregoing analysis and optimization, core losses in magnetic components (transformer, inductor) are not explicitly considered in the design formulation. However, these considerations are implicit in the optimization, as elaborated next.

Core losses depend on the switching frequency and the waveform of magnetic flux density, or, in the original Steinmetz relation, on the peak flux density. In the proposed design, the switching frequency is selected based on considerations of device switching losses and transformer size; the peak flux density

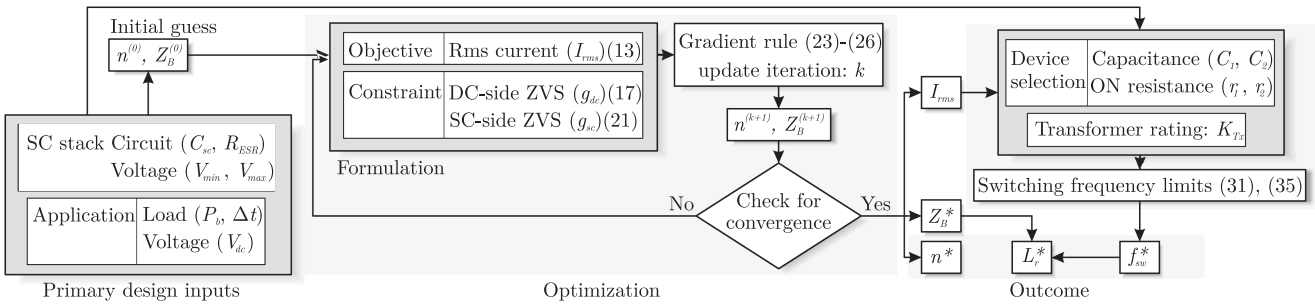


Fig. 6. Flowchart summarizing the proposed design optimization of the DAB.

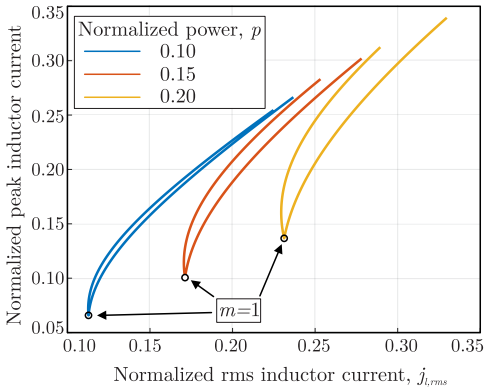


Fig. 7. Variation of normalized peak inductor current with normalized rms inductor current at three normalized power levels, showing a strong positive correlation of the two quantities.

is an available degree of freedom to reduce core loss. This quantity is dictated by the peak current and the applied voltage, in the inductor and the transformer, respectively.

In the case of the transformer, the applied voltage on the secondary (SC-side) winding is fixed by the SC voltage, which, for the present application, is a design input. Hence, this applied voltage, and hence the peak flux density, does not lend itself to further modification through circuit design alone.

The peak current through the inductor, which affects its peak flux density, can be minimized through circuit design. The proposed design executes the minimization of the rms current, rather than the peak current; however, these quantities are strongly correlated at a given terminal condition. A plot of the normalized peak current and the normalized rms current of the DAB under SPS modulation is presented in Fig. 7. In general, as $j_{L,\mathrm{rms}}$ reduces, so does the normalized peak inductor current, as evident from the plot. Hence, the minimization of the peak inductor current is implicit in the proposed optimization procedure.

Thus, the core loss in the transformer is insensitive to the proposed design procedure, and the approximate minimization of the core loss in the inductor is implicit in the method.

E. Comparison With Existing Design Algorithms

The proposed design optimization is suitable for the SC application under consideration. Existing methods for the optimization of the design of the DAB consider a worst-case or multi-operating-point rms current or efficiency, rather than that over the operating interval. Although the discharging cycle efficiency is considered in [19], this work does not consider ZVS constraints and is not suitable to address switching loss, and hence, overall efficiency. Further, the systematic implementation of the optimization is not clearly described in [20], which considers a linear scan of the search space, in [31], which selects the parameters based on qualitative arguments, or in [32], which utilizes a proprietary software library. The method outlined in [21] is applicable to the present scenario, except that the minimization objective does not coincide with overall discharge-cycle efficiency. Further, the online modulation parameter optimization described in [33] does not consider the optimization of the circuit parameters. The proposed design approach addresses these issues in existing design methodologies and is suitable for the SC application considered. The comparison of the proposed technique with design strategies in the literature is summarized in Table III.

IV. Design Optimization Example

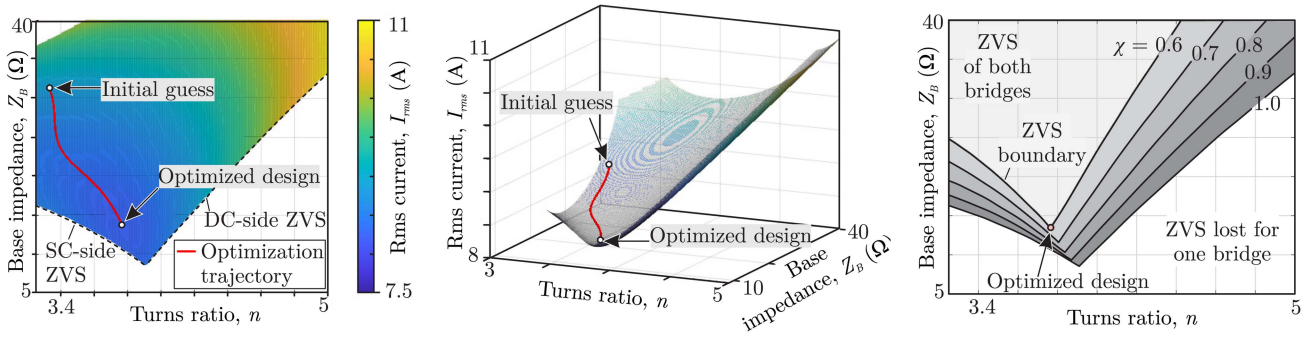
The foregoing design optimization is executed for an SC-DAB system whose ratings and parameters are presented in Tables IV and V, respectively. The ratings of the prototype are scaled down from the ratings of a target application, also given in Table IV. In particular, the maximum voltage, 120 V, of the SC in the target application corresponds to the rated voltage of a stack with 40× Maxwell BCAP0050P300X11 SCs. The minimum voltage, 102 V, is selected to utilize both the energy and power limits of the stack. The scale factor for voltage is 3.2X, while that for power is (3.2^2 =) 10X.

A. Design Outcome

The optimization trajectory in the space of design parameters is shown in Fig. 8(a). The avail of the optimization is illustrated by the separation in the design space between the initial guess based on the conventional design approach, and the optimized design. The variation of the minimization objective, I_{rms}, over the design space is illustrated in Fig. 8(b). The rms current does not reduce monotonically with the parameter Z_B, as discussed in Section III-A. Fig. 8(b) also verifies the convergence to the unique minimum rms current. The outcome of the optimization is presented in Table VI. The optimized design is contained within the region in the design space where ZVS is achieved over

TABLE III
COMPARISON OF PROPOSED DAB DESIGN OPTIMIZATION METHODOLOGY WITH METHODS IN THE LITERATURE

Design	Modulation	Optimization				ZVS
		Mode	Objective	Parameters	Algorithm	
Ref. [19]	SPS	Offline	Discharging interval rms current	Circuit parameters (n, L_r)	Gradient descent	No
Ref. [20]	SPS	Offline	Multi-point rms current	Circuit parameters (n, L_r)	Linear search	Yes
Ref. [21]	TPS	Offline	Worst-case rms current	Circuit parameters (n, L_r)	Lagrange multipliers	Yes
Ref. [31]	Asymmetrical	Offline	ZVS range	Circuit parameters (n, L_r)	Heuristic	Yes
Ref. [32]	TPS	Offline	Multi-point rms current	Circuit parameters (n, L_r)	Proprietary software	Yes
Ref. [33]	TPS	Online	Worst-case peak current	Modulation parameters	Improved Lagrange extreme	Yes
Proposed	SPS	Offline	Discharging interval rms current	Circuit parameters (n, L_r)	Projected gradient descent	Yes



(a) (b) (c)

Fig. 8. (a) Optimization trajectory in the design space with the rms current objective represented using a color gradient. The ZVS boundaries of SC- and DC-side full bridges are also marked. (b) 3-D plot of objective function showing the identification of the minima of the objective function through the optimization. (c) Dependence of the ZVS boundaries on the operating power of the SC, represented as a fraction, χ, of nominal power. The location of the optimized design in the design space is marked.

TABLE IV
ACTUAL AND SCALED RATINGS OF THE DAB INTERFACED SC

	Target application	Scaled
DC bus voltage, V_{dc}	400 V	125 V
Backup power, P_b	2.5 kW	250 W
Support duration, Δt	1.0 s	1.0 s
Maximum SC voltage, V_{max}	120 V	37.5 V
Minimum SC voltage, V_{min}	102 V	31.9 V

TABLE V
CIRCUIT PARAMETERS OF THE DAB INTERFACED SC

SC capacitance, C_{sc}	1.25 F
SC ESR, R_{ESR}	0.38 Ω
DC bus capacitance, C_{dc}	22 μF

TABLE VI
OUTCOME OF THE DESIGN OPTIMIZATION

Optimized turns ratio, n^*	3.77
Optimized base impedance, Z_B^*	13.6 Ω
Minimized secondary rms current, I_{rms}	8.2 A
Load fraction for loss-of-ZVS, χ_z	0.6

the entire SC operating range, as shown in Fig. 8(a). However, this region constricts with decrease in load power, as illustrated in Fig. 8(c), to eventually exclude the optimized design. For the present design, ZVS is lost at a fraction, $\chi_z = 0.6$, of the nominal power. ZVS is always lost at light load for the SPS modulation under consideration, but the total device power loss, following

TABLE VII
EXTRACTED PARAMETERS OF THE SEMICONDUCTOR DEVICES

	DC-side ($i = 1$)	SC-side ($i = 2$)
Output capacitance, C_i (nF)	0.30	1.12
On resistance, r_i (mΩ)	40	20

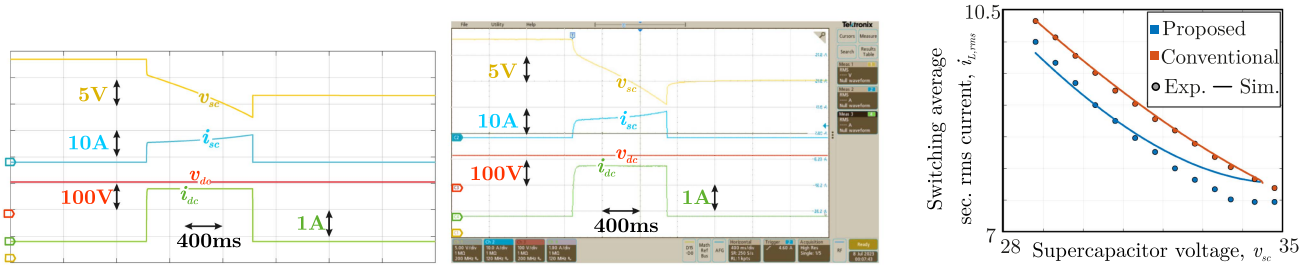
loss of ZVS, is not allowed to increase by selecting the switching frequency as per (32).

The ON resistance and energy-equivalent output capacitance parameters of the SC- (ST SCTH100N65G2-7AG, 650 V, 95 A, 20 mΩ) and dc-side (Cree C3M0040120J1, 1.2 kV, 64 A, 40 mΩ) SiC MOSFETs, extracted from the respective data sheets, are presented in Table VII. The optimization outcome and the device parameters, presented in Tables VI and VII, respectively, are substituted in (32) to obtain the upper limit on switching frequency.

The volume of the SC stack is obtained for the ratings of Table IV considering a nominal power density of 2 kWL^{-1} for the SC. The planar transformer design considers a peak flux density of 0.2 T, an rms current density of 6 A mm^{-2}, and a window fill-factor of 0.1. The lower limit of switching frequency is selected according to (36) such that the transformer volume is at most 10 % of the SC stack volume.

From the preceding considerations, the limits on switching frequency are obtained as (37).

$$37.5\text{kHz} \leq f_{sw} \leq 51.6\,\text{kHz}. \tag{37}$$



(a) (b) (c)

Fig. 9. (a) Simulated and (b) experimental waveforms of the SC-side and DC-side voltages and currents for SC discharging at 250 W over a 1 s interval. (c) The variation of simulated and experimental switching-cycle rms currents over the SC voltage range for both conventional and proposed designs.

TABLE VIII
DESIGN CONSTRAINTS AND PARAMETERS OF THE FABRICATED PLANAR TRANSFORMER

Peak flux density	0.2 T
Rms current density	6 A mm^{-2}
Window fill factor	0.1
Core	2 × ELP64/10/50
Primary turns, N_1	15
Secondary turns, N_2	4
Interleaving	P-S-P-S-P

TABLE IX
DETAILED SPECIFICATION OF THE OPTIMIZED DAB PROTOTYPE

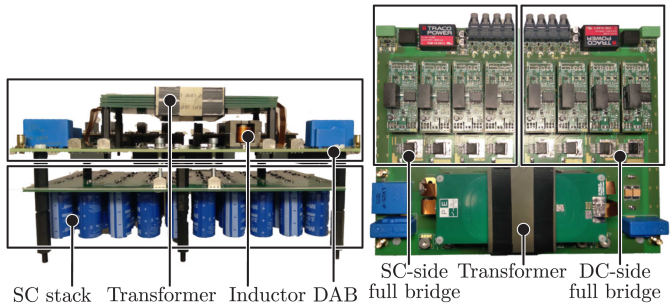
Primary (dc bus) voltage, $V_{\rm dc}$	125 V
Secondary (SC) voltage, $v_{\rm sc}$	31.9 – 37.5 V
Output power, P_b	250 W
Switching frequency, $f_{\rm sw}$	50 kHz
Turns ratio, n	3.73:1
Coupling inductance, L_r	41.6 µH
DC bus capacitance, $C_{\rm dc}$	22 µF

A switching frequency, $f_{\rm sw}^* = 50$ kHz, is selected. The coupling inductance, $L_r^* = 43.3\,\mu$H, is subsequently obtained using (1). The detailed specifications of the DAB are given in Table IX.

B. Realization of Magnetic Components

The required inductance is realized using two commercial 20 μH inductors in series. For this purpose, EPCOS-TDK B82559A0203A024 flat wire inductors, rated 24 A and with 3.4 mΩ dc resistance, are selected. The series resistance of each inductor is measured to be 360 mΩ at 50 kHz, so that the current derating factor at switching frequency is approximately 10X. Thus, the inductor is suitable for the 2.5 A primary current for the present exercise.

The transformer is designed using the area-product method outlined in [34], considering the design constraints given in Table VIII. The transformer design outputs are also summarized in Table VIII. A planar design is executed using two ELP 64/10/50 cores. The 15:4 winding is realized using three primary-side (P) PCBs with five turns each, and two secondary-side (S) PCBs with two turns each. The windings are interleaved in a P-S-P-S-P order to minimize leakage inductance and stray loss.



(a) (b)

Fig. 10. (a) Front view, and (b) top view of the SC interface DAB prototype.

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed design optimization is verified in circuit simulation and also on a laboratory prototype, shown in Fig. 10. The simulations and experiments are performed with two sets of circuit parameters: those recommended by the conventional design strategy, and those obtained through the proposed design optimization. The SC discharging is simulated for the ratings given in Table IV, with the operating waveforms of the SC and the dc bus presented in Fig. 9(a). The corresponding experimental waveforms are presented in Fig. 9(b). An appreciable voltage drop in the ESR of the SC is observed both in simulation and experiment, validating the inclusion of the ESR-adjusted voltage limits, $m_{\rm min}$ and $m_{\rm min}$, in the design.

Suitable computation blocks are used in simulation to extract the secondary (SC-side) switching-cycle rms current. The variation of this quantity over the ESR-adjusted voltage range is plotted for both designs in Fig. 9(c). The switching-cycle rms current is consistently lower in the proposed design. The accurate extraction of the switching-cycle rms current in SC discharging experiments requires the sampling of the current at a rate much higher than the switching frequency. This complication is avoided by recording the rms current at individual experimental steady-state operating points, each of which occur during SC discharging. The simulated and experimental operating waveforms of the DAB at three such steady-state operating points of the optimized design, are presented in Fig. 11. The waveforms illustrate the fact that the proposed design matches

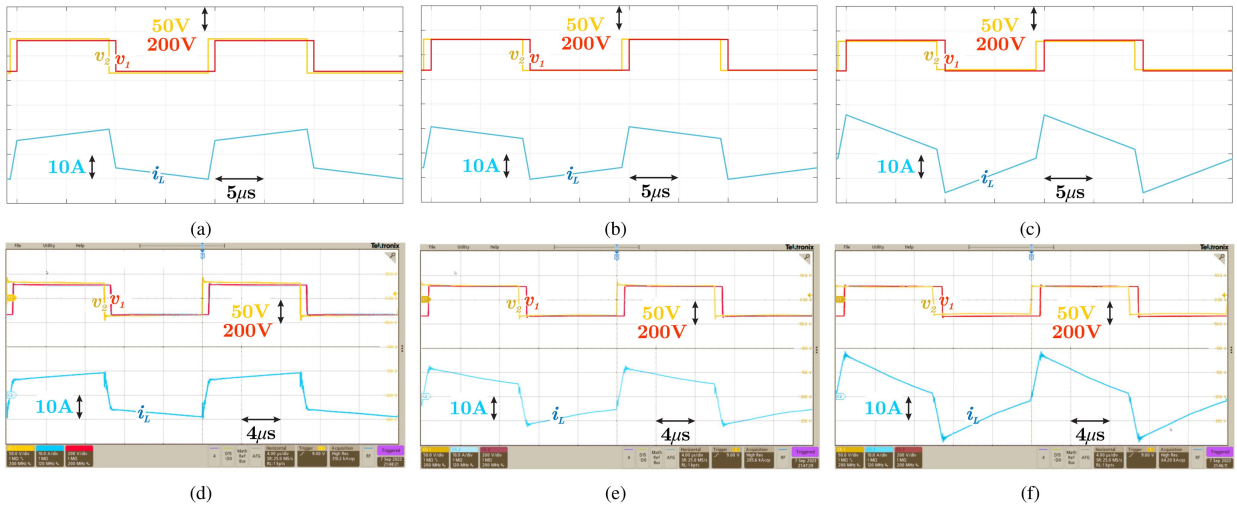


Fig. 11. Operating waveforms of the DAB in the SC discharging mode. Simulated waveforms at (a) maximum SC voltage, $v_{sc} = 34.8$ V, (b) intermediate SC voltage, $v_{sc} = 31.8$ V, and (c) minimum SC voltage, $v_{sc} = 28.8$ V. Corresponding experimental waveforms at (d) maximum, (e) intermediate, and (f) minimum SC voltage.

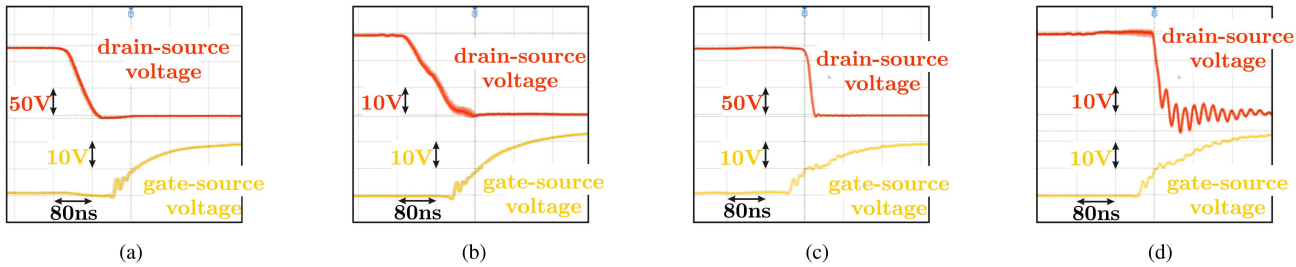


Fig. 12. Experimental drain-source and gate-source voltage waveforms of the DAB at nominal power for the (a) DC-side MOSFET at maximum SC voltage, and (b) SC-side MOSFET at minimum SC voltage, with ZVS achieved in both cases. Corresponding waveforms at $\chi = 60\%$ of nominal power for the (c) DC-side MOSFET at maximum SC voltage, and (d) SC-side MOSFET at minimum SC voltage, exhibiting loss of ZVS in both cases.

TABLE X
COMPARISON OF THE PERFORMANCE OF CONVENTIONAL AND PROPOSED APPROACHES FOR THE DESIGN OF THE SC INTERFACE DAB

Design approach	Turns ratio, n	Inductance L_r (μH)	Rms current					ZVS		Efficiency†	
			An. (A)	Err. (%)	Sim. (A)	Err. (%)	Exp. (A)	DC side	SC side	Sim. (%)	Exp. (%)
Conventional [13]	3.33	45.6	8.53	3.8	9.03	1.8	8.87	Yes		94.12	93.25
Proposed	3.73	41.6	8.24	2.0	8.59	2.1	8.41	Yes		95.84	95.04

† Evaluated over the entire discharging cycle. An. = Analytical, Sim. = Simulated, Exp. = Experimental, Err. = error with respect to experiment.

transformer primary and secondary voltages at an intermediate-voltage operating point.

The experimental values of switching cycle rms current, obtained from these individual steady-state operating points, is overlaid on Fig. 9(c). The experimental currents for both designs follow the same trend as in simulation. The marginally lower values of experimental rms current are attributed to increased converter efficiency at these operating points.

The rms current over the discharging interval, I_{rms}, is calculated in simulation and from the analytical expressions. The steady-state data are used to calculate the experimental I_{rms}, using a discrete form of the integral in (12). The rms currents are compared for the proposed and conventional approaches in Table X. The analytical, simulated, and experimental currents are in mutual agreement with a worst-case error of less than 5%. Further, the proposed design achieves a 5% reduction in rms current compared to the conventional design, corresponding to a 10% reduction in conduction loss.

The ZVS behavior discussed in Section II-E illustrates the fact that dc-side and SC-side ZVS are lost at higher and lower values of SC voltage, respectively. Hence, ZVS over the whole operating range is confirmed by verifying the ZVS of the dc-side and the SC-side bridges at the maximum and minimum SC voltages, respectively. The gate-source and drain-source voltage waveforms corresponding to these conditions are presented in Fig. 12(a) and 12(b), respectively. ZVS is achieved at each of these operating points, and hence over the entire SC operating region. Since both designs achieve ZVS for both bridges, their switching losses are low and comparable.

At $\chi = 60\%$ of the rated load in the optimized design, ZVS is lost for the dc-side bridge at the maximum SC voltage, and for the SC-side bridge at the minimum SC voltage. This is illustrated by

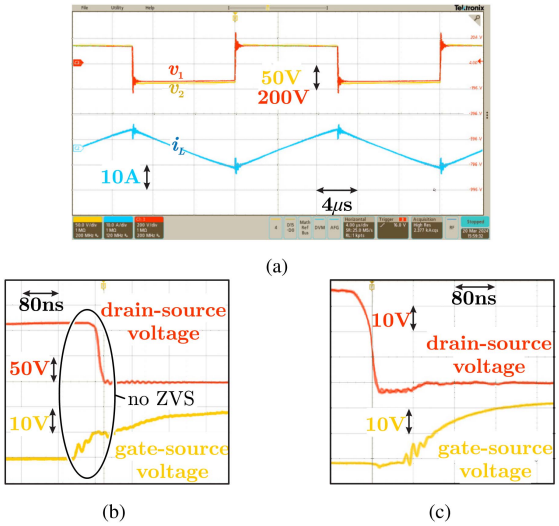


Fig. 13. (a) Operating waveforms of the DAB at light load (10 W) and nominal SC voltage (37.5 V). Gate-source and drain-source voltage waveforms at the MOSFET turn-on transitions, showing (b) loss of ZVS for the DC-side bridge, and (c) ZVS for the SC-side bridge.

the drain-source and gate-source voltage waveforms presented in Fig. 12(c) and 12(d), respectively, and validates the loss-of-ZVS load condition obtained in Fig. 8(c). ZVS is also lost for still lighter load conditions. Operating waveforms at very light load (10 W) and nominal SC voltage (37.5 V) are presented in Fig. 13, illustrating the loss of ZVS for the dc-side MOSFETs.

The efficiency of the DAB over the entire SC discharging interval is of interest, rather than the efficiency at a particular operating condition. The discharging efficiency is obtained from simulation as the ratio of output and input energy, corresponding to the dc and SC sides, respectively, considering datasheet and measured values of series nonidealities. As with the rms current, the discharging efficiency in experiment is obtained by a weighted average of the efficiencies at discrete operating points. The time spent at each operating point is used as the weight. The average efficiency over the discharging interval for both designs is recorded in Table X. In both simulation and experiment, the efficiency of the proposed design is about 2% higher than the conventional case. The simulated efficiency is higher in general due to magnetic and switching losses being neglected. The SC losses depend only on the power level and not on the rms current of the DAB. These losses are hence considered the same in both designs.

The detailed analytical breakdown of the experimental power loss is presented in Fig. 14. The total power loss is measured using a Yokogawa WT1800 precision power analyzer. The ON resistances of the MOSFETs are obtained from device datasheets, and the winding resistances of the inductor and the transformer are measured using a Keysight E4990 A impedance analyzer. These parameters, given in Table XI, are used along with the experimentally measured rms currents to estimate the conduction loss components. The peak flux density of the transformer and the inductor are estimated from the applied voltage and the peak current, respectively, obtained from experiment. The core losses

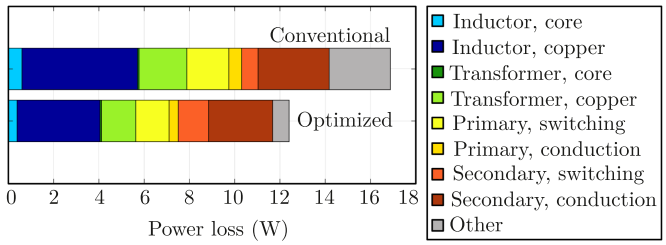


Fig. 14. Analytical breakdown of experimental power loss over the complete discharging interval for the conventional and optimized designs.

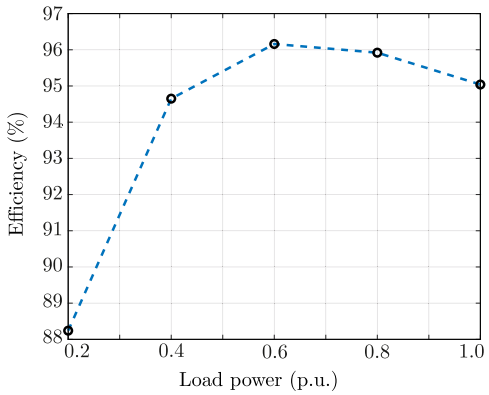


Fig. 15. Plot of the variation of experimental discharging efficiency of the DAB with the per-unit (p.u.) load power level.

TABLE XI
MEASURED AND DATASHEET NON-IDEALITIES OF THE DAB PROTOTYPE

Primary (DC-side) MOSFET on resistance	40 mΩ
Secondary (SC-side) MOSFET on resistance	20 mΩ
Inductor series resistance	720 mΩ
Transformer series resistance†	298 mΩ
Transformer leakage inductance†	1.92 μH
Transformer magnetizing inductance†	2.31 mH
Transformer parasitic capacitance†	48.1 pF

† Referred to the HV (primary) side.

are then obtained from the corresponding magnetic loss curves given in the ferrite material datasheets. The device turn-OFF losses are estimated using the measured current at the switching instant; turn-ON losses are assumed to be absent due to ZVS over the entire operating range. In both designs, the conduction loss in the secondary (SC-side) MOSFETs is significant due to the high SC current. The reduction in conduction loss components in the optimized designs is evident from Fig. 14. The magnetic loss in the inductor is reduced in the optimized design due to lower peak currents, as discussed in Section III-D.

The variation of discharge efficiency with the load power is presented in Fig. 15. While the optimization is performed considering nominal power, the DAB exhibits an efficiency greater than 95% down to approximately 40% of the nominal load. The overall efficiency figure is on par with the maximum single-operating-point efficiency figure reported for the dual phase shift-modulated DAB in [13].

VI. Conclusion

This article proposes a circuit design optimization of the DAB converter for SC interface applications. The optimization aims to minimize the rms current and achieve ZVS by considering the terminal characteristics of the SC, including its ESR. The optimal parameter set is obtained by executing a constrained gradient optimization following an inspection of the design space. The choice of switching frequency is based on considerations of load variation and overall system size. The proposed design method is validated through simulation and experiment, and compared with a conventional design approach from the literature. The experimental results show improvements of 5% and 1.8% in rms current and efficiency, respectively, and demonstrate the effectiveness of the optimal formulation in achieving ZVS during the turn-ON process under different conditions.

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