Current Source Gate Drivers: Topologies, Applications, and Future Research Needs

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***Abstract*—The gate-driver circuits are required to control the switching dynamics of the power electronic (PE) devices. These gate drivers can be categorized as voltage-source drivers (VSDs) and current-source drivers (CSDs) based on their operating natures. The VSDs control the dynamics of the power device by means of an external gate resistor, which accounts for loss and it increases with switching frequency. On the other hand, CSDs with controlled gate current account for negligible loss and allow faster switching transition of the power device. This article provides a categorization of the prior-art CSDs based on their nature of operation and structural orientation. A comparative study is carried out between these CSDs based on the control switch count, switching frequency, and the passive components utilized. Furthermore, a case study of a representative CSD topology from each category is carried out and compared with the conventional VSD. An experimental setup for the double-pulse test is developed to prove the efficacy of CSD over VSD. It is observed that the power device when driven by CSD achieves lower turn-OFF and turn-ON times compared to VSD by 75% and 50%, respectively. The effectiveness of CSDs for various applications is also highlighted in this article.**

***Index Terms*—Current source gate driver (CSD), double pulse test (DPT), power electronic (PE) switch, voltage source driver (VSD), wide bandgap (WBG) devices.**

I. Introduction

In RECENT years, power electronic (PE) applications have seen vast growth due to various desired features, such as high power density, high efficiency, improved reliability, and enhanced control [1], [2], [3], [4], [5], [6]. This attributes to the developments in the PE switch technology and converter topologies. Nonetheless, only these advancements were not enough as the performance of the converter is highly dependent on the gate-driver circuit. The gate-driver circuits play an important role in the operation of the PE converter, where in addition to supplying the control signal to the switch, it also provides electrical isolation, required protection, and switching energy [7]. In a typical gate-driver circuit, the charge delivered to the power device is controlled to govern its switching performance. The method of driving the power device is determined by the nature of the signal applied across the gate or base terminal. As far as the FETs are concerned, it requires a constant voltage across its gate, while in the case of the bipolar junction transistors (BJTs), a constant current has to be fed into the base to drive the corresponding power device. Based on this, all the drivers discussed in the literature can be grouped into two categories, which are termed voltage-controlled gate driver (V-CGD) and current-controlled gate driver (C-CGD) [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64].

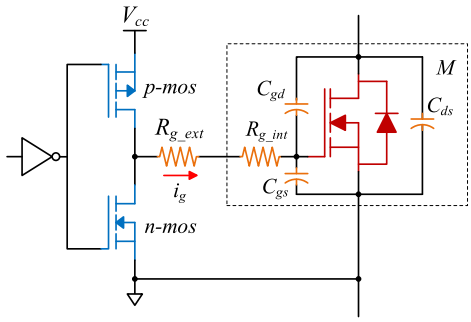

Fig. 1. Conventional totem-pole voltage-source gate driver [11].

Typically, in the V-CGD, the voltage at the gate terminal of the power device is adjusted to control its switching parameters, such as turn-ON and turn-OFF timings, ON-state voltage drops, and turn-OFF leakage current [8], [9]. V-CGDs can be classified according to their principles of operation, such as totem-pole drivers, Miller clamp-based drivers, and active gate drivers. The totem-pole gate driver has the simplest structure of all the V-CGDs, and hence, it is widely adopted in converters for driving power devices because of its ease of implementation. A generalized structure of the conventional totem-pole driver driving the power device denoted as *M* is depicted in Fig. 1. This power device is turned ON and OFF by the charging and discharging of the switch input capacitance ($C_{\text{iss}} = C_{\text{gs}} + C_{\text{gd}}$). Such an operation is termed the gating process in this article. Moreover, the turning ON and OFF of the power device is defined as switching transitions. The gate resistor ($R_{\text{g}} = R_{\text{g(ext)}} + R_{\text{g(int)}}$) and the switch input capacitance determine the duration of the

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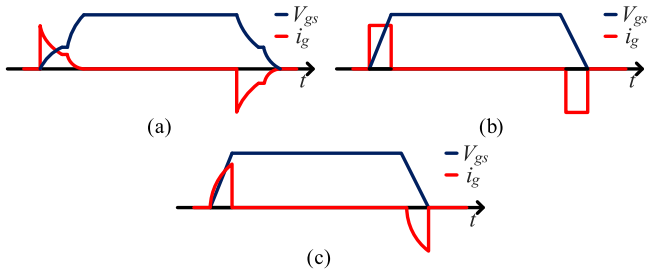

Fig. 2. Gate voltage and current. (a) VSD. (b) CSD. (c) RGD.

switching transitions [10]. It is to be noted that the duration of switching transitions can be varied by changing the value of the external gate resistor ($R_{g(ext)}$) (see Fig. 1), where a smaller value of $R_{g(ext)}$ achieves faster switching transitions, thereby reducing the switching loss of the power device. On the other hand, the larger value of $R_{g(ext)}$ slows down the switching transitions. However, this results in a longer switching time and larger switching losses [11]. Therefore, such drivers suffer from complex methodology for $R_{g(ext)}$ selection. In addition, $R_{g(ext)}$ also incurs power loss, which further increases with an increase in switching frequency [12].

In order to address the aforementioned challenges, the C-CGDs can be utilized. In C-CGDs, a constant gate current is provided throughout the gating process, which enables the fast switching transitions without the need of $R_{g(ext)}$. The key waveforms explanting the operating principle of V-CGDs and C-CGDs are depicted in Fig. 2(a) and (b), respectively. As can be seen in Fig. 2(a), in the case of the V-CGDs, the current decays over the switching interval, which results in a slow turn-ON of the power devices. On the other hand, the C-CGDs maintain a constant current throughout the switching transition, as can be seen in Fig. 2(b). In turn, the constant gate current causes faster charging and discharging of the C_{iss}, which henceforth results in a shorter switching transition time of the power device [13]. However, the fast switching transition of the power devices will result in a larger overshoot and oscillation in the switch voltage and current due to the presence of parasitic in the circuit.

Based on the principle of constant current generation, the C-CGDs can be categorized as resonant gate drivers (RGDs) and current source gate drivers (CSDs) configurations. In RGD, the current source is obtained by creating a resonance between the external inductor and the inherent gate–source capacitance (C_{gs}) of the switch, as shown in Fig. 2(c) [14], [15], [16], [17], [18], [19], [20], [21]. However, in order to maintain the continuous current throughout the gating process, a large-sized inductor is required in RGDs. This leads to an increase in the footprint of the driver and additional losses in the gate driver as well as in the switching device. It can be observed from Fig. 2(c) that the input gate current being not constant will cause slow charging and discharging of C_{gs}, and hence increased switching losses. Moreover, due to the fixed value of inductor and C_{gs}, the switching frequency of the power device remains fixed to the resonant frequency. Also, the peak value of the inductor current changes with the change in duty cycle, resulting in the uneven magnitude of the initial gate current during the switching of the power device [16]. The inductor current peak value increases with the increase in duty cycle and also the higher value of current into the gate of the power device may damage it. In the operation of RGD, the switching frequency of the power device is fixed over a single frequency, which is the function of the inductor value for the required input gate current. For applications with variable duty and switching frequencies, such as pulsewidth modulation (PWM) based converters, variable frequency motor drives, dual active bridges, and much more, these drivers are not capable of driving the power devices. A constant current source can be employed to resolve the aforementioned challenges during the switching transitions, thereby referred to as CSDs. The constant current prior to the switching transition in CSDs is achieved with the use of passive or active circuitry in conjunction with *nmos/pmos*, BJTs, or inductors. By using these additional circuits, the nonzero initial gate current results in a reduction of charging and discharging time of C_{gs}. This leads to faster turn-ON and turn-OFF of the power devices resulting in lower switching loss and enabling them for high switching frequency applications [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64].

Considering the afore-discussed benefits of the CSDs, significant research works are being carried out in developing its various configurations. The CSDs proposed in the literature were developed specifically to drive a power device in a particular converter operated over a single switching frequency [27], [33], [41]. Therefore, there is an added challenge in selecting the best CSD for a given application. Furthermore, with the recent developments in the power devices, such as wide bandgap (WBG) devices, it calls for the need for additional research in the gate driver's technology. The conventional voltage-source drivers (VSDs) are also not capable of driving these devices to their full extent due to the restriction incorporated by the higher switching frequency leading to an increase in driver losses. Moreover, the existing CSDs discussed in the literature were developed to drive the low-voltage devices at a very high frequency ranging from 500 kHz to a few megahertz. These existing CSDs can have the future potential to drive the WBG devices with higher voltage ratings at a very high frequency. However, the selection and utilization of the most appropriate CSDs is more challenging. In the literature, no such work has been reported on the analysis, comparison, and relative usefulness of the available driver solutions for the various power devices. However, a few literature reviews have presented comparative studies of V-CGDs and RGD, where they have categorized the gate drivers based on their application to different power devices, their working principle, and their effects on the switching dynamics [7], [10], [20], [21], [22], [23], [24]. As of yet, no such work is available, which provides a detailed overview of the CSD circuits that are currently been used. This article bridges the gap by providing a detailed classification of CSDs based on their operating principle and structural orientation in order to provide a brief understanding of and need for such drivers in the present converter technologies.

The contributions of this article are summarized as follows.

1) A detailed comparative investigation of all CSDs and their classification based on their nature of operation and structural orientation is presented.
2) A detailed case study is carried out to understand the operational behavior of the CSDs classified based on the nature of the operation. Furthermore, one-to-one comparisons of each driver and VSD are carried out and are investigated based on their nature of operation, switching dynamics, and losses.
3) An experimental investigation of a CSD and VSD is carried out to understand the difference in their operations and the benefits achieved by CSD over VSD.
4) The challenges in applications of the CSDs for WBG devices, series/parallel connections, high-voltage applications, and device protection are also discussed.
5) This research will be a useful reference point for the CSD developers and engineers, and help them in selecting optimal drivers for high-speed switching devices, ensuring they meet the specific requirements.

The rest of the article is organized as follows. In Section II, all the existing CSDs are classified based on their operating principles and structures. In Section III, a comprehensive comparative investigation is presented to analyze all the considered categories of the CSDs. Furthermore, to validate the operating principles of the various categorized CSDs, a case study is conducted by simulating a CSD from each category. To prove the effectiveness of CSD over VSD, an experimental study is carried out by developing a double-pulse test (DPT) setup in Section IV. Later, in Section V, the suitability and scopes of CSDs for various application scenarios are discussed. Finally, the conclusions are presented in Section VI.

II. Classification of CSDs

In spite of the variation in topologies, application scenarios, and control schemes among the CSDs, the majority of them were first derived from the conventional totem-pole driver topology. However, the CSDs differ in principle of operation, desired objective, and structural configuration. The main objective of CSD is to provide a constant gate current during the switching transition to achieve fast turn ON and turn OFF. This can be achieved by creating a current source, and based on the method of creation, the CSDs can be classified as inductor-based and inductorless CSDs.

In inductor-based CSD, an external inductor (L_r) is precharged from the driving source (V_{cc}) prior to the switching transition. This precharged inductor functions as a current source at the time of switching and provides almost constant current during the switching interval. The constant gate current accelerates the charging and discharging of the gate–source capacitor (C_{gs}), resulting in faster turn ON and turn OFF. The inductor-based CSD can be in general represented as shown in Fig. 3. With the terminals A and C connected together, the current in L_r starts to build up, and once the required peak is achieved, the terminals A and B are connected further. A constant current is then delivered to C_{gs} and provide fast switching. Some inductor-based CSD also offers other benefits, such as

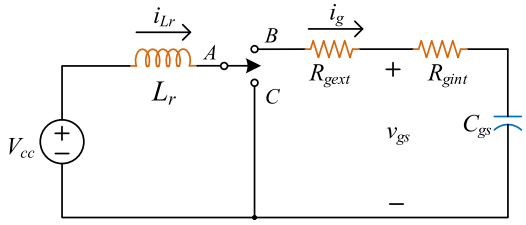

Fig. 3. Equivalent circuit of an inductor-based CSD.

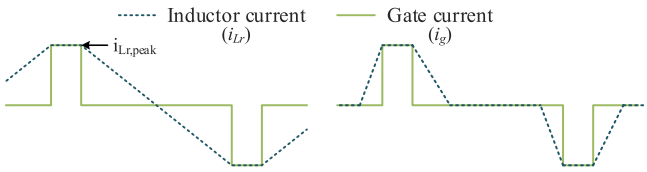

Fig. 4. Ideal gate and inductor current waveform of (a) continuous and (b) discontinuous CSD.

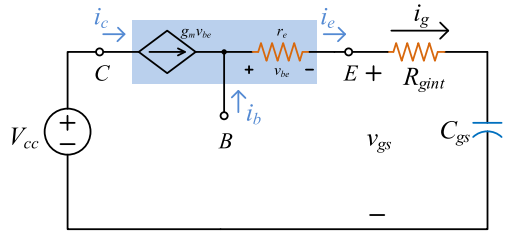

Fig. 5. Equivalent circuit of an inductorless CSD.

gate energy recovery in which the energy from C_{gs} is extracted to L_r during turn-OFF interval. By transferring the stored energy in L_r to V_{cc} by some external means will allow further improvement in driver efficiency. Based on the nature of current in L_r, as depicted in Fig. 4, the inductor-based CSDs are further subcategorized into continuous and discontinuous CSDs [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52]. The continuous CSD requires a larger inductor to maintain continuous current flow, as shown in Fig. 4(a), resulting in increased footprint, size, and conduction losses of the gate driver [25], [27], [29]. In contrast, the discontinuous CSD, with its inductor current nature, as shown in Fig. 4(b), will result in much lower conduction loss and require a much smaller inductor than the one in continuous CSD [39], [43], [45]. This results in a smaller footprint along with the enhanced efficiency of the driver. Furthermore, the inductor-based CSDs can provide a constant negative current during turn-OFF instant, which results in faster turning OFF of the power device and hence a shorter turn-OFF time.

In an inductorless CSD, a virtual current source is created using some transistor-based circuits, which provide a constant current during switching transitions. The general representation of inductorless CSD is shown in Fig. 5, which comprises a voltage-controlled current source. In Fig. 5, g_m stands for the transconductance of the transistor, which, in general, defines the value of current to be developed by the driver circuit [53]. Since these CSDs do not use inductors and associated circuitry,

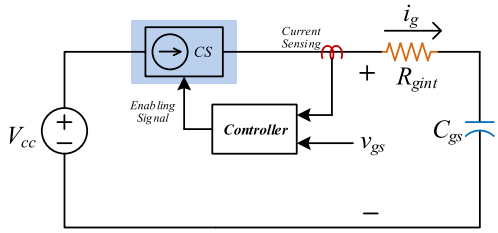

Fig. 6. Equivalent circuit of an ACSGD.

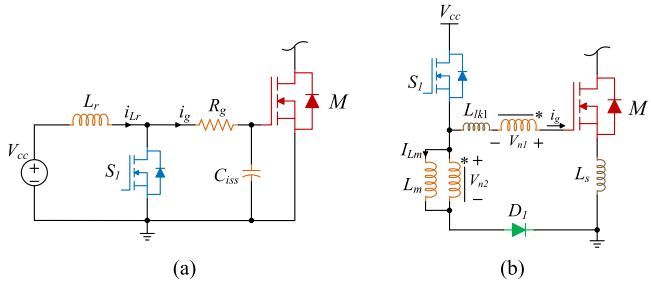

Fig. 7. (a) Single-switch sinusoidal CSD [25]. (b) Single-switch discontinuous CSD with voltage boosting capability [26].

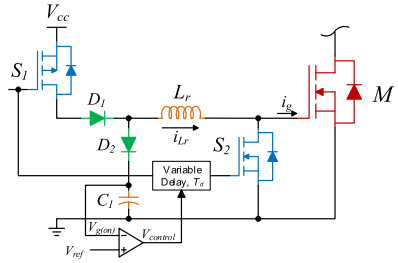

Fig. 8. CSD with controlled peak voltage [31].

the overall footprint of the driver is reduced. As a result, the complexity and propagation delays are also minimized. The existing inductorless CSDs primarily utilize transistor-based current mirror circuits that reflect the input current at the output terminal irrespective of load conditions [57], [59]. Cascode current mirror circuit is widely used in such drivers due to its higher current gain accuracy along with the large output impedance [56]. However, the absence of energy storing elements in these drivers makes them incapable of retrieving energy during turn-OFF intervals. The inductorless CSDs are further evolved with the ability to control the switching dynamics of the power semiconductor device by controlling the input gate current magnitude. These are termed active CSD (ACSD) with the equivalent circuit shown in Fig. 6. In these drivers, the controlled gate current is obtained with the help of an additional sensing unit to sense the power device parameters, such as switch current and voltage, as shown in Fig. 6. This sensing unit gives feedback to the gate driver, which, in turn, controls the gate current. However, the ACSDs require high-bandwidth comparators and complex control that are much more sensitive to the surrounding noise. Furthermore, to have a detailed understanding of all the existing CSDs and to gain insights into their configuration, they are classified based on their structural configuration into six classes, as discussed in the following section.

A. Classification Based on Driver Structure

A simple CSD is comprised of elements to control the gate current of the power device with the input from a controller. For this, the majority of the CSDs utilize one or more number of control switches, inductors, transformers, and voltage sources with single/multiple input gate command signals. Depending on the circuit configurations and the similarity of utilizing the aforementioned components, CSDs are classified into the following different classes.

1) Single-Switch CSDs: The first single-switch CSD has been reported in [25] to overcome the limitation of high-frequency operation in VSDs. The schematic of this driver is depicted in Fig. 7(a). The nature of the output voltage in this driver is similar to a sinusoidal waveform whose peak and frequency depend on the amount of energy stored in L_r. In this driver, the power device remains turned ON for the duration till the driver output voltage is higher than the power device threshold value. In addition, the variable output voltage of the driver results in higher conduction losses. In [26], another single-switch CSD, as shown in Fig. 7(b), has been proposed mostly suitable for ultralow voltage applications. The proposed gate driver features voltage boosting capabilities resulting in larger gate voltage, allowing reduction in ON-state resistance along with no current diversion problem. The current in both the inductor starts to build simultaneously by turning ON controls switch S. The energy stored in L_m is used for fast turn OFF of the power semiconductor device. The proposed gate driver when used to drive the switches of VRM module at 1 MHz switching frequency allows the improvement in overall efficiency by 5.7% compared to the conventional gate driver. However, the magnitude of the input gate current during the turn-OFF interval changes with the change in duty cycle, making the driver not much suitable for variable duty cycle applications. In order to have more control over the CSD's gate voltage and current, a new circuity was developed by including an additional control switch as discussed in the following.

2) Dual-Switch CSDs: With the addition of an extra control switch, the dynamics of both the driver and power device can be improved. This section discusses the dual-switch CSDs that utilize two control switches operating independently of each other. The first dual-switch CSD, as depicted in Fig. 8, has been reported for precise control over the energy in the driver along with maintaining the constant gate voltage during turn-ON [31]. As seen from Fig. 8, the charging of L_r in this driver is controlled by controlling the ON-period of control switch S_2. This is achieved by implementing a negative feedback loop, which compares the capacitor C_1 voltage with the required reference value. The aforementioned driver is implemented to drive the power device at 70 kHz with the input of 800 V and 10 A. The reduction of 20% in switching loss is reported in comparison to the conventional VSD. Moreover, the driver is also capable of eliminating the overshoot and ringing in

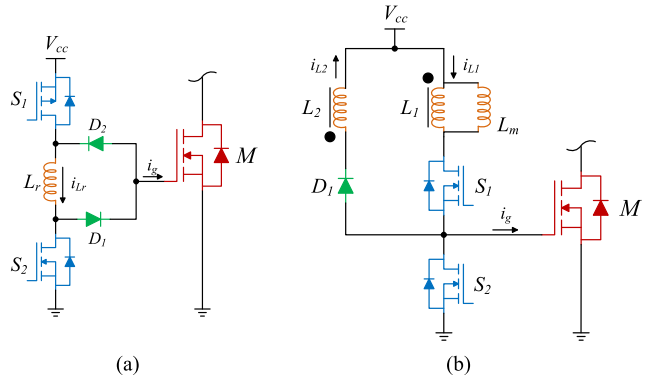

Fig. 9. (a) Megahertz switching speed CSD [32]. (b) CSD for narrow ON-time buck converter [33].

gate voltage due to the presence of diode D_1 in the circuitry. Furthermore, the diode D_1 prevents the ringing in gate–source voltage during the turn-OFF instant. In order to eliminate the need for an additional sensing circuit in the above-discussed CSD, a much more efficient driver is introduced with a dual-switch configuration, as depicted in Fig. 9(a) [32]. With both control switches turned-ON, L_r is charged for the given duration till the required current value is obtained. These control switches are later operated in a complementary manner for turning-ON and OFF of the power device. In addition to that, the diodes in this driver allow the clamping of gate terminal to V_{cc} after the power device is turned ON and the L_r acts as the energy storing element to store the gate energy. In comparison to conventional VSDs, the above-mentioned driver results in a 20% and 32% reduction in turn-OFF and turn-ON times, respectively, of the silicon carbide (SiC) MOSFETs when switched at 13.56 MHz [32].

Additional research in dual-switch drivers has been reported for applications requiring very short turn-ON periods. The earlier discussed driver lacks the ability to drive the power device in applications such as narrow ON-time buck converters due to the requirement of low duty cycle in the range of 2%–5%. This is due to the longer reversal time of current through the inductor prior to turning-OFF the power device. This challenge is addressed with the dual-switch driver with two separate inductors coupled to each other, as depicted in Fig. 9(b) [33]. In this driver, the inductor L_1 is precharged to provide a constant current during turning-ON the power device, while the additional inductor L_2 provides constant current at the time of turn-OFF. In this way, there is no need for current reversal in the inductor. This makes the driver capable of operating at a minimum duty cycle. In comparison to the conventional VSDs, the above-discussed driver improves the converter efficiency by 4.1% when operated for 1 MHz application [33]. However, the common problem existing in most of the inductor-based CSDs is the current diversion, which results in slower turning-OFF of the power device. In the following section, the underlying causes and their effects on the driver performance are discussed.

Another dual-switch driver to solve the current diversion problem existing in the afore-discussed CSDs is developed, as depicted in Fig. 10, presented in [34]. This driver is designed to drive the buck converter rated for 1.3 V/20 A switched at 1 MHz.

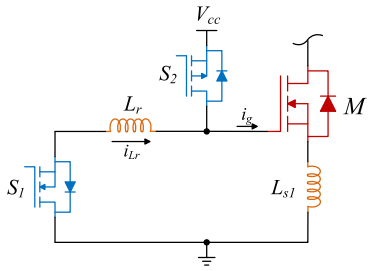

Fig. 10. CSD for overcoming the current diversion problem [34].

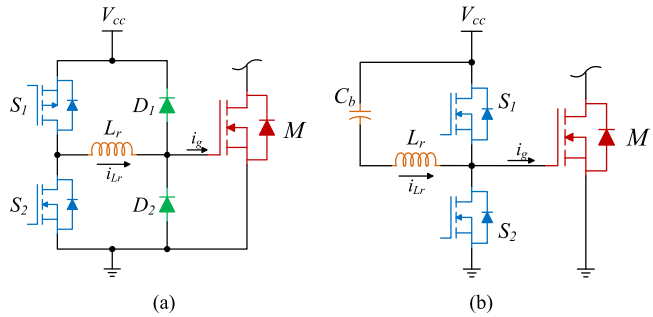

Fig. 11. (a) CSD with efficient energy recovery [35]. (b) Inductor-based continuous current half-bridge CSD [27].

The above-mentioned driver increases the converter efficiency by 4% over the CSD mentioned in [33] [see Fig. 9(b)] and by 7% over the conventional VSD. However, due to higher conduction losses in the above-discussed driver, they are only suitable for narrow ON-time applications. Furthermore, such drivers do not reduce the turn-ON losses, so they cannot be used in applications where the turn-ON loss is the most prevalent.

The further classification of the CSDs is drawn out based on their structural orientation similar to some existing configurations as well as based on the nature of control switches. One such configuration with two control switches, termed half-bridge, is discussed as follows.

3) Half-Bridge-Based CSDs: This category of CSDs includes the drivers with their structural orientation similar to the conventional half-bridge leg having two control switches operating in a complementary manner. The first such half-bridge-based CSD is reported to recover the excessive energy stored in L_r, as depicted in Fig. 11(a) [35], where the power device is turned ON with the zero initial gate current. After the power device is turned ON or OFF, the excessive stored inductor energy is reverted back with the conduction of freewheeling diodes D_1 and D_2. Moreover, the diode D_1 avoids the overshoot in gate voltage by clamping the gate terminal to V_{cc} during the turn-ON interval. For the switching frequency of 500 kHz, the above-discussed driver reports a reduction of losses by 45% in comparison to the conventional VSD. This driver is further developed to drive the gallium nitride (GaN) MOSFET switching at 5.55 MHz for integrated circuit applications [36]. However, the above-mentioned driver does not have the ability to provide a constant current during the turn-ON interval, which results in larger turn-ON time. This leads to a larger turn-ON losses in the power device. To

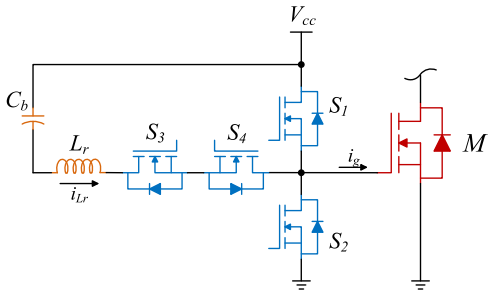

Fig. 12. Inductor-based discontinuous current half-bridge CSD [37].

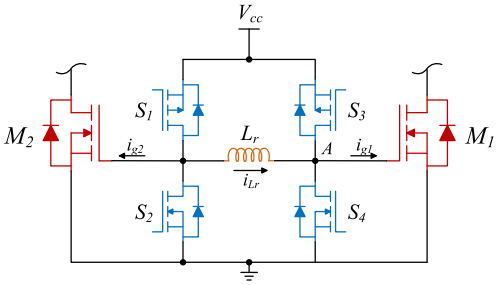

Fig. 13. Dual-channel CSD [29].

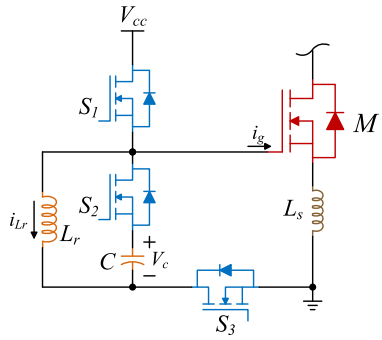

Fig. 14. CSD without current diversion at turn-OFF transition [38].

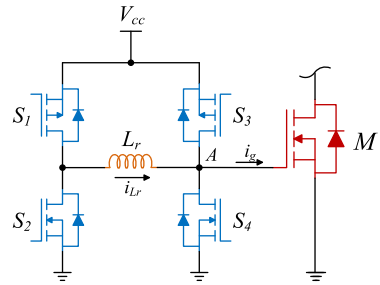

Fig. 15. CSD for switching loss saving and gate energy recovery [39].

overcome the above challenge, another such half-bridge-based CSD is reported, as depicted in Fig. 11(b), which has the ability to provide the constant current during the switching transitions [27], [28]. Prior to turning-ON the power device, current in L_r is build up in the positive direction, and while turning-OFF the current in L_r is reversed. During the switching instant, the driver provides nearly constant current resulting in faster switching of the power device. With the above-discussed CSD, the efficiency improvement of 3.3% is reported for the Si MOSFET driven at 1 MHz in the synchronous buck converter rated for 1.5 V/30 A. The problem associated with this driver is the need for large L_r and the continuous current in the driver circuit leads to additional conduction losses.

Further research is accompanied by the addition of an extra bidirectional control switch in series with L_r, as depicted in Fig. 12 [37]. This newly configured CSD operates similarly to the aforementioned CSD [see Fig. 11(b)]. Moreover, the additional control switches help in the generation of the discontinuous inductor current, resulting in lower conduction losses and smaller size of L_r. This leads to higher driver efficiency and power density. For the same synchronous buck converter rated for 1.5 V/30 A, the above-discussed driver improves the converter efficiency by 6.5% compared to the conventional VSD, both switched at 1 MHz frequency. The applications of these half-bridge drivers have been further extended to drive the two different power devices with a common source configuration. One such CSD is reported in [29], generally preferred for applications, such as current doubler, voltage/current fed push–pull, where the overlapping of the two gate pulses is required. The corresponding driver circuitry driving the two power devices is depicted in Fig. 13. This driver has a lower device count and can reduce the gate loss by almost 67% in comparison to the conventional VSD. Furthermore, a discontinuous CSD is proposed in [38], as shown in Fig. 14, to address the problem of current diversion during the turn-OFF instant. With S1 turn ON, the gate terminal is clamped to the positive driving voltage. Prior to turning OFF the main switch, the inductor is charged, which provides the required magnitude of gate current for faster turning OFF the switching device. Post turn OFF, the energy stored in the inductor causes the capacitor to charge and the negative voltage appears across the gate terminal of the device, which mitigates the current diversion problem. The energy transferring from the current source inductor to the capacitor causes the reversal of the inductor current. The current peak is then utilized for the switching ON the device. The initial nonzero gate current fastens the switching ON process and reduces the turn-ON time. However, the peak current during the turn ON is completely determined based on the turn-OFF period. Such CSDs are not suitable for variable duty cycle converters. In order to have more controllability over the inductor current along with gate energy recovery, additional research on the development of such CSD is reported with the addition of more control switches. Based on these, the following sections are introduced.

4) Full-Bridge-Based CSDs: This category of the CSD shares a similar structural representation to that of the full-bridge converters. The driver categories under this subgroup consist of two identical/nonidentical half-bridges connected together via an inductor. The first such full-bridge CSD is reported in [39], [40], [41], and [42] for achieving higher efficiency and gate energy recovery. The schematic of this driver is depicted in Fig. 15. The driver is demonstrated to drive the power device at 1 MHz switching frequency in a boost converter rated for 10 V/5 A. In comparison to the conventional VSD, the afore-discussed CSD

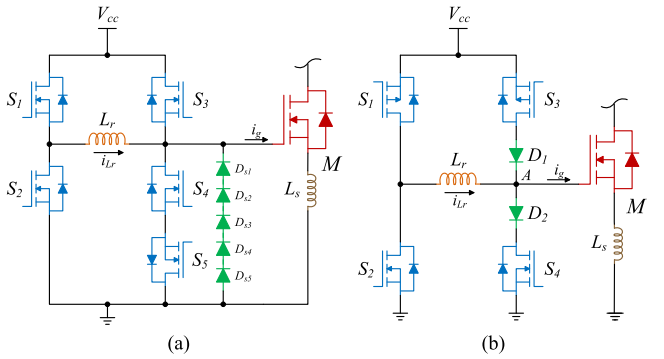

Fig. 16. (a) CSD with bipolar gate voltage [43]. (b) High-dynamic range CSD for switching loss reduction [45].

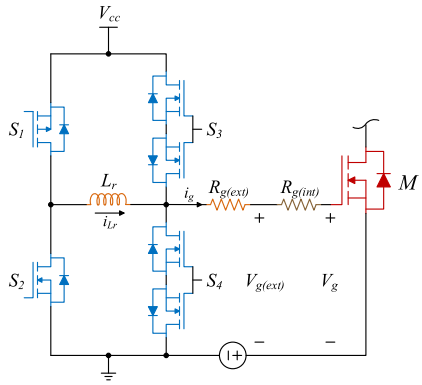

Fig. 17. CSD for maximizing switching speed [46].

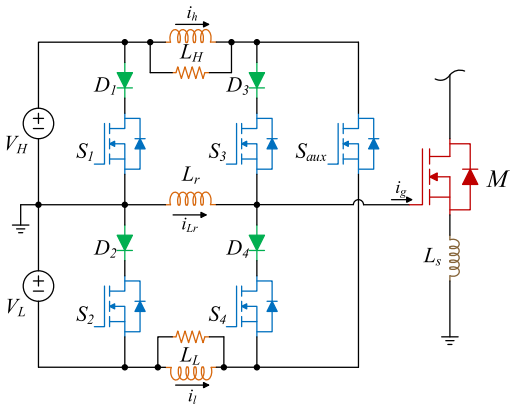

Fig. 18. Adaptive CSD [48].

provided an efficiency improvement of 2.9% and a loss saving of 25%.

However, the presence of common source inductance (L_s) in the gate loop circuit leads to the current diversion problems [43]. This happens due to the false conduction of the antiparallel diode of the control switch connected across the gate–source terminal (such as S_4 in Fig. 15). With the part of the inductor current diverted through the diode during turn-OFF interval reduces the subsequent gate current, resulting in slower turning-OFF of the power device. To address this issue the earlier driver is modified by replacing S_4 with the four-quadrant switch S_4–S_5, as depicted in Fig. 16(a) [43], [44]. With the additional series-connected diodes, −3.5 V is generated across the gate terminal during the turn-OFF interval to accelerate the turn-OFF speed of the power device. This driver is implemented to drive the power device at 1 MHz in a buck converter rated for 1.2 V/30 A. With this driver, the efficiency of the converter is improved by 9.4% and 2%, respectively, as compared to the conventional VSD and the CSD discussed in [39]. However, the driver is not capable of solving the current diversion problem during the turn-ON interval.

In addition to L_s in the gate loop circuit, there exists an additional parasitic gate resistance that creates a large voltage drop in the presence of constant gate current [45]. In order to drive the power device effectively, these drops need to be compensated. Nevertheless, the presence of L_r in CSD helps in boosting the output voltage, which, in turn, can compensate for these additional voltage drops. However, the output voltage of CSD higher than V_{cc} will result in the body diode clamping effect. This is due to the conduction of the antiparallel diode of the control switch connected across V_{cc} and the power device gate terminal (e.g., S_3 in Fig. 15), resulting in the CSD to operate as a conventional VSD. This issue is addressed in [45] by adding extra diodes D_1 and D_2 in series with S_3 and S_4 of the CSD in [39]. The driver circuitry is depicted in Fig. 16(b). These additional diodes eliminate the body diode clamping effect along with the current diversion problem. The above-discussed driver is implemented to switch the Si MOSFET (SiR472DP) at 1 MHz in the buck converter rated for 1 V/15 A. Compared to the drivers in [39] and VSD, the above-discussed driver improves converter efficiency by 2.61% and 4.77%. Nevertheless, in the presence of blocking diode D_1, the driver output voltage continues to rise beyond V_{cc} for the duration till the net energy in L_r is zero. This results in an overshoot in the driver output voltage. In addition, with the current blocked by the diode D_2, the above-discussed driver loses its ability to recover gate energy during the turn-OFF instants. To overcome all the aforementioned challenges associated with the earlier-discussed full-bridge CSDs, the control switches S_3 and S_4 in [39] are replaced with the four-quadrant switches, as depicted in Fig. 17 [46], [47]. The driver provides the control over the inductor current, which, in turn, avoids the body diode clamping and current diversion effect. In comparison to a conventional VSD, the above-discussed driver drives the SiC MOSFET at 500 V/30 A, resulting in a 68% reduction in turn-ON time and a 50% reduction in turn-OFF time. In addition, the switching loss of the device is reduced by 68% compared to VSD. Nevertheless, the presence of the four-quadrant switch in the driver disables the automatic change from CSG to VSG after the switching transitions. This requires accurate time control for the transition of the driver to avoid the overcharging or discharging of C_{iss} for the given value of power device voltage and current. A novel inductor-based CSD is proposed in [48], as shown in Fig. 18, with an adaptive functionality to drive the SiC MOSFET. The proposed CSD aims to decouple and improve the controllability over *dv/dt* and *di/dt* along with a reduction in turn-ON and turn-OFF delay by supplying gate current of

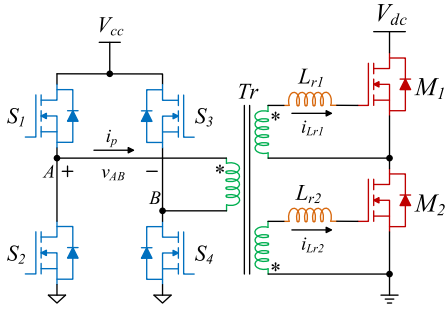

Fig. 19. Dual-channel isolated gate driver [50].

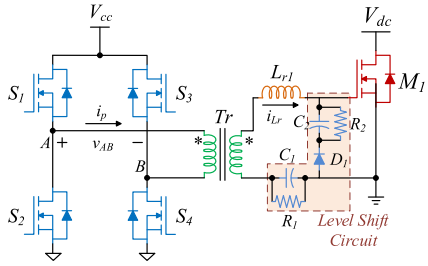

Fig. 20. Isolated CSD with asymmetrical ON/OFF voltage [51].

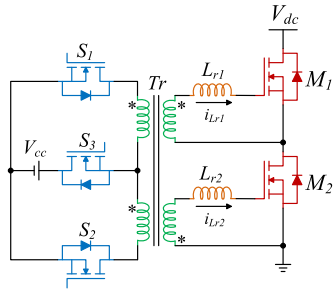

Fig. 21. Dual-channel push–pull isolated CSD [52].

two different peak values at the time of switching transitions. The driver comprises three inductors along with an additional auxiliary branch with control switch S_{aux}, which provides the path for injection and sinking of the second gate current of controlled magnitude to control the current and voltage slew rate. Furthermore, the adaptive control over the gate current provides switching loss manipulation for active thermal control, and also the control over the turn-ON and turn-OFF delay provides the feature of adaptive dead band configuration for critical PE converters. The proposed gate driver provides controllable *di/dt* in the range of 1.24–4.5 A/ns and 87% controllable range for the *dv/dt*. Moreover, the gate driver also provides the reduction in turn-ON and turn-OFF delay by 57% and 33% compared to the conventional gate driver. The driver requires appropriate control over the auxiliary branch and also suffers from high circulating losses. Further research in CSDs leads to the emergence of a new category based on the method of isolation. These drivers are termed isolated CSDs and are discussed as follows.

5) Isolated CSDs: The CSDs that utilize an external medium of isolation between the driver and the power device are considered in this section. Most commonly, transformers were used to create isolation in VSD for driving the phase leg switches with a single control input pulse [30], [49]. However, such solutions still possess the same limitation that exists in conventional VSD. To overcome the challenge, the VSDs are replaced by the CSD at the primary side of the isolation transformer. The first such CSD-based isolated driver is reported in [50]. The driver is reported to drive the complimentary pair of switches in a phase leg, as depicted in Fig. 19. In the above-mentioned isolated CSD, switching transitions of the power devices occur only when the input voltage to the transformer is zero ($v_{\text{AB}} = 0$), resulting in the secondary winding voltage being clamped to zero. This isolated CSD is used to drive the phase leg of the full-bridge converter rated for 48 V/20 A. In comparison to VSD, this driver improves converter efficiency by 2% at 500 kHz switching frequency. Further modification in the above-discussed driver is reported in [51], where an additional level shift circuit is implemented on the secondary side, as depicted in Fig. 20. Such drivers are beneficial where the negative voltage requirement during the turn-OFF interval is lower, such as in case of SiC MOSFET. Also, the implementation of the level shift circuitry leads to a lower input driving voltage requirement. The driver is implemented to switch the SiC MOSFET at 500 kHz frequency. Further research has been done to reduce the number of control switches in the driver. A dual-channel isolated three-switch CSD working on push–pull configuration is proposed in [52], as depicted in Fig. 21. The working of the driver is similar to that earlier discussed isolated CSD in [50]. The driver is implemented to drive the phase leg of the full-bridge converter rated for 48 V/10 A at 500 kHz switching frequency. When compared to a conventional VSD, the above-mentioned driver increases the converter efficiency by 1.8%. Furthermore, there is a reduction in gate driver loss by 70.7%.

The challenge associated with the isolated CSDs is the efficient design of the transformer with minimum leakage flux. In addition to that, all the aforementioned CSDs require an additional driver in order to drive the control switches. These extra drivers are termed predrivers. To overcome these, self-biasing circuits are utilized to create the current source using transistors, as discussed in the following.

6) Transistor-Based CSDs: There are several passive circuit-based solutions that utilize transistors besides inductors and active sources to create a current source. Among all the existing transistor circuits, three circuits, as depicted in Fig. 22, are found to be more suitable to create a current source for driving the power device [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63], [64]. The transistor-based circuit depicted in Fig. 22(a) utilizes the Zener diode-based configuration to create a current source during the turn-ON instant. From Fig. 22(a), the constant output gate current is computed as follows:

$$i_{\text{g}} = I_{\text{Ron}} = \frac{V_{\text{Z}} - V_{\text{BE}}}{R_{\text{on}}} \tag{1}$$

where V_{Z} is the Zener diode breakdown voltage, V_{BE} is the base–emitter voltage drop of BJT, and R_{on} is the current regulated resistor. The second method uses a current mirror-based circuit to generate a current source, as shown in Fig. 22(b). By controlling

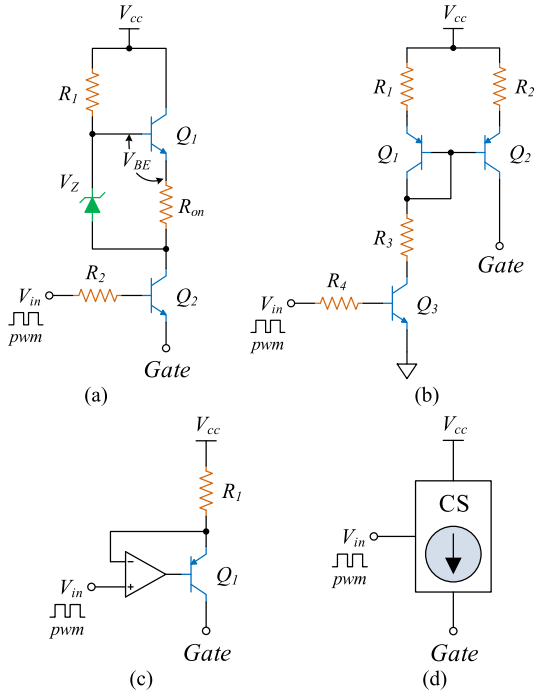

Fig. 22. (a) Zener diode CSD. (b) Current mirror CSD. (c) Op-Amp CSD. (d) Transistor-based CSD representation [53].

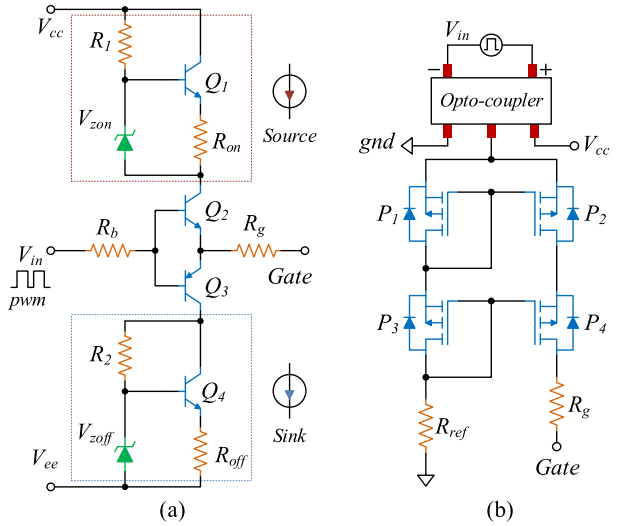

Fig. 23. (a) Transistor-based CSD with source and sink ability [54]. (b) Inductorless discontinuous CSD [56].

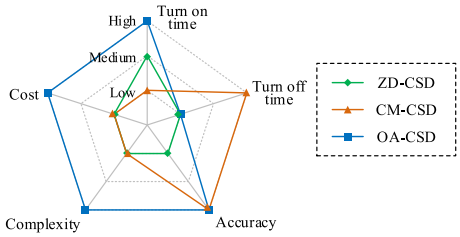

Fig. 24. Comparison of different transistor-based CSDs [62].

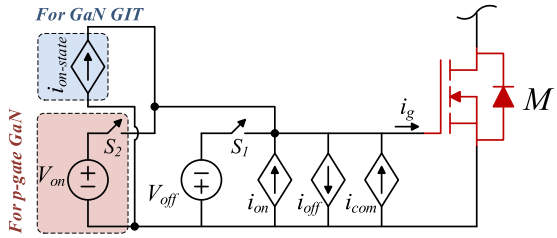

Fig. 25. Simplified schematic of an ACSD for series connection [58].

the current in another active element of a circuit, a current mirror duplicates the output current, also keeping it constant regardless of load. Another approach is to use an op-amp-based current source, as shown in Fig. 22(c). This configuration increases the output voltage by compensating the base–emitter drop in the Zener-transistor-based current source [see Fig. 22(a)]. The transistor-based CSDs have been developed to drive the power device with constant gate current during switching transitions based on the combination of the above-mentioned configurations.

The Zener-transistor-based CSD is implemented in [54] to drive the IGBT module, as depicted in Fig. 23(a). As part of the proposed driver, two different current sources are utilized, one acts as a source during the turn-ON period and the other as a sink during the turn-OFF period. Moreover, to control the slew rate, i.e., *dv/dt* and *di/dt*, an additional current source circuit is implemented in the same driver, which controls the current flowing into the gate terminal during the switching intervals. Compared with the simple transistor-based current-source-driven gate driver discussed in [53], the overall driver configuration in [54] reduces losses by 56% and 69% during turn-ON and turn-OFF intervals, respectively. In [55], a current mirror-based circuit is used in conjunction with VSD to control the input gate current, which is then used to control the switching dynamics of the power device. In addition, a cascode mirror-based configuration utilizing the pmos has been developed to drive the SiC MOSFET, as depicted in Fig. 23(b) [56]. However, the proposed driver has more losses than the VSD but provides a reduction in voltage and current slew rate of 65% and 45%, respectively. Tan et al. [53] explored the possibility of using multiple parallel-connected transistor-based drivers to drive the IGBT modules with advanced control over the trajectory. Furthermore, it compares different transistor-based drivers that can be used to drive the power device. The simulations and experimental studies in [53] have led to the comparative performance shown in Fig. 24 . Also, the current mirror circuit has further been modified to actively control the SiC MOSFET, as described in [57]. Through active control of the input gate current, the proposed driver reduces the switching loss of the converter nearly by 50%.

In [58] and [59], an ACSD is proposed to address the challenges of dynamic voltage sharing in series-connected devices. The proposed gate driver targets to address the dynamic voltage sharing issue among the series-connected switches by controlling the switching dynamics of those switches. This is achieved by injecting additional compensation gate current during the turning ON and OFF of the devices. Fig. 25 depicts a simplified

schematic of this CSD comprising four different current mirror circuits, each providing a constant current. The implementation of the proposed gate driver for series-connected devices provides a cut down of 10% in the overvoltage across the device under various loads and different switching speed (dv/dt) conditions. However, these drivers are incapable of providing balanced voltage sharing during the hard switching of the devices. Furthermore, He et al. [60] proposed an ACSD to address the challenge of dynamic current sharing in parallel-connected devices, especially SiC MOSFETs. The proposed gate driver driving the two parallel-connected devices allows the reduction in turn-ON and turn-OFF switching energy imbalance from 13.4% and 56% to 8.8% and 15.3%. Also, the proposed gate driver can be easily extended for the multiple devices connected in parallel for better dynamic current sharing. However, for sensing the device current, an additional source inductance is required to be added to the power loop. Furthermore, a very high bandwidth BJT is needed for effective operation of the proposed driver. In order to distinguish the driver operations, an investigative analysis and case study are carried out in the following section.

III. Investigative Analysis and Case Study

In the preceding sections, different types of CSDs were reviewed in detail based on their operating principles and structural orientations. This section carries out the comparative conclusion of all the above-discussed CSDs. Later, a comparative case study is carried out and the performance of the considered CSDs is compared with respect to each other against the conventional VSD.

A. Prior-Art Conclusion

From the discussion presented in previous sections, it can be commented that the CSDs can maximize the power conversion efficiency in medium- and high-frequency applications. This is due to their inherent ability to provide a constant gate current during the switching transitions. It leads to reduction in turn-ON and turn-OFF times of the power device, resulting in lower switching losses. Furthermore, for the low-power high-frequency applications, the inductor-based CSD helps in recovering the gate energy during the turn-OFF interval and improves the driver efficiency by reverting back the stored energy. However, increasing the number of control switches in CSDs reduces the maximum achievable switching frequency for the main switching device. Moreover, more number of control switches need complex control, but on the other hand, it helps to improve the performance of the power device by gaining better control over the input gate current. With further development of isolated CSDs, it may become the suitable choice to drive a complimentary power device pair using a single control input along with the isolation barrier. To eliminate the need for such an additional complex control circuitry in inductor-based CSD, the self-biased transistor-based CSDs were introduced. These drivers utilize various transistor-based circuits to create a voltage-controlled current source during the switching transitions. Also, by connecting such multiple parallel driver circuits provides the active gate current control but with the increased complexity. The literature reveals that most CSDs outperform VSDs in terms of high speed and reduced losses. The prior-art researched CSD topologies are summarized in Table I with the ascending order of switching frequency to provide an intuitive comparison. The complete data are gathered from the literature and filled up accordingly. From Table I, it can be clearly observed that the CSDs are implemented over a wide switching frequency range from 70 kHz to 20 MHz. Table I also provides the information regarding the number of control switches, additional passive elements, and considered current source inductor values. Based on the available data, the rated power of the converter utilizing the corresponding CSD is also reported in Table I. In the additional component column, the notation "D" stands for the diode, "C" for the capacitor, "L" for the inductor, "T" for the transformer, and "ZD" for the Zener diode. It is also clearly observed from Table I that for fewer control switches, the operating switching frequency of the driver is higher and reduces with an increase in control switch count. Furthermore, it is reported that the CSD provides a reduction in switching loss due to its ability of faster switching, resulting in lower switching time. The percentage loss reduction and efficiency improvement achieved by the CSDs discussed in this article are plotted in Fig. 26. In order to have an in-depth study of the operation of various CSDs, a case study is performed in the following section to describe their operation in detail.

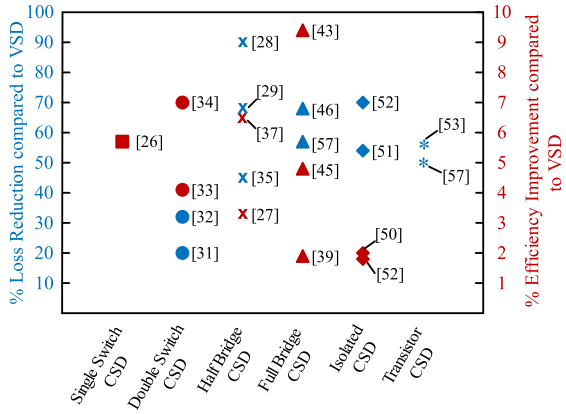

Fig. 26. Loss reduction (%) and efficiency improvement (%) achieved by CSDs compared to conventional VSD.

B. Case Study

This section aims to compare and investigate various classes of CSDs with the conventional VSD based on various performance parameters. Simulation studies are carried out in order to have one-to-one comparative analysis with each other.

1) Selected Driver Configurations: Among the various existing CSDs based on their nature of operation, three CSDs, as depicted in Fig. 27, are selected and investigated in detail. The obtained results are then analyzed and compared with the conventional VSD under similar operating conditions. Cases A and B are the driver circuits from the inductor-based CSD, which differs in the nature of inductor current, while the Case C driver is from inductorless CSD class. These drivers are more

TABLE I
CSD COMPARISON TABLE

Ref.	Fsw (MHz)	Switch Count	Add. Comp	*Lr* (nH)	Pout (W)	CSD Type	Features	Challenges	Applications used for
[31]	0.07	2	2-D, 1-C, 1-L	100	8000	D-IB	controlled peak gate voltage and 20% reduction in switching losses	Higher chance of shoot through problems in case of inverter leg	Boost Converter
[47]	0.4	6	1-L	1000	15000	D-IB	Provide constant current during switching transitions, no current diversion, and control over the transition from CSD to VSD	increased dv/dt, overvoltage, cross talk issues, higher noise and EMC	SiC-based converters
[35]	0.5	2	2-D, 1-L	470	435	D-IB	Gate energy recovery at both charging and discharging transitions	Suffers from current diversion problem	-
[50]	0.5	4	2-L, 1-T	250	576	D-IB	Provides isolated complementary drive signals, negative voltage during turn OFF, and gate energy recovery	The peak gate current depends on device input capacitance C_{iss},	Phase-shift ZVS FB converter
[51]	0.5	4	2-C, 1-D, 1-L, 1-T	700		C-IB	Provides adjustable asymmetrical ON/OFF gate voltages,	Oscillations in the gate–source voltage,	Suitable for phase leg configuration
[52]	0.5	3	2-L, 1-T	350	480	D-IB	Two isolated complementary drive signals, low-gate driver loss, and high reliability of turn- OFF status	Ringing in the inductor current, slower	ZVS phase-shifted FB converter
[59]	0.5	1	-	-	-	IL	Best suitable for series-connected devices, more accurate dv/dt control	More compelx	Series-connected GaN MOSFETs
[33]	1	2	1-D, 2-L	64	390	D-IB	Gate energy recovery, low circulating losses, and high *Cdv/dt* immunity	Suffers from current diversion problem	Narrow on-time Buck Converter
[34]	1	2	1-L	160	260	D-IB	No current diversion problem, faster turn OFF with higher gate current	Inductor peak current changes with change in duty cycle.	Narrow on-time VRM
[27]	1	2	1-C, 1-L	1200	45	C-IB	Gate energy recovery, ZVS of all control switches	Peak gate current varies with respect to duty cycle, current diversion	Buck voltage regulator
[37]	1	4	1-C, 1-L	22	39	D-IB	Gate energy recovery, wide duty cycle range operation, and low circulating losses	Suffers from current diversion problem, and fixed switching frequency operation	Synchronous buck converter
[29]	1	4	1-L	2200	20	C-IB	Can drive two synchronous switches using single gate driver, energy recovery, and high Cdv/dt immunity	Inductor current varies with duty cycle	Current doubler, push pull converters
[39]	1	4	1-L	100	50	D-IB	Gate energy recovery, lowe circulating losses, and constant peak current for wide duty cycle operation	Suffers from current diversion problem,	Boost Converter
[43]	1	5	5-D, 1-L	43	36	D-IB	No current diversion problem, gate energy recovery, and flexible negative voltage magnitude	Additional diodes are required for generating negative voltage casuing higher condcution losses	Synchronous buck converter
[45]	1	4	2-D, 1-L	100	25	D-IB	More dynamic range curent source, and control over the transition form CSD to VSD (gate clamping)	Can increase the gate source voltage beyound the rated value and damnage the gate oxide	Buck converter
[38]	1	3	2-D, 1-L	180	36	D-IB	no currnet divesion during turn-OFF transition	Turn pff peak indcutor current varies with change in duty cycle, Also, the magnitude of gate voltage is defined by *L* and *C*	Narrow on time buck converter
[26]	1	1	1-D, 2-L	650	36	D-IB	Higher gate current, cdv/dt immunity, boosting of gate voltage	The indcuctor peak current varies with change in duty cycle,	Buck VRM
[32]	13.56	2	2-D, 1-L	79	2000	D-IB	Reduces the ON and OFF time by 80% and 68%	Ringing in the gate-source voltage is larger	Medical applications within Industry science medical (ISM) Band
[25]	20	1	1-L	200	300	C-IB	low compoenet count, small energy storage and low complexity	Gate voltage and current magnitude varies with device Ciss	Telecom and RF with fixed duty cycle converters.
[54]	-	4	6-R, 2-ZD	-	-	IL	Active control over the gate current to reduce the overshoot and oscillations in voltage and current	slower response of BJT, increase in switching time and losses	Si IGBT converters
[56]	-	4	2-R	-	-	IL	Very low propogation delay, less compexity, and compact footprint	There exists a trade off between switching losses and EMI	SiC MOSFETs
[60]	-	-	-	-	-	IL	dynamic current balancing for parallel-connected switches by active current balancing approch	More complex	Parallel-connected SiC MOSFET
[48]	-	5	4-D, 3-L, 2-R	700	-	D-IB	adapctive functionality and improved controllability over di/dt and dv/dt	More circulating losses	High-voltage SiC MOSFETs

popular among each category and are the first to be implemented. They are subsequently utilized for the development of more effective CSDs. Fig. 28 illustrates the ideal waveforms of all the three considered CSDs. In Case A, the driver consists of a half-bridge leg, a capacitor, and an inductor. Fig 28(a) depicts the charging and discharging of C_{gs} with positive and negative peaks of the inductor current during both control switches S_1 and S_2 turned-OFF. The CSD in Case B has two half-bridges and an inductor. In Fig. 28(b), it is evident that the current source inductor is precharged prior to the switching transitions. The inductor is precharged with positive current when the control switches S_1 and S_4 are turned ON for the $t_0 - t_1$ time instant. In addition, the inductor is precharged with the negative current by turning-ON the switches S_2 and S_3 for the time interval $t_4 - t_5$. The transistor-based CSD in Case C is composed of four pmos connected in cascode current mirror configuration, as depicted in Fig. 28(c). The current mirror is driven by an optocoupler using an external PWM control signal. If the input voltage is high, the self-biased configuration of P_1 and P_3 will create a current mirror action in P_2 and P_4. When the input to the optocoupler is low, the mirror circuit voltage is zero, so the power device C_{gs} discharges through the body diodes of P_2 and P_4. The selected driver topologies are further analyzed and simulated in the following sections.

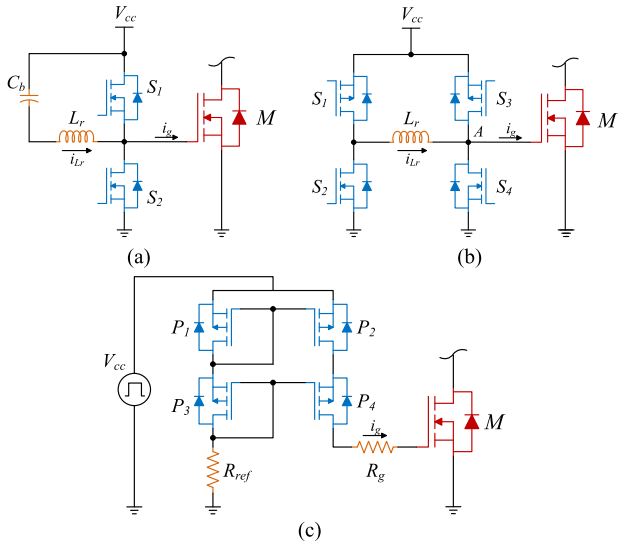

Fig. 27. CSDs in comparison. (a) Case A [27]. (b) Case B [39]. (c) Case C [56].

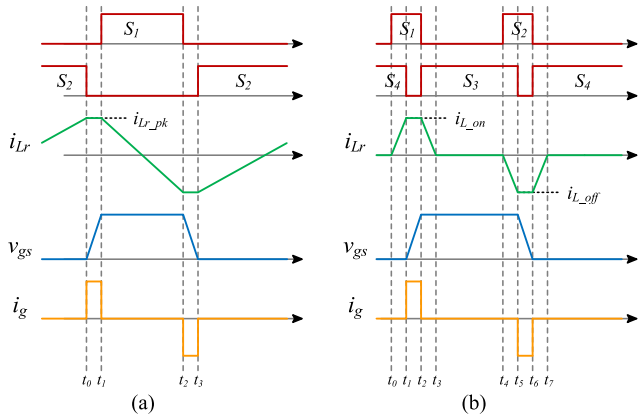

Fig. 28. Ideal switching waveform of (a) case A and (b) case B.

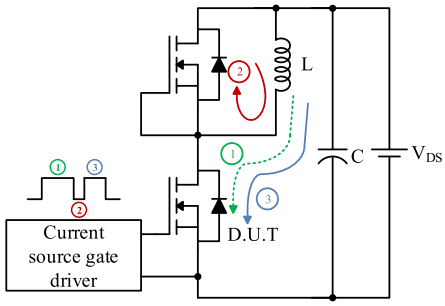

Fig. 29. DPT bench setup for evaluating the CSDs performance.

2) Simulation Model and Driver Specifications: The DPT setup shown in Fig. 29 is modeled in LTspice simulation software to investigate the performance of considered CSDs [65], [66]. In general, a DPT setup consists of an inductor, dc source, diode, device under test (DUT), and the gate driver. The current in the circuit is built up with the lower switch turned ON, and when the switch is turned OFF, the current freewheels through the diode. Given that SiC MOSFETs are utilized for many high-frequency applications, the C3M0045065D SiC MOSFET with 650 V/37 A rating has been chosen as DUT. This device has a lower gate charge of 20 nC and a gate voltage of 20 V due to it being a WBG switch. The CSDs are switched at a switching frequency of 1 MHz with a 50% duty cycle. In Cases A and B, the inductor-based CSDs use RSQ020N03 as the control switches, while in the current mirror of Case C, pmos Si7143DP is used in the driver circuitry. The performance of the considered CGDs is compared with that of the conventional VSD driving the same power device. In Case A, the peak value of the gate current prior to the switching transitions can be expressed as follows:

$$i_{\mathrm{g-pk}} = i_{\mathrm{Lr-pk}} = \frac{V_{\mathrm{cc}} \cdot D \cdot (1-D)}{2 \cdot L_{\mathrm{r}} \cdot f_{\mathrm{sw}}} \tag{2}$$

where D is the duty cycle and f_{sw} is the switching frequency. Maintaining the continuous current throughout the switching period requires a larger value of L_{r} in the range of 1–2 μH for the switching frequency of 1 MHz. From (2), it can be observed that the peak inductor current is the function of the duty cycle and switching frequency. This limits the driver to operate over a given single point. However, peak inductor current value prior to switching transitions in Case B driver is derived as follows:

$$\begin{aligned} i_{\mathrm{g\_on}} &= i_{\mathrm{Lr-on}} = \frac{V_{\mathrm{cc}}}{L_{\mathrm{r}}}\, t_{10} \\ i_{\mathrm{g\_off}} &= i_{\mathrm{Lr-off}} = \frac{V_{\mathrm{cc}}}{L_{\mathrm{r}}}\, t_{54} \end{aligned} \tag{3}$$

where t_{10} $(t_1 - t_0)$ and t_{54} $(t_5 - t_4)$ are the precharging intervals prior to the switching transitions. Depending on the power device selected, the peak inductor current can be varied by controlling the pre-charging interval. The discontinuous nature of the inductor current leads to less energy storage requirements, resulting in a smaller inductor value in the range of 50–200 nH. It can also be seen from (3) that the peak inductor current does not depend on the duty cycle or the switching frequency, which makes it ideal for applications involving variable switching frequencies over a wide range of operating conditions. However, in Case C driver, the reference current is obtained using the following equation:

$$i_{\mathrm{g}} = i_{\mathrm{ref}} = \frac{\mu_{\mathrm{n}} \cdot C_{\mathrm{ox}}}{2} (V_{\mathrm{gs}} - V_{\mathrm{th}})^2 \tag{4}$$

where C_{ox} is the oxide capacitance per unit area, and V_{gs} and V_{th} are the gate–source and threshold voltages of the pmos used in the driver circuit. The simulation of all the considered CSDs is carried out and the obtained results are further analyzed in the following section.

3) Comparative Investigations and Results: Simulations are carried out for the parameters discussed, and the switching waveforms are extracted and compared in the following.

1) *Gate voltage and current analysis:* The case A and B drivers have been proposed in the literature for driving Si MOSFETs, while the Case C driver has been proposed for driving SiC MOSFETs. However, as discussed in the earlier section, SiC MOSFET is switched at high frequency and the corresponding waveforms are extracted. For each

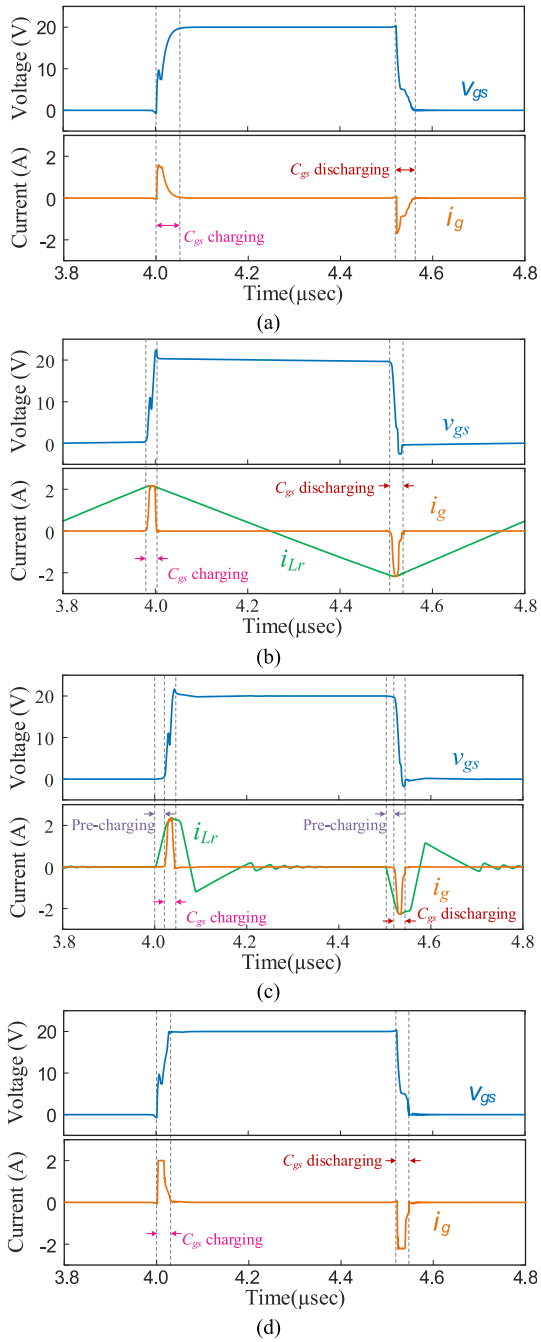

Fig. 30. Simulation results of gate voltage and gate currents of (a) totem-pole VSD, (b) case A, (c) case B, and (d) case C.

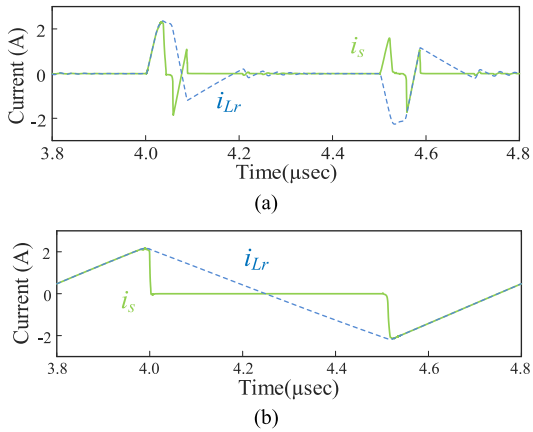

Fig. 31. Source and inductor current in (a) case A and (b) case B.

of the drivers under comparison, $v_{\rm gs}$ represents the gate voltage, $i_{\rm g}$ represents the gate current, and $i_{\rm Lr}$ represents the inductor current, as shown in Fig. 30. From Fig. 30(a), the peak gate current decays slowly in a conventional VSD during the gating transition, which slows the switching process. Despite this, the constant current in the inductor-based CSD at the switching interval enables the fast charging and discharging of $C_{\rm gs}$, resulting in a lower switching time, as can be observed in Fig. 30(b) and (c).

On the other hand, the transistor-based CSD provides a relatively constant current during the turn-ON period, while during the OFF period, its operation is similar to that of the conventional VSD, as shown in Fig. 30(d). In comparison to VSD, the drivers in Cases A and B achieve lower overall switching losses, whereas the driver in Case C only reduces turn-ON switching losses. In addition, we can conclude from the above results that the CSDs are quite capable of driving the SiC MOSFET at very high switching frequencies. The additional benefit of gate energy recovery is obtained in the case of inductor-based CSD, as explained in the following.

2) *Gate energy recovery:* In order to improve the driver's efficiency, its net energy consumption must be as low as possible. Neither VSDs nor transistor-based CSDs can recover gate energy from power devices during turn-OFF interval. In an inductor-based CSD, the energy is stored in the inductor itself. Nonetheless, inductor-based CSDs can also revert back the excessive stored energy to the driving source. The inductor current and the supply current for the CSDs in Cases A and B are depicted in Fig. 31. From Fig. 31, it can be observed that for the negative source current, there is a transfer of energy back to the driving source, which results in the overall efficiency improvement of these drivers. Fig. 31(a) shows that the Case A driver can only recover the energy during the turn-OFF interval. In addition to recovering the gate energy, the case B driver has the ability to deliver back the excess energy after the power device is turned ON, as depicted in Fig. 31(b).

Furthermore, the discontinuous nature of the inductor current in Case B reduces conduction loss by 80% as compared to Case A for the same operating conditions. A detailed loss analysis of all the consider drivers is further carried out in the following section.

3) *Gate driver loss analysis:* A detailed breakdown of the gate driver loss is provided here in order to have a thorough comparison. The total gate driver losses are further segmented in the following components:

a) the loss across the internal parasitic resistor and the external gate resistor;

TABLE II
GATE DRIVER LOSS OF ALL THE CASES

	VSD	Case A	Case B	Case C
Internal R_g loss	0.05 W	0.07 W	0.068 W	0.07 W
External R_g loss	0.30 W	-	-	0.25 W
Conduction loss	-	0.90 W	0.12 W	0.92 W
Control switch loss	0.025 W	0.15W	0.20 W	0.25 W
Total	0.375 W	1.12 W	0.388 W	1.49 W

TABLE III
RELATIVE COST COMPARISON FOR THE CASE STUDY

Driver Type	Control switches	Passive Components	Predrivers and additional circuitry	Overall Cost
VSD	1 $	0.1 $	2 $	Low
Case A [27]	1 $	1 $	4 $	Medium
Case B [39]	2 $	0.2 $	8 $	High
Case C [56]	2 $	0.1 $	3 $	Medium

b) losses across the passive components and the conduction losses in the capacitor and inductor in Cases A and B;
c) gate losses in the control switch and the pmos in the CSDs used to drive the power device.

The total loss across the internal and external resistors together is termed gating loss [10]. In the case of VSD, the external resistor controls the slew rate of the power device [22]. However, in CSD, the external resistor is either replaced by the inductor-based or the transistor-based circuit that, in turn, controls the behavior of the power device. In order for CSDs to have lower or negligible external losses, control switches with low ON-state resistance and small output capacitance must be chosen.

The loss breakdown for the conventional VSDs and all CSDs driving the SiC MOSFET with the switching frequency of 1 MHz and 50% duty cycle are obtained and illustrated in Table II. As can be observed, in comparison to the VSD, the total gating loss is reduced by 80%, 80.5%, and 8.5% in Cases A, B, and C, respectively. The additional external gate resistor connected in the VSD and Case C driver dominates the gating loss. Due to the presence of the capacitor and inductor, along with the continuous current in the Case A driver, the conduction loss accounts for 80% of the total losses. Furthermore, compared to Case A, the conduction loss for Case B driver is 86% lower due to the discontinuous nature of the inductor current. Due to the mirror current functionality in Case C, the current continues to flow through the R_{ref} resistor during the turn-ON interval, causing additional losses in the driver. These losses account for roughly 62% of total losses. Table II illustrates that among all the cases, Case C has the highest loss. Furthermore, overall losses of the VSD and the Case B driver are nearly the same, but the VSD results in more switching time, which, in turn, results in more switching losses in comparison to the CSDs. Moreover, Case B drivers offer more flexibility than the other drivers, as it allows control of the switching dynamics of the power device by adjusting the gate current in accordance with the application. Nevertheless, the implementation of such a driver results in additional control switch losses and much greater complexity, which can increase the overall driver cost. To have a detailed insight, a comparative analysis is carried out among the above-mentioned cases and is listed in Table III. From Table III, it can be observed that the predrivers and additional circuitry accounts for major costs in the case of CSDs, resulting in much higher costs. Nonetheless, with the further development in device fabrication technologies, it is projected that the CSDs can be obtained as a single chip solution, which will further lower down the overall cost in such cases. Since these drivers are not fully explored in the industry, their cost is still high because of the utilization of discrete components with nonoptimized cost. Henceforth, with the rise in CSD utilization, the cost and complexity can be reduced to a greater extent. Furthermore, to prove the effectiveness of CSDs and their benefits over VSDs, a comparative experimental study is carried out with detail discussed in the following section.

IV. EXPERIMENTAL VALIDATION

To further evaluate the performance and the benefits of CSDs over VSDs, a comparative experimental investigation is carried out in this section. Among various existing CSDs as discussed above and by considering the advantages and ease of implementation, a CSD, as shown in Fig. 26(b), [39] is developed along with the conventional VSD, as shown in Fig. 1. The selected CSD is a discontinuous type inductor-based driver in which the inductor is charged prior to turning ON and OFF the power device. For VSD, BROADCOM make ACPL-W346-000E is used to drive the switching device with a driving voltage of 20 V. The CREE make C3M0045065D is selected as the switching device having the input capacitance of 1621 pF. For any given semiconductor switch, the input gate current should be limited to its maximum value in order to avoid several undesirable effects, such as gate oxide layer damage and insulation breakdown between the gate and channel [67]. This leads to serious consequences in terms of reliability and the performance of the device or even can lead to permanent damage to the switching device. In addition, the excessive gate current above the limit can cause overheating and thermal damage to the device. The continuous degradation of the device due to excessive gate current can also cause nonideal behaviors, such as increased leakage current, reduced transconductance, and change in threshold voltage [68]. The maximum value of the gate current for the given switching device can be expressed as [69]

$$I_{g(\max)} = \frac{C_{iss} \cdot \Delta V_{\text{gs}}}{\Delta t} \tag{5}$$

where C_{iss} is the input capacitance, ΔV_{gs} is the change in voltage during the switching transition, and Δt is the estimated time the entire turn-ON event should occur, which is taken from the datasheet of the respective switching device. For the selected device with the voltage swing $\Delta V_{\text{gs}} = 20$ V and $\Delta t = 15$ ns, the maximum gate current is computed as 2.16 A. By considering the maximum gate current limit, I_g is set to 2 A for both the cases. To limit the gate current in VSD, an external gate resistor is added such that the effective resistance of 10 Ω is maintained, which would limit the gate peak current to 2 A when driven using 20 V

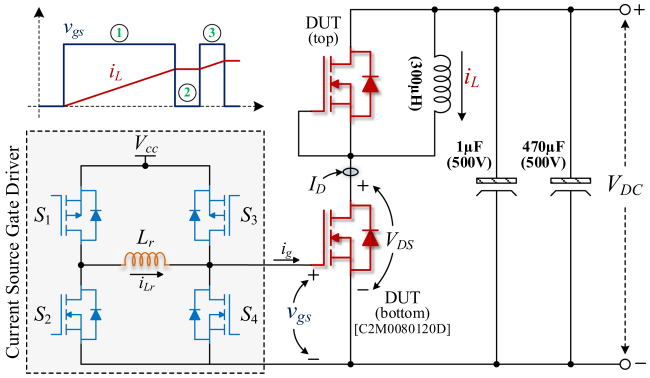

Fig. 32. Circuit schematic of the DPT setup integrated with CSD.

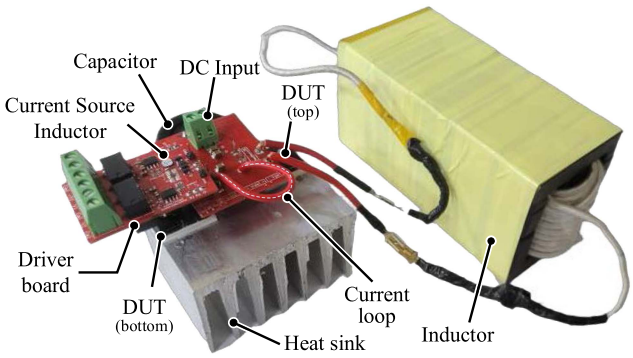

Fig. 33. Experimental setup of DPT with CSD.

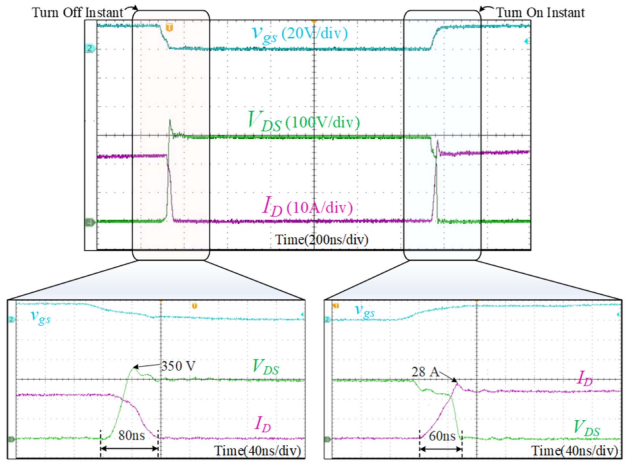

Fig. 34. Experimental results for the DPT on SiC MOSFET with voltage-source gate driver.

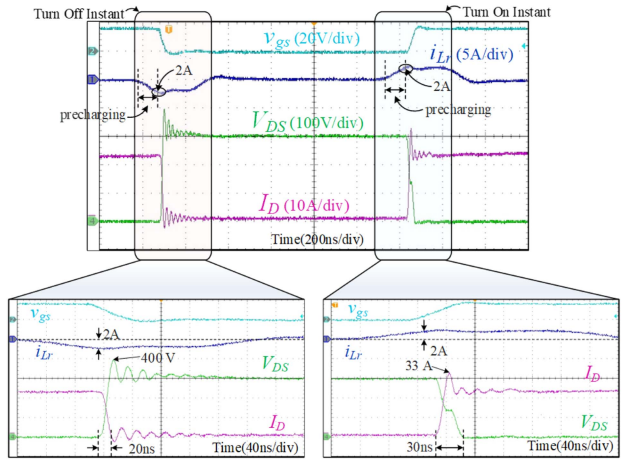

Fig. 35. Experimental results for the DPT on SiC MOSFET with CSD.

driving source. However, for the CSD, the inductor is precharged for 100 ns from the driving source of 20 V, which builds 2 A of current prior to the switching ON or OFF the device. To evaluate the driver performance, a DPT test setup with circuit schematic shown in Fig. 32 is developed, as shown in Fig. 33. The DPT setup comprises a half-bridge leg supplied from an isolated dc power supply. Furthermore, CREE make C3M0045065D rated for 650 V/35 A is selected as DUT. An external inductor (L) of 300 μH is connected across the top DUT, which is used to build the current in the circuit. The top DUT is always kept turned OFF by shorting the gate–source terminal, while the bottom DUT is driven using the gate drivers with the double pulse input, as shown in Fig. 32. The TI make TMS320F28379D digital signal processor with the clock frequency of 200 MHz is used to generate the pulses for the control switches in both the gate drivers. Furthermore, the key switching waveforms are measured using the Tektronix make MDO 3014 oscilloscope. For measuring the switch current, Yokogawa make high bandwidth current probes are used and for measuring the switch voltage and gate–source voltage, Tektronix make THDP0200HV differential probes are used. To measure the inductor current in the CSD, a current sense resistor of 0.1 Ω is placed in series with the inductor.

At first, the bottom DUT is switched ON, which causes the current in the inductor to rise. The duration of the first pulse (①) is determined based on the test current to be obtained. For the experimental studies carried out in this article, a dc input of 300 V is applied and the duration of the first pulse is set to 25 μs to obtain the test current of 25 A. Later, the DUT is turned OFF and the current freewheels through the antiparallel diode of the top DUT for the shorter duration of 1 μs. During this interval (②), the current level remains almost unchanged. At next, another turn-ON pulse (③) is applied for a shorter duration in order to limit the inductor current to rise more. The first turn-OFF event of the DUT determines the turn-OFF switching characteristic of both device and gate driver, while the second turn-ON instant will determine the turn-ON characteristic, respectively. Both the VSD and CSD are used to drive the DUT and the key waveforms are obtained as shown in Figs. 34 and 35.

The switching energy for a given power device can be obtained as the product of switch voltage, current, and the transition time. For the selected DUT when driven by VSD, the turn-OFF and turn-ON transition times are equal to 80 and 60 ns, respectively, as can be observed in Fig. 34. However, for the DUT driven using CSD, the switching transition times during the turn OFF and turn ON are observed to be 20 ns and 30 ns, respectively, as illustrated in Fig. 35. The reduction in switching transition period for the CSD is due to its ability to provide nearly constant current during

TABLE IV
EXPERIMENTAL SWITCHING ENERGIES

	VSD	CSD	% Reduction
Turn ON	369 μJ	148 μJ	60%
Tun OFF	616 μJ	176 μJ	71%

the switching transitions, which results in fast turning ON and OFF of the power device. Prior to the turn-OFF instant, the current source inductor in CSD is precharged to generate the required negative peak current of 2 A, as can be seen in Fig. 35. The DUT is switched OFF with the nonzero initial current, which results in faster discharging of C_{gs} and hence results in lower turn-OFF time. With the similar operating conditions, the CSD allows almost 75% reduction in turn-OFF time compared to the VSD. Furthermore, prior to turning ON the DUT, the current source inductor is again charged for the positive peak current of 2 A, which allows the faster charging of C_{gs}. This results in reduction of the turn-ON time by almost 50% compared to the VSD. The overall reduction in the switching time when the DUT is driven by CSD allows the reduction in switching losses and hence improves the converter efficiency. The obtained switching energies from the experimental results are listed in Table IV. Furthermore, the CSD is capable of reducing the overall switching losses by almost 67% when compared to the conventional VSD. In another word, for the given losses, the operating switching frequency can be increased further, which allows the reduction in the size of passive components and, hence, leads to higher power density. Furthermore, the applications and challenges associated with the CSDs are discussed in the following section.

V. CSDs: APPLICATIONS AND CHALLENGES

Providing a constant current prior to the switching transition is a major consideration for the CSDs. In most of the cases, the application of CSD is mainly emphasized in driving the conventional Si MOSFETs. However, recent advancements in the semiconductor technologies have led to additional challenges. This section discusses the various applications and challenges involved with integrating the CSDs.

A. Wide Bandgap Devices

With advancements in semiconductor technology, WBG devices based on SiC and GaN are becoming increasingly popular [70]. Due to the higher electron mobility of these devices, they are capable of switching at very high frequencies [71]. In addition, the higher breakdown field of these devices lowers the input gate capacitance value compared to the counter Si devices. Due to these characteristics, the WBG devices are suitable to switch the converter at high frequency with a low switching loss. In general, the switching performance of the device is determined primarily by the gate driver. The VSDs are been widely adopted to drive these devices but suffer from various challenges. One such challenge is the large internal gate resistance, especially in SiC devices, and the presence of a common source inductor that accounts for additional voltage drop during the switching instants. Due to this, the net voltage appearing across the internal gate–source capacitor is reduced, which slows down the charging and discharging of the gate–source capacitance and hence larger switching time and losses. Furthermore, with the fixed gate resistor, the switching dynamic of the device is fixed and cannot be controlled in the case of VSD. Moreover, it is not yet clear whether the VSDs are capable of operating these WBG devices to the fullest extent. The fast switching of the WBG devices causes additional issues as a result of high *dv/dt* and *di/dt*. In order to control the slew rate, active gate drivers were introduced, which utilized dynamic control over external gate resistance, capacitance, and gate voltage [72], [73], [74], [75]. Nevertheless, implementing such drivers is more challenging. To address all the afore-discussed challenges, CSDs can be one of the best suitable solutions. The constant current provided by the CSDs prior to the switching transitions leads to a shorter switching time for the WBG device making them capable of operating at high frequency. The advantage of lower switching time and losses offered by the CSDs provides an extra room for an increase in switching frequency.

In addition, the conventional VSD driving the SiC MOSFETs in general provides negative gate voltage during turn-OFF interval to speed up the turn-OFF process and also to avoid the false turn ON due to cross-talk effect [76]. However, the ability of CSD to provide a constant current even during turn-OFF interval allows the device to turn OFF at a faster rate. Furthermore, in the absence of an external gate resistor in most of the CSDs, there is no chance for the building up of gate voltage across the turned OFF switch due to miller current and hence no crosstalk effect occurs. Hence, it can be said that the SiC MOSFET driven by CSD does not necessarily require the negative turn-OFF voltage. However, there exist some CSDs that can provide negative voltage during the turn-OFF interval [38], [43]. [46], [48], [50], [51], [52] and provide the benefits of fast turn OFF and no crosstalk in phase leg. It is well known that the presence of common source inductance (L_s) in the gate loop leads to an additional voltage drop during switching transitions [39]. This leads to the reduced voltage appearing across the C_{gs} causing the slow turn ON and turn OFF. However, CSD providing a constant current during the switching transitions allows the faster turn ON and OFF, and hence lower switching losses. In addition, inductor-based CSD provides a boosted voltage during turn-ON instant, which compensates for the voltage drop occurred due to L_s [39], [43], [46]. So, it can be said that even in the presence of L_s in SiC MOSFETs, the CSDs can provide better performance in terms of lower switching times and losses compared to the conventional VSD.

In [14], [15], [20], [36], [58], [59], and [77], it is reported that the CSD can effectively drive the GaN devices at very high switching frequency. In [77], a GaN FET is switched at 13.56 MHz ISM band frequency using a CSD. Furthermore, Zhang et al. [59] utilized inductorless CSD to switch the series-connected GaN devices with controlled device switching time and *dv/dt* with fine accuracy by directly regulating the input gate current across each device. However, there is a need for additional research to study the suitability of inductor-based CSD for GaN devices. However, this CSD does not address the problem of high *dv/dt* and *di/dt*. Moreover, the transistor-based CSDs have also been utilized to drive the SiC MOSFETs

[56], [60], [61], [62], [63]. As discussed earlier, in contrast to inductor-based CSDs, these drivers do not require predrivers or an inductor making them to have a lower footprint with reduced complexity. A transistor-based CSD with programmable current was proposed in [63] that controls *dv/dt* and *di/dt* and reduces peak voltage and current overshoots in the SiC MOSFET. However, the complexity in such driver increases due to the requirement of two input control waveforms that are to be preprogramed. Moreover, the additional circuits also add delay in the signal. A digitally controlled ACSD is implemented in [62] to drive the SiC MOSFETs in order to avoid the complexity and to minimize the delay. However, not much research work has been done to drive the GaN MOSFET using the CSDs. Furthermore, researchers are also interested in developing inductor-based CSDs for medium- and high-power converters based on WBG devices [32], [47], [51], [61], [62]. In addition to that, there has been a shift in the research to integrate the complete CSD circuit on a single chip, referred to as monolithic gate drivers. Few such drivers based on inductorless configurations are developed and discussed in [78], [79], and [80]. In the case of the inductor-based CSDs, the monolithic drivers can be developed where all the control switches can be integrated together and a provision to integrate the current source inductor externally can be provided. Furthermore, it can be said that even though the CSDs are not very popularly utilized to drive the present power semiconductor devices, especially GaN, but they truly can provide a potential gate driver solution with enhanced properties compared to the conventional VSD solutions. Therefore, there is an immense possibility of exploring the use of CSDs for driving the WBG devices for future applications.

B. Series- and Parallel-Connected Switches

As a way of increasing the power handling capacity in the converters, semiconductor devices are usually connected either in series or parallel. However, these connections create additional problems. Due to the different ON-state resistance, pinch-off voltage, reverse breakdown voltage of the gate, and static properties of the devices, parallel connections create problems [81]. On the other hand, when these devices are connected in series, their distinct parameters, such as capacitance and threshold voltage, can cause unequal voltage sharing [82], [83]. Furthermore, nonidentical gate loops formed between the device and driver can cause a mismatch in the driving signal leading to additional delay. In order to mitigate these problems, either passive circuitry such as *RC* snubber or active gate drivers are utilized [84], [85], [86], [87], [88]. However, the addition of passive components results in an increase in losses, while active gate drivers limit fast switching operations. In order to drive the series-connected switches, a CSD is proposed in [89]. This CSD is implemented using a current source inverter connected to the primary of the transformer with multiple secondary winding connected to the series-connected switches. With multiwinding transformers, the need for signal isolation barriers and isolated power supplies can be eliminated. On the secondary side of the transformer winding, a simple self-driving circuit is implemented to drive the series-connected SiC MOSFETs. As proposed in [59], a similar circuit has been modified to provide active voltage balancing control for series-connected GaN HEMTs. The current mirror circuit is used in addition to the self-driving circuit to develop an additional current source at the secondary side. Furthermore, the proposed driver provides soft switching for all series-connected devices. Under the same operating conditions, it was observed that with the series connection of GaN MOSFETs, the switching loss is reduced by 36% in comparison to the single SiC MOSFET for a similar voltage rating.

For the parallel-connected devices or the high current module, the effective C_{gs} is very large. Moreover, the current imbalance in these parallel switches can cause overcurrent, which may lead to overheating of the devices. Also, due to the higher gate current requirement during the turning ON interval, the conventional VSDs may not be the best choice. Nonetheless, active VSDs have been proposed to address the issues related to the current imbalance. The active VSD uses the device current as a feedback signal, which controls the gate voltage output [90], [91], [92]. Furthermore, these drivers cannot maintain a constant current throughout the whole gating process, which results in slow switching transitions of the device. As a consequence of the CSD's ability to provide constant current, it can be used to maintain a constant current during the switching transitions. Such a CSD has been developed to drive an 800 A SiC module [61]. However, no CSD is known to drive multiple parallel switches, creating an entirely new area of research.

C. Device Protection

PE circuits are prone to both short-circuit and overcurrent [93]. There are a lot of solutions in the literature for detecting the short-circuit events and turning-OFF the power device. All these are compatible with the conventional VSDs. However, these solutions are ideally suited for Si devices due to their much higher short-circuit withstanding limits [94]. On the other hand, with the limited short-circuit withstand capability of WBG devices of as low as 2 μs, conventional protection methods incorporating VSDs may not be an appropriate solution [95], [96]. Besides the detection time, the power device has to be turned OFF more quickly. The *RC*-type discharging of C_{iss} in VSD results in slow turning-OFF of the power device. For C_{iss} to be discharged at a faster rate, a constant current must be maintained over the period, resulting in the power device to be turned OFF faster. It is possible to achieve this with the help of CSDs having the ability to provide controlled constant current prior to the switching transition. It is to be noted that no such CSDs have further been investigated for providing protection to the power device. In addition, there exist crosstalk effects, especially in phase leg configuration due to the high *dv/dt* slew rate in the power devices. In [97], a study is carried out for the optimal selection of L_{r} in order to have the least effect due to crosstalk. However, no such CSDs have been developed to mitigate the crosstalk effect. Furthermore, in [98], a short-circuit detection circuit is integrated with the CSD, which features a two-stage turn OFF.

D. High-Voltage Applications

Medium- and high-voltage power devices have problems in terms of isolation and electromagnetic interference (EMI) due to their high voltage magnitude and higher voltage slew rate (*dv/dt*). Recent developments in the semiconductor field have led to the production of SiC MOSFETs and SiC IGBTs with 10 kV and 15 kV blocking voltages, respectively [99], [100], [101]. As a result of the higher blocking voltage capacity of these devices, higher insulation and isolation voltage requirements are necessary. In such cases, isolated CSDs can be the most appropriate solution compared to the conventional VSDs. The use of such CSDs does not require a high isolation power supply, and the presence of an isolated pulse transformer enables the driver to operate at higher voltages. Furthermore, they allow low coupling capacitance in the gate loop leading to reduced common mode current. There have been no isolated CSDs explored for these high-voltage power devices. Developing a current source transformer with less interwinding capacitance and the required insulation for the higher voltage side can be challenging.

E. EMI Susceptibility

The ability of CSD to provide almost constant current during the switching transition allows faster turn ON and turn OFF of the power semiconductor device. This results in higher current and voltage slew rate (*di/dt* and *dv/dt*) and interacts with the circuit parasitic causing the overshoots and oscillations in the voltage and current [22]. These switching oscillations along with the resonance of the parasitic inductor and capacitor may cause severe conducted and radiated EMI noise in the circuit [102]. The problem of EMI can be reduced by suppressing the switching oscillation by reducing the voltage and current slew rate. In the conventional voltage source gate driver, increasing the gate resistance can slow down the *dv/dt* and *di/dt*, which dampen the switching oscillations to a certain extent [49]. Furthermore, the turn-ON and turn-OFF times are increased significantly, resulting in larger switching losses and reduced switching speed. With the introduction of active gate drivers, the switching oscillations can be suppressed without affecting the switching time and hence realizing the full potential of high switching-speed capability, especially for the WBG devices. Various active voltage source gate drivers are proposed in the literature which provide the control over gate voltage and gate loop impedance to suppress the switching oscillations [103], [104], [105]. However, the driver being voltage driven still suffers from the similar challenges associated with the conventional voltage source gate drivers, as discussed in the article. To address the issue of lower switching oscillations along with faster switching transition, an active current source gate driver (ACSGD) based on a switched current source is proposed for driving SiC MOSFET [57]. The ACSGD provides a controllable gate current during the switching transition, which leads to better controllability over the switching dynamics of the power device. In [106], a gate current profile-based approach is proposed for reducing the conducted EMI by appropriately injecting different current levels during the turn-ON interval. He et al. [60] explored the possibility of using multiple parallel-connected transistor-based drivers to drive the IGBT modules with advanced control over the trajectory. In addition, the active voltage-source gate driver integrated with current source can be one of the best feasible solutions. In such drivers, the current source speeds up the switching transition process, while the active voltage control provides the control over the gate voltage which results in the control over the slew rate. In [107], a current-fed active voltage gate driver is proposed in which the current mirror provides constant current during the switching transitions and the active gate voltage control provides the control over slew rate at post turn ON and turn OFF. Also, the decrement of gate voltage during the post turn-ON interval increases the device's ON-state resistance, which dampens outs the oscillation in the device current and hence reduces the chance of EMI in the circuit. Additional research is required to further investigate the effect of gate current injection on the generation of switching oscillation. For a current-fed active voltage gate driver, a closed-loop-based approach can be implemented where the active voltage control can be automatically enabled based on the required control over the current and voltage slew rates. Such an approach has already been implemented for only active voltage gate drivers [19].

F. Current Diversion in CSD

Most of the inductor-based CSDs presented in the literature suffer from the current diversion problem where a part of the inductor current is diverted, which reduces the net current flowing into the gate terminal. With the reduction in the gate current magnitude over the switching period, the charging and discharging of the gate–source capacitor slows down. This results in increased switching time and hence larger switching losses. The major cause of the current diversion problem is due to the presence of intrinsic parasitic, mainly the common source inductor $L_{\rm s}$ and internal gate resistor $R_{\rm g(int)}$. To understand the current diversion phenomenon during the turn-ON and turn-OFF interval, an inductor-based CSD presented in [39] is taken as a reference with the circuit schematic depicted in Fig. 15. The SiC devices have larger $R_{\rm g(int)}$ accounting for larger voltage drop. This additional voltage drop can be compensated by increasing the magnitude of external gate–source voltage during the turn-ON instant. Prior to turning ON the power device, the current source inductor $L_{\rm r}$ is charged to the required magnitude of $i_{\rm Lr}$. Furthermore, during turn-ON instant, the stored energy in the inductor boost up the external gate–source voltage (voltage at point x), which can be expressed as follows:

$$V_x = V_{cc} \ + L_r \frac{di_{Lr}}{dt}. \tag{6}$$

The boosted voltage provides a compensation for the voltage drop caused due to $R_{\rm g(int)}$ but it also results in forward biasing of the body diode of S_3. With the diode being forward biased, it starts to conduct and a part of the inductor current is diverted through it and supplied back to the driving source as shown in Fig. 36(a). This effect is also termed body diode clamping effect. The CSDs proposed in [27], [35], [37], and [43] also suffer from a similar current diversion during turn-ON instant. The reduction in the input gate current slows down the charging of

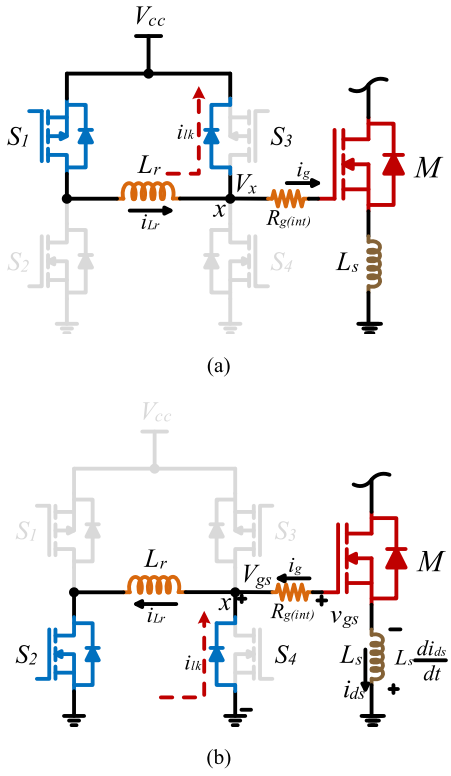

Fig. 36. Current diversion problem during (a) turn-ON instant and (b) turn-OFF instant.

gate–source capacitor, which results in larger turn-ON time and hence increased turn-ON switching losses. The current diversion, as reported in [39], can be avoided by blocking the conduction of S_3 body diode, which is achieved by placing a series diode with S_3, as proposed in [45]. During the turn-OFF instant, the common source inductor L_s has the major impact on the current diversion problem. The external voltage during the turn-OFF instant can be obtained as follows:

$$V_{\text{gs}} = -i_g R_{g(\text{int})} + v_{\text{gs}} - L_s \frac{di_{ds}}{dt}. \tag{7}$$

With the higher current falling rate (di_{ds}/dt), the voltage V_{gs} falls at a faster rate and once it goes beyond -0.7 V, it causes the body diode of control switch S_4 to be forward biased. With its conduction, a part of the inductor current is diverted through it, as shown in Fig. 36(b), and is termed the current diversion problem. With the reduction in effective gate current during the turn-OFF interval, it causes the slower discharging of the gate–source capacitor resulting in a larger turn-OFF time, and hence increased turn-OFF switching. It is also to be noted that because of L_s, the gate current diversion problem can become even worse under a high load current condition. This can be eliminated by blocking the conduction of body diode of S_4. In [43], it is achieved by replacing the control switch S_4 with the four-quadrant switch. However, this driver suffers from body-diode clamping during turn-ON instant. The CSDs proposed in [45], [46], and [48] are capable of eliminating the current diversion problem during both turn-ON and turn-OFF instants.

The development of WBG devices started over a decade ago and it still continues to push the boundaries to further improve their performance and overall switching characteristic. Talking about the maturity and the adoption of these devices, over the last ten years, there has been a tremendous boost in the utilization of WBG devices in various applications from both academia and industries due to their well-proven advantages over the conventional Si devices. The use of WBG devices in real-application products has started in the last few years, especially in low and medium power ranges. These devices have not yet completely penetrated the PE market as in most of the applications the conventional Si-based devices are still preferred widely. When the utilization of the device itself is not matured, its peripheral circuits, such as the gate driver and its technology, still lack further progress. Based on the WBG device development and utilization, its peripheral also needs further development to meet the additional requirement that the old generation VSDs fail to meet.

Based on the above discussion carried out, it can be said that the CSD can be a potential solution for driving the WBG devices due to its unique feature of constant current during switching transition allowing lesser switching time. This allows reduced switching loss and high-frequency switching operation. At present, researchers are using the current booster for increasing the magnitude of the input gate current magnitude [108]. Infineon [13] and ROHM [109], the pioneers in gate drivers manufacturing, have also started to explore the area of CSD and have claimed that the CSD boosts the turn-ON performance. There has been a lot of advancement in the field of device technology; however, they are still driven by the same conventional gate drivers used for the earlier ones. So, there is need to investigate further the best suitability of CSD for driving these new switching devices and to bring out their full potential by operating them at higher switching frequencies. All the CSDs either utilize discrete control switches or transistors for achieving the desired operation. There is a scope of integrating these switches or transistors to form a single package that are often termed monolith driver [32], [110]. Only the passive components and the driving supply can be integrated from outside along with the control signals. With these future developments carried out, it can be well said that CSD can be the most suitable choice for switching the WBG devices at higher frequency.

VI. Conclusion

In this article, a comprehensive review of CSD is described. On the basis of the operating principle, CSDs are grouped into two different categories: inductor-based CSDs and inductorless CSDs. According to the nature of the inductor current, they are further classified as continuous or discontinuous CSDs. When compared to continuous CSDs, discontinuous CSDs require a smaller current source inductor, and the discontinuous nature of the inductor current results in lower gate driver losses. In addition, the peak input gate current in discontinuous CSDs is independent of switching frequency and duty cycle, which results in better performance during sudden changes. However,

the complexity of the inductor-based driver increases due to the additional circuitry required for generating the constant current prior to switching transitions. The inductorless CSDs use various transistor-based circuits in order to generate a consistent current for fast switching ON and OFF of the power device. As a way to better understand the existing CSDs, they are categorized according to their structural characteristics, which include single-switch, dual-switch, half-bridge, full-bridge, isolated, and transistor-based CSDs. All CSDs are compared and the case studies are performed for the three different types of drivers selected based on the nature of the operation.

As a means of obtaining the switching performance of all the selected drivers, DPT has been performed on the SiC MOSFET. Simulation results indicated that continuous current inductor-based CSDs excelled in terms of fast switching action and low driver losses, although it comes at a high cost in terms of complexity. The transistor-based CSD is easier to implement but has higher driver losses. Although the CSDs have more gate driver losses than the VSD, the constant current prior to the switching transition reduces the switching time for power devices, resulting in lower switching losses. In order to prove the effectiveness of CSD over VSD, a comparative experimental study is carried out which proves that the CSD allows faster switching transition. Also, it is found that the turn-OFF and turn-ON times in the case of CSD are reduced by almost 75% and 50%, respectively, when compared to VSD. Furthermore, the general discussion and challenges in implementing the CSD applications are discussed. As a result of the constant current supplied by the CSDs, the WBG devices can operate at very high frequencies. In addition, CSDs can be found to be more advantageous in the case of series/parallel-connected power devices, protection, and high-voltage applications.

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