Boost-Based Active Power Decoupling Converter With Voltage Complementary for Electrolytic Capacitor-Less PMSM Drive System

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***Abstract*—A new boost-based active power decoupling circuit (APDC) with voltage complementary is proposed for electrolytic capacitor-less (ECL) permanent magnet synchronous motor (PMSM) drive systems. To increase the dc-link voltage level of the drive system, the decoupling capacitor of the APDC and the output capacitor of a boost converter are connected in series. Then, the decoupling capacitor and the boost output capacitor are complementarily controlled by the APDC to suppress the dc-link voltage ripple effectively. The capacitance and operation voltage of the two capacitors are diverse, improving the drive system's robustness to capacitance. By using this APDC, the speed range of ECL drive systems can be increased and good performance of PMSMs under stable and dynamic operation conditions can be implemented due to small dc-link voltage ripple. Finally, the experiments with the ECL drive system are accomplished to verify the feasibility.**

***Index Terms*—Active power decoupling circuit, complementary voltage, electrolytic capacitor-less drive system, high voltage gain converter.**

I. Introduction

NOWADAYS, electrolytic capacitor-less (ECL) drive systems have received more and more attention in permanent magnet synchronous motor (PMSM) drive systems due to their high reliability and long lifespan [1], [2]. However, owing to the use of small film capacitors rather than bulky electrolytic capacitors to decouple the grid pulsating power and the motor power, there is a large voltage ripple on the dc-link of ECL drive systems [3], [4], [5]. Therefore, resolving this issue has become a hot research topic in the PMSM drive system field.

In general, there are two typical approaches to suppress the dc-link voltage ripple, which are realized by the control strategies and active power decoupling circuits (APDCs). In the first approach, the dc-link small film capacitor is the only power decoupling unit for ECL drive systems. To relieve the decoupling power of the small film capacitor, the motor is used to buffer part of the grid pulsating power [6] or to inject a certain amount of harmonic current into the grid [7]. Although the structure is simple and easy to implement, ECL drive systems based on control strategies suffer from high grid current THD, large dc-link voltage ripple, and high motor torque fluctuation. Therefore, this type of ECL drive system can only be used in applications that do not require high motor performance, such as air conditioners, refrigerators, and washing machines [8], [9], [10].

In the second approach, the APDC is used as a power decoupling unit to replace the bulky electrolytic capacitor in ECL drive systems [11], [12]. It can actively and precisely buffer the grid pulsation power with small decoupling capacitors, thus significantly suppressing dc-link voltage ripple. As a result, ECL drive systems based on APDC offer the advantages of high-power factor, low dc-link voltage ripple, and low torque ripple. Depending on whether the voltage gain is greater than 1, APDCs can be divided into two categories: buck-based and boost-based. Higher dc-link voltage can expand the maximum speed and power of the motor and increase the power density of ECL drive systems [13], [14], [15]. Therefore, boost-based APDCs are the key research direction.

As for the boost-based APDCs, there are three main topologies. The first type is called split capacitor APDC, where two capacitors are connected in series to form the dc-link, and a half-bridge is used to control the voltage complementarity of the two capacitors to suppress the voltage ripple in the dc-link [16], [17]. However, a slight mismatch of the split capacitors leads to significant low-frequency components and odd harmonics in the dc-link voltage. Therefore, this type of APDC has strict requirements for the consistency of the two capacitors. No doubt, this issue increases the dc-link voltage ripple and degrades the grid current quality. In [18], a double-line frequency current was used as the control target in the decoupling controller instead of the line-frequency current, and a dc voltage bias factor was also introduced. The method was experimentally verified to be immune to capacitor mismatch. In [19], the single inductor is replaced by a split inductor. This configuration enhances the

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adjustability of split capacitors' voltage control and enables better dc-link voltage ripple suppression despite the discrepancy between the two capacitors.

The second type is parallel APDCs, which consists of a bidirectional power converter and a small power decoupling capacitor with high ripple voltage. The two ports of the parallel APDCs are, respectively, connected to the dc-link capacitor and the power decoupling capacitor. The operation principle of parallel APDCs is that when the dc-link voltage exceeds the set value, APDCs absorb the grid pulsating power and store it in the decoupling capacitor, and the dc-link voltage drops. On the contrary, APDCs release energy in the decoupling capacitor to the dc-link capacitor, and the load, the dc-link voltage rises. Some parallel APDCs are presented, where boost or buck–boost dc–dc converters can be used as bidirectional power converters [20], [21], [22], [23]. In addition, modified H-bridge inverters can also be used in parallel APDCs [24]. Compared with split-capacitor APDCs, the voltage of the power decoupling capacitor in parallel APDCs is independent of the dc-link capacitor voltage. Hence, the design of the parallel APDCs controller is easier, and the dc-link voltage ripple suppression effect is more robust to the APDCs parameter errors.

The third type is series APDCs, which are also known as high-gain APDCs due to their 1.5–2 times voltage gain. In this kind of APDC, the power decoupling capacitor is placed between the PFC converter and the dc-link capacitor, and the voltage of the power decoupling capacitor is the same polarity as the PFC output capacitor. In [25], the voltage of the power decoupling capacitor is controlled by the PWM H-bridge converter to achieve the same polarity and complementarity as the output voltage of the PFC converter. As a result, higher voltage gain is achieved and dc-link voltage ripple is effectively suppressed. In [26], this APDC can more accurately compensate for the output voltage distortion of the rectifier. However, this circuit is only suitable for PWM rectifiers. These two APDCs in [25] and [26] need more power switches, which increases the cost of ECL drive systems. To solve this problem, a modified boost converter is applied in APDC [27]. In essence, this topology is also a kind of split-capacitor APDC, but it is not strict with the consistency of split-capacitors. However, the voltage control of the split-capacitor is related to the grid current quality, which increases the design difficulty of the controller.

This article presents a novel high-gain APDC with two small unequal film capacitors. The primary aim of the proposed APDC is to increase the dc-link voltage level and increase the maximum speed of the motor. The APDC is composed of a boost PFC and an auxiliary power converter with only one power switch. The capacitors of the two converters are connected in series with the same polarity to form the dc-link with high voltage gain. The voltage ripple of the output capacitor of the boost PFC converter is related to the motor power, and only the average voltage needs to be controlled. Therefore, it is easier for the auxiliary power converter to control the decoupling capacitor voltage to be complementary with the PFC capacitor voltage. As a result, the dc-link voltage ripple is always controlled with a small range even under dynamic conditions, which can improve the dynamic state performance of the motor.

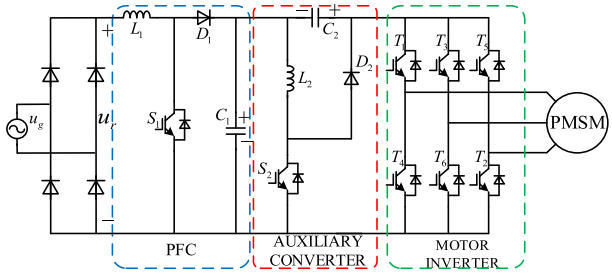

Fig. 1. ECL drive system based on the proposed APDC.

The rest of this article is organized as follows. In Section II, the structure of the proposed APDC and the voltage characteristics of ECL drive systems are studied. In addition, this section analyzes the operation theory of the proposed APDC. Section III presents the model of the proposed APDC and its control strategy. Section IV presents the design guidelines of key parameters. Section V verifies the performance of the ECL drive system based on the proposed APDC. Finally, Section VI concludes this article.

II. Proposed APDC and Voltage Characteristics

A. Structure of the Proposed APDC

Fig. 1 shows the ECL drive system based on the proposed APDC. The APDC consists of a boost converter and an auxiliary converter. The boost converter consists of a power switch S_1, a diode D_1, an inductor L_1, and a small film capacitor C_1. The auxiliary converter consists of a power switch S_2, a diode D_2, an inductor L_2, and a small film capacitor C_2. C_1 and C_2 are connected in series to form the dc-link capacitor $C_{\rm dc}$.

As a PFC converter, the boost converter controls the grid current to meet IEC 61000-3-2 harmonic and power factor standards. Meanwhile, the boost converter increases the voltage level of C_1. The auxiliary converter controls the voltages of C_1 and C_2 to be complementary to suppress the dc-link voltage ripple and achieve a higher dc-link voltage.

It is known that the voltage across C_1 can be expressed as [27]

$$u_{C1} = U_{C1} + F\sin(2\omega t + \theta). \tag{1}$$

To suppress the dc-link voltage ripple, the voltage across C_2 should be complementary to the voltage across C_1

$$u_{C2} = U_{C2} - F\sin(2\omega t + \theta) \tag{2}$$

where u_{C1}/u_{C2} and U_{C1}/U_{C2} are the instantaneous voltages and average voltages of C_1/C_2, respectively. F is the peak voltage of the ac components of u_{C1} and u_{C2}, θ is the phase difference between the grid voltage and u_{C1}/u_{C2}, and ω is the angular frequency of the grid voltage. The dc-link voltage can be obtained from (1) and (2)

$$U_{\rm dc} = u_{C1} + u_{C2}. \tag{3}$$

The voltage waveforms of u_{C1}/u_{C2} and $U_{\rm dc}$ are plotted in Fig. 2, which shows the dc-link voltage of the ECL drive system based on the proposed APDC is higher than that of a conventional boost converter and there is no voltage ripple. Therefore,

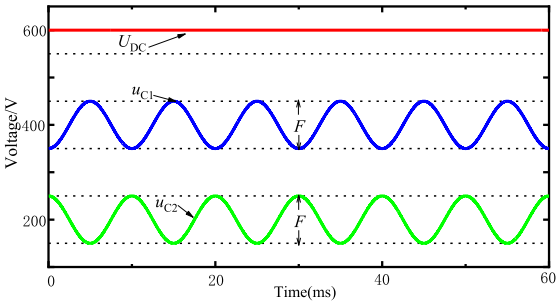

Fig. 2. Waveforms of u_{C1}/u_{C2} and U_{dc}.

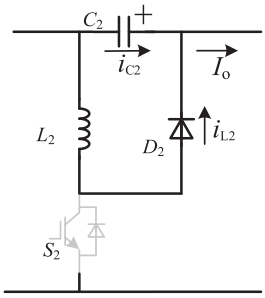

Fig. 3. State of i_{L2} when S_2 is OFF.

the proposed APDC can extend the speed range of the motor and the ECL drive system has good performance under both steady and dynamic working conditions. In addition, S_1 and S_2 have the same ground, which simplifies the design of the driver of the proposed APDC.

B. Voltage Analysis of the ECL Drive Based on the Proposed APDC

It is assumed that the grid voltage and current are in the same phase and are expressed as

$$u_g = \sqrt{2}U_g \sin(\omega t) \tag{4}$$

$$i_g = \sqrt{2}I_g \sin(\omega t) \tag{5}$$

where U_g and I_g are the grid rms voltage and current. The motor input instantaneous power p_g is expressed as

$$p_g = 2U_g I_g \sin^2(\omega t) = \underbrace{P_g}_{P_M} - \underbrace{P_g \cos(2\omega t)}_{p_r}. \tag{6}$$

Equation (6) shows that p_g consists of a dc component and a 2ω ac component. P_g and p_r are the average input power and pulsating power of the ECL drive system, respectively. P_M is the motor power and is equal to P_g. In the proposed APDC, p_r is stored in C_1/C_2 and L_1/L_2. According to the power balance relationship, there exists

$$p_r = p_C + p_L \tag{7}$$

where p_L and p_C are the total power of L_1/L_2 and C_1/C_2.

According to (4), the instantaneous power of L_1 is expressed as

$$p_{L_1}(t) = L_1 \frac{di_{L1}}{dt} i_{L1} = \omega I_g^2 L_1 \left|\sin(2\omega t)\right|. \tag{8}$$

The current through L_2 has different expressions according to the operation states of S_1 and S_2. Fig. 3 shows the state of i_{L2} when S_2 is OFF, and its expression is as follows:

$$i_{L2} = I_O - i_{C2} = I_O - C_2 \frac{du_{C2}}{dt} \tag{9}$$

where I_o is the load current, which is constant under steady-state operation conditions. It is well known that the current of the inductor cannot change abruptly. Therefore, (9) is used to analyze the instantaneous power of L_2. The instantaneous power of L_2 is obtained according to (2) and (9)

$$P_{L_2} = L_2 \frac{di_{L2}}{dt} i_{L2} = 4L_2 C_2 F \omega^2 [I_O - \omega C_2 F \sin(2\omega t + 2\theta)]. \tag{10}$$

The total instantaneous power of C_1/C_2 can be expressed as

$$\begin{aligned} p_C &= C_1 \frac{du_{C1}}{dt} u_{C1} + C_2 \frac{du_{C2}}{dt} u_{C2} \\ &= 2\omega F \left[\frac{F(C_1 + C_2)}{2} \sin(4\omega t + 2\theta) \right. \\ &\quad \left. + (C_1 U_{C1} - C_2 U_{C2}) \cos(2\omega t + \theta) \right]. \end{aligned} \tag{11}$$

From (8), (10), and (11), it can be seen that the instantaneous power of L_1/L_2 is much lower than that of C_1/C_2, so it is ignored in the following power analysis. According to the power balance principle, it can be obtained from (6) and (11)

$$\begin{aligned} p_r &= P_M \cos(2\omega t) \\ &= 2\omega F \left[\frac{F(C_1 + C_2)}{2} \sin(4\omega t + 2\theta) \right. \\ &\quad \left. + (C_1 U_{C1} - C_2 U_{C2}) \cos(2\omega t + \theta) \right]. \end{aligned} \tag{12}$$

Equation (12) shows that the frequency of grid instantaneous power is 2ω and the instantaneous power of C_1/C_2 has the 2ω and 4ω ac components. To meet the power balance, (12) is rewritten as

$$P_M \cos(2\omega t) \approx 2\omega F (C_1 U_{C1} - C_2 U_{C2}) \cos(2\omega t). \tag{13}$$

Accordingly, the product of U_{C1} and C_1 should be higher than the product of U_{C2} and C_2. In addition, F should be lower than U_{C2}, and θ equals zero. F is expressed as

$$F = \frac{P_M}{2\omega (C_1 U_{C1} - C_2 U_{C2})}. \tag{14}$$

In addition, F can also be expressed as [27]

$$F = \frac{K_1 P_M}{2\omega C_1 U_{C1}} = \frac{K_2 P_M}{2\omega C_2 U_{C2}} \tag{15}$$

where K_1/K_2 are the ratio of the grid instantaneous power absorbed by C_1/C_2 to the total grid instantaneous power.

Equation (15) shows that F and K_1/K_2 are inversely proportional to the capacitance and the voltages of C_1/C_2.

Furthermore, it can be seen from Fig. 2 that when C_1 (C_2) absorbs the grid pulsating power, $C_2(C_1)$ releases the stored pulsating power. Thus, the relationship between K_1 and K_2 is expressed as

$$K_1 - K_2 = 1 \& K_1 > 1. \tag{16}$$

Equation (16) means that the instantaneous power absorbed by C_1 is greater than the grid instantaneous power. To simplify the analysis, it is assumed that U_{C2} is $0.5U_{C1}$ and C_2 is $0.5C_1$. C_2 is calculated according to (14)

$$C_1 = \frac{2P_M}{3\omega F U_{C1}}. \tag{17}$$

Equation (17) shows that C_1 decreases with the increment of F. In the proposed ECL drive system, ω is 314 rad and U_{C1} is set as 400 V. It is assumed that the rated motor power is 1 kW and F is 100 V, and the total capacitance of C_1 and C_2 is 80 μF. For conventional drive systems with bulky electrolytic capacitors [8], the dc-link capacitor is

$$C = \frac{P_M}{2k\omega U_{C1}^2} \tag{18}$$

where k is the dc-link voltage ripple factor. When k is set as 2.5%, the capacitance is 398 μF, which is much larger than the required capacitance for the proposed APDC.

C. Suppression Principle of the DC-Link Voltage Ripple

It is assumed that the proposed APDC has stable input and output power during one operation cycle and that u_{C1} and u_{C2} remain constant. In this APDC, S_1 is used to control the grid power quality of the boost converter. In the existing literature, the control theory and the controller design of the boost PFC converter have been explained in detail and are not discussed in this article. Therefore, only the suppression principle of the dc-link voltage ripple is discussed.

Fig. 4. shows the four operating modes of the proposed APDC.

Mode I, S_1 is OFF and S_2 is ON. C_1 and L_1 store the grid power, and u_{C1} increases. The grid and C_2 in series supply power to the load. u_{C2} is controlled by adjusting the duty cycle of S_2 to increase or decrease the dc-link voltage.

Mode II, S_1 and S_2 are both OFF. C_1 continues to store the grid power and u_{C1} furtherly increases. L_2 releases some energy and stores in C_2 and u_{C2} increases. Since S_2 determines the energy released by L_2, the increase of u_{C2} is controlled by adjusting the duty cycle of S_2. In this mode, the dc-link voltage increases.

Mode III, S_1 and S_2 are both ON. The grid no longer supplies power to the load and L_1 stores the grid power. Meanwhile, C_1 not only supplies power to L_2 but also supplies power to the load in series with C_2. Therefore, u_{C1} and u_{C2} drop simultaneously, which results in the reduction of the dc-link voltage.

Mode IV, S_1 is ON and S_2 is OFF. C_1 continues to release energy and u_{C1} furtherly decreases. L_2 releases energy to C_2 and u_{C2} increases. Since S_2 determines the energy released by L_2, the increase or decrease of dc-link voltage can be controlled by adjusting the duty cycle of S_2.

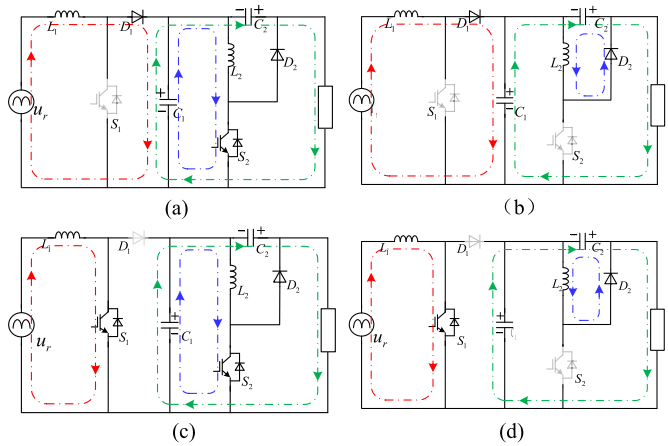

Fig. 4. Operation states of the proposed APDC. (a) Mode I; (S_1 = OFF/S_2 = ON). (b) Mode II (S_1 = OFF/S_2 = OFF). (c) Mode III (S_1 = ON/S_2 = ON). (d) Mode IV(S_1 = ON/S_2 = OFF).

These four modes indicate that u_{C1} and u_{C2} can be complementary by the coordinated control of S_1 and S_2. Therefore, the dc-link voltage ripple in the proposed APDC can be effectively suppressed.

III. System Modeling and Controller Design

A. Modeling of the Proposed APDC

According to Fig. 4, the state-space average model is formulated as follows:

$$L_1 \frac{di_{L1}}{dt} = u_r + (1 - d_1)u_{C1} \tag{19}$$

$$C_1 \frac{du_{C1}}{dt} = d_1' i_r + (2d_1 - 1)I_o \tag{20}$$

$$L_2 \frac{di_{L2}}{dt} = d_2 u_{C1} - d_2' u_{C2} \tag{21}$$

$$C_2 \frac{du_{C2}}{dt} = I_o - d_2' i_{L2} \tag{22}$$

where d_1 and d_2 are the duty cycles of S_1 and S_2, respectively. u_r is the full-wave rectified sine wave voltage, as shown in Fig. 4. According to (15) and (20), d_1 is obtained as

$$d_1 = 1 - \frac{u_r}{u_{C1}} - \frac{sgn(\cos(\omega t)) \cdot \omega L_1 I_g \cos(\omega t)}{u_{C1}} \tag{23}$$

where sgn is the sign function. Since the last term on the right-hand side of (23) is sufficiently small to be ignored, d_1 is further rewritten as

$$d_1 = 1 - \frac{u_r}{u_{C1}}. \tag{24}$$

Similarly, according to (17), the steady-state expression for d_2 is obtained as follows:

$$d_2 = \frac{u_{C2} + \mathrm{sgn}(\cos(\omega t))\omega L_2 I_{L2} \cos(\omega t)}{u_{C1} + u_{C2}}. \tag{25}$$

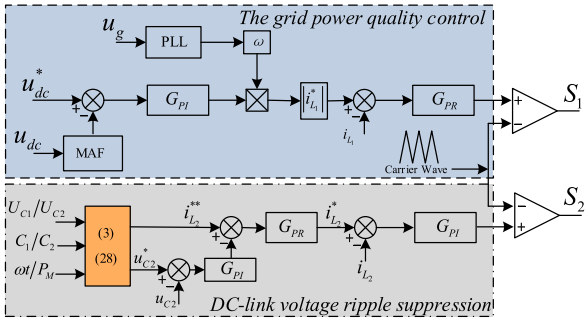

Fig. 5. Control strategy of the proposed APDC.

The ac term in (25) can be ignored, the above equation is simplified as

$$d_2 = 1 - \frac{u_{C1}}{u_{C1} + u_{C2}} = 1 - \frac{u_{C1}}{U_{\rm dc}}. \tag{26}$$

Equations (24) and (26) show that u_{C1} and u_{C2} can be effectively controlled by adjusting the duty cycle of S_1 and S_2. Equation (26) is further rewritten as

$$U_{\rm dc} = \frac{u_{C1}}{1 - d_2}. \tag{27}$$

It can be known that u_{C1} is higher than the grid peak voltage. Equation (27) indicates that the voltage gain of the proposed APDC is significantly higher than that of a conventional boost converter. As a result, the proposed APDC can extend the maximum speed range of the PMSM and increase its power level.

B. Controller Design

The control objective of the ECL drive system is to achieve high performance of drive systems under steady-state and dynamic operation conditions. Thus, the grid power quality of the ECL drive system should always satisfy the harmonics standard of IEC61000-3-2. Meanwhile, the dc-link voltage ripple should be controlled within the specified range, which is very important for high-performance motor operation.

The control diagram of the PFC converter is shown in the upper part of Fig. 5. This article still adopts the double-loop control structure of the traditional PFC controller. However, $U_{\rm dc}$ has a 2ω ac component due to the reduction of the decoupling capacitor. Thus, the moving average method is introduced to obtain the average dc-link voltage. In the output loop, a PI controller $G_{\rm PI}$ is adopted to calculate the grid average current referenceI_g^*, which is multiplied by the grid frequency ω and used as the reference current i_{L1}^* of the inner loop. Since i_{L1}^* is a 2ω full-wave rectified sine wave, the proportional-resonant (PR) controller $G_{\rm PR}$ is designed to regulate the grid current in the inner loop. The grid voltage frequency is provided by a single-phase phase-locked loop.

The control diagram of the dc-link voltage ripple suppression is shown in the lower part of Fig. 5, and it is performed by adjusting the duty cycle of S_2. According to the analysis in Section II, if i_{L2} is controlled as (9), the APDC can effectively suppress the dc-link voltage ripple.

Taking (14) into (9), the following equation is obtained:

$$i_{L2} = I_O - i_{C2} = \frac{P_M}{U_{\rm dc}} - \frac{C_2 P_M}{(C_1 U_{C1} - C_2 U_{C2})} \cos(2\omega t). \tag{28}$$

Equation (28) shows that the amplitudes of the dc component and ac components of i_{L2} can be considered constant under steady operation conditions. Under dynamic operation conditions, the amplitudes of the dc component and ac component of L_2 vary with the load, and the amplitude of the ac component is related to the capacitances and voltages of C_1/C_2 and the motor power.

However, there exists some error between the feedback and reference $i_{\rm L2}$ in (28) due to parameter error, controller bandwidth, and other factors, which will degrade the performance of the dc-link voltage ripple. To resolve this issue, the error between u_{C2} and u_{C2}^* is introduced to modify the reference current i_{L2}^{**}.

IV. Design of Decoupling Capacitor and Inductor

A. Selection of C_1 and C_2

In the proposed APDC, the rated $U_{\rm C1}$ and $U_{\rm C2}$ are 400 V, and the rated dc-link voltage is 600 V. The maximum value of F is 100 V, i.e., $0.5U_{\rm C2}$. The motor power is maximum when the ECL drive system operates under dynamic operation conditions, which is 0.8 kW.

Equation (28) indicates that the ac component should be smaller than the dc component. The following constraint is obtained:

$$\frac{P_M}{U_{\rm dc}} > \frac{C_2 P_M}{(C_1 U_{C1} - C_2 U_{C2})}. \tag{29}$$

Taking these voltages into (29), the relation of C_1 and C_2 should be met

$$C_1 > 2C_2. \tag{30}$$

When the motor power is maximum, F is $0.5U_{\rm C2}$. Equation (14) is rewritten as

$$C_1 U_{C1} - C_2 U_{C2} = 2C_1 - C_2 > \frac{P_{M-\max}}{\omega U_{C2}^2}. \tag{31}$$

Combining (30) and (31), C_1 and C_2 can be calculated by

$$\begin{cases} C_1 > \frac{2P_{M-\max}}{3\omega U_{C2}^2} \\ C_2 > \frac{P_{M-\max}}{3\omega U_{C2}^2} \end{cases}. \tag{32}$$

When the rated power of the ECL drive system is 400 W, C_1 is greater than 20 μF and C_2 is greater than 10 μF. Under dynamic working conditions, the maximum motor power is less than 800 W. C_1 is greater than 40 μF and C_2 is greater than 20 μF. In the actual APDC, considering system efficiency and margin, C_1 is finally selected as 50 μF and C_2 is selected as 25 μF.

TABLE I
KEY PARAMETERS OF THE PROPOSED ECL DRIVE SYSTEM

APDC		PMSM			
Symbol	Value	Symbol	Value	Symbol	Value
U_g	220 V	Rated power	0.4 kW	p	2
ω	314 rad/s	Rated torque	2N·m	Rated voltage	400V
C_1/C_2	50 μF/25μF	Rated speed	3000 rpm	L_d/L_q	2.7mH/6.7mH
L_1 and L_2	3 mH/3mH	Vpk/krpm	98.3V		

B. Selection of L_1 and L_2

The design guideline of L_1 is the same as the traditional Boost PFC converter

$$L_1 \geq \frac{\sqrt{2} \times U_{g-\min} \times D_{\min}}{\gamma \times I_{PK} \times f_s} \tag{33}$$

where $U_{\text{g-min}}$ is the minimum grid voltage, which is 200 V. $D_{\min}$ is the minimum duty cycle of $U_{\text{g-min}}$, which is about 0.293.γ is the current coefficient, which is 0.4. f_s is the switching frequency of S_1, which is equal to 20 kHz. I_{PK} is the peak current of the grid, which is 2.98 A at the rated power, and when the motor is running at the maximum power, I_{PK} is 5.95 A. Based on the above currents, L_1 is calculated to be 3.48 mH and 1.74 mH, respectively, and L_1 is chosen as 3 mH according to the experimental performance of the ECL drive system.

The switching frequency of S_2 is much higher than the grid frequency. Thus, it can be assumed that u_{C1} and u_{C2} remain unchanged within one switching cycle. According to the above analysis, when S_2 is ON, the voltage of L_2 is equal to u_{C2}. There is

$$L_2 \frac{\Delta i_{L2}}{d_2 T_s} = u_{C2}. \tag{34}$$

Substituting (2) and (26) into (34), L_2 can be expressed as

$$L_2 = \frac{(U_{C2} - F\cos(2\omega t))^2}{\Delta i_{L2}} T_s. \tag{35}$$

Considering dynamic operation conditions, (35) is further rewritten as

$$L_2 > \frac{(U_{C2} - F)^2}{\Delta i_{L2-\min}} T_s. \tag{36}$$

In this article, L_2 works in the current continuous mode, and the key parameters of the proposed APDC are listed in Table I. According to (36) and Table I, it is calculated that L_2 should be larger than 0.5 mH. Although a smaller L_2 can improve the power density of the ECL drive system, it leads to a large ripple current, which not only reduces the efficiency of the ECL drive system but also degrades the control accuracy of u_{C2}. Therefore, L_2 should be optimized according to the operation state of the ECL drive system. Finally, L_2 is chosen as 3 mH.

V. EXPERIMENTAL RESULTS

To verify the feasibility of the ECL drive system based on the proposed APDC, the experimental results are presented in this section. The experimental system is shown in Fig. 6. A PMSM is tested and the other PMSM acts as the loaded, which is linked to a motor using a coupling. A controller based on

Fig. 6. Experimental platform setup. (a) Controller and power converter. (b) Motor test platform.

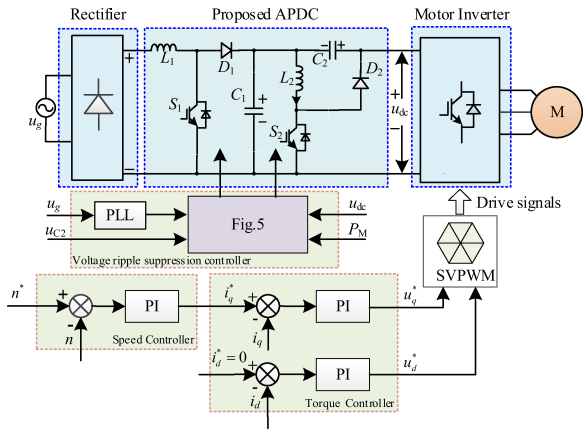

Fig. 7. Control diagram of the proposed SC drive system.

DSP TMS320F28335 with a 150 MHz clock is employed. The detailed parameters of PMSM and APDC are listed in Table I.

An inverter with a 5 kHz switching frequency is used to control the tested PMSM. In this inverter, Infineon IKP04N60T is selected as the power switch, which is 600 V, 4 A IGBT with the antiparallel diode. In the proposed APDC, S_1 and S_2 are IKA15N60T IGBTs with 600 V and 15 A, and D_1 and D_2 are IDV08E65D2 with 650 V and 8 A. The switching frequency of S_1 and S_2 is 20 kHz. C_1 and C_2 are WIMA film capacitors. 2ED020I12-F are used to drive S_1 and S_2. Voltage Hall sensors and current Hall sensors are used to accurately measure the voltage and current required by the controller. The actual motor speed and the rotor position are measured by a photoelectric encoder.

Fig. 7 shows the overall control scheme of the proposed ECL drive system. The control method of the grid current quality and the dc-link voltage ripple suppression have been discussed in detail in the previous section. For the PMSM control, there is a closed-loop speed controller and a closed-loop current controller. The output of the speed controller is the current

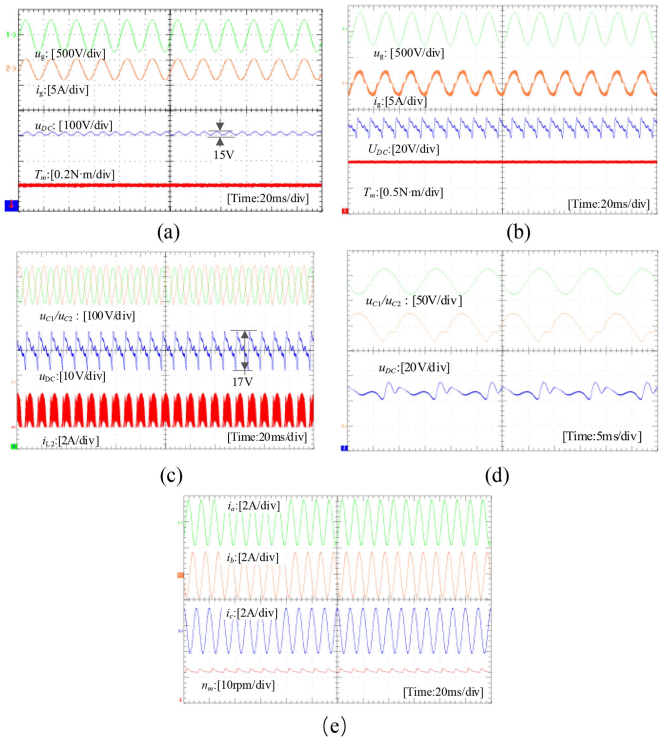

Fig. 8. Steady-state experimental waveforms. (a) u_g, i_g, n, and T_m of the conventional drive system. (b) u_g, i_g, n, and T_m of the proposed ECL drive system. (c) u_{C1}, u_{C2}, u_{dc}, and i_{L2} of the proposed ECL drive system. (d) Zoom-in view of u_{C1}, u_{C2}, and u_{dc} of the proposed ECL drive system. (e) Three-phase currents and motor speed of the proposed ECL drive system.

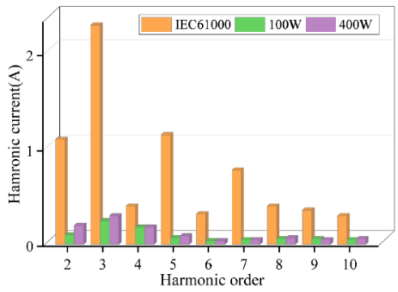

Fig. 9. Harmonics analysis of the grid current i_g.

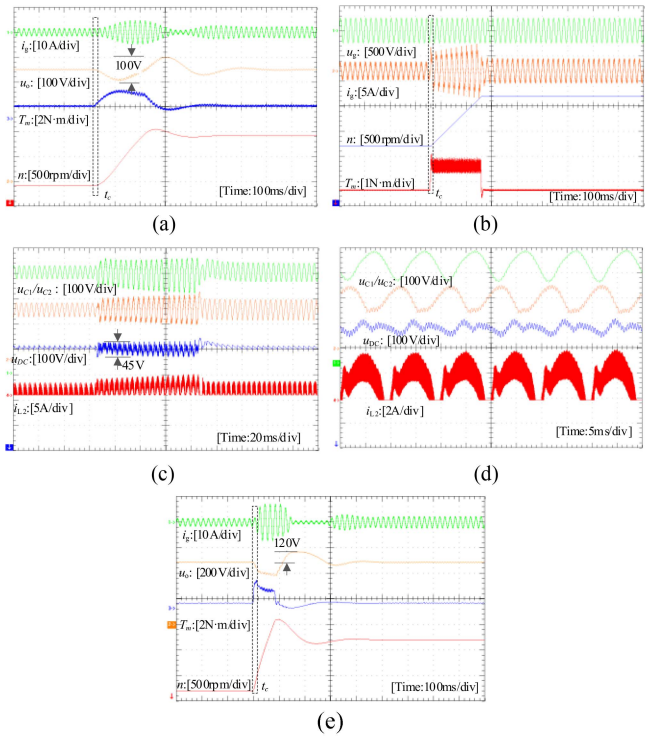

Fig. 10. Speed-up experimental waveforms. (a). i_g, u_{dc}, n, and T_M of the conventional drive system. (b) u_g, i_g, n, and T_M of the proposed ECL drive system. (c) u_{C1}, u_{C2}, u_{dc}, and i_{L2} of the proposed ECL drive system. (d) Zoom-in view of u_{C1}, u_{C2}, u_{dc}, and i_{L2} of the proposed ECL drive system. (e)i_g, u_{dc}, n, and T_M of the conventional drive system with the same control parameters as ECL drive system.

reference i_q* according to the error between the given speed $n*$ and the feedback speed n. Space vector control with $i_d = 0$ is applied in the current control, and a PARK transformation is used to transform three-phase currents into i_d and i_q, and the outputs of the current controller are u_d and u_q. And then, the control signal of the motor inverter is generated by SVPWM control according to u_d and u_q to realize the high-performance PMSM operation.

Four experiments are performed to evaluate the performance of the ECL drive system based on the proposed APDC. In the first experiment, the steady experimental is conducted. In the second experiment, the performance of speed-up operation conditions is analyzed. In the third experiment, the experimental waveforms are presented for load-up. Finally, two drive systems are tested at a 5000 r/min.

In the first experiment, the conventional drive system and the proposed drive system are tested. The experimental conditions are a given speed of 3000 r/min and a given load of 1 N·m. The conventional drive system has a 1000 μF electrolytic capacitor for power decoupling and uses a boost converter as a frond-end converter for power factor correction. In this drive system, the dc-link voltage is set as 450 V.

Fig. 8(a) and (b) shows that the two drive systems have steady dc-link voltage. As a result, lower speed ripple and lower torque ripple are achieved, which verifies the good steady performance of the ECL drive system. Fig. 8(c) and (d) shows that u_{C1} and u_{C2} are almost perfectly complementary and there is only 17 V peak–peak voltage on the dc-link, which proves that the structure of the proposed APDC and control strategy is correct. Meanwhile, u_{C2} and i_{L2} have the same frequency, and the waveform of i_{L2} validates the theory of (28). This means u_{C2} can be controlled by the duty of S_2. Fig. 8(e) shows the waveforms of the three-phase current and the speed of the motor. These experimental results show the motor has lower current harmonics and speed ripple in steady operation conditions. Fig. 9 shows that although the proposed ECL drive system has higher THD than the conventional drive system, it still meets the harmonic standard of IEC61000-3-2.

Fig. 10 compares the performance of speed-up change between the conventional drive system and the proposed drive

system. In this experiment, the load is always 1 N·m. The initial given speed is 2000 r/min, and it increases to 3000 r/min at t_C.

In Fig. 10(a) and (b), different FOC and dc-link voltage control parameters were used for the two drive systems due to the difference in dc-link capacitor. The experimental results show that the response time during the speed transient period is 0.34 s and 0.24 s for the conventional drive system and the proposed ECL drive system, respectively. This indicates that the proposed ECL drive system has a shorter response time than the conventional drive system. In addition, the speed overshoot of the proposed ECL drive system and the conventional drive system is 12 r/min and 125 r/min, respectively. Therefore, with the same speed overshoot requirement, it is reasonable to assume that the proposed ECL drive system reacts faster than the conventional drive system. Also, as can be seen in Fig. 10(a) and (b), the maximum dc-link voltage drop of the conventional system is 45 V and the maximum dc-link peak–peak voltage is 100 V, which is about two times higher than that of the proposed ECL drive system. This explains why the speed response of the conventional drive system is not as good as the proposed one. In addition, it can be seen that the 100 V voltage drop degrades the performance of the gird current.

Fig. 10(c) and (d) shows that the ac components of u_{C1} and u_{C2} increase correspondingly with the increase of the motor output power when the given speed increases from 2000 r/min to 3000 r/min. In addition, it is noted that the above ac components remain better complementary during the transient with the control strategy shown in Fig. 5. As a result, the voltage ripple of the dc-link is only 50 V in the case of sudden speed changes. This is also the guarantee of good speed-up performance of the proposed ECL drive system. In addition, it can be seen that the current of L_2 increases during transient, which is consistent with the theoretical analysis. Fig. 10(e) shows that the key experimental waveforms of the conventional drive system with the same control parameters as ECL drive system. It can seen that the dynamic response of motor torque and speed is greatly improved, and the dc-link voltage restabilization time is reduced from 0.6 s to 0.4 s. However, the maximum dc-link voltage is 570 V, which is already more than the rated voltage of the electrolytic capacitor. Therefore, different control parameters should be used for the two motor drive systems.

Fig. 11 shows the experimental waveforms of the conventional drive system and the proposed ECL drive system under load-up operation conditions. In this experiment, the given speed is 1000 r/min. The initial load is 1 N·m and it becomes 1.5 Nm at t_C. Fig. 11(a) and (b) shows that the speed drop of the proposed ECL drive system and the conventional drive system is 6 r/min and 70 r/min during the load-up transient period, respectively. Meanwhile, it can be seen that the transient recovery times for load changes of the conventional drive system and the proposed drive system are 0.25 s and 0.24 s, respectively. In Fig. 11(a) and (c), the maximum dc-link voltage drop during the transient period of the load change experiment is 30 V for the proposed ECL drive system, which is one-third of the conventional drive system. These experiments show that the proposed ECL drive system has better performance than the conventional drive system for reasons similar to the speed change experiments. In addition, large voltage drop also leads to degradation of the grid power quality. Fig. 11(c) and (d) shows that u_{C1} and u_{C2} are still complementary during load-up operation conditions. Therefore, the proposed ECL drive system has only a 30 V voltage drop on the dc-link. This again verifies that the proposed dc-link voltage ripple suppression control strategy is effective.

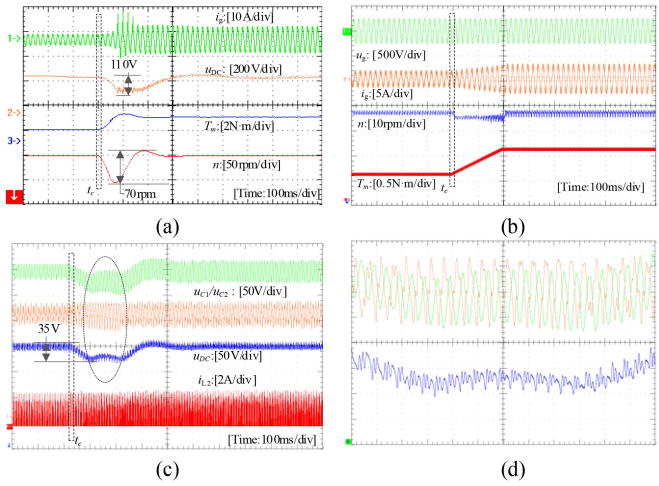

Fig. 11. Load step-up experimental waveforms of two-drive systems. (a) i_g, u_{dc}, n, and T_M of the conventional drive system. (b) u_g, i_g, n, and T_M of the proposed ECL drive system. (c) u_{C1}, u_{C2}, u_{dc}, and i_{L2} of the proposed ECL drive system. (d) Zoom-in view of u_{C1}, u_{C2}, and u_{dc} of the proposed ECL drive system.

The dynamic experimental results show the proposed ECL drive system has better performance than that of the conventional drive system. The reason is that the conventional system voltage control uses a PI controller, which has a delay due to an integral unit. In the proposed APDC, the dc-link voltage is controlled by instantaneous current control. Figs. 10(c) and 11(c) shows the average voltage of C_1 keeps stable and the peak–peak voltage of C_1 increases with the increase of the motor power. The decoupling capacitor C_2 has the same peak–peak voltage as C_1 by adopting the instantaneous current control. Therefore, u_{C1} and u_{C2} are always complementary under steady or dynamic operation conditions. Therefore, the proposed APDC can effectively suppress the dc-link voltage ripple.

Fig. 12 shows the experimental waveforms of the two drives at a given speed of 5000 r/min and 1 N·m load. At the given speeds, the theoretical values of the back EMF of the motor are 491 V. According to the LVL principle, it is known that the dc-link of the conventional drive system with a 450 V dc-link voltage can only provide energy to the motor intermittently, Fig. 12(a) shows that there is a peak–peak voltage of over 150 V on the dc-link. As a result, the motor phase current and the grid current have 153.6% and 179.2% THD, as shown in Fig. 12(b). This not only degrades the grid current quality but also increases the torque ripple of the conventional drive system. and the motor speed fluctuates by a maximum of 120 r/min, which means that conventional drive systems cannot run at 5000 r/min with high performance.

It can be seen from Fig. 12(c) that the dc-link ripple voltage is less than 10% in the proposed ECL drive system. Therefore,

TABLE II
COMPARISON OF KEY PARAMETERS OF EXISTING APDCS

APDCs	Rating power	Passive Components	IGBT/Diode	Input/output Voltages (V)	Peak-Peak voltage Steady/dynamic (V)	Volume (cm^3)	Price ($)
[19]	700W	2×150μF/0.2mH/0.5mH	6/4	393/220	12.67/×	691.53	87.92
[20]	800W	120μF/5μF/300μH/2mH	2/4	220/190	×	252.94	55.00
[21]	300W	90μF/30μF/3mH/1.5mH/200μH	3/6	110/250	12/×	213.29	50.90
[22]	2kW	110μF/135μF/1.44mH/ 0.72mH	6/×	220/400	×	604.30	171.27
[23]	100W	40μF/10μF/1.8mH	2/6	110/150	×	85.2	44.21
[24]	400W	22μF/1.5mH/30μH	5/1	130/400	14.68/×	128.09	30.67
[25]	2kW	2000μF/220μF/3.3μF/ 100μH/100μH	5/1	400/220	14.9/56	175.95	150.22
[26]	4kW	220μF/220μF/8.5mH/ 2*1.85mH	6/×	220/450	27.5/100	677.81	136.61
[27]	400W	50μF/25μF/2*4mH	2/6	220/600	27/50	174.16	20.9
This paper	400W	50μF/25μF/2*3mH	2/6	220/600	17/45	172.55	20.78
Electrolytic capacitor		1000μF/575V				271.7	34.57

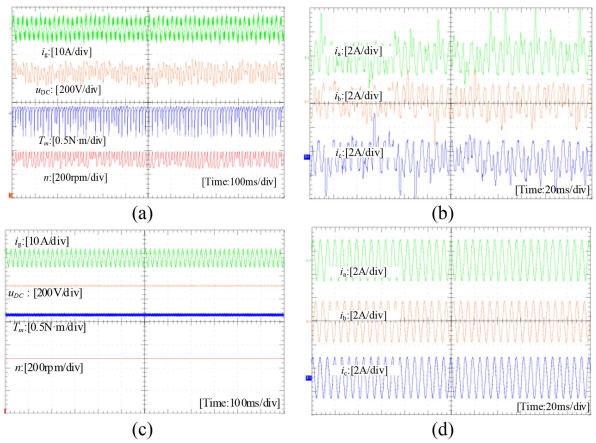

Fig. 12. As 5000 r/min experimental waveforms of two-drive systems. (a) i_g, u_{dc}, n, and T_M of the conventional drive system. (b) Three-phase currents of the conventional drive system. (c) u_g, i_g, n, and T_M of the proposed ECL drive system. (d) Three-phase currents of the proposed ECL drive system.

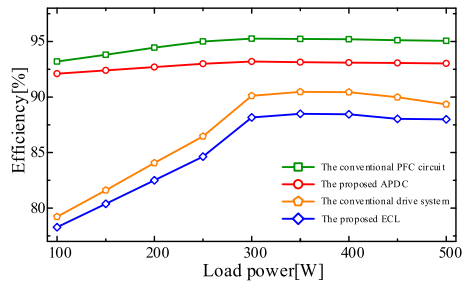

Fig. 13. Efficiency curves of the proposed APDC and ECL drive system.

the THD of i_g reaches 13.27% and the THD of motor phase current is 15.5%, as shown in Fig. 12(d). As a result, the proposed ECL drive system can still operate with a 20 r/min ripple due to the 600 V dc-link voltage. The performance of a conventional drive system is the same as that of an ECL drive system when operated at 600 V dc link voltage. However, four 1000 μF/450 V electrolytic capacitors need to be connected in series-parallel to form a 1000 μF/600 V dc link capacitor bank, which significantly increases the cost and size of the conventional drive system. This validates the overall performance advantage of the proposed ECL drive system at high speeds.

Fig. 13 shows the efficiency of the proposed APDC and a boost converter. To improve the measurement accuracy, the efficiency tests are performed with resistive loads, and the dc-link voltage is fixed at 600 V and 450 V. For the proposed APDC, the peak efficiency is 93.22% at 400 W and the lowest efficiency is 91.4% at 150 W. For the boost converter, the peak efficiency is 94.23% at 400 W and the lowest efficiency is 93.4% at 150 W. The efficiency of the proposed system is lower than that of a conventional boost PFC rectifier due to the auxiliary power converter and the secondary flow of the grid pulsating power.

In Fig. 13, the whole efficiency curves of the conventional drive and the proposed drive under steady-state conditions are also provided. These curves indicate that the efficiency of the proposed drive system is still inferior to that of the conventional drive system. The reason is that under steady-state conditions, both drive systems can operate at lower current harmonics, resulting in essentially the same motor efficiency. Therefore, the difference in efficiency between the two systems is mainly due to the APDC power loss.

Table II compares the main parameters of the existing APDCs. It can be found that all existing APDCs can effectively suppress voltage ripples under stable operation conditions, but the peak–peak voltage of [25] is greater than the given dc-link voltage by 14% under dynamic operation conditions. Although [24] has a lower voltage ripple under dynamic operation conditions, it has a higher size and price due to more power devices and passive components. The APDC in [23] has the smallest volume. However, it is rated at only 100 W. Compared to other APDCs, the proposed APDC has only two power devices, which is the least among all circuits. In addition, the proposed APDC has a voltage gain of 2.72 times, which widens the speed range and power range of the motor. Overall, the proposed APDC is very competitive considering cost, size, peak–peak voltage, and voltage gain.

VI. Conclusion

In this article, a high gain APDC is proposed to expand the motor speed range from 3000 to 5000 r/min. The proposed APDC consists of a boost converter and an auxiliary converter. The dc-link consists of two small unequal film capacitors connected in series, which not only increases the dc-link voltage but also improves the immunity to capacitive errors. An instantaneous current control strategy is proposed to make the voltages of two capacitors be complementary under steady and dynamic operation conditions. Thus, the proposed ECL drive system always has small voltage ripple and a voltage gain of 600 V on the dc-link. As with the conventional ECL drive, the THD of the proposed ECL drive system under steady-state conditions meets the ICE-61000-3-2 standard. In addition, compared with the conventional system, the proposed ECL drive system reduces the dc-link voltage drop by 40%, improves the transient response time by 29.4% and reduces the speed overshoot by 10 times under speed-up operation conditions. The proposed ECL drive system reduces the dc-link voltage drop by 5 times and the speed overshoot by 11 times under load-up operation conditions. These experiments verify that the proposed ECL drive and control method is significant and efficient.

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