Adaptive Damping Ratio Control of Parallel Buck Converters for the Marine Pulsed Power Loads

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***Abstract*—Parallel buck converters are increasingly being taken to interface pulsed power loads (PPLs) in ships. The voltage of the converters will deteriorate under the periodic power steps of PPL in a very short time. To this end, this article proposes an adaptive damping ratio control (ApDRC) for the parallel converters. The mechanism of voltage regulation is explored, enabling the voltage to be regulated directly and accurately by the damping ratio of the system. Unlike most existing controls, of which performances are parameter-associated, ApDRC is parameter-independent through adaptive damping ratio design, such that good voltage regulation can be always ensured regardless of varying changes in the load. Moreover, the load transient evolution is first investigated, revealing how duty-cycle saturation affects the load transients, and what is the corresponding solution. Experimental results demonstrate that the proposed control can achieve fast voltage regulation while having small static errors and good disturbance rejection.**

***Index Terms*—Damping ratio, duty-cycle saturation, parallel buck converters, pulsed power load (PPL), voltage regulation.**

NOMENCLATURE

m	Number of parallel buck converters.
L_i, C_i	Inductor and output capacitor of the *i*th buck converter, where $i \in [1, m]$.
r_{Li}, r_{Ci}	Equivalent series resistances of L_i and C_i.
i_{oi}, i_{Li}, i_{Ci}	Load current, inductor current, and capacitor current of the *i*th buck converter.
v_{in}, v_o	Input voltage and output voltage of parallel buck converters.
i_o, i_L	Sum of i_{oi}, and sum of i_{Li}.
T_s	Control cycle.
t, t_n	Time and time of the *n*th control cycle.
W_S	Converters' energy deviation from the steady states.
k_S^+, k_S^-	Rising slope and falling slope of W_S.
v_o^{ref}	Reference of v_o.
W_S^{ref}	Reference of W_S.
$x(t)$	Discrete-time value of generalized variable x at t, such as $v_{in}(t_n)$, $v_o(t_n)$, and $i_{Li}(t_n)$.
$\tilde{x}(t)$	Estimated value of generalized variable x at t, such as $\tilde{v}_o(t_{n+1})$, $\tilde{i}_{Li}(t_{n+1})$, and $\tilde{W}_S(t_{n+1})$.
$\Delta\tilde{x}(t_{n+1})$	Increment of generalized variable x from t_n to t_{n+1}, such as $\Delta\tilde{v}_o(t_{n+1})$, $\Delta\tilde{i}_{Li}(t_{n+1})$, and $\Delta\tilde{W}_S(t_{n+1})$.
ζ	Damping ratio of second-order systems.
ζ^*	Desired damping ratio.
ζ^{op}	Overshoot-preventing damping ratio.
ω_n	Natural oscillation frequency of second-order systems.
w_{ic}	Introduced gain that affects damping ratio ζ.
r_{di}	Droop coefficient for the *i*th converter.
$v_o{}^*$	New reference of v_o under drop action.

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I. INTRODUCTION

PULSED power loads (PPLs), such as radar, sonar, and electromagnetic devices, are increasingly being utilized in ships [1], [2]. These loads consume a large amount of energy in a short time once triggered, resulting in an instantaneous voltage drop. Serving as an important interface of PPLs [3], [4], parallel buck converters play a vital role in achieving fast voltage regulation through control. The converter control directly determines the actual power exported to the PPLs, acting as an energy transfer regulator between the PPLs and the source, which usually uses an energy storage system (ESS) due to its fast dynamic response [5]. In improving the voltage regulation, aggressive converter control without a transfer pace limit may accumulate too much energy in the converters, leading to undesired voltage overshoot and energy loss of the ESS. By contrast, conservative converter control prolongs the voltage regulation [6], increasing the risk of continuous voltage deterioration under the repeated pulses of the PPLs. This can trip the sensitive loads offline and even lead to a system-wide stability issue [7], [8]. Therefore, the converter control with fast voltage regulation through providing accurate energy transfer is the key to handling the voltage issue caused by the PPLs.

Linear controls are commonly applied in buck converters for the superiorities of simple structure and ease of design. They are usually designed at a steady-state operating point so that the transfer function of the voltage can be obtained to improve the performance. However, the control precisions are limited

since the performances vary with the operating points [9], especially under large load transients. The performances would exacerbate if the new steady-state point is far away from the selected point [10]. Consequently, for the converters with high-power PPLs, linear controls fall short of providing good performance.

In contrast, nonlinear controls have exhibited better performance in handling large load transients, as they often introduce the disturbance dynamics between the old and new steady states into the control design. Several prevailing nonlinear controls, such as sliding mode control (SMC), active disturbance rejection control (ADRC), and passivity-based control (PBC), which can be classified as observer-based controls for the critical role of state observer, perform well in achieving fast voltage regulation. However, these observer-based controls are usually parameter-dependent due to the presence of the parameters introduced in the observer and the controller, thus degrading the robustness of the performance. For example, the second-order-type, PI-type, and PID-type sliding functions of SMCs proposed in [11], [12], and [13], introduce different numbers of controller parameters. As these parameters determine the convergence rate of SMCs, the parameter-tuning guidelines have been released in [11], [12], [13], [14], and [15] to enhance performance. Similarly, the tracking error/disturbance observers of ADRC with different orders are proposed in [16], [17], [18], [19], and [20], where the number of observer parameters will increase if a higher-order observer is adopted [17]. Disturbance observers with introduced parameters are employed in PBCs likewise, as reported in [21] and [22]. In summary, these observer-based controls are typically parameter-dependent such that the control performance could vary with the parameters, and the parameter tuning will become tricky if the load is of uncertain varying transients.

Quite different from observer-based controls, robust controls deal with uncertain load transients by confining the eigenvalues of the closed-loop system within the expected region, therefore, no observer is required. They can be regarded as parameter-independent as they are often designed based on performance-associated indices, e.g., the maximum natural frequency and the maximum settling time [10], [23]. However, these boundary-constrained indices indicate that there is a compromise between robustness and performance, thereby bringing on difficulties in obtaining both strong robustness and high control precision. Besides, almost all the aforementioned observer-based controls and robust controls are exclusive to the single buck converter, therefore, current sharing for parallel converters is not included. In this regard, finite time technique-based controls proposed in [22] and [24], achieve both good voltage regulation and current sharing for parallel buck converters. The strict derivations of finite-time technique-based controls prove that the voltage and the output current can converge to their respective references in a finite time. Nevertheless, they are also parameter-associated. Therefore, there is still a lack of parameter-independent control for parallel buck converters, especially in handling varying load transients and taking current sharing into account.

Another important focus of the converter control is the effect of duty-cycle saturation on control performance. In this regard, two concerns regarding the effect of duty-cycle saturation arise. First, duty-cycle saturation is intrinsic to practical applications but is often not directly considered in the control designs [14], [15], [16], [17], [18], [19], [20]. As a result, the effect of duty-cycle saturation can cause a difference between theoretical and actual control performances. The effect of duty-cycle saturation can be alleviated by using a high control frequency, but it can lead to increase in switching loss and high-frequency noise [25]. In addition, this approach may also cause some typical practical control application issues, such as the more serious chattering phenomenon in SMCs [26]. Second, how duty-cycle saturation affects load transients is less discussed. If duty-cycle saturation occurs, which makes the actual duty cycle stay within the range of [01], it will be unclear whether the duty cycle is still optimal in accelerating voltage regulation or if it could increase the risk of voltage overshoot. The insight into load transient evolution accounting for duty-cycle saturation can assist in designing a control that realizes the full potential of the regulation capacity of the duty cycle. However, to the best knowledge of the authors, this load transient evolution has not been explored yet.

In summary, due to the introduced parameters and skipping the effect of duty-cycle saturation in control designs, the performance of most prevailing controls can vary with load transients and exhibit a difference between theoretical and actual indices. To realize good performance in converter control, exploring the mechanism of voltage regulation as an alternative to complex nonlinear control techniques would be an effective way to make the control more straightforward. However, there is still a lack of mechanism-based parameter-independent control for buck converters. Given all of this, this article attempts to fill this gap. The main contributions are summarized as follows.

1) The mechanism of fast voltage regulation is explored by the single-input single-output (SISO) transfer function of the voltage and its reference, enabling the voltage to be adjusted directly and accurately by the damping ratio of the control system.
2) This control is parameter-independent due to its adaptive damping ratio design, and the effect of duty-cycle saturation on control performance has been eliminated through the introduced overshoot-preventing damping ratio. As a result, fast voltage regulation performance can be always obtained regardless of varying transients in the load.
3) The load transient evolution, accounting for duty-cycle saturation, is explored from the perspective of damping ratio, revealing how duty-cycle saturation affects the load transients and why there is a tradeoff between accelerating voltage regulation and reducing the risk of voltage overshoot.

The rest of this article is organized as follows. The model of parallel buck converters is introduced in Section II, Section III proposes the adaptive damping ratio control (ApDRC), and

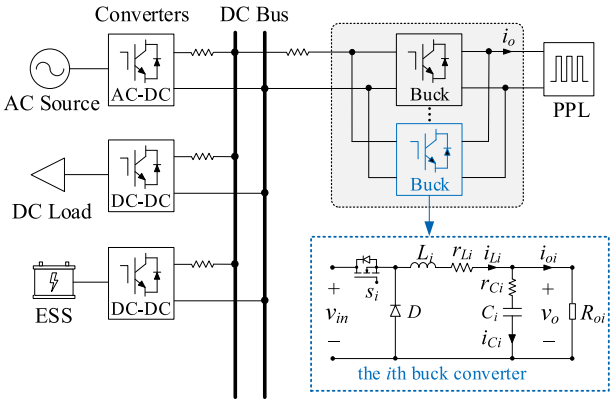

Fig. 1. Studied PPL supply structure in ship DC microgrids.

Section IV investigates the adaptive damping ratio design accounting for duty-cycle saturation. Simulation and experiment results are given in Sections V and VI. Finally, Section VII concludes this article.

II. Power Supply Structure for PPLs

A. Parallel DC–DC Buck Converters

Parallel buck converters are increasingly utilized to interface PPLs and have been applied in ship dc microgrids, to satisfy the high-power supply and high-reliability requirements. The transfer power of the converters can be equally distributed through control, reducing the output imbalance and the current stress on the gate switches. The investigated PPL supply structure in ship dc microgrids is given in Fig. 1.

For the m-parallel converters, the ith converter ($i \in [1, m]$) is composed of a gate switch s_i, a diode D, an inductor L_i, and a capacitor C_i. The ESRs of L_i and C_i are shown as r_{Li} and r_{Ci}. v_{in} and v_o are the input voltage and the output voltage, i_{oi}, i_{Li}, and i_{Ci} are the load current, the inductor current, and the capacitor current, whose respective sums are denoted by i_L, i_C, and i_o. And, R_{oi} is the equivalent load resistance for the ith converter, which can be estimated by $R_{oi} = v_o/i_{oi}$.

The average model of dc–dc converter is often used to mimic the converter dynamics as it closely approximates the switching model within a certain frequency range. Considering r_{Li} and r_{Ci} are small and the converters commonly operate in continuous conduction mode [27], the inductor current of the ith converter can be expressed in a discrete-time form as

$$\begin{cases} \Delta\tilde{i}_{Li}(t_{n+1}) = \frac{v_{in}(t_n)}{L_i} d_i(t_n) T_s - \frac{v_o(t_n)}{L_i} T_s \\ \tilde{i}_{Li}(t_{n+1}) = i_{Li}(t_n) + \Delta\tilde{i}_{Li}(t_{n+1}) \end{cases} \tag{1}$$

where T_s is the control cycle, and t_n is the time of the nth control cycle. The variable followed with a (t_n) denotes its discrete-time value at t_n. For example, $d_i(t_n)$ is the discrete-time value of d_i at t_n. The variable with a "$\sim$" on top indicates that it is an estimated value and $\Delta\tilde{i}_{Li}(t_{n+1})$ is the increment of $\tilde{i}_{Li}(t_{n+1})$ at t_{n+1}.

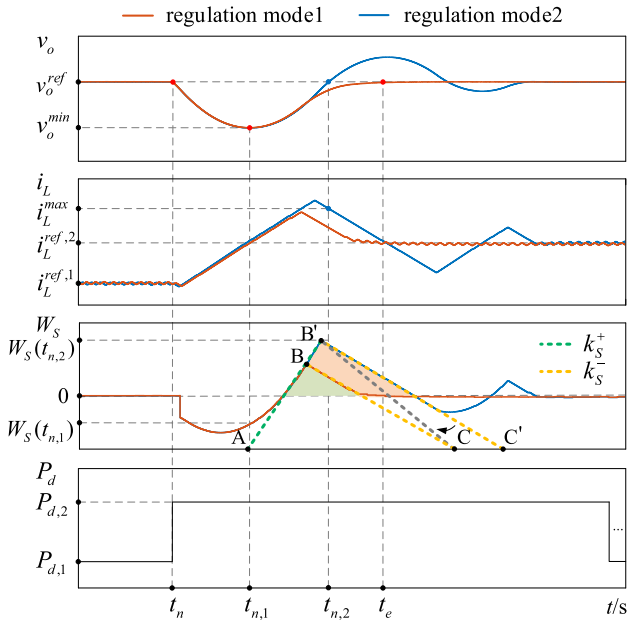

Fig. 2. Performance comparison under different regulation modes.

Then, the estimated voltage at t_{n+1}, $\tilde{v}_o(t_{n+1})$, and its increment, $\Delta\tilde{v}_o(t_{n+1})$, can be obtained as

$$\begin{cases} \Delta\tilde{v}_o(t_{n+1}) = \frac{T_s}{C}\left\{\sum_{i=1}^{m}\left[i_{Li}(t_n) + \Delta\tilde{i}_{Li}(t_{n+1})\right] - i_o(t_n)\right\}, \\ \left(C = \sum_{i=1}^{m} C_i\right) \\ \tilde{v}_o(t_{n+1}) = v_o(t_n) + \Delta\tilde{v}_o(t_{n+1}) \end{cases} \tag{2}$$

where it is considered that the dc component of the inductor current enters into the load, while the ac component flows into the capacitors, leading to the change in the voltage [28].

B. Problem Description of Voltage Regulation

The load transient is actually a process of energy transferring and rebalancing in the converters, accompanied by the voltage recovering to its reference. Fig. 2 compares different regulation modes to explain the necessity of exploring the optimized trajectory of voltage regulation, and how duty-cycle saturation affects the transient, where v_o^{ref} is the reference of v_o, W_S is the converters' total energy deviation from the steady states, whose time-domain expression can be defined as (3). k_S^+ and k_S^- are the rising slope and falling slope of W_S, which are manifested as the green and the orange dotted lines in the 3rd subplot of Fig. 2, and P_d is the load power

$$W_S(t) = \frac{1}{2}\sum_{i=1}^{m} L_i\left\{i_{Li}(t)^2 - \left[\frac{1}{m}i_o(t)\right]^2\right\} + \frac{1}{2}C\left[v_o(t)^2 - v_o^{ref\,2}\right]. \tag{3}$$

In the transient, two aspects shall be concerned about.

1) Optimized Trajectory of V_o *Regulating to its Reference:* Once the optimized trajectory of v_o can be obtained, the control only needs to track it by adjusting the duty cycle. To this end,

establishing the SISO transfer function of v_o and v_o^{ref} is a direct way to explore this trajectory by means of performance design. However, the converter control with voltage tracking is actually multiple-inputs single-output (MISO) [29], as the input voltage acts as another input in the closed-loop system, and thus makes the design of the voltage regulation complex and unclear.

In addition, the optimized trajectory of v_o is also the accurate dynamics of the converter energy balance. Whether fast voltage regulation can be achieved, depends on the dynamics of W_S. As illustrated in Fig. 2, $W_S > 0$ acts as an accelerator in the voltage regulation when $v_o < v_o^{\text{ref}}$, but it would increase the risk of voltage overshoot when $v_o > v_o^{\text{ref}}$. For example, the enclosed green area in W_S can effectively accelerate the voltage regulation; by contrast, the enclosed orange area in W_S, which appears in the regulation mode2, will result in the voltage overshoot and the unnecessary power loss of the ESS.

2) Effect of Duty-Cycle Saturation on the Transient: Even if the optimized trajectory of v_o can be obtained, it is still not enough to ensure the control applicable to any load with varying transients, since the effect of duty-cycle saturation has not been considered yet.

In Fig. 2, the corresponding actual k_S^-s of these two regulation modes are manifested as the dotted lines BC and B'C'. It is seen that, before $t_{n,2}$, the regulation mode2 could be advantageous in minimizing the regulation time of v_o compared to the regulation mode1 if the actual k_S^- is not limited by the duty-cycle saturation (i.e., the actual k_S^- alters from the line B'C' to the line B'C). However, the excess energy manifested as the enclosed orange area, would backfire and bring about a voltage overshoot, once it cannot reduce to zero in time due to the effect of duty-cycle saturation. Therefore, the insight into load transient evolution accounting for duty-cycle saturation could assist the control to maximize the regulation capacity of the duty cycle.

III. Adaptive Damping Ratio Control

A. Embedded Optimal Control Scheme

1) Adjustable Gain-Based Voltage Regulation Control: Voltage regulation control is to adjust the output voltage to its reference quickly in the transients. Note that the capacitor current directly reflects the change in the voltage, it is small in the steady states since the load current is mainly provided by the inductor current [27], while varying to maintain the current balance in the transients.

Then, the objective function $J_1(v_o)$ is set up, where the effect of the capacitor currents on the voltage regulation is considered, providing the option to further change the regulation pace of v_o. $J_1(v_o)$ is defined as

$$J_1(v_o) = {X_1}^T Q X_1, X_1 = \begin{bmatrix} v_o^{\text{ref}} - \tilde{v}_o(t_{n+1}) \\ \tilde{i}_C(t_{n+1}) \end{bmatrix},$$
$$Q = \begin{bmatrix} 1 & 0 \\ 0 & w_i \end{bmatrix} \tag{4}$$

where $\tilde{i}_C(t_{n+1})$ is the estimated value of i_C at t_{n+1}, whose gain in $J_1(v_o)$ is w_i. Q is the gain matrix. The optimal solution for the control at t_{n+1} is calculated based on the inputs at t_n.

Replacing $\tilde{i}_C(t_{n+1})$ with the discrete-time expression shown in (5), and substituting it into (4) yields an updated $J_1(v_o)$, which is shown in (6), where $w_{ic} = w_i(C/T_s)^2$

$$\tilde{i}_C(t_{n+1}) = C\frac{\tilde{v}_o(t_{n+1}) - v_o(t_n)}{T_s} = C\frac{\Delta\tilde{v}_o(t_{n+1})}{T_s} \tag{5}$$

$$J_1(v_o) = {X_1}^T Q X_1, X_1 = \begin{bmatrix} v_o^{\text{ref}} - \tilde{v}_o(t_{n+1}) \\ \Delta\tilde{v}_o(t_{n+1}) \end{bmatrix},$$
$$Q = \begin{bmatrix} 1 & 0 \\ 0 & w_{ic} \end{bmatrix}. \tag{6}$$

To get the minimum $J_1(v_o)$, the derivative of $J_1(v_o)$ is obtained in (7), as Q is a symmetric matrix

$$J_1'(v_o) = \frac{\partial J_1(v_o)}{\partial X_1} = QX_1 + Q^T X_1 = 2QX_1. \tag{7}$$

Let $J_1'(v_o) = 0$, we can obtain the optimal $\Delta\tilde{v}_o(t_{n+1})$ as

$$\Delta\tilde{v}_o(t_{n+1}) = \tilde{v}_o(t_{n+1}) - v_o(t_n) = \frac{v_o^{\text{ref}} - v_o(t_n)}{1 + w_{ic}}. \tag{8}$$

Substituting (8) into (2) yields (9), which should be followed to ensure the above-mentioned optimal $\Delta\tilde{v}_o(t_{n+1})$

$$\sum_{i=1}^{m} \tilde{i}_{Li}(t_{n+1}) = \frac{v_o^{\text{ref}} - v_o(t_n)}{1 + w_{ic}} \frac{C}{T_s} + i_o(t_n). \tag{9}$$

2) Current Sharing Control: It is necessary for parallel buck converters due to the presence of the ESRs and the differences in the circuit parameters. The control objective is to minimize the total deviation between the inductor currents and the reference $i_L^{\text{ref}}(t_{n+1})$ which is defined as

$$i_L^{\text{ref}}(t_{n+1}) = \frac{1}{m}\sum_{i=1}^{m}\left[\tilde{i}_{Li}(t_{n+1})\right]. \tag{10}$$

Then, the objective function $J_2(i_L)$ is set up in (11), where the weight matrix R is an identity matrix I with m rows and m columns, making all the inductor currents have the same weight tending towards $i_L^{\text{ref}}(t_{n+1})$. E is a matrix with m rows and m columns, whose elements are all equal to 1

$$\begin{aligned} J_2(i_L) &= \sum_{i=1}^{m}\left[i_L^{\text{ref}}(t_{n+1}) - \tilde{i}_{Li}(t_{n+1})\right]^2 \\ &= \left[\left(\frac{1}{m}E - I\right)X_2\right]^T R \left[\left(\frac{1}{m}E - I\right)X_2\right] \\ &= {X_2}^T \underbrace{\left(-\frac{1}{m}E + I\right)}_{W} X_2. \end{aligned} \tag{11}$$

X_2 and $\bar{X}_2$ are the vectors of the inductor currents and their references, which are defined as

$$X_2 = \begin{bmatrix} \tilde{i}_{L1}(t_{n+1}) & \cdots & \tilde{i}_{Lm}(t_{n+1}) \end{bmatrix}^T$$
$$\bar{X}_2 = \begin{bmatrix} i_L^{\text{ref}}(t_{n+1}) & \cdots & i_L^{\text{ref}}(t_{n+1}) \end{bmatrix}^T. \tag{12}$$

To minimize $J_2(i_L)$, the derivative of $J_2(i_L)$ can be obtained as

$$J_2'(i_L) = \frac{\partial J_2(i_L)}{\partial X_2} = WX_2 + W^T X_2 = 2WX_2. \tag{13}$$

3) Optimal Solution: The unique optimal solution cannot be obtained from $J_2'(i_L) = 0$ as the matrix W is singular. According to $J_1'(v_o) = 0$, the sum of X_2 should satisfy the requirement of (9). Replacing the last row of W with (9) to update W to W', we can obtain a new expression as

$$\underbrace{\begin{bmatrix} -\frac{1}{m}+1 & \cdots & -\frac{1}{m} & -\frac{1}{m} \\ \cdots & \cdots & \cdots & \cdots \\ -\frac{1}{m} & \cdots & -\frac{1}{m}+1 & -\frac{1}{m} \\ 1 & \cdots & 1 & 1 \end{bmatrix}}_{W'} X_2 = \begin{bmatrix} 0 \\ \cdots \\ 0 \\ \frac{v_o^{\text{ref}} - v_o(t_n)}{1+w_{ic}} \frac{C}{T_s} + i_o(t_n) \end{bmatrix}. \tag{14}$$

Combining (1) with (14), the duty cycle of the ith converter, $d_i(t_n)$, can be solved as

$$d_i(t_n) = \frac{L_i \left\{ -m i_{Li}(t_n) + m \frac{v_o(t_n) T_s}{L_i} + i_o(t_n) + \frac{v_o^{\text{ref}} - v_o(t_n)}{1+w_{ic}} \frac{C}{T_s} \right\}}{m v_{in}(t_n) T_s}. \tag{15}$$

Equation (15) shows that w_{ic} is the only variable to be decided, and the control will be parameter-independent once w_{ic} can be adjusted automatically.

B. Mechanism of Fast Voltage Regulation

The knowledge about the SISO closed-loop transfer function of the voltage and its reference enables an accurate time-domain regulation design. In other words, the trajectory of the output v_o regulating to the input v_o^{ref} can be optimized thus. To obtain this SISO transfer function, the key step is to transform d_i and v_{in} into a specific form that removes their presence in the function. Otherwise, that v_{in} acts as another input making the closed-loop system turn to be MISO, and the nonlinearity introduced by the saturation of d_i makes the time-domain control design more complex. Fortunately, (15) transforms the joint effect of d_i and v_{in} into the change of v_o, providing the option to obtain the SISO transfer function.

Here, the current balance of the converters can be shown as

$$\begin{cases} i_{Li}(t_n) = \frac{v_o(t_n)}{R_{oi}} + C_i \frac{\partial v_o(t_n)}{\partial t} \\ \sum_{i=1}^{m} i_{Li}(t_n) = \frac{v_o(t_n)}{R_o} + C \frac{\partial v_o(t_n)}{\partial t} \quad \left(\frac{1}{R_o} = \sum_{i=1}^{m} \frac{1}{R_{oi}} \right) \end{cases} \tag{16}$$

where the ESRs are ignored since they are relatively small and cannot be accurately obtained.

Substituting (15) into (1) and (10) yields (17). It is considered that $\tilde{i}_{Li}(t_{n+1})$ can fully respond to $i_L^{\text{ref}}(t_{n+1})$ as expected, while the effect of duty-cycle saturation cannot be ignored and will be discussed in Section IV

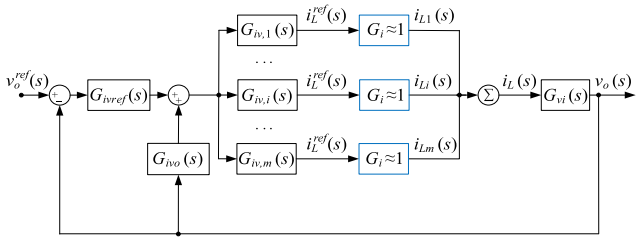

Fig. 3. Closed-loop diagram of parallel buck converters.

$$\tilde{i}_{Li}(t_{n+1}) \approx i_L^{\text{ref}}(t_{n+1}) = \frac{1}{m} \frac{v_o(t_n)}{R_o} + \frac{1}{m} \frac{v_{\text{ref}} - v_o(t_n)}{1+w_{ic}} \frac{C}{T_s}. \tag{17}$$

Combining with the z-domain discrete transform, $\tilde{i}_{Li}(t_{n+1}) = z\, i_{Li}(t_n)$, and the transform between z domain and s domain, $z = 1 + sT_s$, the s-domain transfer functions in (18) can be obtained, where the variables with a (s) indicate their s-domain forms

$$\begin{cases} G_{iv\text{ref}}(s) = \frac{1}{1+w_{ic}} \frac{C}{T_s}, \; G_{ivo}(s) = \frac{1}{R_o} \\ G_{vi}(s) = \frac{R_o}{1+CR_o s}, \; G_{iv,i}(s) = \frac{1}{m} \frac{1}{1+sT_s} \quad (\forall i \in [1,m]) \end{cases}. \tag{18}$$

According to (18), the closed-loop diagram of the converters is illustrated in Fig. 3, where $G_i \approx 1$ indicates $\tilde{i}_{Li}(t_{n+1}) \approx i_L^{\text{ref}}(t_{n+1})$ mentioned above.

Then, the closed-loop transfer function of the voltage and its reference, $G_c(s)$, can be obtained as

$$\begin{aligned} G_c(s) = \frac{v_o(s)}{v_o^{\text{ref}}(s)} &= \frac{m G_{iv\text{ref}}(s) G_{iv,i}(s) G_{vi}(s)}{1 + m[G_{iv\text{ref}}(s) - G_{ivo}(s)] G_{iv,i}(s) G_{vi}(s)} \\ &= \frac{1}{(1+w_{ic}) T_s{}^2 s^2 + (1+w_{ic}) \left(1 + \frac{T_s}{CR_o}\right) T_s s + 1}. \end{aligned} \tag{19}$$

$G_c(s)$ is a typical second-order system, of which the damping ratio ζ and the natural oscillation frequency ω_n are

$$\zeta = \frac{1}{2} \left(1 + \frac{T_s}{CR_o}\right) \sqrt{1+w_{ic}}, \; \omega_n = \frac{1}{T_s} \sqrt{\frac{1}{1+w_{ic}}}. \tag{20}$$

According to the performance of second-order systems, the step response of $G_c(s)$, which exhibits the time-domain trajectory of v_o regulating to its reference, is decided by the damping ratio [30]. Specifically, an overshoot in v_o occurs when the system is underdamped (i.e., $0 < \zeta < 1$), while it can be avoided when the system becomes overdamped (i.e., $\zeta > 1$). This does not mean that a larger damping ratio is better since the settling time of v_o increases with the damping ratio.

The step responses of $G_c(s)$ under various damping ratios and the same ω_n are illustrated in Fig. 4. Unlike the underdamped and overdamped systems, fast voltage regulation without any overshoot is obtained when the system is critically damped (i.e., $\zeta = 1$). Therefore, taking $\zeta^* = 1$ as the desired damping ratio, fast voltage regulation can be achieved easily by adjusting the initial damping ratio to the desired damping ratio ζ^* via w_{ic}. Therefore, by rearranging (20), the selection of w_{ic}, $w_{ic,1}$, is

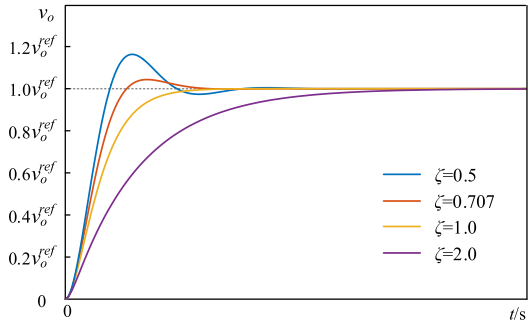

Fig. 4. Step responses of $G_c(s)$ under the input $v_o^{\text{ref}}(s) = v_o^{\text{ref}}/s$.

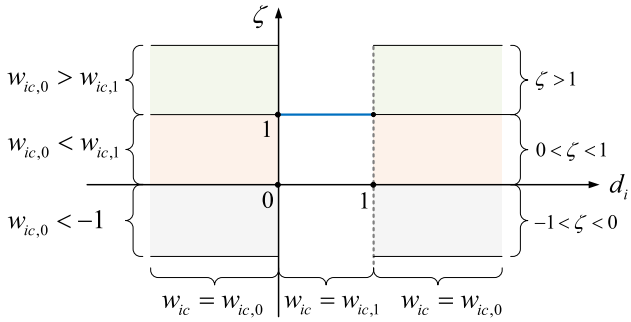

Fig. 5. Relationship between the actual damping ratio and w_{ic}.

obtained as

$$w_{ic,1} = \left(\frac{2\zeta^*}{1 + \frac{T_s}{CR_o}} \right)^2 - 1. \tag{21}$$

Moreover, according to the stability criterion of second-order systems that requires $\zeta > 0$, this system will be stable if $w_{ic} > -1$ is held, otherwise, it will fall into oscillation and divergence, since one eigenvalue of $G_c(s)$ is positive and the other one is negative, and thus the damping ratio becomes $-1 < \zeta < 0$.

Remark 1: The exploration of the SISO transfer function $G_c(s)$ enables the voltage to be regulated directly and accurately by changing the damping ratio. It is based on the assumption that the initial damping ratio can be always regulated to the desired damping ratio without being affected by duty-cycle saturation. However, this assumption may not always hold true for all load transients, especially for large load transients. Hence, to realize our goal of making the control with strong performance robustness, how duty-cycle saturation affects load transients and what the corresponding solution is will be discussed next.

IV. Adaptive Damping Ratio Design Accounting for Duty-Cycle Saturation

A. Load Transient Evolution Accounting for Duty-Cycle Saturation

According to (15), the duty-cycle saturation can be avoided by scaling w_{ic} to make all the duty cycles stay within the range of [0, 1]. Once the effect of duty-cycle saturation is transformed into the change in the damping ratio, the analysis of the load transient evolution from the perspective of the damping ratio will become straightforward. Here, we define $D_i(t_n)$ as the upper and lower boundaries of $d_i(t_n)$ in (15), which is expressed as

$$D_i(t_n) = \begin{cases} 1, & (d_i(t_n) > 1) \\ 0, & (d_i(t_n) < 0) \end{cases}. \tag{22}$$

Substituting (22) into (15) yields the boundary of w_{ic}, $w_{ic,0}$, which is shown as

$$w_{ic,0} = \max \left\{ \frac{v_o^{\text{ref}} - v_o(t_n)}{\frac{D_i(t_n) v_{in}(t_n) T_s}{L_i} + i_{Li}(t_n) - \frac{v_o(t_n) T_s}{L_i} - \frac{i_o(t_n)}{m}} \frac{1}{m} \frac{C}{T_s} - 1 \right\} \quad (\forall i \in [1, m]) \tag{23}$$

where $\max(\cdot)$ is the maximum value operator.

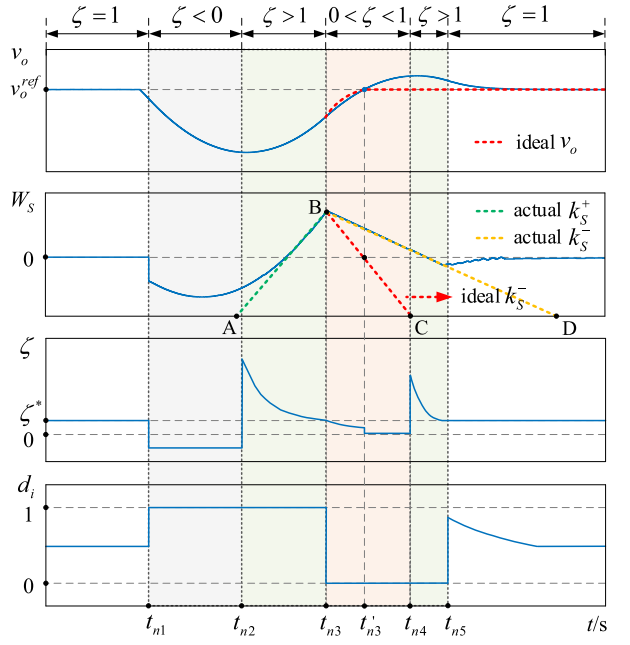

Fig. 6. Illustration of the load transient evolution accounting for duty-cycle saturation from the perspective of damping ratio.

Since w_{ic} turns to be determined by $w_{ic,0}$ instead of $w_{ic,1}$ when duty-cycle saturation occurs, the effect of duty-cycle saturation on the load transients is essentially manifested as the change in the damping ratio, making the corresponding analysis clearer. The relationship between the actual damping ratio and w_{ic} is illustrated in Fig. 5. During duty-cycle saturation, the system is overdamped when $w_{ic,0} > w_{ic,1}$, whereas it becomes underdamped when $w_{ic,0} < w_{ic,1}$. Although $w_{ic} > -1$ is always guaranteed in the control, the system will be unstable if $w_{ic,0} < -1$.

Then, the load transient evolution accounting for duty-cycle saturation can be detailed into different stages according to the change of the damping ratio, as illustrated in Fig. 6. It should be mentioned that the following full stages are illustrated to explain how duty-cycle saturation affects the load transient and explore the reason for potential voltage overshoot. The 2nd, 3rd, and

4th stages, which are described as "conditional," only occur on condition that the transients encounter duty-cycle saturation.

1) Unstable Stage (in $\mathrm{t_{n\,1}}$–$\mathrm{t_{n\,2}}$*):* It occurs at the beginning of the transient. w_{ic} is determined by $w_{ic,0}$ due to duty-cycle saturation, and becomes smaller than -1, which conflicts with the stability criterion. Thus, the system is unstable. From the perspective of converter dynamics, although all the duty cycles have reached their maximum, v_o keeps decreasing as the capacitors have to discharge to balance the output current, which is contrary to the theoretical expectation of increasing v_o.

2) Overdamped Stage (in $\mathrm{t_{n\,2}}$–$\mathrm{t_{n\,3}}$*, Conditional):* It is a mixed stage that can accelerate voltage regulation while increasing the risk of voltage overshoot. Although the actual $\zeta > 1$, the control is still optimal in minimizing the regulation time of v_o since the maximum duty cycles are taken. On the other hand, whether the control is aggressive depends on the damping ratio of the next stage. Once the system becomes underdamped in the next stage such that W_S cannot reduce to zero in time, this stage could backfire and become the risk source of voltage overshoot.

3) Underdamped Stage (in $\mathrm{t_{n\,3}}$–$\mathrm{t_{n\,4}}$*, Conditional):* It occurs on condition that $w_{ic,1} < w_{ic,0}$ is still held due to duty-cycle saturation, otherwise, the load transient will directly jump to the 5th stage, achieving the optimal voltage regulation. In this stage, if things go as we desired, W_S should reduce to zero in pace with v_o recovering to its reference. As illustrated in Fig. 6, W_S should reduce to zero at $t_{n3}^{'}$ under the work of the ideal k_S^- which is shown as the red dotted line BC. However, the underdamped system would force the actual k_S^- operate as the orange dotted line BD, making the excess energy of W_S cause a voltage over-shoot. In summary, the duty-cycle saturation in this stage is the decisive reason for voltage overshoot.

4) Reoverdamped Stage (in $\mathrm{t_{n\,4}}$–$\mathrm{t_{n\,5}}$*, Conditional):* It always appears in pair with the 3rd stage and gets a large damping ratio, which can be treated as a self-mitigating measure of the system to suppress the voltage overshoot caused by the 3rd stage. It should be noted that though the 3rd and 4th stages only appear once in Fig. 6, they might repeat if the system falls into a damped oscillation.

5) Desired Damping Ratio Stage (After $\mathrm{t_{n\,5}}$*):* The system comes to this stage when duty-cycle saturation has not occurred or has ended. The desired damping ratio takes over the choice of w_{ic}, i.e., $w_{ic} = w_{ic,1}$. It should be mentioned that this 5th stage could come after the 1st or 2nd stage immediately if the duty-cycle saturation ends after t_{n2} or t_{n3}.

Remark 2: As revealed by (20) and illustrated in Fig. 4, the voltage regulation performance is determined by the damping ratio, e.g., a voltage overshoot occurs indicating that the system is underdamped. Thus, the load transient evolution is essentially the dynamics of the damping ratio, enabling it to be divided into different stages.

Remark 3: For the load transients without being affected by duty-cycle saturation, there only exists the 1st and 5th stages; by contrast, for the load transients encountering duty-cycle saturation, the conditional stages, the 2nd, 3rd, and 4th stages, may appear, in which the underdamped characteristic of the 3rd stage may cause a voltage overshoot. Therefore, to ensure the control applies to all load transients, an adaptive damping ratio design will be carried out next.

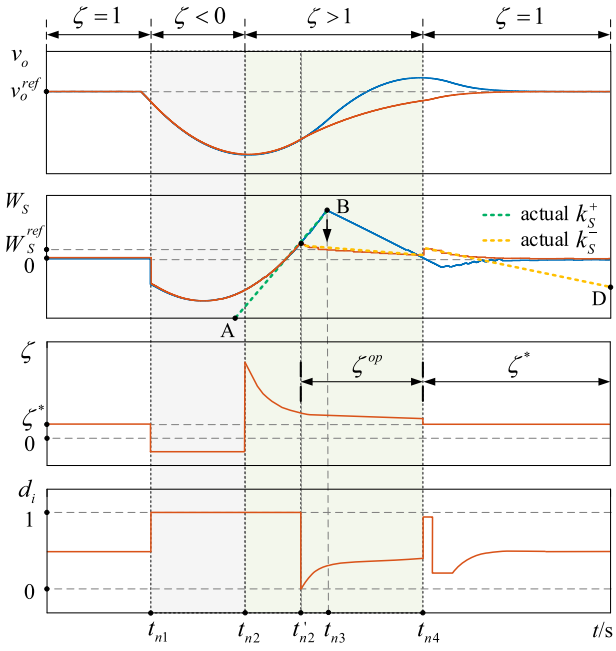

Fig. 7. Illustration of regulation process under ApDRC with enabled ζ^{op}.

B. Adaptive Damping Ratio Design

Since the duty cycles get the maximum in t_{n2}–t_{n3}, whether the overshoot will occur depends on the actual k_S^- of the next stages, as shown in Fig. 6. Unfortunately, it is impossible to precheck the k_S^- of t_{n3}–t_{n5} when the control is in t_{n2}–t_{n3}, as the input voltage and the load are uncertain and unpredictable.

Thanks to the energy balance indicated by W_S, further control improvement can be introduced accordingly. Still within Fig. 6, although the system is overdamped in t_{n2}–t_{n3}, the control is still so aggressive that accumulates too much energy in W_S. Here, a smaller W_S in t_{n2}–t_{n3} is more favorable to improving the voltage regulation while reducing the risk of overshoot. This smaller W_S can be achieved easily by increasing the damping ratio via w_{ic} in t_{n2}–t_{n3}. Therefore, we call this increasing damping ratio the overshoot-preventing damping ratio and denote it with ζ^{op}.

The process under the control with the overshoot-preventing damping ratio is illustrated by the red curves in Fig. 7, and the blue curves in the 1st and 2nd subplots remain the same as those plotted in Fig. 6. In t_{n2}–$t_{n2}^{'}$, despite the duty-cycle saturation, it does not need to enable the overshoot-preventing damping ratio since W_S can be decreased to zero in time. However, when the control enters into the stage of $t_{n2}^{'}$–t_{n4}, w_{ic} is first initialized as $w_{ic,0}$ due to duty-cycle saturation, then the overshoot-preventing damping ratio should be activated to eliminate the duty-cycle saturation effect. The resulting smaller W_S switches the system from underdamped to overdamped in t_{n3}–t_{n4}, thus preventing the occurrence of voltage overshoot. Finally, the desired damping ratio ζ^* takes over the selection of w_{ic} again after t_{n4}.

With the scheme of achieving an overshoot-preventing damping ratio being determined, the next step only needs to optimize W_S for the control. As the estimated values of the next control cycle can be obtained based on (1) and (2), the control is designed as one-step-forward to optimize $\tilde{W}_S(t_{n+1})$ based on the control inputs at t_n.

An initial maximum W_S at t_{n+1}, $\tilde{W}_S^{\max}(t_{n+1})$, is first estimated from the required energy of v_o recovering to its reference, which is defined as

$$\tilde{W}_S^{\max}(t_{n+1}) = \frac{1}{2}C\left[v_o^{\text{ref}\,2} - \tilde{v}_o(t_{n+1})^2\right]. \tag{24}$$

Taking the crucial role of k_S^+ and k_S^- on the change of W_S into account, then $\tilde{W}_S^{\max}(t_{n+1})$ is updated to the reference W_S^{ref}, which is shown in (25), to ensure W_S can be decreased to zero in time if needed

$$W_S^{\text{ref}} = \text{abs}\left(\frac{k_S^-}{k_S^+}\right)\tilde{W}_S^{\max}(t_{n+1}). \tag{25}$$

Defining the maximum and minimum of $\tilde{i}_{Li}(t_{n+1})$, $\tilde{i}_{Li}^{\max}(t_{n+1})$ and $\tilde{i}_{Li}^{\min}(t_{n+1})$, can be got by substituting $d_i(t_n) = 1$ and $d_i(t_n) = 0$ into (1). Substituting them into (2) yields the corresponding $\tilde{v}_o(t_{n+1})$ marked as $\tilde{v}_o^{\max}(t_{n+1})$ and $\tilde{v}_o^{\min}(t_{n+1})$. Then, k_S^+ and k_S^- are obtained as (26), shown at the bottom of this page.

According to (3), the initial estimated W_S at t_{n+1}, $\tilde{W}_S(t_{n+1})$, can be obtained as

$$\tilde{W}_S(t_{n+1}) = \frac{1}{2}\sum_{i=1}^{m} L_i\left\{\left[\tilde{i}_{Li}(t_{n+1})\right]^2 - \left[\frac{1}{m}i_o(t_n)\right]^2\right\} + \frac{1}{2}C\left[\tilde{v}_o(t_{n+1})^2 - v_o^{\text{ref}\,2}\right] \tag{27}$$

where the initial $\tilde{i}_{Li}(t_{n+1})$ and $\tilde{v}_o(t_{n+1})$ are obtained when w_{ic} is determined by duty-cycle saturation (i.e., $w_{ic} = w_{ic,0}$), which are

$$\begin{cases} \tilde{i}_{Li}(t_{n+1}) = \frac{1}{m}\left[\frac{v_o^{\text{ref}} - v_o(t_n)}{1+w_{ic,0}}\frac{C}{T_s} + i_o(t_n)\right] \\ \tilde{v}_o(t_{n+1}) = \frac{v_o^{\text{ref}} - v_o(t_n)}{1+w_{ic,0}} + v_o(t_n) \end{cases}. \tag{28}$$

The effect of duty-cycle saturation can be mitigated by updating $w_{ic,0}$ to a larger value $w_{ic,2}$ to switch $\tilde{W}_S(t_{n+1})$ to W_S^{ref}. Replacing $w_{ic,0}$ of (28) with $w_{ic,2}$ and updating $\tilde{W}_S(t_{n+1})$ of (27) with W_S^{ref}, $w_{ic,2}$ can be solved based on these two joint equations. A fast-solving process for obtaining $w_{ic,2}$ is provided as follows.

Solving Process: Solving $w_{ic,2}$ to Achieve the Overshoot-Preventing Damping Ratio ζ^{op}.

Inputs: $v_{in}(t_n)$, $v_o(t_n)$, $i_{Li}(t_n)$, $i_o(t_n)$
Output: $w_{ic,2}$

1: set $w_{ic,2} = w_{ic,0}$, $\Delta w_{ic} = 0.05$, $n = 1$
2: calculate $\tilde{i}_{Li}(t_{n+1})$ and $\tilde{v}_o(t_{n+1})$ of (28), $\tilde{W}_S(t_{n+1})$ of (27)
3: calculate k_S^+ and k_S^- of (26), W_S^{ref} of (25)
4: **while** $\tilde{W}_S(t_{n+1}) > W_S^{ref}$ **do**
5: update $w_{ic,2} = (1 + n\Delta w_{ic})w_{ic,2}$
6: $n = n + 1$
7: replace $w_{ic,0}$ with $w_{ic,2}$ in (28), calculate $\tilde{i}_{Li}(t_{n+1})$, $\tilde{v}_o(t_{n+1})$,$\tilde{W}_S(t_{n+1})$
8: **end while**
9: get the final $w_{ic,2}$
10: update w_{ic} in (15) with $w_{ic,2}$, getting the final $d_i(t_n)$.
11: apply w_{ic} into (20), getting the overshoot-preventing damping ratio

C. Decentralized ApDRC for Distributed Converters

In the implementation described above, the characteristic of PPLs being interfaced by parallel converters in a short distance in ship dc microgrids, enables the inductor currents and output currents to be sampled for each controller. However, to apply the proposed control for distributed converters, a decentralized method needs to be introduced into the control.

To achieve current sharing among the converters without the need for communication, the droop method is introduced into ApDRC, as it is commonly employed in decentralized controls. The steady-state value of v_o will stay around the new reference, $v_o{}^*$, rather than the original value, v_o^{ref}, due to the droop action. The droop method utilized in the control of the ith converter is expressed as

$$v_o^* = v_o^{\text{ref}} - r_{di}\cdot i_{oi} = v_o^{\text{ref}} - \frac{r_{di}}{R_{oi}}\cdot v_o \tag{29}$$

where r_{di} is the droop coefficient of the control for the ith buck converter.

In decentralized ApDRC, each converter is controlled locally. To update the control of the ith converter, substituting $m = 1$ and $i_o = i_{oi}$, and replacing v_o^{ref} with $v_o{}^*$ into (15), and (23)–(28), the duty cycle $d_i(t_n)$ can then be rewritten as

$$d_i(t_n) = \frac{L_i\left\{-i_{Li}(t_n) + \frac{v_o(t_n)T_s}{L_i} + i_{oi}(t_n) + \frac{v_o^* - v_o(t_n)}{1+w_{ic}}\frac{C_i}{T_s}\right\}}{v_{in}(t_n)T_s}. \tag{30}$$

Substituting the above-mentioned equation into (10) yields

$$\tilde{i}_{Li}(t_{n+1}) \approx i_L^{\text{ref}}(t_{n+1}) = \frac{v_o(t_n)}{R_{oi}} + \frac{v_o^* - v_o(t_n)}{1+w_{ic}}\frac{C_i}{T_s}. \tag{31}$$

$G_c(s)$ of the decentralized ApDRC, is updated by substituting (31) into (18), which is shown as

$$G_c(s) = \frac{v_o(s)}{v_o^{ref}(s)}$$

$$\begin{cases} k_S^+ = \frac{1}{2}\sum_{i=1}^{m} L_i\left[\tilde{i}_{Li}^{\max}(t_{n+1})^2 - i_{Li}(t_n)^2\right] + \frac{1}{2}C\left[\tilde{v}_o^{\max}(t_{n+1})^2 - v_o(t_n)^2\right] \\ k_S^- = \frac{1}{2}\sum_{i=1}^{m} L_i\left[\tilde{i}_{Li}^{\min}(t_{n+1})^2 - i_{Li}(t_n)^2\right] + \frac{1}{2}C\left[\tilde{v}_o^{\min}(t_{n+1})^2 - v_o(t_n)^2\right] \end{cases}. \tag{26}$$

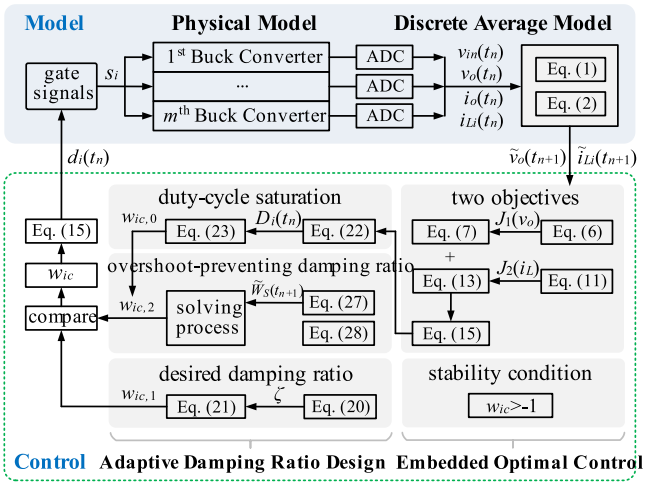

Fig. 8. Control implementation.

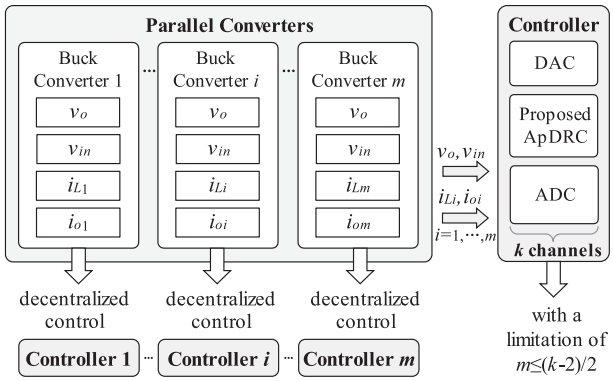

Fig. 9. Sampling information required for the controller(s).

$$= \frac{1}{1+\frac{r_{di}}{R_{oi}}} \frac{1}{(1+w_{ic})T_s{}^2 s^2+(1+w_{ic})\left(1+\frac{T_s}{C_i R_{oi}}\right)T_s s+1}. \quad (32)$$

$G_c(s)$ becomes a nonstandard second-order system with a correction factor of $1/(1+r_{di}/R_{oi})$. Fast voltage regulation can be achieved by changing the damping ratio to ζ^* via w_{ic}, while the steady-state v_o will stay around $v_o^{\text{ref}}/(1+r_{di}/R_{oi})$ finally.

D. Control Structure

The control implementation is illustrated in Fig. 8, where the duty cycles are solved by the embedded optimal control, and the selection of w_{ic} is determined by the adaptive damping ratio automatically. Then, substituting w_{ic} into (15) yields the optimal duty cycles to generate the gate signals for the converters, and thus the proposed control is achieved.

Fig. 9 provides clarification on the sampling information that is required for the controller(s). If the decentralized method is not enabled in ApDRC, all of the inductor currents and output currents must be sampled for each controller. In this scenario, the number of parallel buck converters, m, should be limited by $m \leq (k\text{-}2)/2$, where k is the total number of channels in the ADC module. In contrast, the limitation on the number of parallel buck converters will no longer be in force, if the decentralized ApDRC is enabled.

TABLE I
CONVERTER PARAMETERS

Description	Symbol	Value	Unit
Nominal input voltage	v_{in}	1500	V
Nominal output voltage	v_o^{ref}	710	V
Inductors	L_1 and L_2	3.95, 4.0	mH
Capacitors	C_1 and C_2	1050, 1000	μF
ESRs of the inductors	r_{L1} and r_{L2}	0.1, 0.01	Ω
ESRs of the capacitors	r_{C1} and r_{C2}	0.001, 0.002	Ω

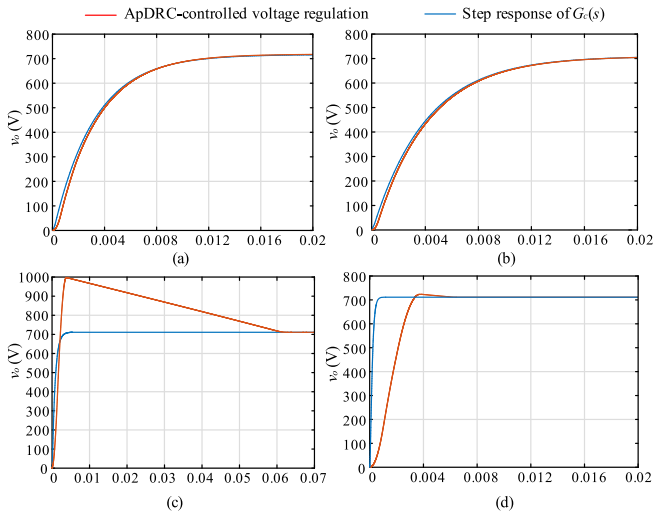

Fig. 10. Comparison between the voltage regulation under ApDRC and the step response of $G_c(s)$.

V. SIMULATION VERIFICATION

Simulations are conducted on the PPL supply structure, which consists of two parallel buck converters to validate the proposed ApDRC. The converter parameters are listed in Table I, and the control frequency is 20 kHz (i.e., $T_s = 50$ μs). The PPL is modeled as a constant power load (CPL) and a 200-Ω constant impedance load in parallel, whose pulses are achieved by stepping up/down the power P_d of the CPL.

A. Effect of Damping Ratio and Duty-Cycle Saturation on Voltage Regulation

Fig. 10 compares the voltage regulation performance under ApDRC with the step response of $G_c(s)$, where the parallel buck converters are in the startup with $P_d = 5$ kW. The four subplots are to illustrate how the damping ratio and duty-cycle saturation affect voltage regulation. The following are observed.

1) To ensure that the choice of w_{ic} is decided by the desired damping ratio, a large $\zeta^* = 4.0$ is taken to avoid the occurrence of duty-cycle saturation. The step response of $G_c(s)$ is obtained under the parameters: $\zeta^* = 4.0$, $\omega_n \approx 2.5\text{e}^3$ rad/s, and the input $v_o^{\text{ref}}(s) = v_o^{\text{ref}}/s$. As seen in Fig. 10(a), the voltage regulation under ApDRC is nearly identical to

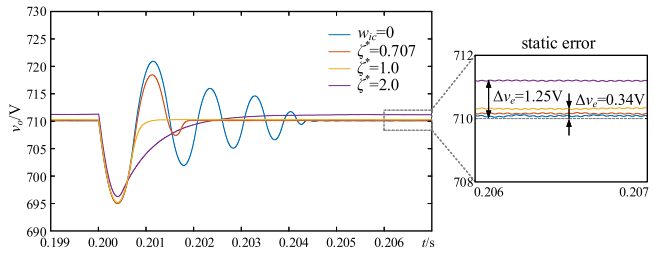

Fig. 11. Voltage regulation performance under ApDRC with different desired damping ratios.

the step response of $G_c(s)$, which verifies the correctness of $G_c(s)$.

2) Similarly, the voltage regulation under ApDRC with $\zeta^* = 4.5$, as illustrated in Fig. 10(b), agrees with the step response of $G_c(s)$ whose parameters are $\zeta = 4.5, \omega_n \approx 2.22e^3$ rad/s. It should be noted that the slight difference is mainly caused by the errors from the average model, the sampling delay, and the step delay of discrete-time simulation.
3) $\zeta^* = 2.0$ is employed to illustrate the impact of duty-cycle saturation on voltage regulation. As seen in Fig. 10(c), a voltage overshoot occurs as the choice of w_{ic} is decided by duty-cycle saturation rather than ζ^* during $0 \le t \le 0.05565$ s. It takes 0.06 s for v_o to recover to its reference, even longer than 0.016 s shown in Fig. 10(a).
4) The merit of the overshoot-preventing damping ratio in mitigating the effect of duty-cycle saturation is verified in Fig. 10(d). The voltage is effectively smoothed such that the settling time is shortened to 0.006 s, compared to the case shown in Fig. 10(c). By contrast, in the case of ApDRC with the same $\zeta^* = 1.0$ but disabling overshoot-preventing damping ratio, the voltage, and the inductor currents will rise to the maximums of 1287 V and 591 A, posing high current stress on the gate switches of the converters.

To validate the effect of the desired damping ratio ζ^* on voltage regulation, the case of load power stepping from 5 to 100 kW is taken to compare the performance difference caused by ζ^*. To avoid the interference of the overshoot-preventing damping ratio, it is disabled. As shown in Fig. 11, the voltage overshoot and oscillation can be greatly mitigated by adjusting the original damping ratio to the desired damping ratio. For example, the regulation time of v_o is about 4.8 ms when $w_{ic} = 0$, but it will be shortened to 1.2 ms if ζ^* is given as $\zeta^* = 1.0$. In addition, the static error of v_o, Δv_e, which is caused by the disturbances from the ESRs, the average model, and the sampling errors, can also be improved by ζ^*, as the open-loop gain of second-order systems equals to $\omega_n/2\zeta$. For example, Δv_e is up to 1.25 V when $\zeta^* = 2.0$, but it will reduce to 0.34 V if $\zeta^* = 1.0$ is taken. This will be further discussed in Section V-B through the Bode plots of the open-loop transfer function $G_o(s)$.

B. Response Performance Analysis

The open-loop transfer function of the voltage and its reference, $G_o(s)$, can be expressed as $G_o(s) = \omega_n^2 / s(s + 2\zeta\omega_n)$. The

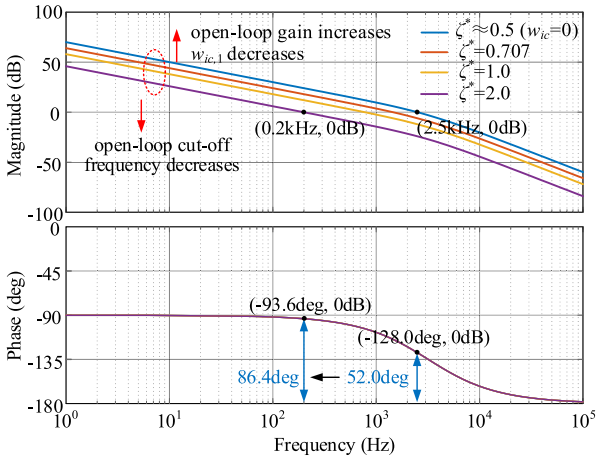

Fig. 12. Bode plot of $G_o(s)$ under various desired damping ratios.

Bode plots of $G_o(s)$ under different desired damping ratios are shown in Fig. 12, where ω_n is taken as $\omega_n = 1/(2\zeta T_s)$ due to $T_s/(CR_o) << 1$, thus there exists $\zeta^* \approx 0.5$ when $w_{ic} = 0$. The following can be seen.

1) For the steady-state response, the open-loop gain increases as the desired damping ratio decreases, making a decrease in the static error of v_o. The smaller the desired damping ratio is, the better steady-state response will be realized, which has been validated in Fig. 11.
2) For the transient response, the open-loop cut-off frequency reduces as the desired damping ratio ζ^* increases, improving the phase margin but degrading the fast response performance. The cutoff frequency decreases from 2.5 to 0.2 kHz when the desired damping ratio increases from $\zeta^* \approx 0.5$ to $\zeta^* = 2.0$, while the phase margin increases from 52.0° to 86.4°. On the other hand, for the underdamped system, fast dynamic response is always accompanied by voltage overshoot, which prolongs the settling time (see Fig. 10).
3) According to (21), $w_{ic,1}$ increases with the desired damping ratio, indicating that the larger ζ^* has a smaller probability of encountering duty-cycle saturation during load transients.

Given all of this, $\zeta^* = 1.0$ is preferable to obtain the small static error of v_o, fast voltage regulation, and small probability of encountering duty-cycle saturation.

VI. Experimental Results

Sections VI-A–E utilize a hardware-in-the-loop (HIL) system based on an RT-LAB real-time simulator and FPGA controller to validate the performance of the converters that supply high-power PPL. In Section VI-E, a laboratory-scale power platform is used to confirm the performance of the converters that supply low-power PPL, in which a simple STM32 hardware controller is employed.

In the HIL system depicted in Fig. 13, the switched model of parallel buck converters is established in the RT-LAB platform and controlled by FPGA Xilinx ZYNQ7020. In the controller,

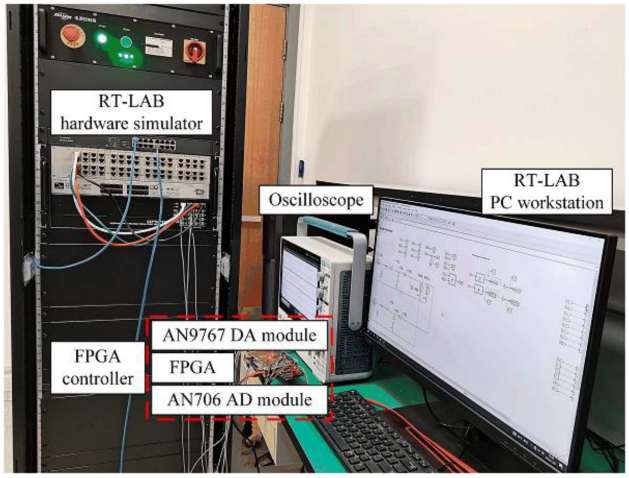

Fig. 13. HIL platform based on RT-LAB simulator and FPGA controller.

the inputs are sampled by the AN706 AD module with a 20 kHz sampling frequency. The average model shown in (1) and (2) is adopted for control design to output the optimal duty cycles d_i. These duty cycles then are converted to the gate signals $s_i$by the AN9767 DA module and sent back to the RT-LAB DI module. In addition, the converter parameters remain the same as those listed in Table I.

A. Voltage Regulation Performance During PPL Pulses

The PPL with the same power step as Fig. 11 is employed to further validate the proposed ApDRC and overshoot-preventing damping ratio. The only difference in the control between Figs. 11 and 14 is that the overshoot-preventing damping ratio is enabled here, thus, the effects of the desired damping ratio and the overshoot-preventing damping ratio on voltage regulation can be both examined. First, although the desired damping ratio is given as $\zeta^* = 0.707$, Fig. 14(a) shows that the voltage overshoot can be greatly mitigated by the overshoot-preventing damping ratio, as compared to Fig. 11. Despite there is a slight overshoot, the settling time t_s and the regulation time t_r have been improved to 1.293 ms and 1.626 ms, respectively. Next, keep increasing the desired damping ratio to $\zeta^* = 1.0$, it can be seen that the control performance can be further enhanced, achieving $t_s = 0.804$ ms, $t_r = 1.190$ ms, and fast voltage regulation without any overshoot, as illustrated in Fig. 14(b). Moreover, with ζ^* increasing to $\zeta^* = 2.0$, the voltage regulation performance starts to degrade due to the overdamped control, which makes t_s and t_r rise to 3.036 ms and 3.348 ms respectively, even longer than the case of Fig. 14(a). In addition, increasing ζ^* from 0.707 to 2.0 improves the disturbance rejection performance, as observed in the three subplots of Fig. 14, which is attributed to the reduction in the magnitude of $G_o(s)$ with the increase of ζ^*.

To illustrate how duty-cycle saturation affects load transients and the merit of the added overshoot-preventing damping ratio, another PPL case with a larger pulse is carried out, which steps up from 5 to 200 kW within a duration of 10 ms. For a clear

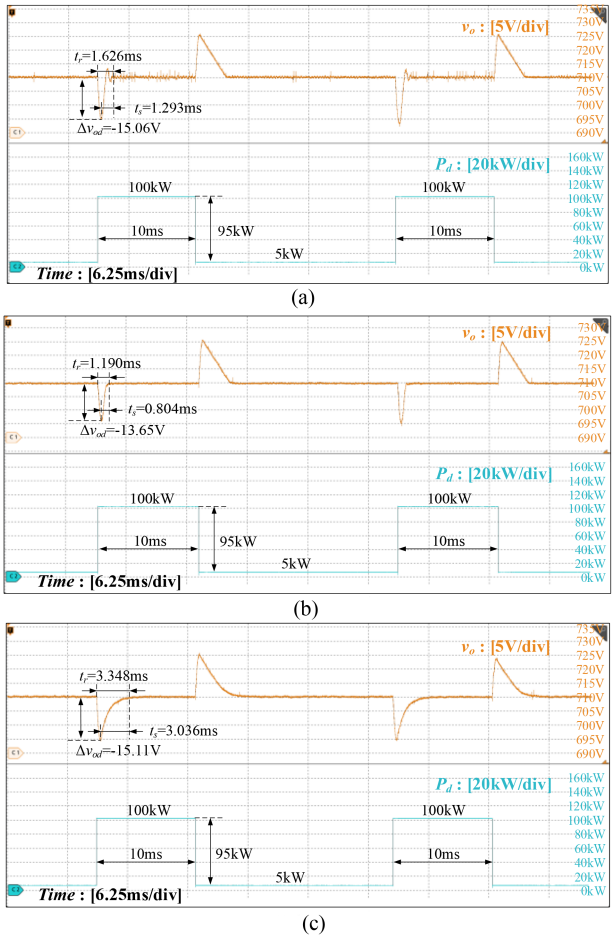

Fig. 14. Voltage regulation performance under ApDRC with various ζ^*. (a) ApDRC with $\zeta^* = 0.707$. (b) ApDRC with $\zeta^* = 1.0$. (c) ApDRC with $\zeta^* = 2.0$.

comparison, the overshoot-preventing damping ratio is disabled in Fig. 15(a), while it is enabled in Fig. 15(b). As w_{ic} is decided by duty-cycle saturation instead of the desired damping ratio ζ^* in some control cycles, an overshoot of 32.82 V occurs when the overshoot-preventing damping ratio is unactivated, although ζ^* has been given as $\zeta^* = 1.0$, as illustrated in Fig. 15(a). By contrast, the effect of duty-cycle saturation can be markedly eliminated by the overshoot-preventing damping ratio, which can lead to a reduction in t_s and t_r to 1.946 ms and 2.802 ms, respectively, as shown in Fig. 15(b).

B. Current Sharing Performance

Due to the differences in the circuit parameters and the ESRs, current sharing should be taken to reduce the output imbalance among the buck converters. As the current sharing performance is usually checked under various load powers, the case with P_d pulsing from 50 to 200 kW at an interval of 50 kW is taken for testing. As seen in Fig. 16, good current sharing performance is always achieved with the small mismatch in the steady states and fast response in the transients. At the beginning of the load steps, the transient portions of the inductor currents represented by the cyan circles in Fig. 16(b) provide additional energy to

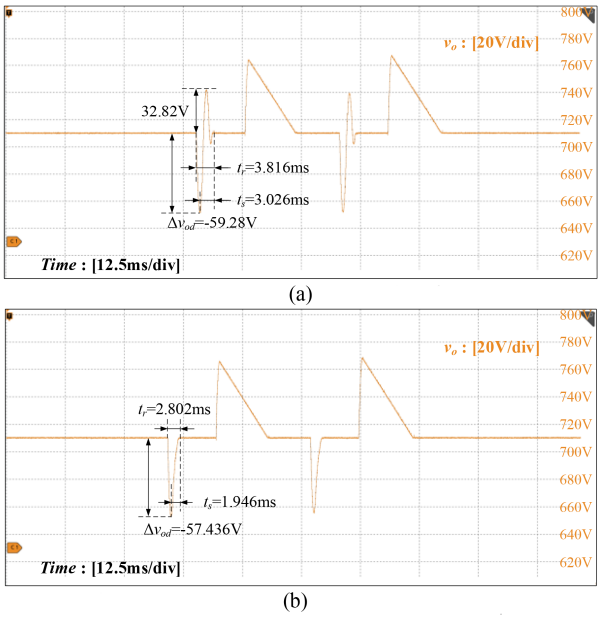

Fig. 15. Voltage regulation performance under ApDRC with $\zeta^* = 1.0$. (a) Without overshoot-preventing damping ratio. (b) With enabled overshoot-preventing damping ratio.

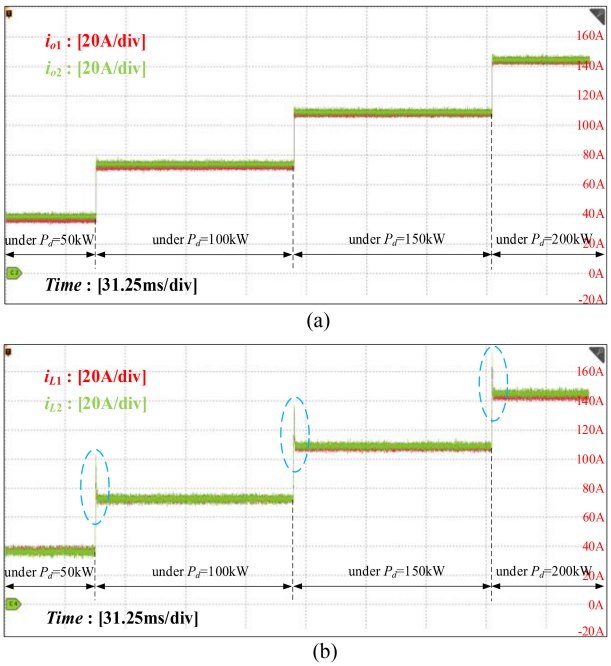

Fig. 16. Current sharing performance tested under various load powers. (a) Output currents. (b) Inductor currents.

enhance voltage regulation. With the voltage recovering to its reference, the inductor currents and the output currents quickly track to the new steady-state values in a short time. Therefore, besides fast voltage regulation, good current sharing can also be guaranteed under ApDRC.

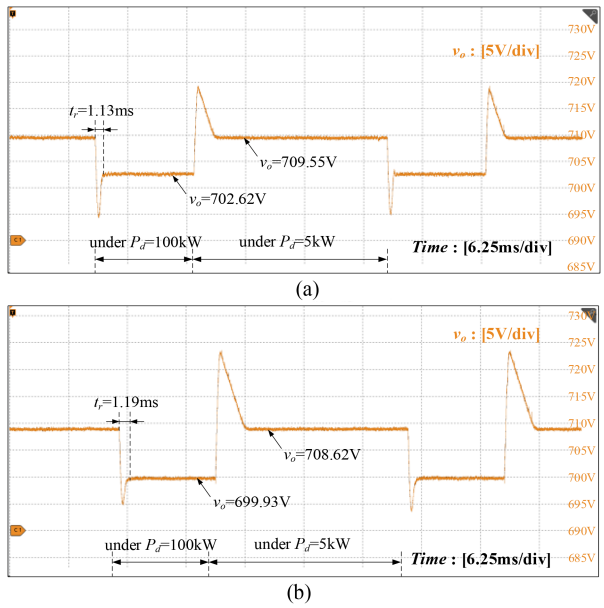

Fig. 17. Voltage regulation performance under decentralized ApDRC. (a) Under r_{d1}:r_{d2} = 1:1. (b) Under r_{d1}:r_{d2} = 1:2.

C. Control Performance of Decentralized ApDRC

In decentralized ApDRC, the voltage regulation performance is still tested under the case of P_d stepping from 5 to 100 kW. Fig. 17 provides the voltage regulation performance when using different drop coefficients, in which $r_{d1} = r_{d2} = 0.1$ is used in Fig. 17(a), while $r_{d1} = 0.1$ and $r_{d2} = 0.2$ are employed in Fig. 17(b). Compared to Fig. 14(b), the faster voltage regulation achieved in Fig. 17 comes at the expense of the steady-state v_o staying around 702.62 V instead of 710 V, despite having a t_r of 1.13 ms. Under the effect of drop action, current sharing performs well without the need for communication, as illustrated in Fig. 18(a). Moreover, as r_{d1}: r_{d2} = 1:2 is given in Fig. 17(b), the equivalent load resistances for the converters are calculated as $R_{o1} = 7.56\ \Omega$ and $R_{o2} = 15.12\ \Omega$. The steady-state voltage stays near 699.93 V, which is very close to its theoretical value of 700.73 V. Fig. 18(b) confirms the accuracy of the current sharing, as it demonstrates that the ratio of the output currents is 98.24:49.01, which agrees with r_{d2}:r_{d1} = 2:1.

D. Control Performance of Three Parallel Converters

To validate that the proposed ApDRC can be utilized in the structure with multiple converters, three parallel converters are taken for control performance test under the same PPL shown in Fig. 14. The experimental setup is depicted in Fig. 19, where the 1st and 2nd buck converters are controlled by FPGA Xilinx ZYNQ7020, and the 3rd converter is controlled by STM32F405. This is also done to validate the effectiveness of ApDRC under controllers with different performance levels. It is important to note that due to the simple sampling solution used in the STM32 controller, which is achieved through its general-purpose input/output port, an RC filter consisting of 100 Ω and 0.1 μF is added to suppress high-frequency noise.

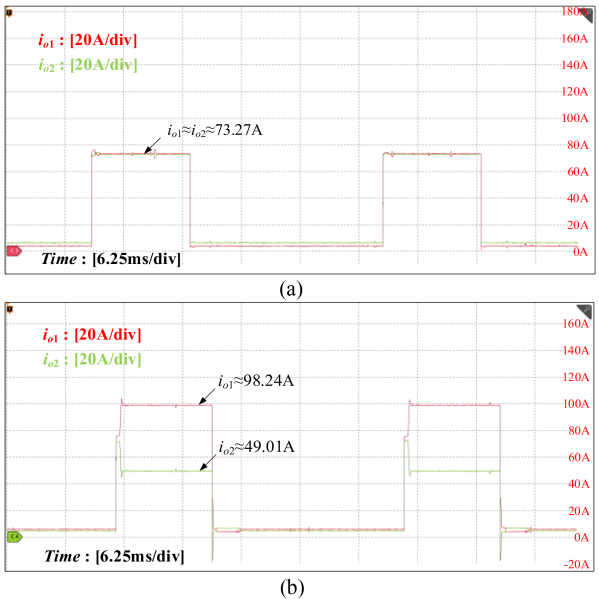

Fig. 18. Current sharing performance under decentralized ApDRC. (a) Under r_{d1}:r_{d2} = 1:1. (b) Under r_{d1}:r_{d2} = 1:2.

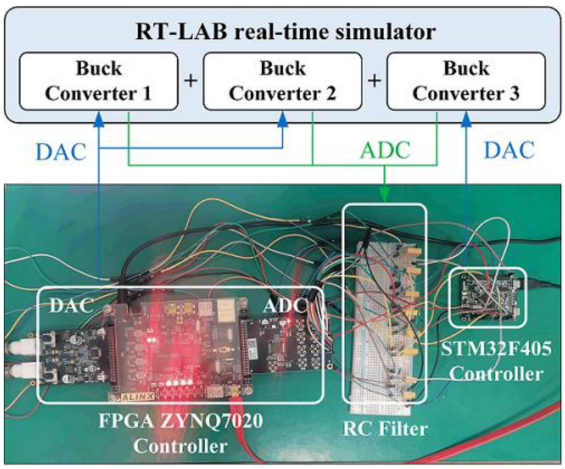

Fig. 19. Experimental setup of three parallel converters controlled by FPGA and STM32 controller.

Fig. 20 illustrates the voltage regulation performance when three converters are taken in parallel, with the load case being the same as that in Fig. 14. Compared to Fig. 14, faster voltage regulation with a smaller regulation time of 1.182 ms is obtained, and the voltage drop Δv_{od} can be significantly reduced to -8.13 V. As the 3rd converter increases the output capacitors, the power step can be buffered with a smaller voltage drop at the start of the load transients. Then, the inductor current of the converters starts to contribute to recovering the voltage by increasing itself, thus accelerating the voltage regulation.

E. Experiments in Laboratory-Scale Power Platform

A laboratory-scale power platform consisting of two parallel buck converters and a small-power PPL is established to verify

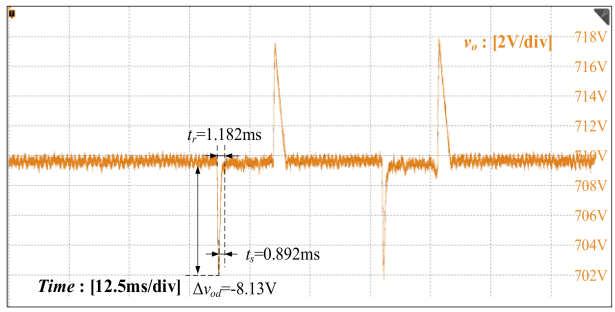

Fig. 20. Voltage regulation performance of three parallel converters.

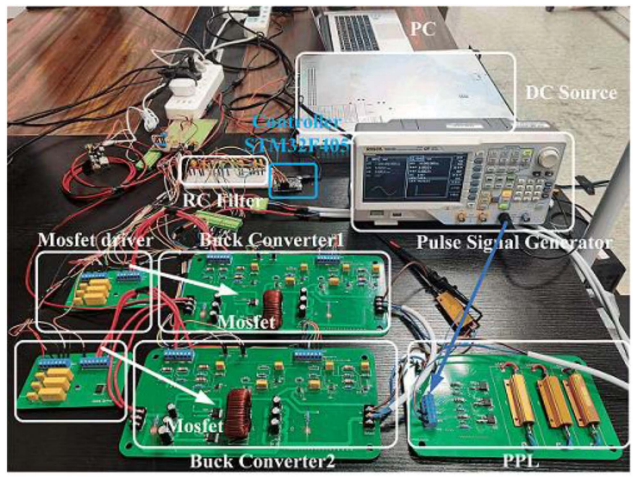

Fig. 21. Experimental setup of the laboratory-scale power platform.

TABLE II
CONVERTER AND CONTROL PARAMETERS

Description	Symbol	Value	Unit
Nominal input voltage	v_{in}^{ref}	60	V
Nominal output voltage	v_o^{ref}	30	V
Inductors	L_1 and L_2	2.0, 2.0	mH
Capacitors	C_1 and C_2	300, 300	μF
Control frequency	f_s	10	kHz
Sampling frequency	f_c	10	kHz

the control, as illustrated in Fig. 21. These two converters can provide the sampling of v_{in}, v_o, i_{Li}, and i_{oi}, and are controlled by STM32F405 controller. The PPL is simulated by changing the load resistances via the PWM signals to the MOSFETs, which is controlled by the pulse signal generator. The relevant converter parameters are listed in Table II.

Fig. 22 illustrates the performance of ApDRC when the PPL changes from 100 to 5 Ω repeatedly. It is seen that fast voltage regulation can be achieved without any overshoot, and it takes 1.509 ms to recover the voltage to its reference during transients. The output currents perform well in current sharing with a small imbalance, they quickly increase to the new steady-state value after the load power step, as shown in Fig. 22(b).

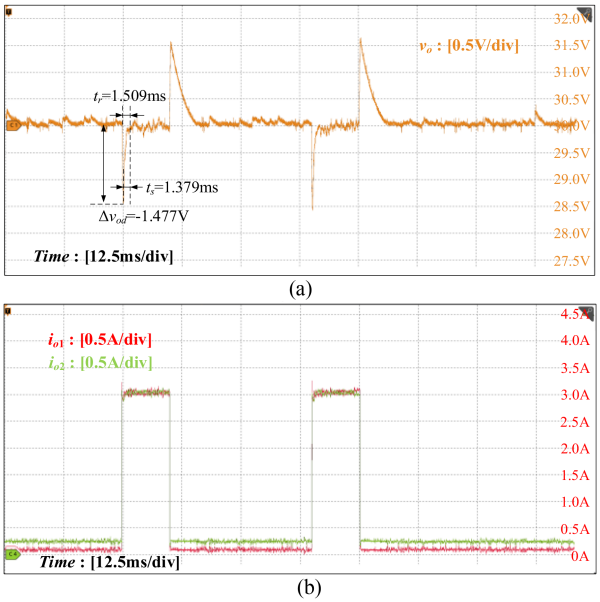

Fig. 22. Control performance under ApDRC. (a) Output voltage. (b) Output currents.

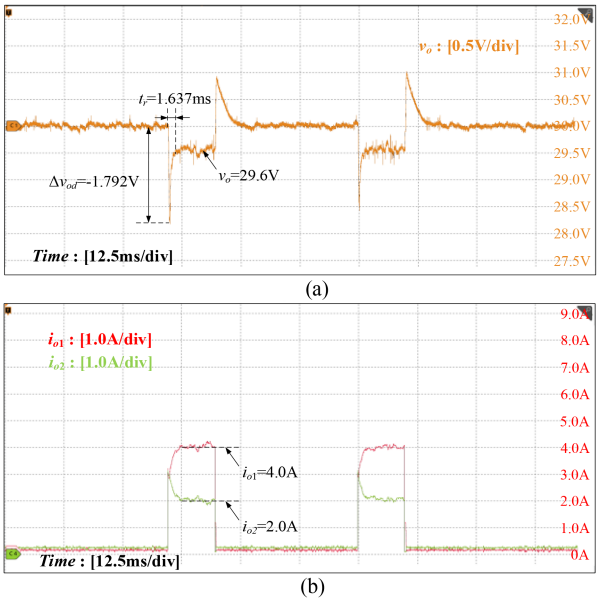

Fig. 23. Control performance under decentralized ApDRC. (a) Output voltage. (b) Output currents.

To verify the effectiveness of the decentralized ApDRC, the same load case used in Fig. 22 is employed in Fig. 23 for testing. The drop coefficients for the converters are given as $r_{d1} = 0.1$ and $r_{d2} = 0.2$, hence, the equivalent load resistances obtain $R_{o1} = 7.5\ \Omega$ and $R_{o1} = 15\ \Omega$ during $P_o = 5\ \Omega$. Fig. 23(a) shows that the voltage stays around 29.6 V when the load steps up from 100 to 5 Ω, which agrees with the theoretical value calculated in (32). In addition, the accuracy of the current sharing is confirmed in Fig. 23(b), as it demonstrates that the ratio of the output currents is 4.0:2.0, which agrees with r_{d2}:$r_{d1} = 2$:1.

VII. Conclusion

In this article, an ApDRC is proposed for the parallel buck converters with PPL, to obtain fast voltage regulation during load transient. The mechanism of fast voltage regulation is obtained by the SISO closed-loop transfer function of the output voltage and its reference, enabling the voltage to be regulated accurately by adjusting the original damping ratio to the desired damping ratio. Simulation results validate that the desired damping ratio $\zeta^* = 1$ is advantageous in achieving fast voltage regulation, good disturbance rejection, and small static error. Moreover, since the desired damping ratio cannot be fully guaranteed in all load transients due to duty-cycle saturation, the load transient evolution is investigated, revealing how duty-cycle saturation affects load transients and what the corresponding solution is. Then, the overshoot-preventing damping ratio is proposed to mitigate the effect of duty-cycle saturation. Experimental results indicate the voltage overshoot caused by duty-cycle saturation can be effectively smoothed. In summary, this control is parameter-independent under an adaptive damping ratio design, such that good voltage regulation performance can be always guaranteed regardless of varying changes in the load.

Appendix

A. Comparison With Other Controls

Dual-loop PI control is commonly utilized in industrial applications due to its advantages of ease of implementation and low complexity, which can be used to provide a benchmark for comparing control performance and complexity. Compared to dual-loop PI control, nonlinear controls are effective in addressing uncertain varying transients by utilizing a disturbance observer. Thus, the finite-time current sharing control (FTCSC) reported in [24] and the finite-terminal SMC (FTSMC) reported in [14], are used to demonstrate the performance under uncertain varying load transients.

To ensure a fair comparison, the official MATLAB particle swarm optimization (PSO) was used to optimize the controller parameters for the controls employed. This was done to provide optimal performance for control comparison, as the selection of controller parameters can affect control performance. However, the proposed ApDRC is parameter-independent, and therefore, no parameter tuning is required. In addition, all the controls employed were implemented in the RT-LAB platform, and their switching frequency and sampling frequency were both set to 20 kHz to match that of ApDRC.

1) PSO utilized for optimizing controller parameters

To achieve fast regulation in transients and small static error in steady states, both the voltage deviation during transients and steady states need to be accounted for in the fitness selection of PSO. During load transients, the output voltage may experience disturbances but will ultimately be regulated to its reference by the controller. Therefore, the sum of voltage deviation obtained in both transients and steady states is selected as the fitness of PSO, as illustrated in Fig. 24. The standardized fitness designed for PSO is given in (33), where t_0 and t_1 are the start and stop

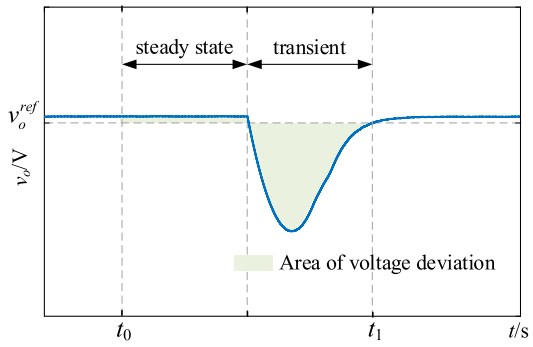

Fig. 24. Fitness selected for PSO to optimize voltage regulation.

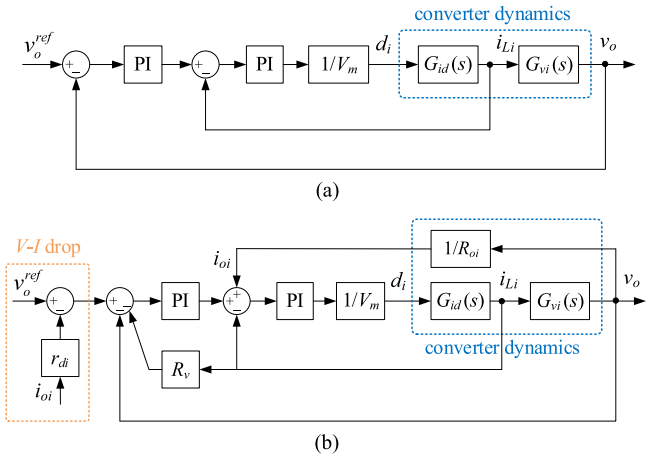

Fig. 25. Dual-loop PI controls for the ith buck converter. (a) Typical dual-loop PI control. (b) Improved dual-loop PI control.

times

$$\text{fitness} = \frac{1}{v_o^{\text{ref}}} \sum_{t=t_0}^{t=t_1} \left| v_o^{\text{ref}} - v_o \right| = \sum_{t=t_0}^{t=t_1} \left| 1 - \frac{v_o}{v_o^{\text{ref}}} \right|. \tag{33}$$

2) Description of the controls used for comparison

The typical dual-loop PI control shown in Fig. 25(a), is used for control complexity comparison, as it has the advantages of a simple structure and ease of design but is not effective in addressing varying load transients. On the other hand, the improved PI control shown in Fig. 25(b), has a load current feedforward in the inner loop and an inductor current feedback linearization in the outer loop. This enhances the performance in addressing load transients and achieves current sharing when the *V-I* drop method is enabled. Hence, the improved dual-loop PI control is employed for control performance comparison.

In Fig. 25, $G_{id}(s)$ and $G_{vi}(s)$ denote the s-domain small-signal transfer functions of i_{Li} to d_i and v_o to i_{Li}, respectively. The two PI regulators are expressed in (34), where k_{vp} and k_{vi} are the proportional and integral parameters of the voltage-loop PI regulator, and k_{ip} and k_{ii} are the proportional and integral parameters of the current-loop PI regulator. e_{pi}^u and e_{pi}^i are the inputs of the loops, u_{pi}^{out} and i_{pi}^{out} are the outputs of the loops, and $1/V_m$ is the linear gain of PWM [31], [32]. In addition, R_v is the feedback linearization coefficient in the outer voltage loop, and r_{di} is the drop coefficient of the ith buck converter

$$\begin{cases} u_{pi}^{\text{out}} = k_{vp} e_{pi}^u + k_{vi} \int e_{pi}^u dt \\ i_{pi}^{\text{out}} = k_{ip} e_{pi}^i + k_{ii} \int e_{pi}^i dt \end{cases}. \tag{34}$$

TABLE III
OPTIMAL CONTROLLER PARAMETERS

Controls	Structures	Controller parameters
improved dual-loop PI	Fig. 25(b)	k_{vp}=5.9389, k_{vi}=198.2978, k_{ip}=11.1765, k_{ii}=1.2863, R_v=0.0023 R_{oi}=0, V_m=100
FTCSC	Ref. [24]	a_1=1/2, a_2=2/3, K_1=88.0281, K_2=0.1855, K_3=0
FTSMC	Ref. [14]	c_1=13880.0, c_2=2355.8, α=11/23
ApDRC	Fig. 8	--

To achieve optimal voltage regulation performance, PSO is used to optimize the controller parameters for the dual-loop PI control and nonlinear controls. In the comparison experiments, the load transient case of P_d stepping from 5 to 100 kW was assumed to be known, allowing the corresponding optimal controller parameters to be obtained through PSO for each control. This was done to provide optimal performance for comparison. These fixed controller parameters were then applied to the load transient case of P_d stepping from 5 to 150 kW to evaluate their performance in handling uncertain varying load transients. The optimal controller parameters of the controls were obtained by utilizing PSO and are given in Table III.

3) Control performance comparison

Fig. 26 illustrates the voltage regulation performances under different controls. By utilizing PSO to optimize controller parameters, the transient response of the controls can be improved while maintaining a small static error in steady states. As shown in Fig. 26(a) and (b), the static error of the improved dual-loop PI control and FTCSC is almost optimized to close to 0. When attempting to improve the steady-state response of FTSMC, it may lead to a decline in transient response performance. Therefore, the controller parameters of FTSMC are optimized with an allowable static error of 1.5 V to emphasize the improvement in transient response.

As the load transient of P_d stepping from 5 to 100 kW was assumed to be known when finding the optimal controller parameters for the controls, good transient responses were obtained, leading to fast and smooth regulation in the improved dual-loop PI control and FTCSC. By applying these fixed controller parameters to address different transients, the ability of the controls to handle uncertain varying load transients can be evaluated. As observed in the second transient of P_d stepping from 5 to 150 kW, the transient response performances of the improved dual-loop PI control, FTCSC, and FTSMC, start to degrade and overshoot occurs as duty-cycle saturation is not accounted for.

For a clearer comparison, all the performance indices of the dual-loop PI control, FTCSC, FTSMC, and ApDRC are listed in Table IV, where the marked gray cells indicate the optimal

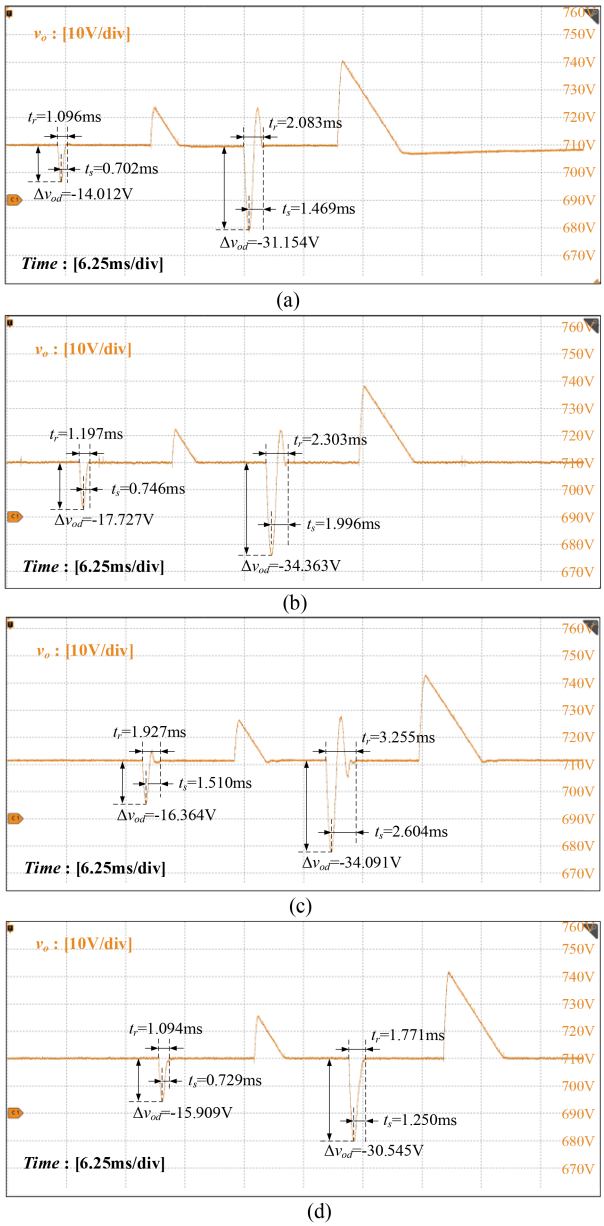

Fig. 26. Performance comparison of voltage regulation under various controls. (a) Under improved dual-loop PI control. (b) Under FTCSC. (c) Under FTSMC. (d) Under ApDRC.

indices. When compared to the controls with pretuned optimal controller parameters based on a known load transient, ApDRC can perform well, achieving near-optimal control performance. When applied to uncertain and varying load transients, ApDRC offers more advantages, ensuring fast and smooth regulation, as indicated in Fig. 26. This is due to the parameter-independent characteristic of ApDRC and its consideration of the duty-cycle saturation in control design, which enhances the performance robustness against varying disturbances in load.

Fig. 27 compares the current sharing under different controls. There is an obvious imbalance among the output currents under FTSMC, as current sharing is not included in the control. The small current imbalance seen in Fig. 27(a) results from the *V-I* drop method not being enabled to achieve accurate voltage regulation, which has no static error in Fig. 26(a). Compared to FTCSC, ApDRC performs better in disturbance rejection, achieving current sharing with small disturbances. This validates the effectiveness of ApDRC in achieving good current sharing.

TABLE IV
CONTROL PERFORMANCE COMPARISON

Varying transients	Controls	Performance indices					
		t_s/ms	t_r/ms	Δv_{od}/V	Δv_e /V	current sharing	parameter independent
5-100 kW	improved dual-loop PI	0.702	1.096	-14.012	0.02	×	×
	FTCSC	0.746	1.197	-17.727	0.02	√	×
	FTSMC	1.510	1.927	-16.364	1.52	×	×
	ApDRC	0.729	1.094	-15.909	0.42	√	√
5-150 kW	improved dual-loop PI	1.469	2.083	-31.154	0.02	×	×
	FTCSC	1.996	2.303	-34.363	0.02	√	×
	FTSMC	2.604	3.255	-34.091	1.52	×	×
	ApDRC	1.250	1.771	-30.545	0.42	√	√

4) Discussion on control complexity

To provide a complete assessment, the control complexity of ApDRC is also discussed by analyzing the number of numerical computations required in the detailed equations. As dual-loop PI controls are commonly employed in industrial applications, they are used as a benchmark to evaluate the increase in control complexity of ApDRC.

Before evaluating the control complexity of the dual-loop PI controls depicted in Fig. 25, the expression of the voltage-loop and current-loop PI regulators, (34), is transformed into discrete forms as (35) and (36)

$$\begin{cases} \Delta u_{pi}^{\text{out}}(t_n) = k_{vp}\left[e_{pi}^{u}(t_n) - e_{pi}^{u}(t_{n-1})\right] + k_{vi}e_{pi}^{u}(t_n) \\ u_{pi}^{\text{out}}(t_n) = \Delta u_{pi}^{\text{out}}(t_n) + u_{pi}^{\text{out}}(t_{n-1}) \end{cases} \tag{35}$$

$$\begin{cases} \Delta i_{pi}^{\text{out}}(t_n) = k_{ip}\left[e_{pi}^{i}(t_n) - e_{pi}^{i}(t_{n-1})\right] + k_{ii}e_{pi}^{i}(t_n) \\ i_{pi}^{\text{out}}(t_n) = \Delta i_{pi}^{\text{out}}(t_n) + i_{pi}^{\text{out}}(t_{n-1}) \end{cases}. \tag{36}$$

According to the structure shown in Fig. 25(a), in the typical dual-loop PI control, the inputs of the voltage-loop and current-loop PI regulators, and the duty cycle, can be expressed as (37) and (38)

$$\begin{cases} e_{pi}^{u}(t_n) = v_o^{\text{ref}} - v_o(t_n) \\ e_{pi}^{i}(t_n) = u_{pi}^{\text{out}}(t_n) - i_{Li}(t_n) \end{cases} \tag{37}$$

$$d_i(t_n) = \frac{i_{pi}^{\text{out}}(t_n)}{V_m}. \tag{38}$$

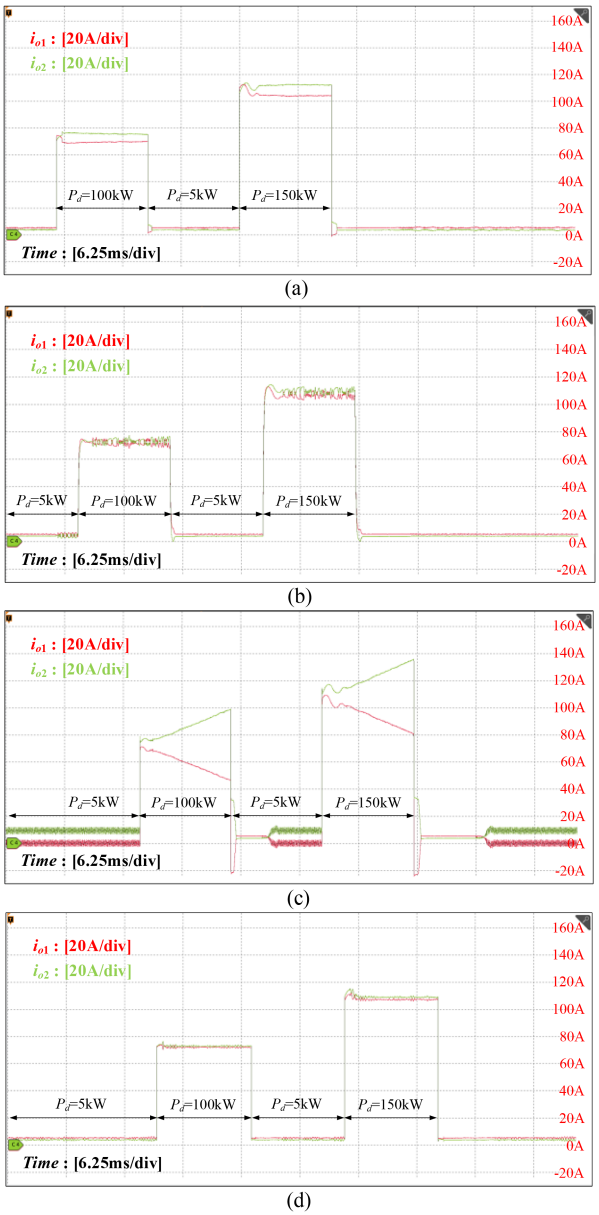

Fig. 27. Performance comparison of current sharing under various controls. (a) Under improved dual-loop PI control. (b) Under FTCSC. (c) Under FTSMC. (d) Under ApDRC.

Similarly, as indicated in Fig. 25(b), the inputs of the voltage-loop and current-loop PI regulators, and the duty cycle in the improved PI control, can be expressed as (39) and (40)

$$\begin{cases} e_{pi}^{u}(t_n) = v_o^{\text{ref}} - r_{di} i_{oi}(t_n) - v_o(t_n) - R_v i_{Li}(t_n) \\ e_{pi}^{i}(t_n) = u_{pi}^{\text{out}}(t_n) + i_{oi}(t_n) - i_{Li}(t_n) \end{cases} \tag{39}$$

$$d_i(t_n) = \frac{i_{pi}^{\text{out}}(t_n)}{V_m}. \tag{40}$$

The control complexity of each control can be assessed based on the number of numerical computations required in detailed equations. The proposed ApDRC can be divided into two parts: the basic part to get the desired damping ratio ζ^*, and the additional part to obtain the overshoot-preventing damping ratio ζ^{op}.

TABLE V
NUMBER OF NUMERICAL CALCULATIONS REQUIRED

Controls	Equations	Number of numerical computations		Details
		multiplication and division	addition and subtraction	
typical dual-loop PI	(35)-(38)	4	8	--
improved dual-loop PI	(35)-(36), (39)-(40)	7	11	--
ApDRC	(21)-(23), (15), sum of C_i sum of i_{oi}	17	2m+17	obtain ζ^* (Basic)
	(25)-(28)	22	13	obtain ζ^{op} (Additional)

The role of the basic part of ApDRC is similar to that of the two dual-loop PI controls, which is to calculate the duty cycle without taking the duty-cycle saturation into account. The additional part of ApDRC is designed to mitigate the impact of duty-cycle saturation on control performance.

In the control of the ith buck converters, the number of numerical computations required in the detailed equations is roughly counted in Table V, where the same terms in the equations are all saved as temporary variables to avoid duplicate calculations, such as the terms of $[v_o^{\text{ref}} - v_o(t_n)]C/mT_{\text{s}}$, $v_{in}(t_n)]T_{\text{s}}/L_i$, and $i_{Li}(\text{t}_{\text{n}}) - i_o(t_n) + v_o(t_n)T_{\text{s}}/L_i$, in the equations of ApDRC.

Taking two parallel buck converters as an example, the basic part of ApDRC requires about 10 times more multiplication/division operations and 10 times more addition/subtraction operations than the improved dual-loop PI controls. The additional part of ApDRC, which is to mitigate the impact of duty-cycle saturation, requires 22 times more multiplication/division operations and 13 times more addition/subtraction operations in each cycle.

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