A Self-Tuned Class-E/F_3 Power Oscillator

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***Abstract*—Class-E/F_3 power amplifier (PA) is a hybrid switching PA that enhances the performance of Class-E PA by reducing its peak switch voltage. The output power and the efficiency of a Class-E/F_3 PA are sensitive to the values of the load network components. To minimize this issue, we propose a Class-E/F_3 power oscillator (PO) whose feedback network is composed of a low-Q *RC* circuit. In the proposed circuit, the switching frequency of the PO is defined by the resonance frequencies of the load network, and as such, the PO remains fairly tuned, even if the load network components vary considerably. As a result, the output power and the efficiency of the proposed PO show negligible sensitivities to the changes in the component values. Additionally, we present a design procedure for the proposed PO. To verify the circuit operation and the design procedure, a prototype circuit was designed and implemented. At $V_{DD} = 4.5$ V, the measured output power, the efficiency, and the switching frequency of the prototype PO are 1.023 W, 93.5%, and 800 kHz, respectively. Simulation and measurement results confirm that the output power and the efficiency of the proposed PO have negligible sensitivities to the variations in the component values.**

***Index Terms*—Class-E power amplifier (PA), class-E/F_3 power amplifier, feedback network, harmonic filter, power oscillator (PO), switching power amplifier.**

I. Introduction

CLASS-E power amplifier (PA) has high power conversion efficiency, and therefore, is extensively used in power applications [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. The efficiency of a Class-E PA approaches 100% if its switch voltage satisfies zero-voltage switching (ZVS) and zero-voltage derivative switching (ZVDS) conditions [6]. Unfortunately, the output power and the efficiency of this type of PA are sensitive to the component values. Moreover, Class-E PA has large peak switch voltage [13], [14], [15], [16].

The peak switch of a Class-E PA with a duty cycle of 50% is 3.56 × V_{DD}. This voltage stress is larger than that of Class-D and Class-F switching PAs [2], [6]. To reduce the peak switch voltage, a series resonant filter tuned to the third harmonic of the switching frequency f_s is added across the switch of a Class-E PA. The resulting PA, as shown in Fig. 1, is called a Class-E/F_3 PA [17], [18], [19], [20], [21], [22], [23], [24]. The series resonant filter, consisting of C_3 and L_3 suppresses the third harmonic of the switch voltage and reduces the peak switch voltage by about 12%.

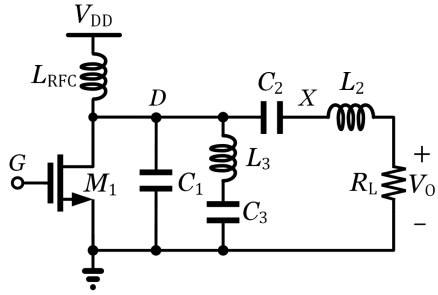

Fig. 1. Circuit schematic of a Class-E/F_3 PA.

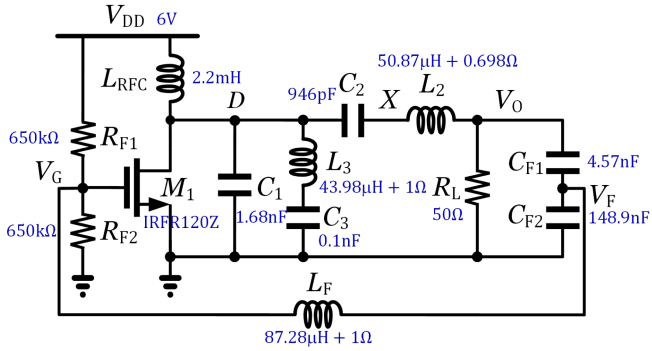

Fig. 2. Circuit schematic of the simulated Class-E/F_3 PO presented in [23].

Similar to a Class-E PA, the output power and the efficiency of a Class-E/F_3 PA are very sensitive to the values of C_2 and L_2. This sensitivity is due to the fact that the load network of a Class-E/F_3 PA is a resonant circuit and only at a certain frequency, the PA satisfies ZVS and ZVDS conditions. The switching frequency of the PA should be equal to that certain frequency in order for the PA to remain tuned and provide large efficiency. If the values of the load network components change, the circuit becomes untuned and the output power and the efficiency substantially change. To overcome this issue, one can take advantage of the feedback theory and convert a Class-E/F_3 PA to a Class-E/F_3 power oscillator (PO), in which the switching frequency is defined by the resonance frequencies of the load network.

The schematic of the existing Class-E/F_3 PO proposed in [23] is depicted in Fig. 2. The feedback network of this circuit consists of L_F, C_{F1}, C_{F2}, and the gate capacitance C_g of M_1. Unfortunately, the feedback network of this circuit is a resonant circuit. The resonance frequencies of the load network and the resonance frequency of the feedback network do not necessarily track each

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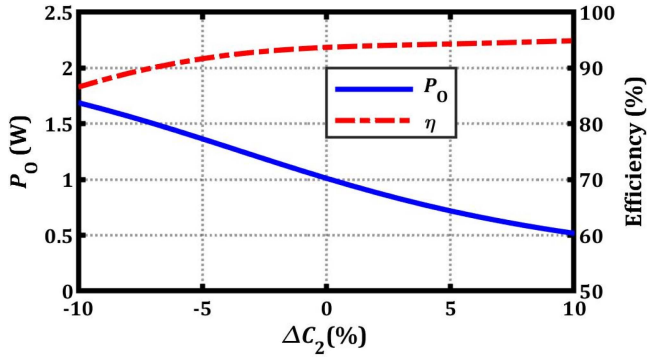

Fig. 3. P_o and η curves of the simulated Class-E/F$_3$ PO presented in [23].

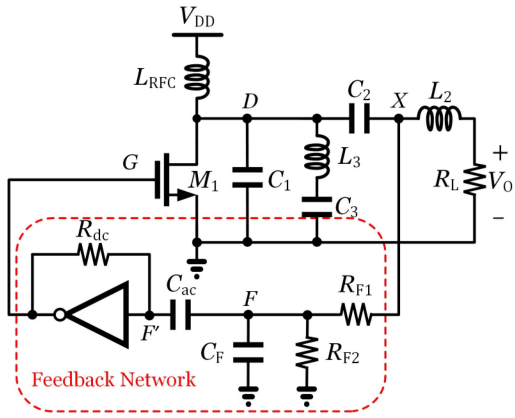

Fig. 4. Circuit schematic of the proposed Class-E/F$_3$ PO.

other and they can move in the opposite directions depending on the changes in the component values. Consequently, the output power and the efficiency of the circuit shown in Fig. 2 are still very sensitive to the values of C_2 and L_2. To demonstrate this issue, we simulated the circuit proposed in [23] and plotted the efficiency and the output power versus the changes in C_2 in Fig. 3. It can be observed that, for example, if C_2 decreases by 10%, $P_{\rm O}$ increases by 67.1%, and η decreases by 7.1%.

To improve the robustness of a Class-E/F$_3$ PO, in this article, we propose a Class-E/F$_3$ PO whose feedback network is a low-Q *RC* circuit. The proposed feedback network is not a resonant circuit and provides a fairly constant phase shift in the vicinity of the switching frequency. Moreover, we present a simple and straightforward design procedure for the proposed circuit. Finally, we provide the simulation and the experimental results of an implemented Class-E/F$_3$ PO to validate the circuit operation and the design procedure.

II. Fundamentals of a Class-E/F$_3$ Power Amplifier

A Class-E/F$_3$ PA, as shown in Fig. 1, consists of an RF choke $L_{\rm RFC}$, a transistor M_1, a load network, and a load resistor $R_{\rm L}$. $L_{\rm RFC}$ has a high impedance at $f_{\rm s}$ so that it behaves like an ideal current source. M_1 operates as an ideal switch. An external clock signal periodically turns M_1 ON and OFF at $f_{\rm s}$. The load network is composed of a shunt capacitor C_1, a series resonant branch consisting of C_2 and L_2, and a harmonic filter $C_3 - L_3$. The $C_2 - L_2$ branch filters out the dc and the harmonics of the drain voltage $V_{\rm D}$ of M_1 and delivers a near sinusoidal waveform to $R_{\rm L}$. The harmonic filter is tuned to $3 \times f_{\rm s}$, and suppresses the third harmonic of $V_{\rm D}$.

If the $C_3 - L_3$ branch is not designed properly, the performance of the Class E/F$_3$ PA would be very sensitive to the values of C_3 and L_3. It has been shown in [25] that the ratio of C_1 over C_3, denoted by $r_{\rm C}$, should be in the range of $[1.5, 2.5]$, to have a robust PA against the typical variations in C_3 and L_3. In that case, the values of the circuit components can be calculated using

$$R_{\rm L} = \left(\frac{0.66\, r_{\rm C} - 0.239}{r_{\rm C} + 0.624}\right) \frac{V_{\rm DD}^2}{P_{\rm O}}, \tag{1}$$

$$C_1 = \frac{0.21\, r_{\rm C} - 0.076}{(r_{\rm C} + \ 0.624)\, \omega_{\rm s} R_{\rm L}}, \tag{2}$$

$$L_2 = \frac{Q_{\rm L} R_{\rm L}}{\omega_{\rm s}}, \tag{3}$$

$$C_2 = \frac{(\omega_{\rm s} R_{\rm L})^{-1}}{\left(Q_{\rm L} - \frac{0.962\ r_{\rm C} + 0.855}{r_{\rm C} - 0.083}\right)}, \tag{4}$$

$$C_3 = \frac{C_1}{r_{\rm C}}, \tag{5}$$

$$L_3 = \frac{r_{\rm C}}{9\ C_1 {\omega_{\rm s}}^2}, \tag{6}$$

where $P_{\rm O}$ is the output power, $V_{\rm DD}$ is the supply voltage, $Q_{\rm L}$ is the load quality factor, and $\omega_{\rm s} = \ 2\pi f_s$ is the operating frequency in terms of rad/s [25]. Equations (1)–(6) are with the assumptions that:

1) The quality factor $Q_{\rm L}$ of the $C_2 - L_2 - R_{\rm L}$ branch is selected high enough so that the current through this branch $i_{\rm O}$ can be approximated as

$$i_{\rm O}(\omega_{\rm s} t) = I_{\rm O} \sin(\omega_{\rm s} t + \varphi)\,, \tag{7}$$

where $I_{\rm O}$ is the amplitude and φ is the initial phase of $i_{\rm O}$. In (7), it is assumed that the phase of the gate voltage $V_{\rm G}$ is zero.

2) The inductance of $L_{\rm RFC}$ is sufficiently large so that its current ripple can be neglected.
3) All the circuit components are ideal.
4) $V_{\rm G}$ is a square waveform with a duty cycle D of 50%.

III. Proposed Class-E/F$_3$ Power Oscillator

The schematic of our proposed Class-E/F$_3$ PO is shown in Fig. 4. The feedback network of this PO consists of a low-pass *RC* filter and an inverting gate driver. The resonance node in the load network of the PO provides the input signal of the feedback network. The *RC* filter, consisting of $R_{\rm F1}$, $R_{\rm F2}$, and $C_{\rm F}$, attenuates the input signal and shifts its phase and then applies it to the gate driver.

In a Class-E/F$_3$ PA, the phase shift from the fundamental component of the gate voltage waveform to that of the drain voltage waveform can be calculated using

$$\varphi_{\rm GD} = \ \varphi + \psi, \tag{8}$$

where ψ is the phase of the $C_2 - L_2 - R_{\rm L}$ impedance and can be calculated using [6]

$$\psi = \tan^{-1}\left(\frac{L_2\omega_{\rm s} - (C_2\omega_{\rm s})^{-1}}{R_{\rm L}}\right). \tag{9}$$

By substituting L_2 and C_2 from (3) and (4), in (9), we obtain

$$\psi = \tan^{-1}\left(\frac{0.962\, r_{\rm C} + 0.855}{r_{\rm C} - 0.083}\right). \tag{10}$$

By solving the circuit equations of a Class-E/F$_3$ PA, and also by running numerous circuit simulations, we have observed that $\varphi_{\rm GD}$ is fairly insensitive to $r_{\rm C}$ and is approximately $-170°$. The small variations in $\varphi_{\rm GD}$ due to different $r_{\rm C}$ values can be later compensated by fine-tuning the circuit.

The voltage transfer function from node *D* to node *X* in Fig. 1 is obtained as

$$\frac{V_{\rm X}}{V_{\rm D}}({\rm s}) = \frac{L_2{\rm s} + R_{\rm L}}{L_2{\rm s} + R_{\rm L} + (C_2{\rm s})^{-1}}. \tag{11}$$

Substituting $j\omega$ for s in (11), we obtain the phase shift from node *D* to node *X* at $\omega_{\rm s}$ as

$$\begin{aligned}\varphi_{\rm DX} &= \measuredangle\frac{V_{\rm X}}{V_{\rm D}}(j\omega_{\rm s}) \\ &= \tan^{-1}\left(\frac{L_2\omega_{\rm s}}{R_{\rm L}}\right) - \tan^{-1}\left(\frac{L_2\omega_{\rm s}}{R_{\rm L}} - \frac{1}{R_{\rm L}C_2\omega_{\rm s}}\right).\end{aligned} \tag{12}$$

Substituting L_2 and C_2 from (3) and (4) in (12), we arrive to

$$\varphi_{\rm DX} = \tan^{-1}(Q_{\rm L}) - \tan^{-1}\left(\frac{0.962\, r_{\rm C} + 0.855}{r_{\rm C} - 0.083}\right). \tag{13}$$

According to the *Barkhausen criteria,* the phase shift in the entire loop of the PO should be $-360°$. The phase shift from node *G* to node *X* or $\varphi_{\rm GX}$ equals to $\varphi_{\rm GD} + \varphi_{\rm DX}$. Therefore, the phase shift that the feedback network has to provide, denoted by $\varphi_{\rm F}$, is obtained by

$$\varphi_{\rm F} = -360° - \varphi_{\rm GD} - \varphi_{\rm DX} = -190° - \varphi_{\rm DX}. \tag{14}$$

The first assumption in Section II implies that the first term in the right side of (13) is nearly 90°; therefore, if $r_{\rm C}$ is chosen to be in the range of 1.5 to 2.5, $\varphi_{\rm GX}$ would be in the range of $-138.3°$ to $-133.5°$ and the phase shift that the feedback network should provide would be in the range of $-226.5°$ to $-221.7°$. This amount of phase shift can be achieved by cascading a first order *RC* filter and a digital inverter. The inverter can provide a phase shift larger than $-180°$; therefore, the *RC* filter should provide a phase shift between $-46.5°$ to $-41.7°$. This amount of phase shift can be easily provided by an *RC* circuit consisting of $R_{\rm F1}$ and $C_{\rm F}$ shown in Fig. 4, but because the amplitude of the signal at node *X* is usually very large, we have added $R_{\rm F2}$ to adjust the attenuation of the signal before being applied to the inverter.

The gate driver circuit consists of an inverter, a resistor $R_{\rm dc}$, and a capacitor $C_{\rm ac}$. $R_{\rm dc}$ has a large resistance and connects the output of the inverter to its input. It adjusts the dc bias voltage of the input and output nodes of the inverter equal to the switching threshold voltage $V_{\rm th,INV}$ of the inverter. $C_{\rm ac}$ is an ac-coupling capacitor, which decouples the dc voltage of node F from that of node F'. When $Q_{\rm L}$ is sufficiently large, the voltage waveform at node F' is nearly sinusoidal with a dc value of $V_{\rm th,INV}$. This results in the duty cycle of $V_{\rm G}$ to be approximately 50%. Furthermore, the inverter is biased in its high-gain region and as such, the feedback loop of the PO has a large gain at the switching frequency. As a result, the PO is self-starting and does not need a start-up circuit [13].

IV. Design Procedure of the Feedback Network

Here, we explain the design procedure for the *RC* circuit of the feedback network, assuming that it should provide a phase shift of $\varphi_{\rm RC}$ and an attenuation of α at $\omega_{\rm s}$. Since the inverter provides a phase shift of $-180°$, $\varphi_{\rm RC}$ is calculated as follows:

$$\varphi_{\rm RC} = \varphi_{\rm F} + 180° = -10° - \varphi_{\rm DX}. \tag{15}$$

In Fig. 4, the voltage transfer function from node *X* to node *F* is given by

$$\frac{V_{\rm F}}{V_{\rm X}}({\rm s}) = \frac{R_{\rm F2}}{R_{\rm F1} + R_{\rm F2} + R_{\rm F1}R_{\rm F2}C_{\rm F}{\rm s}}. \tag{16}$$

According to (16), the phase shift from node *X* to node *F*, defined by $\varphi_{\rm XF}$, at $s = j\omega$ is obtained as

$$\varphi_{\rm XF} = \measuredangle\frac{V_{\rm F}}{V_{\rm X}}(j\omega) = -\tan^{-1}((R_{\rm F1}||R_{\rm F2})\, C_{\rm F}\omega). \tag{17}$$

$\varphi_{\rm XF}$, at $\omega_{\rm s}$, is equal to $\varphi_{\rm RC}$. α, which is the magnitude of (16) at $\omega_{\rm s}$, can be calculated by

$$\alpha = \left|\frac{V_{\rm F}}{V_{\rm X}}(j\omega_{\rm s})\right| = \frac{R_{\rm F2}}{R_{\rm F1} + R_{\rm F2}}\cos\varphi_{\rm XF}. \tag{18}$$

To choose an appropriate value for α, we should calculate the amplitude of the signal at node *X*, and also choose an appropriate amplitude for the signal driving the gate driver. The voltage waveform at node *X* is

$$V_{\rm X}(\omega_{\rm s}t) = R_{\rm L}I_{\rm O}\sin(\omega_{\rm s}t + \varphi) + L_2I_{\rm O}\omega_{\rm s}\cos(\omega_{\rm s}t + \varphi). \tag{19}$$

Therefore, the peak of $V_{\rm X}$ is obtained using

$$|V_{\rm X}(j\omega_{\rm s})| = I_{\rm O}\sqrt{\omega_{\rm s}^2L_2^2 + R_{\rm L}^2}. \tag{20}$$

Substituting (3) in (20), we arrive to

$$|V_{\rm X}(j\omega_{\rm s})| = I_{\rm O}\, R_{\rm L}\sqrt{Q_{\rm L}^2 + 1}. \tag{21}$$

In a tuned Class-E/F$_3$ PA, the efficiency η is nearly 100%; thus, the output power $P_{\rm O} = I_{\rm O}^2R_{\rm L}/2$ equals to the input power $P_{\rm in} = I_{\rm DD}V_{\rm DD}$. Therefore, we can substitute $I_{\rm O}R_{\rm L}$ with $2V_{\rm DD}(I_{\rm DD}/I_{\rm O})$ in (21), which results in

$$|V_{\rm X}(j\omega_{\rm s})| = \frac{2V_{\rm DD}I_{\rm DD}}{I_{\rm O}}\sqrt{Q_{\rm L}^2 + 1}. \tag{22}$$

It is mentioned in [25] that if $r_{\rm C}$ is in the range of [1.5,10], the value of $I_{\rm DD}/I_{\rm O}$ can be obtained using

$$\frac{I_{\rm DD}}{I_{\rm O}} = \frac{0.574\, r_{\rm C} - 0.1}{r_{\rm C} + 0.31}. \tag{23}$$

Substituting (23) in (22), we obtain the amplitude of V_X as

$$|V_X(j\omega_s)| = \frac{1.148\, r_C - 0.2}{r_C + 0.31}\, V_{DD}\sqrt{Q_L^2 + 1}\,. \quad (24)$$

The values of Q_L and V_{DD} are known for each design. We should choose a proper value for r_C and then calculate V_X using (24).

It is mentioned in [25] that when r_C is chosen between $[1.5, 2.5]$, P_O and η have minimal sensitivities to the variations in C_3 and L_3 [25]. During the fine-tuning of the circuit, the value of C_1 might vary. The variation in C_1 changes r_C. To be on the safe side, we choose $r_C = 2.0$ to be in the mid-range between 1.5 and 2.5.

The amplitude of V_F should be chosen based on the selected gate driver and its supply voltage $V_{DD,inv}$. V_F should remain between -0.7 V and $V_{DD,inv} + 0.7$ V so that it does not trigger the ESD diodes of the input pin of the gate driver.

To obtain R_{F1}, R_{F2}, and C_F, we should have three equations, while, up to now, we attain only two, i.e., (17) and (18). We can choose a value for C_F and then calculate R_{F1} and R_{F2} using

$$R_{F1} = \frac{-\sin\varphi_{RC}}{\alpha C_F \omega_s}, \quad (25)$$

and

$$R_{F2} = \frac{\alpha}{\cos\varphi_{RC} - \alpha}\, R_{F1}, \quad (26)$$

respectively.

From (25) and (26), we can conclude that selecting a smaller value for C_F will result in larger values for R_{F1} and R_{F2}, which itself minimizes the ac power loss in the feedback network. Therefore, we should choose a very small value for C_F. We choose C_F to be at least twice the input capacitance of the gate driver, to be certain that the input capacitance of the gate driver does not overwhelm the value of C_F.

V. Design Procedure of the Class-E/F$_3$ PO

In this section, we present a straight-forward design procedure based on the analytical approach described in Section II, III, and IV. In those sections, the effects of circuit nonidealities, including the ON-resistance R_{on} of M_1, the parasitic capacitances of M_1, the turn-ON and turn-OFF delays of M_1, the loading effect of the feedback network on the load network, the propagation delay of the gate driver, and the parasitic elements of the circuit components, were neglected. In this section, we analytically incorporate these circuit nonidealities into the design process. We describe our design procedure for a Class-E/F$_3$ PO, which has the same specifications described in [26], i.e., as follows:

1) The output power $P_O = 1$ W;
2) The supply voltage $V_{DD} = 4.5$ V;
3) The switching frequency $f_s = 800$ kHz;
4) The load quality factor $Q_L = 13$.

Step 1. Designing the Class-E/F$_3$ PA

We first design a Class-E/F$_3$ PA with the abovementioned specifications, and then convert the PA to a PO using the proposed design procedure.

The design equations listed in (1)–(6) are based on the assumption that no power is wasted in the circuit and all the power supplied from V_{DD} is delivered to R_L. In practice, the nonidealities of the circuit components reduce η. Moreover, in a Class-E/F$_3$ PO, the resistive loading of the feedback network wastes a portion of the input power and further reduces η. We make a realistic assumption for η, and then, we replace P_O in the equations with $P_{in} = P_O/\eta$ and calculate the values of the Class-E/F$_3$ PA components.

We assume $\eta = 90\%$, and calculate the component values with $P_{in} = 1.11$ W and $r_C = 2$ using (1)–(6). These calculations result in $R_L = 7.51\ \Omega$, $L_2 = 19.42\ \mu$H, $C_1 = 3.47$ nF, $C_2 = 2.293$ nF, $C_3 = 1.74$ nF, and $L_3 = 2.53\ \mu$H.

We can now choose an appropriate MOSFET for the circuit. The MOSFET should be chosen based on the following criteria:

1) Its R_{on} should be much smaller than R_L.
2) The output capacitance C_o of MOSFET should be considerably less than C_1.
3) The drain-source breakdown voltage $V_{BR(DS)}$ should be larger than $3.2 \times V_{DD}$.
4) The input capacitance C_g should be sufficiently small to minimize the power loss in the gate driver.
5) Its maximum allowed power dissipation $P_{D,max}$ should be more than P_O, because during the start-up, the Class-E/F$_3$ PO is not fully tuned and the power loss in the MOSFET can be prohibitively large.

We choose RQ6E045BN MOSFET manufactured by ROHM Semiconductor to realize M_1. RQ6E045BN has a typical R_{on} of 35 mΩ, C_o of 55 pF, C_g of 330 pF, $V_{BR(DS)}$ of 30 V, and $P_{D,max}$ of 1.25 W. The output capacitance of RQ6E045BN MOSFET is much smaller than C_1. Therefore, we can neglect the nonlinearity in C_o.

The wasted power in R_{on} can be obtained using [25]

$$P_{R_{on}} = \frac{2R_{on}P_O}{R_L}\left(\frac{0.874\, r_C + 0.534}{r_C + 1}\right)^2. \quad (27)$$

The power for charge/discharge of C_g equals

$$P_g = C_g V_{DD,inv}^2 f_s. \quad (28)$$

According to (27) and (28), we expect to have a degradation of about 0.54% and 0.33% in η due to R_{on} and C_g of M_1, if $V_{DD,inv} = 3.7$ V. The power loss, excluding P_g, are supplied through L_{RFC}. P_g is the dissipated power in the gate driver and is supplied from the supply voltage of the inverter.

The equivalent series resistances (ESRs) of the inductors are other major sources of power loss. The ESR of L_2 is often the greatest source of power loss and should be minimized as much as possible. To this end, we constructed L_2 and L_3 using Litz wire wound on a toroidal magnetic iron powder core. Using a GW 8101G LCR meter, we measured the inductance and the ESR of L_2 (R_{L2}) at 800 kHz to be 19.42 μH and 0.3 Ω, respectively. To keep $Q_L = 13$, we should reduce R_L by an amount equal to $R_{L2} = 0.3\ \Omega$. The new value of R_L would be 7.21 Ω. Since R_{L2} is in series with R_L and its value is about 4.2% of R_L, we expect R_{L2} to degrade η by about 4.2%.

The measured inductance of L_3 is 2.53 μH and the measured ESR of L_3, is 0.2 Ω, which causes 0.23% degradation in η. We

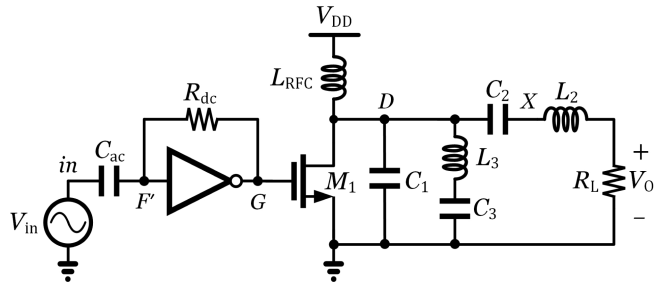

Fig. 5. Circuit schematic used for tuning the basic Class-E/F_3 PA.

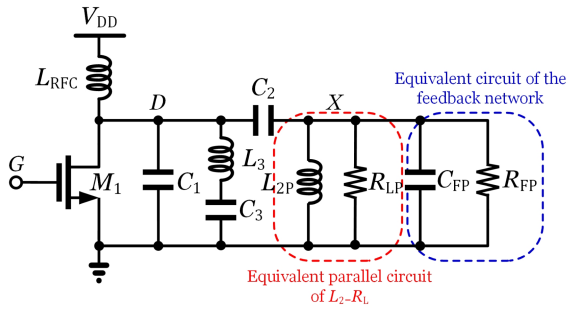

Fig. 6. Schematic to calculate the loading effect of the feedback network on the load network.

choose $L_{RFC} = 800\ \mu H$ to make it much larger than L_2. The current in L_{RFC} is almost a dc current and we can neglect its ripple, as such, the power loss in L_{RFC} is negligible.

We use the schematic shown in Fig. 5 and simulate the designed PA. We select R_{dc} and C_{ac} equal to 1 MΩ and 100 pF, respectively. We choose 74AHC04 as the inverting gate driver. We put a sinusoidal waveform as an input voltage to node in and select its amplitude equal to V_F, which we choose it to be 2.5 V. Then, we simulate and fine-tune the PA. As a result of fine-tuning, the value of C_1 changes from 3.47 nF to 3.65 nF. The simulation results indicate that the output power, i.e., the power delivered to R_L, the drawn power from V_{DD}, and P_g are 1.056 W, 1.108 W, and 5.9 mW, respectively. Therefore, η including P_g is about $1.056\ W/1.1139\ W = 94.8\%$.

Step 2. Designing the Feedback Network

In Sections III and IV, we presented formulae to calculate φ_{DX} and V_X. Using (13) and (24), we calculated φ_{DX} and V_X to be about 53.24 V and 30.2°, respectively. To verify the accuracy of (13) and (24), we simulate the circuit. The simulation of the circuit designed in Step 1 indicates that the amplitude of V_X is 53.16 V, which is in good agreement with what (24) predicted. We run an ac simulation on the $C_2 - L_2 - R_L$ branch and measure the phase shift at node X. Since during the fine-tuning of the PA, the values of the C_2, L_2, and R_L did not change, we obtain φ_{DX} equal to the calculated value, i.e., $\varphi_{DX} = 30.2°$.

The delay of MOSFET $t_{d,M1}$ and the propagation delay of the inverter $t_{pd,INV}$ change the phase shift in the entire oscillation loop. We should calculate the respective phase shift due to the delays of the MOSFET and the inverter and adjust the required phase shift in the passive part of the feedback network. The new value of the phase shift that the *RC* filter should provide equals

$$\varphi_{RC} = -10° - \varphi_{DX} + 360° f_s \left(t_{pd,INV} + t_{d,M1}\right). \tag{29}$$

We obtain $t_{pd,INV}$ and $t_{d,M1}$ separately using simulation. In this design, $t_{pd,INV}$ and $t_{d,M1}$ were measured to be 7.3 ns and 3.2 ns, respectively. By using (29), we obtain φ_{RC} to be −37.2°.

Instead of calculating each term of (29) to obtain φ_{RC}, we can directly measure φ_{RC} using simulation. In this approach, we simulate the circuit shown in Fig. 5 and measure the phase shift from node in to node X, i.e., φ_{in-X}. φ_{in-X} should actually be equal to $-\varphi_{RC}$. Since $Q_L = 13$, the voltage waveform at node X, i.e., V_X is not a pure sinusoid. To accurately calculate the phase shift, one can use a very narrow band-pass filter and extract the first harmonic of V_X. The simulation results indicate that φ_{in-X} is equal to 37.3°, which is in a good agreement with the previously calculated value for φ_{RC}. The difference between the calculated and simulated values of φ_{RC} is 0.1°. This small error is due to the assumption that φ_{GD} is constant when r_C is chosen in the range of $[1.5, 2.5]$.

Since we measured the amplitude of V_X to be 53.2 V, we can calculate $\alpha = V_F/V_X = 0.047$. To minimize the power loss in the feedback network, we select C_F to be 30 pF, which is larger than the input capacitance of the 74AHC04 inverter. Substituting $\alpha = 0.047$ and $\varphi_{RC} = -37.3°$ in (25) and (26), we obtain $R_{F1} = 85.5\ k\Omega$ and $R_{F2} = 5.37\ k\Omega$.

Step 3. Compensating the Loading Effect of the Feedback Network

If a suitable gate driver with a small input capacitance is chosen, C_F can have a very small value. In such a case, the loading effect of the feedback network on the load network is negligible and we can skip this step. Otherwise, we can calculate the loading effect of the feedback network and compensate for it.

To calculate the loading effect, we can model the feedback network with a parallel *RC* circuit consisting of R_{FP} and C_{FP}, as shown in Fig. 6. R_{FP} and C_{FP} can be obtained by

$$R_{FP} = \frac{R_{F_1}}{1 - \alpha \cos(\varphi_{RC})}, \tag{30}$$

and

$$C_{FP} = \alpha^2 C_F, \tag{31}$$

respectively. We can also model the $L_2 - R_L$ branch with an equivalent parallel *RL* circuit, consisting of R_{LP} and L_{2P}, as shown in Fig. 6. R_{LP} and L_{2P} are placed in parallel with R_{FP} and C_{FP}. Since, C_{FP} is in parallel with L_{2P} and R_{FP} is in parallel with R_{LP}, they change the values of the $L_2 - R_L$ branch and therefore, the PO becomes mistuned. To compensate for this, we can simply change the values of L_2 and R_L. To that end, we calculate the values of L_{2P} and R_{LP} using

$$L_{2P} = L_2 \frac{Q_L^2 + 1}{Q_L^2}, \tag{32}$$

and

$$R_{\mathrm{LP}} = R_{\mathrm{L}}\left(Q_{\mathrm{L}}^2 + 1\right), \tag{33}$$

respectively. We can easily prove that the new values of L_2 and R_{L} can be obtained using

$$L_{2\mathrm{n}} = \frac{L_{2\mathrm{p}}}{1 + L_{2\mathrm{p}} C_{\mathrm{Fp}} \omega_{\mathrm{s}}^2} \times \frac{Q_{\mathrm{L}}^2}{Q_{\mathrm{L}}^2 + 1}, \tag{34}$$

and

$$R_{\mathrm{Ln}} = \frac{R_{\mathrm{Lp}} R_{\mathrm{FP}}}{R_{\mathrm{FP}} - R_{\mathrm{Lp}}} \times \frac{1}{Q_{\mathrm{L}}^2 + 1}. \tag{35}$$

It should be noted that selecting a smaller value for C_{F} reduces the loading effect of the feedback network on the load network. In our design example, we calculate C_{FP} to be 66.3 fF using (31). Since C_{FP} has a negligible value, we only consider the resistive loading of the feedback network. Using (30) and (33), we calculate the values of R_{FP} and R_{LP} to be 88.82 kΩ and 1.28 kΩ, respectively. Since R_{FP} is much larger than R_{LP}, the resistive loading of the feedback network is also negligible and does not affect the circuit operation. Therefore, we connect the feedback network to the PA designed in Step 1 without any modification in the load network components.

Step 4. Closing the Feedback Network and Fine-Tuning the PO

When the feedback network is closed, i.e., V_{in} is removed and node *F* is connected to node *in*, the circuit should start oscillating by itself; however, the duty cycle of the gate signal may be deviated from 50%, which causes the circuit to be mistuned. As a result, we should fine-tune the drain voltage and the switching frequency of the PO. In Class-E/F$_3$ PA and PO, f_{s} is sensitive to L_2, C_2, and C_1, therefore, these components should not be considerably changed. We suggest starting the tuning process with C_{F} and then, C_1 and C_2.

In our design example, we need to change the values of C_{F} from 30 pF to 29.55 pF and C_1 from 3.65 nF to 3.54 nF. The simulated values of the output power, the efficiency excluding P_{g}, the efficiency including P_{g}, and the switching frequency are 1.06 W, 93.6%, 93.1%, 799.97 kHz, respectively. Since the output power is different from the desired value, we can reiterate the design procedure, but this time with 6% less input power or $P_{\mathrm{in}} = 1.05$ W. The final values of the components in simulation are written in Table I. The final values of the output power, the efficiency, and the switching frequency are 1.00 W, 93.0%, and 800.02 kHz, respectively, in simulation. Fig. 7 shows the simulated waveforms of V_{D}, V_{G}, and the output voltage V_{O}.

VI. Experimental Results

To validate the circuit operation and the design procedure, we built and tested the designed Class-E/F$_3$ PO in Section V. Fig. 8 shows the experimental waveforms of V_{D}, V_{G}, and V_{O}. We observe in Fig. 8 that V_{D} satisfies ZVS and ZVDS conditions.

Fig. 9 shows a photograph of the test set-up and the implemented Class-E/F$_3$ PO. To have large self-resonance frequencies, we employed SMD and DIP ceramic capacitors for C_{ac}, C_1, C_2, and C_3 with a nominal tolerance of 10% [27], [28].The component values and the experimental parameters are reported in Table I, alongside the simulation results. Most of the measured values match well with the simulated results. The differences in C_1 and C_{F} are due to underestimating the values of the output capacitance of M_1 and the input capacitance of the gate driver, respectively.

TABLE I
Values of the Parameters and the Circuit Components Resulted From Simulation and Experiment

Parameter	Sim.	Exp.	Diff.
L_{RFC} (μH)	800	745	−6.87%
C_1 (nF)	3.24	3.07	−5.25%
C_2 (nF)	2.169	2.174	0.23%
L_2 (μH)	20.533	20.52	−0.06%
R_{L} (Ω)	7.77	7.74	−0.39%
C_3 (nF)	1.642	1.646	0.24%
L_3 (μH)	2.679	2.673	−0.22%
R_{F1} (kΩ)	71.279	71.3	0.03%
R_{F2} (kΩ)	5.443	5.41	−0.61%
C_{F} (pF)	30.17	10.6	−64.87%
V_{DD} (V)	4.5	4.5	0.00%
f_{s} (kHz)	800.02	800.04	0.00%
P_{O} (W)	1.00	1.023	2.3%
η (%)	93.1 %	93.5%	0.4%

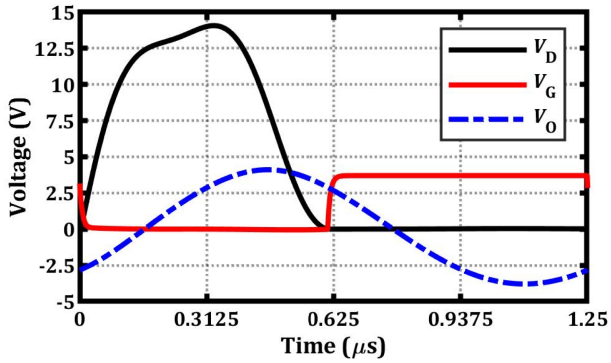

Fig. 7. Simulation results of the designed Class-E/F$_3$ PO with actual components.

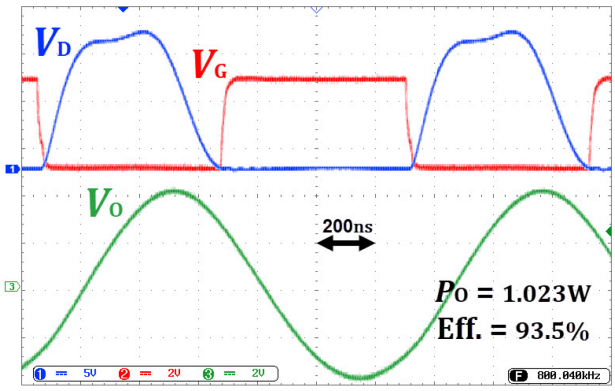

Fig. 8. Experimentally obtained waveforms of the implemented Class-E/F$_3$ PO.

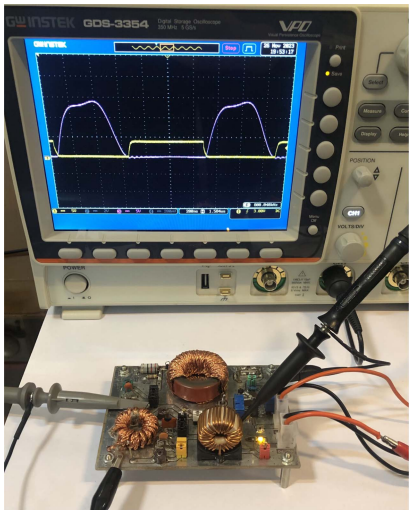

Fig. 9. Photograph of the experimental setup for testing the proposed PO.

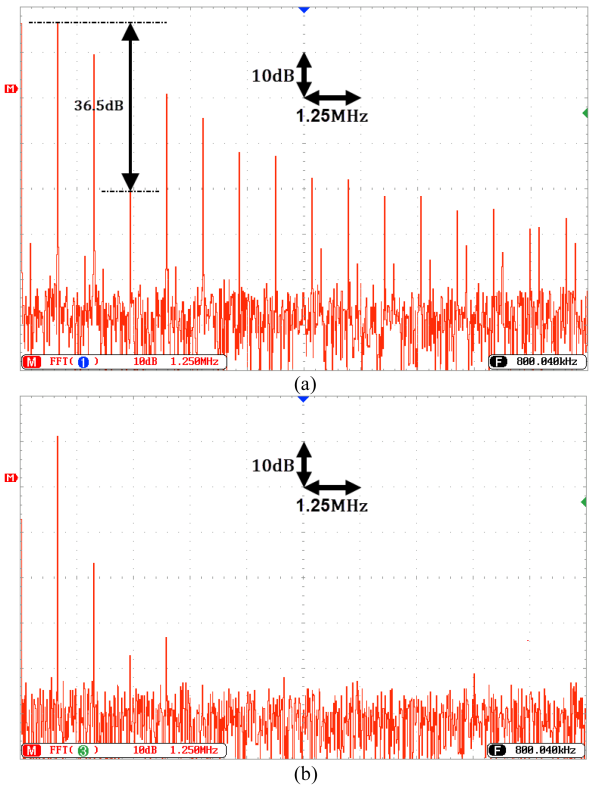

Fig. 10. Spectrum of (a) the drain voltage and (b) the output voltage.

The Fourier transform of V_D is plotted in Fig. 10(a), showing that the third harmonic is markedly minimized in the drain voltage. Considering Fig. 10(a), the amplitude of the third harmonic is about 36.5 dB lower than that of the fundamental frequency. Fig. 10(b) shows the Fourier transform of the output voltage. Considering Fig. 10(b), the measured total harmonic distortion is equal to 3.97%.

The amplitude of V_O is 3.98 V, which translates to an output power of 1.023 W. η and f_S of the PO were measured to be 93.5% and 800.04 kHz, respectively. P_g is included in the reported η. The measured η is 0.4% larger than the simulated value. This increase is due to overestimating the ESRs of the inductors and the input capacitance of M_1.

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART

Parameter	**This work**	[23] 2018	[25] 2023	[22] 2016	[18] 2017	[19] 2015
η (%)	**93.5**	86.2	94.2	95	96	93.5
P_O (W)	**1.02**	0.91	0.96	5.54	4.8	10
f_S (MHz)	**0.8**	0.8	0.8	4	4	4
V_{DD} (V)	**4.5**	6	4.5	25	20	25
Q_L	**13**	12	13	10	10	10
r_C	**2**	$\approx$ 19.5	1.5	$\approx$ 10	$\approx$ 13	$\approx$ 10
Class	**E/F$_3$ PO**	E/F$_3$ PO	E/F$_3$ PA	E/F$_3$ PA	E/F$_3$ PA	E/F$_3$ PA

The performance of the implemented Class-E/F$_3$ PO is compared with that of the previously reported Class-E/F$_3$ circuits designed for similar specifications in Table II. The main advantage of the implemented Class-E/F$_3$ PO over the existing ones is that its η and P_O are much less sensitive to the variations in the component values. This advantage cannot be seen in Table II. It should be noted that the Class-E/F$_3$ PA reported in [25] is also fairly insensitive to the variations in the harmonic filter components, but the operation of the PA is very sensitive to other load network components, C_2 and L_2 [25].

The efficiencies of the PAs in Table II are equal to or slightly larger than our proposed PO. The reason is that a PA does not include a feedback network; therefore, ideally, it can provide a slightly larger efficiency, but this slight increase in efficiency is at the cost of larger sensitivity to the component values.

We evaluated the operation of the implemented PO against the variations in the supply voltage and the load resistor. Fig. 11(a) and (b) shows V_D, V_G, and V_O when V_{DD} changes by -10% and $+10\%$, respectively. As is clear in Fig. 11, V_D satisfies ZVS and ZVDS conditions in both cases; therefore, the PO keeps its high efficiency. The values of η and P_O are specified in Fig. 11.

In Fig. 12(a) and (b), the waveforms of V_D, V_G, and V_O are shown for -12% and $+12\%$ variations in R_L. The values of η and P_O are specified in Fig. 12. We can observe in Fig. 12 that η and P_O are fairly insensitive to the variation in R_L. For example, if R_L decreases by -12%, P_O and η decrease by 3.0% and 0.8%, respectively. Looking at the drain voltage waveforms shown in Fig. 12, we can conclude that increasing the value of R_L moves the trough, i.e., the zero-slope point of V_D, upward.

We also evaluated the sensitivities of P_O and η of the PO to the variation in C_2. In the implemented circuit, we changed the value of C_2 in the range of $\pm 10\%$ and measured P_O and η. The measured results are plotted in Fig. 13. We, also studied the performance of the designed PO against the variation in C_2 in simulation. We simulated the Class-E/F$_3$ PO designed in Section V and swept the value of C_2 up to $\pm 10\%$. The simulation results are superimposed on the experimental results in Fig. 13. As is clear in Fig. 13, the measured results match well with the simulated results and they both show the robustness of P_O and η of the proposed PO against the variation in C_2.

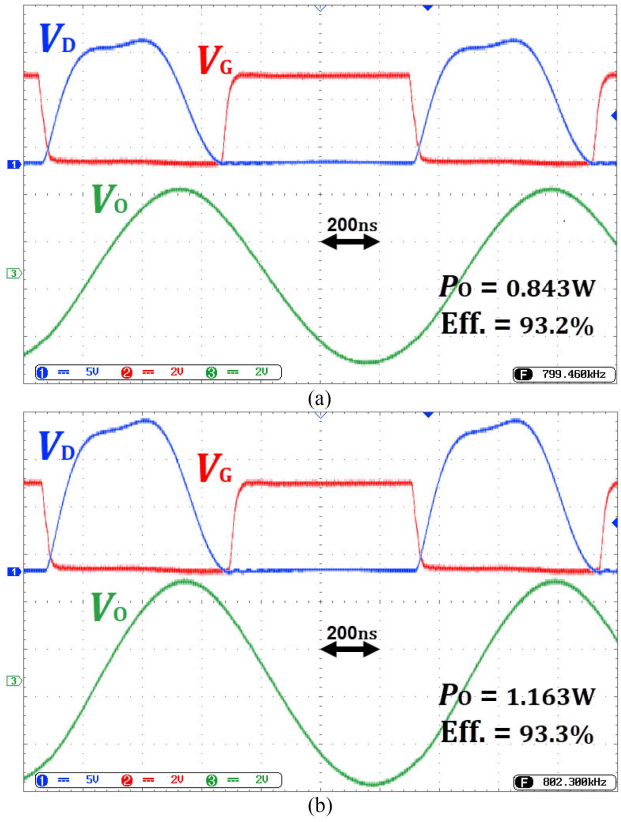

Fig. 11. Experimental voltage waveforms of the implemented Class-E/F$_3$ PO when the value of V_{DD} changes by (a) -10%, (b) $+10\%$.

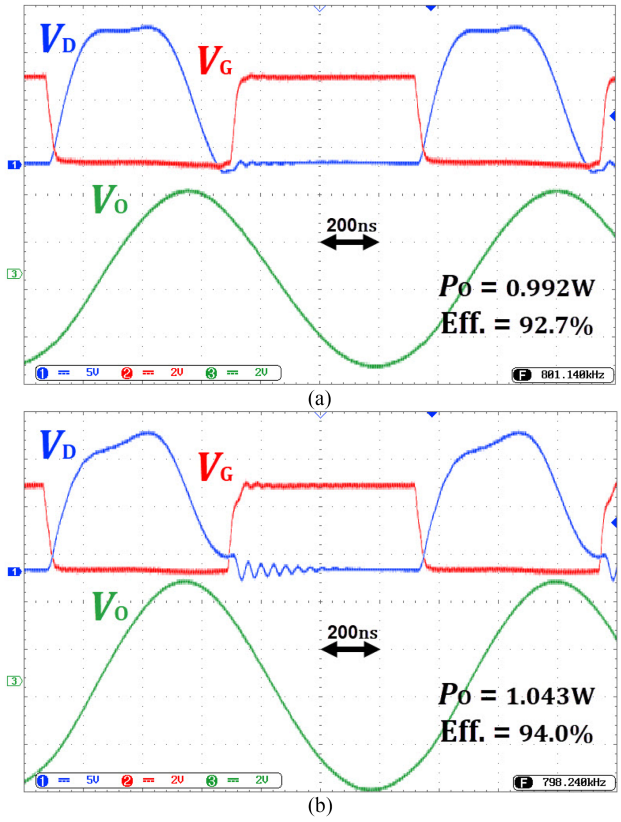

Fig. 12. Experimental voltage waveforms of the implemented Class-E/F$_3$ PO when the value of R_L changes by (a) -12%, (b) $+12\%$.

VII. Discussion

To better clarify the advantages of the proposed Class-E/F$_3$ PO, we compare the performance of the proposed PO with that of the existing circuits.

First, we compare the effects of the component variations on the performance of the proposed PO with that of the existing PO presented in [23]. Then, we compare the proposed PO with its PA counterpart in terms of their sensitivities to the variations in the component values.

A. Comparison with the Existing Class-E/F$_3$ PO

P_O and η of a Class-E/F$_3$ PA are highly sensitive to the values of the load network components, especially to C_2 and L_2. To solve this issue, in [23] and in this work, a feedback network is added to the Class-E/F$_3$ PA to generate the switching frequency according to the resonance frequencies of the load network. Here, we compare the sensitivities of P_O, η, and V_D of the existing Class-E/F$_3$ PO with the ones of the proposed PO in this article. To this end, we change the value of the components having a major effect on the circuit operation up to $\pm 10\%$ and simulate the POs depicted in Fig. 2 (taken from [23]) and the one that was designed in Section V. The simulation results are plotted in Fig. 14.

Fig. 14(a) shows ΔP_O and $\Delta\eta$ curves versus ΔL_2 for both POs and Fig. 14(b) shows the normalized V_D versus ΔL_2. As is shown in Fig. 14(a), when L_2 decreases by 10%, P_O of the PO presented in [23] increases by 71.9%, while it increases by 22.4% in our proposed PO. Fig. 14(b) shows that the normalized V_D of the existing PO has completely deviated from its desired shape when L_2 reduces by 10%. Also, if L_2 increases by 10%, P_O of the presented PO in [23] decreases by 58.9%, while it decreases by 14.0% in the PO proposed in this article. The sensitivity curves against the variation in C_2 are similar to those against the variation in L_2 and, as such, are not plotted for the sake of brevity.

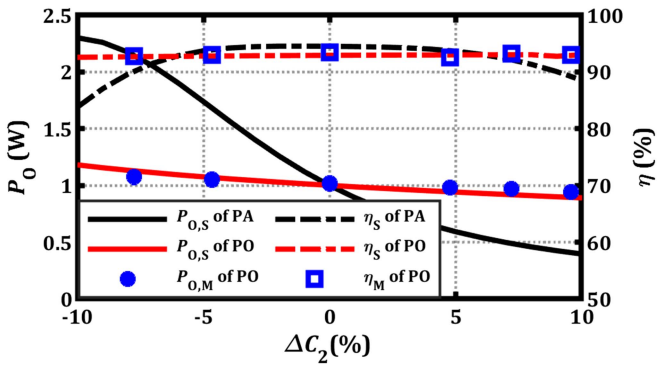

Fig. 13. Comparison of variations in P_O and η of the simulated and implemented Class-E/F$_3$ PO with those of the simulated Class-E/F$_3$ PA designed for the same specifications and with similar components. Subscripts with "S" are the simulated values and those with "M" are the measured values.

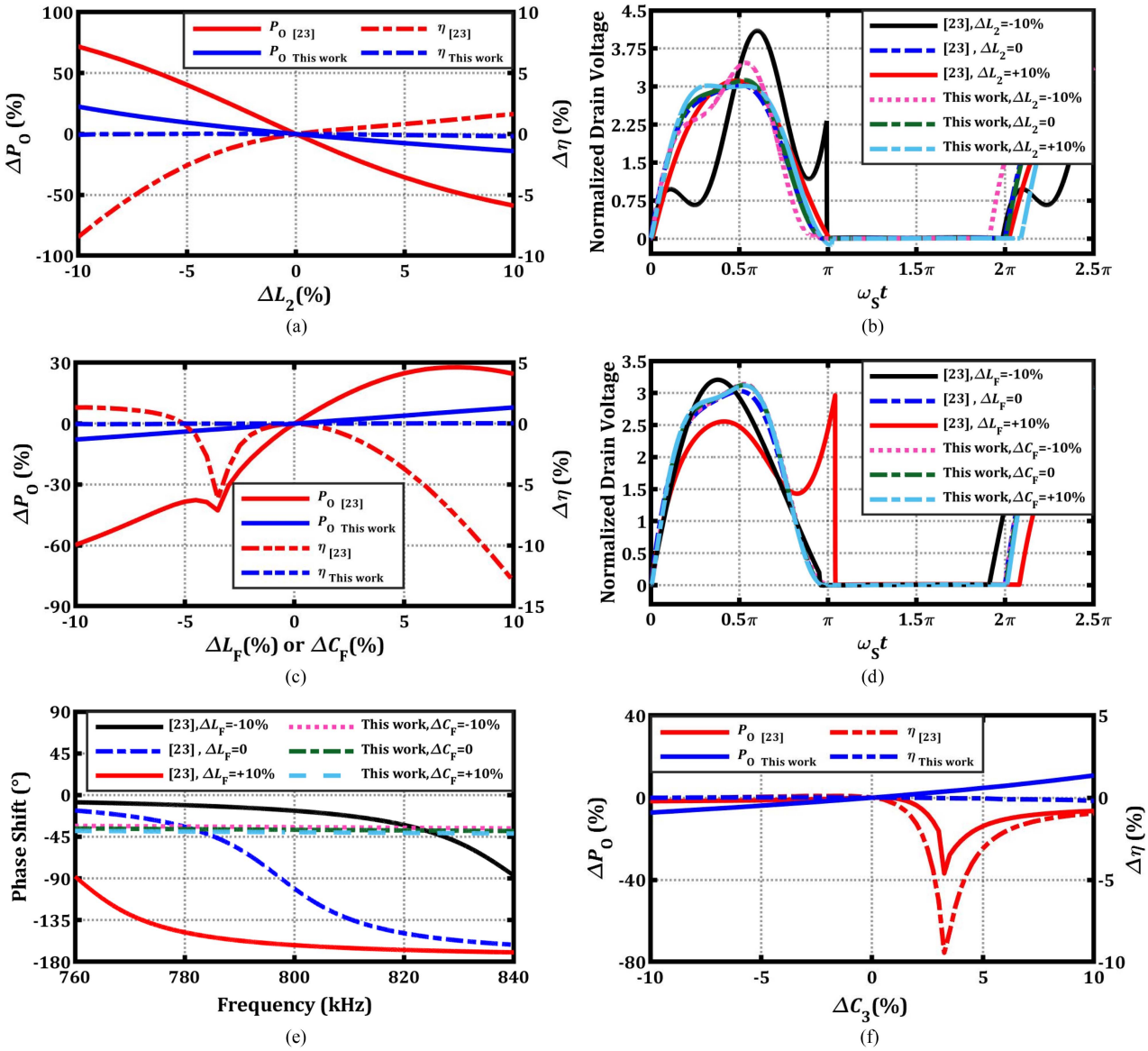

Fig. 14. Comparison of variations in P_O and η of our proposed PO with those of the existing one presented in [23], when the values of (a) L_2, (c) L_F, or C_F, and (f) C_3 were swept up to $\pm 10\%$. (b) and (d) are normalized switch voltage waveforms for both POs when the specified components have their desired values and when they change by $\pm 10\%$. (e) Phase response of the feedback network of both POs when L_F or C_F has its desired value and when it changes by $\pm 10\%$.

Another advantage of the proposed PO is that its η is significantly less sensitive to the changes in C_2 or L_2. For example, when L_2 decreases by 10%, η of the presented PO in [23] decreases by 8.5%, while it decreases only 0.05% in our proposed PO. The proposed PO maintains its high efficiency over the entire range of $\pm 10\%$ variation in L_2.

We can conclude that P_O and η of our proposed Class-E/F$_3$ PO have lower sensitivities to the variations in C_2 or L_2 compared with those of the existing PO. In fact, if the value of C_2 or L_2 changes, the switching frequency of the proposed PO can better track the resonance frequencies of the load network, and therefore, as depicted in Fig. 14(b), V_D will remain close to its desired shape.

In the PO presented in [23], L_F and C_g of M_1 play major roles in the resonance frequency of the feedback network. On the other hand, as we will explain later in this section, the feedback phase shift in our proposed PO is most sensitive to C_F. Therefore, we swept the value of L_F in the PO presented in [23] and the value of C_F in our proposed PO to compare the sensitivities of P_O and η against the variations in the feedback network components. Fig. 14(c) shows the simulated ΔP_O and $\Delta\eta$ of the POs and Fig. 14(d) illustrates the normalized V_D for both POs when L_F or C_F has its desired value and when it changes by $\pm 10\%$.

Fig. 14(c) and (d) show that P_O, η, and f_s of the proposed PO have significantly lower sensitivities to the changes in the feedback network components. Moreover, V_D of the proposed PO maintains its desired shape when C_F changes by $\pm 10\%$. The large sensitivity of the existing PO to its component values is due to the fact that its feedback network is a high-Q *RLC* circuit which has a steep slope in its phase transfer function. Fig. 14(e)

shows the phase shift in the feedback network of the existing and the proposed POs. In this figure, we plotted three curves for each feedback network: one curve for when $L_{\rm F}$ or $C_{\rm F}$ has its desired value and two other curves for when either $L_{\rm F}$ or $C_{\rm F}$ changes by $\pm 10\%$. As Fig. 14(e) shows, when $L_{\rm F}$ decreases by 10%, the phase shift of the feedback network in [23] changes from -100.91° to -16.98° at 800 kHz. As a consequence, the oscillation frequency should change from 800 kHz to 837.3 kHz, to keep the phase shift around the feedback loop -360°. This change in the oscillation frequency, or the signal period, is clear in Fig. 14(d). In contrast, the feedback network of our proposed PO is a low-Q nonresonant circuit. Therefore, when the value of $C_{\rm F}$ decreases by 10%, the value of the phase shift changes by only $+2.87^\circ$. As a result, $f_{\rm s}$ of our proposed PO has negligible sensitivity to the changes in the feedback network components.

It is worth mentioning that the phase shift in the feedback network of our proposed PO is defined by the frequency pole of its *RC* circuit. The pole frequency equals $1/(2\pi(R_{\rm F1}||R_{\rm F2})C_{\rm F})$. Since in the proposed PO, $R_{\rm F1}$ is much larger than $R_{\rm F2}$, that formula simplifies to $1/(2\pi R_{\rm F2}C_{\rm F})$. This formula shows that the sensitivity to $C_{\rm F}$ and $R_{\rm F2}$ are almost the same. Therefore, we only showed the sensitivities of the proposed PO to the variation in $C_{\rm F}$.

In the gate driver circuit, $C_{\rm ac}$ is an ac-coupled capacitor and $R_{\rm dc}$ is added to bias the inverter at its switching threshold voltage. The value of $C_{\rm ac}$ must simply be selected a few times larger than the input capacitance of the inverter and the value of $R_{\rm dc}$ should be large enough such that the output signal of the feedback network is coupled to the input of the inverter with negligible attenuation. If such conditions are met, the sensitivities to the values of $C_{\rm ac}$ and $R_{\rm dc}$ are negligible.

The PO presented in [23] has another drawback, which is related to the design of the $C_3 - L_3$ branch. As we mentioned in Section II, in a Class-E/F$_3$ PA if the value of $r_{\rm C}$ is selected in the range of $[1.5, 2.5]$, $P_{\rm O}$ and η will have negligible sensitivities to the changes in C_3 or L_3. This statement is also valid for a Class-E/F$_3$ PO. In the presented Class-E/F$_3$ PO in [23] depicted in Fig. 2, the ratio of C_1/C_3 is approximately 17. Therefore, we expect $P_{\rm O}$ and η of that PO to be very sensitive to the changes in C_3 or L_3. To investigate this issue, in Fig. 14(f), we plotted the simulated $\Delta P_{\rm O}$ and $\Delta\eta$ curves for that PO and also for the one proposed in this work versus ΔC_3. Looking at Fig. 14(f), we can see that as C_3 increases, there are large drops in $P_{\rm O}$ and η of the existing PO. But the operation of our proposed PO is robust against the variation in C_3. The same conclusion can be made for the variation in L_3, but we have not plotted those sensitivity curves for the sake of brevity.

B. Comparison with Class-E/F$_3$ PA

As mentioned earlier, $P_{\rm O}$ and η of a Class-E/F$_3$ PA are sensitive to the values of C_2 and L_2. This issue is more pronounced when $Q_{\rm L}$ of the PA is large. To compare a Class-E/F$_3$ PO with its PA counterpart in terms of their sensitivities to the values of C_2 and L_2, we simulated the Class-E/F$_3$ PA designed in Section V and swept the value of C_2 up to $\pm 10\%$. Fig. 13 shows these sensitivity curves against the variation in C_2, which

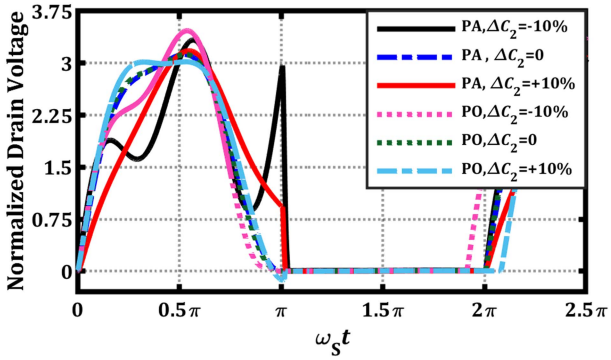

Fig. 15. Comparison of the normalized switch voltage waveform of the simulated Class-E/F$_3$ PO with its PA counterpart, when C_2 changes from -10% to $+10\%$.

are superimposed on the ones resulted from simulation and experiment in Section VI. The sensitivities of $P_{\rm O}$ and η against the variation in C_2 for both Class-E/F$_3$ PA and PO are similar to those against the variation in L_2. Therefore, we have only plotted the sensitivity curves against the variation in C_2. The normalized drain voltage is plotted in Fig. 15 for both circuits, when C_2 has its desired value and when it changes by $\pm 10\%$.

Interestingly, $P_{\rm O}$ of the PA has changed from $+130.3\%$ to -60.4% of its nominal value when C_2 changes by $\pm 10\%$, while $P_{\rm O}$ of the proposed PO has only changed from $+17.9\%$ to -11%. In addition, as shown in Fig. 15, $V_{\rm D}$ of the PA deviates markedly from its desired shape, while $V_{\rm D}$ of the PO remains close to its desired shape. This is a great advantage for the proposed PO. In other word, as is observed in Fig. 15, the switching frequency of PO is adaptively adjusted to keep the circuit tuned.

The same conclusion can be made for the variation in the efficiency. As shown in Fig. 13, η of the proposed PO is almost constant while η of the PA degrades nearly 11%. According to the simulation results, we can conclude that the performance of the proposed PO has much smaller sensitivity against the variations in C_2 and L_2.

VIII. Conclusion

In this article, we introduced a self-tuned Class-E/F$_3$ PO whose feedback network is composed of a low-Q *RC* circuit and an inverting gate driver. The output power and the efficiency of the proposed circuit have negligible sensitivities to the variations in the circuit components. In addition, the circuit autonomously starts oscillating without requiring a start-up circuit. We also presented a design procedure for the proposed Class-E/F$_3$ PO and verified the design procedure with simulation and experimental evaluations.

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