A Novel Extended Sliding-Mode Predictive Control With Dynamic Optimization and Virtual Voltage Vectors

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***Abstract*—This article proposes a novel extended sliding-mode predictive control strategy for three-phase three-level voltage source inverters. Initially, the control domain is established using sliding-mode theory, dynamically reducing the search space. Subsequently, a unique parallel optimization strategy is presented in the two-phase stationary coordinate system, with an analysis of the monotonicity of the cost functions and the constraints within the search space. Compared to traditional model predictive control, this approach results in a calculation time reduction of at least 51.3%. To mitigate output ripple, a novel design method for virtual voltage vectors (VVVs) is proposed based on α and β components, demonstrating notable scalability. At the same time, to maintain neutral point voltage balance, two output modes are devised for the VVVs using redundant small voltage vectors, eliminating weighting factors. Additionally, the excessive voltage jumps are mitigated and the method operates at a constant switching frequency. Experimental results robustly validate the algorithm's superior performance.**

***Index Terms*—Model predictive control, simplified calculation, sliding-mode theory, three-phase three-level voltage source inverters, virtual voltage vectors (VVVs), without weighting factors.**

I. INTRODUCTION

THREE-PHASE three-level voltage source inverters (3P-3L VSIs) with *LC*-filter represent a prevailing topology in applications such as ac microgrids, distributed generation systems, and uninterruptible power supplies [1], [2], [3].

This preference arises from their higher voltage tolerance class, elevated efficiency, diminished harmonic content, and reduced electromagnetic interference (EMI) [4], [5]. Traditional linear control methods, including proportional integral control and proportional resonant control, have been widely used to control 3P-3L VSIs. However, with the growing need for rapid dynamic responses and the inclusion of various nonlinear loads in modern power applications, conventional linear control methods face substantial constraints in fulfilling these changing demands [6], [7].

On the other hand, nonlinear control strategies have demonstrated significant promise as effective solutions. A widely adopted nonlinear control method is sliding-mode control (SMC). In SMC, switching conditions and control laws are designed in accordance with the control objective to compel the system to slide along a predefined sliding surface, which enhances robustness against load disturbances and modeling errors [8], [9]. Many researchers have explored the application of SMC in power converters [9], [10], [11]. In [9], a single-stage sliding-mode voltage controller with state feedback was proposed for a pulsed load microgrid, showcasing a satisfactory dynamic response. Moreover, in [11], a hysteresis SMC technique for grid-connected inverters was introduced, augmenting robustness against disturbances. However, in practical discrete systems, control and sampling signals are frozen in one cycle, preventing the attainment of ideal sliding motion, only quasi sliding-mode near the ideal sliding surface can be achieved [12], [13].

Unfortunately, the aforementioned SMC lacks consideration for tracking error minimization, resulting in undesired output fluctuations and intractable multiobjective optimization problems [14], [15]. Finite-control-set model predictive control

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(FCS-MPC) offers an effective solution, providing excellent dynamic performance and a straightforward control structure [16]. FCS-MPC initially establishes the mathematical model of the system and employs online rolling optimization to determine the optimal voltage vector, minimizing tracking error for the next switching cycle [17]. This control method mitigates control delays. Traditional FCS-MPC operates only one voltage vector in a single switching cycle, leading to significant output ripples and variable switching frequencies. To address this limitation, employing multiple voltage vectors in a switching cycle proves feasible [18], [19], [20]. In [18], three voltage vectors are applied in a switching cycle, with the operation time for each voltage vector inversely proportional to its respective cost value. In [19], FCS-MPC based on optimal switching sequence MPC was proposed, obtaining a dominant solution to minimize the cost function and exhibiting impactful effect. Both methods mentioned above rely on modulation. In [20], virtual voltage vectors (VVVs) are introduced, achieving a constant switching frequency (CSF).

Both modulation-based methods and the VVVs inherently broaden the control domain, complicating the optimization process. Consequently, meticulous preselection becomes indispensable, particularly for 3P-3L VSIs. In [21], deadbeat (DB) control is integrated to confine the search space. However, the accuracy of DB is contingent on system parameters, posing challenges for ensuring robustness. In [22] and [23], preselection schemes based on medium voltage vectors and tolerant sequences are proposed, effectively reducing computational complexity. Notably, all the aforementioned methods consider a finite number of voltage vectors while overlooking the finite nature of real and imaginary axis components. To the best of our knowledge, this aspect is rarely explored in the literatures.

In addition, to leverage the advantages of 3P-3L VSIs and realize smooth switching, it is crucial to ensure that the phase and line-to-line voltage jumps (ΔV) during voltage vector switching should not surpass half of the dc side voltage [24]. Excessive ΔV can introduce harmonics to the output voltage, thereby increasing the burden on the filters [25], [26]. To address this issue, Zhang et al. [24] proposed the insertion of an intermediate voltage vector between two consecutive sectors with excessive ΔV to ensure smooth switching. Zhou et al. [25] selected no more than five candidate voltage vectors based on the reference voltage vector and the previous optimal voltage vector, effectively preventing excessive ΔV.

At the same time, achieving neutral point (NP) voltage balance is also crucial for a 3P-3L VSI, and a common strategy is to introduce a weighting term in the cost function. However, the introduction of weighting factors increases the complexity of the algorithm [27]. An alternative approach to avoid the use of weighting factors is to automatically balance NP voltage by employing different redundant small voltage vectors in conjunction [28], [29]. In addition, the robustness problem of FCS-MPC has also been an open question. Model-free methods including parameter identification, gradient method, and observers have also been proposed to enhance the robustness [30], [31], [32], [33]. Nevertheless, the complexity of these methods is high.

In light of this, exploring a new efficient optimization method that leverages the advantages of both SMC and FCS-MPC is an intriguing research topic. Recently, some scholars have carried out preliminary exploration into this area. In [34], the space vector diagram is divided into 12 sectors and preselected based on the grid voltage's position and sliding-mode theory, with the aim of reducing computational burden. However, this method overlooks the dynamic nature of the grid voltage, and there are still numerous voltage vectors to evaluate, limiting the degree of optimization. Another approach, presented in [35], includes the arrival condition of SMC in the cost function, aiming to identify the maximum negative value of the cost function. Additionally, in [14], the sliding-mode function is explicitly incorporated into the cost function for the first time, enhancing the robustness. However, the cost function does not consider the minimum tracking error, and it introduces a parameter adjustment problem.

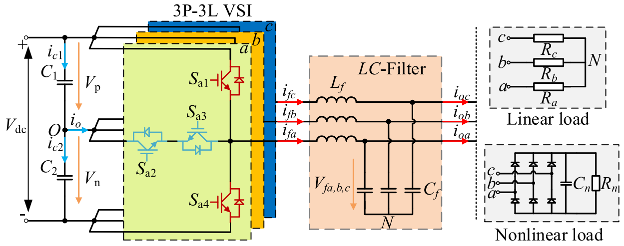


Fig. 1. Circuit structure of a T-type 3P-3L VSI.

To solve the above problems, this article proposes a novel extended sliding-mode predictive control (ESM-PC) for 3P-3L VSIs with *LC*-filters. The primary contributions of this research are outlined as follows.

1) A novel VVVs design method based on real axis and imaginary axis components is proposed. This method mitigates the output ripple, eliminates the weighting factor for NP balance and achieves CSF.
2) A new optimization method is introduced to optimize the real axis and imaginary axis components in parallel. The monotonicity of the cost functions and the constraints within the search space are analyzed, which significantly reduces the computational burden.
3) The sliding-mode theory-based preselection method is enhanced by considering the dynamic characteristics of the output voltage. In comparison with the original method, the new optimization method is dynamic.

The rest of this article is organized as follows. Section II provides a comprehensive description of the whole system model and dynamic model. In Section III, the proposed ESM-PC is detailed. Section IV presents various comparative experimental results. Finally, Section V concludes this article.

II. SYSTEM MODELING AND TRADITIONAL FCS-MPC

The circuit topology of a typical 3P-3L VSI with *LC*-filter is shown in Fig. 1 [5].

As illustrated, V_{dc} denotes the dc voltage, V_p and V_n represent the voltages of the upper and lower capacitors, respectively. In the equilibrium state, $V_p = V_n = V_{dc}/2$. i_{c1}, i_{c2}, and i_o represent the currents flowing through the upper and lower capacitors and the NP current, respectively. L_f and C_f represent the filter inductor and filter capacitor, respectively. $i_{fx} (x = a, b, c)$ is the current of the filter inductor, while $V_{fx} (x = a, b, c)$ and

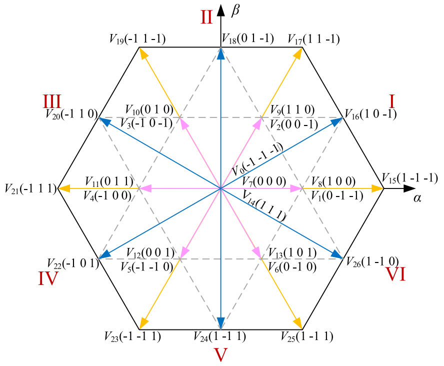


Fig. 2. Space vector diagram.

$i_{ox}(x=a,b,c)$ represent the voltage of the filter capacitor and output current, respectively.

A. General T-Type Inverter Model

For each leg of a 3P-3L VSI, three possible output states are defined as "P", "O," and "N," where "P" signifies that the power switches $S_{x1}(x=a,b,c)$ and $S_{x2}(x=a,b,c)$ are turned ON, "O" signifies that the power switches $S_{x2}(x=a,b,c)$ and $S_{x3}(x=a,b,c)$ are turned ON, and "N" signifies that the power switches $S_{x3}(x=a,b,c)$ and $S_{x4}(x=a,b,c)$ are turned ON. Therefore, as shown in Fig. 2, there are 3^3 (27) possible voltage vectors [18]. In terms of amplitude, they can be divided into zero, small, medium, and large voltage vectors, respectively.

The switching function S_x is defined as

$$S_x=\begin{cases}1 & S_{x1} \text{ and } S_{x2} \text{ ON}, S_{x3} \text{ and } S_{x4} \text{ OFF},\\ 0 & S_{x2} \text{ and } S_{x3} \text{ ON}, S_{x1} \text{ and } S_{x4} \text{ OFF},\\ -1 & S_{x3} \text{ and } S_{x4} \text{ ON}, S_{x1} \text{ and } S_{x2} \text{ OFF},\end{cases} \quad x=a,b,c. \tag{1}$$

Suppose the NP voltage is already effectively balanced. The output voltage of each phase with respect to the load NP "*N*" can be expressed as follows [20]:

$$\begin{bmatrix}V_{aN}\\ V_{bN}\\ V_{cN}\end{bmatrix}=\frac{V_{\text{dc}}}{6}\begin{bmatrix}2 & -1 & -1\\ -1 & 2 & -1\\ -1 & -1 & 2\end{bmatrix}\begin{bmatrix}S_a\\ S_b\\ S_c\end{bmatrix}. \tag{2}$$

The capacitor voltage $\boldsymbol{V}_{fa,b,c}$ and inductor current $\boldsymbol{i}_{fa,b,c}$ are defined as state variables, and from the dynamic relationship of the *LC*-filter in Fig. 1, the continuous-time dynamic model in the $\alpha\beta$ coordinate system can be obtained after the Clark transform

$$\begin{cases}\frac{d\boldsymbol{V}_{f\alpha\beta}}{dt}=\frac{1}{C_f}\left(\boldsymbol{i}_{f\alpha\beta}-\boldsymbol{i}_{o\alpha\beta}\right)\\ \frac{d\boldsymbol{i}_{f\alpha\beta}}{dt}=\frac{1}{L_f}\left(\boldsymbol{V}_{\alpha\beta}-\boldsymbol{V}_{f\alpha\beta}\right)\end{cases}. \tag{3}$$

When the sampling period T_s is sufficiently small, the forward Euler approximation is used to discretize the continuous model. Subsequently, the recursive expression of state variables at (k+1)th and (k)th instants can be obtained and the discrete state-space model of (3) is as follows:

$$\begin{bmatrix}\boldsymbol{V}_{f\alpha\beta,k+1}\\ \boldsymbol{i}_{f\alpha\beta,k+1}\end{bmatrix}=\boldsymbol{A}^{\Gamma}\begin{bmatrix}V_{f\alpha\beta,k}\\ i_{f\alpha\beta,k}\end{bmatrix}+\boldsymbol{B}^{\Gamma}\boldsymbol{V}_{\alpha\beta}+\boldsymbol{C}^{\Gamma}\boldsymbol{i}_{o\alpha\beta,k} \tag{4}$$

where

$$\boldsymbol{A}^{\Gamma}=\begin{bmatrix}1 & T_s/C_f\\ -T_s/L_f & 1\end{bmatrix} \qquad \boldsymbol{B}^{\Gamma}=\begin{bmatrix}0\\ T_s/L_f\end{bmatrix}$$

$$\boldsymbol{C}^{\Gamma}=\begin{bmatrix}-T_s/C_f\\ 0\end{bmatrix}. \tag{5}$$

It is worth noting that all the aforementioned modeling is based on balanced NP voltage. In practice, the capacitor voltage needs to be analyzed. As shown in Fig. 1, the relationship between current and voltage of the upper and lower capacitors on the dc side can be expressed as follows:

$$\begin{cases}i_{c1}=C_1\frac{dV_p}{dt}\\ i_{c2}=C_2\frac{dV_n}{dt}\end{cases}. \tag{6}$$

The balance of the NP voltage is related to the NP current i_o, which can be expressed as

$$i_o=i_{fa}\left(1-|S_a|\right)+i_{fb}\left(1-|S_b|\right)+i_{fc}\left(1-|S_c|\right). \tag{7}$$

Similarly, the discretization can be performed using the forward Euler method. Therefore, the difference between the voltages of the upper and lower capacitors at (k+1)th instant can be obtained

$$\begin{aligned}\Delta V_{\text{NP},k+1}&=V_{p,k+1}-V_{n,k+1}\\ &=(V_{p,k}-V_{n,k})+\frac{T_s}{C}i_{o,k}\\ &=\Delta V_{\text{NP},k}+\frac{T_s}{C}\sum_{x\in\{a,b,c\}}(1-|S_x|)i_{fx,k}\end{aligned} \tag{8}$$

where $C_1=C_2=C$.

B. Traditional FCS-MPC

The traditional FCS-MPC initially formulates the prediction equation for the state variables and subsequently determines the optimal control input through rolling optimization. Thus, the nominal predictive model is derived from (4) as follows:

$$\boldsymbol{i}^{p}_{f\alpha\beta,k+1}=\boldsymbol{i}_{f\alpha\beta,k}+\frac{T_s}{L_f}\left(\boldsymbol{V}_{\alpha\beta}-\boldsymbol{V}_{f\alpha\beta,k}\right) \tag{9}$$

$$\boldsymbol{V}^{p}_{f\alpha\beta,k+1}=\boldsymbol{V}_{f\alpha\beta,k}+\frac{T_s}{C_f}\left(\boldsymbol{i}^{p}_{f\alpha\beta,k+1}-\boldsymbol{i}_{o\alpha\beta,k}\right) \tag{10}$$

where the superscript "p" denotes the predicted value.

Taking into account the inherent one-step delay compensation in FCS-MPC, the predicted value at (k+1)th instant is substituted with the predicted value at (k+2)th instant. Subsequently, the NP voltage balance term is integrated into the cost function as a weighting term. The ultimate form of the cost function can be designed as follows:

$$\begin{aligned}J_0=&\underbrace{\left(V^{*}_{f\alpha,k+2}-V^{p}_{f\alpha,k+2}\right)^2+\left(V^{*}_{f\beta,k+2}-V^{p}_{f\beta,k+2}\right)^2}_{\text{Tracking cost}}\\ &+\lambda\underbrace{\Delta V_{\text{NP},k+2}}_{\text{NP cost}}\end{aligned} \tag{11}$$

where λ is the weighting factor, $\boldsymbol{V}^*_{f\alpha\beta,k+2}$ represents the output voltage reference, which can be calculated using Lagrange interpolation. For the sinusoidal reference, the order "n" should not be less than 2 [18]. Consequently, the reference value of the output voltage in the $\alpha\beta$ system can be expressed as follows:

$$\begin{cases} V^*_{f\alpha,k+2} = 3V^*_{f\alpha,k+1} - 3V^*_{f\alpha,k} + V^*_{f\alpha,k-1} \\ V^*_{f\beta,k+2} = 3V^*_{f\beta,k+1} - 3V^*_{f\beta,k} + V^*_{f\beta,k-1} \end{cases}. \tag{12}$$

Considering the overcurrent protection during actual operation, the overcurrent protection term I_{lim} can be incorporated into the cost function [14]. Finally, the cost function can be expressed as follows:

$$J_1 = J_0 + I_{\text{lim}}$$
$$I_{\text{lim}} = \begin{cases} 0 & \left\| \boldsymbol{i}^p_{f\alpha\beta,k+2} \right\| < I_{\text{up}} \\ \infty & \left\| \boldsymbol{i}^p_{f\alpha\beta,k+2} \right\| \geq I_{\text{up}} \end{cases} \tag{13}$$

where I_{up} represents the upper limit of inductive current.

Each voltage vector corresponds to a specific cost value. Therefore, through rolling optimization, the voltage vector minimizing the cost function is determined and employed for the next switching cycle, which can be expressed as

$$V_{opt} = \arg\text{Min}\left(J_1(i)\right), \quad i = 0, 1 \cdots 26 \ . \tag{14}$$

III. Proposed ESM-PC Algorithm

In this section, a novel ESM-PC is introduced. The traditional FCS-MPC requires the evaluation of the cost value for 27 voltage vectors and adjustment of weighting factors, impacting real-time algorithm performance. To address this challenge, the proposed ESM-PC first dynamically preselects the voltage vectors based on the sliding-mode theory. Then, it eliminates weighting factors by designing VVVs. The specific technical detail is elucidated as follows.

A. *Error Convergence Condition*

The application of sliding-mode theory aims to diminish the pool of candidate voltage vectors and ensure the convergence of output voltage error [34]. To this end, two error functions are initially defined as the difference between the reference voltage and the actual voltage

$$\begin{cases} S_{Vf\alpha} = V^*_{f\alpha,k+2} - V_{f\alpha,k} \\ S_{Vf\beta} = V^*_{f\beta,k+2} - V_{f\beta,k} \end{cases}. \tag{15}$$

For the output voltage to track the reference voltage and ensure error convergence, the above error function must satisfy the Lyapunov stability criterion [9]

$$\begin{cases} S_{Vf\alpha}\dot{S}_{Vf\alpha} < 0 \\ S_{Vf\beta}\dot{S}_{Vf\beta} < 0 \end{cases}. \tag{16}$$

In the discrete model, since the reference voltage is constant during one control cycle [34], the derivative of the error function, based on (9) and (10), can be expressed as follows:

$$\begin{aligned} \dot{S}_{Vf\alpha} &= \frac{d}{dt}\left(V^*_{f\alpha,k+2} - V_{f\alpha,k}\right) \\ &\approx -\frac{T_s}{C_f}\left(i^p_{f\alpha,k+1} - i_{o\alpha,k}\right) \\ &= -\rho[\underbrace{i_{f\alpha\beta,k} - i_{o\alpha,k}}_{I_\alpha} + \delta\left(V_\alpha - V_{f\alpha,k}\right)] \end{aligned} \tag{17}$$

$$\begin{aligned} \dot{S}_{Vf\beta} &= \frac{d}{dt}\left(V^*_{f\beta,k+2} - V_{f\beta,k}\right) \\ &\approx -\frac{T_s}{C_f}\left(i^p_{f\beta,k+1} - i_{o\beta,k}\right) \\ &= -\rho[\underbrace{i_{f\beta,k} - i_{o\beta,k}}_{I_\beta} + \delta\left(V_\beta - V_{f\beta,k}\right)] \end{aligned} \tag{18}$$

where $\rho = T_s/C_f$, $\delta = T_s/L_f$, are constant positive numbers. $\boldsymbol{I}_{\alpha\beta}$ represents the difference between inductor current $\boldsymbol{i}_{f\alpha\beta}$ and output current $\boldsymbol{i}_{o\alpha\beta}$. According to (10), this difference directly influences the change of output voltage $\boldsymbol{V}_{f\alpha\beta}$. Therefore, the relationship between $\boldsymbol{I}_{\alpha\beta}$ and the control domain is further analyzed in the following.

B. *Determination of the Control Domain*

According to (15), (16), (17), and (18), the control domain of the optimal voltage vector can be determined. For better explanation, the case $S_{Vf\alpha} > 0$ and $S_{Vf\beta} < 0$ is taken as an example for analyze without loss of generality.

Then, the α and β components of the candidate voltage vectors should satisfy the following conditions:

$$\begin{cases} V_\alpha > V_{f\alpha,k} + \Psi_\alpha \\ V_\beta < V_{f\beta,k} + \Psi_\beta \end{cases} \tag{19}$$

where $\Psi_\alpha = -I_\alpha/\delta$, $\Psi_\beta = -I_\beta/\delta$.

Therefore, in the space vector diagram, the sampled value of the output voltage at (k)th instant $\boldsymbol{V}_{f\alpha\beta,k}$ is employed as the origin to reconstruct the coordinate system, as depicted by the red arrow in Fig. 3.

There are a total of four possible control domains depending on whether $\boldsymbol{I}_{\alpha\beta}$ is positive or negative. For instance, when $I_\alpha > 0$ and $I_\beta > 0$, the control domain is shown in the yellow area in Fig. 3(a), while the gray area does not satisfy the stability condition of (16), and the remaining cases are illustrated in Fig. 3(b)–(d), respectively.

Considering the inevitable parameter mismatch and external disturbances, Ψ_α and Ψ_β are not strictly determined and can be further expressed as

$$\begin{cases} \Psi'_\alpha = \Psi_\alpha + \sigma \\ \Psi'_\beta = \Psi_\beta + \sigma \end{cases} \tag{20}$$

where $|\sigma| \leq \varepsilon$, is bounded. ε is a constant positive number, which represents the upper bound of the error [12].

C. *Proposed Parallel Optimization Solution Without Considering Excessive* ΔV

If excessive ΔV is not considered, to determine the optimal voltage vector in the control domain obtained in the last section, the conventional approach involves substituting each

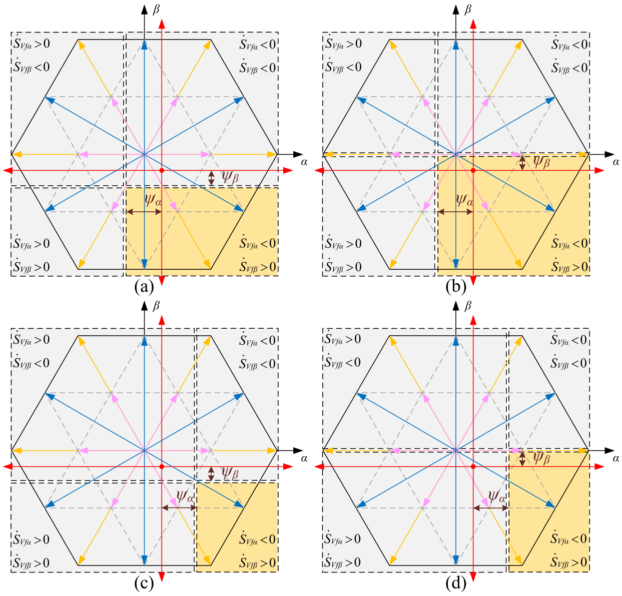


Fig. 3. Control domains under different conditions. (a) $I_\alpha > 0$, $I_\beta > 0$. (b) $I_\alpha > 0, I_\beta < 0$. (c) $I_\alpha < 0, I_\beta > 0$. (d) $I_\alpha < 0, I_\beta < 0$.

voltage vector in the control domain into the cost function (13) and subsequently, identifying the voltage vector that minimizes the cost function through rolling optimization. However, this method imposes a substantial computational burden, especially when the control domain is extensive. To address this issue, this article proposes a parallel optimization strategy, which is explained as follows.

1) Parallel Minimization of the α and β Components: As indicated in (11), the cost function comprises two components: "Tracking cost" and "NP cost". The former is further composed of two parts: 1) the error along the real axis and 2) the error along the imaginary axis, each assigned a weighting factor of 1. Consequently, the minimum cost function for the real axis and imaginary axis can be concurrently determined, and their intersection point constitutes the voltage vector that minimizes the "Tracking cost". The new parallel cost function and optimization procedure can be expressed as follows:

$$\begin{cases} T_\alpha = \left\| V^*_{f\alpha,k+2} - V^p_{f\alpha,k+2} \right\|^2 \\ T_\beta = \left\| V^*_{f\beta,k+2} - V^p_{f\beta,k+2} \right\|^2 \end{cases} \tag{21}$$

$$\begin{cases} V_{\alpha opt} = \arg \mathrm{Min}\left(T_\alpha(i)\right), & i \in \mathbb{C}_\alpha \\ V_{\beta opt} = \arg \mathrm{Min}\left(T_\beta(m)\right), & m \in \mathbb{C}_\beta \end{cases}$$

$$\Rightarrow \boldsymbol{V}_{opt} = V_{\alpha opt} + jV_{\beta opt} \tag{22}$$

where $\mathbb{C}_{\alpha\beta}$ represents control domain. It should be noted that the "NP cost" is not considered here because the weighting term will be eliminated by redundant small voltage vectors in the subsequent analysis.

2) Monotonicity Analysis: In fact, not all α and β components in the control domain should be involved in the optimization, as both cost functions T_α and T_β exhibit monotonicity.

For example, when $S_{Vf\alpha} > 0$, as shown in Fig. 4(a), the α component of the voltage vectors in the control domain always increase $V^p_{f\alpha,k+2}$, and the larger the α component of the voltage vector is, the larger the $V^p_{f\alpha,k+2}$ is. Therefore, when optimizing from the leftmost end of the control domain to the right, the cost function T_α always initially decreases and then increases. Therefore, when the cost value of the latter α component is larger than the former one, the former one can be considered as the $V_{\alpha opt}$.

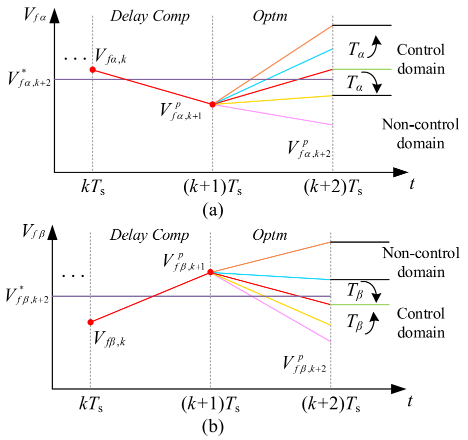


Fig. 4. Monotonicity of the cost functions. (a) $S_{Vf\alpha} > 0$. (b) $S_{Vf\beta} < 0$.

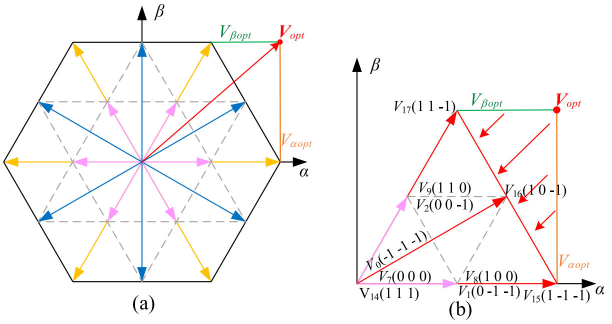


Fig. 5. Constraint analysis. (a) Nonexistent optimal voltage vector. (b) Illustrative example.

Similarly, when $S_{Vf\beta} < 0$, as shown in Fig. 4(b), the cost function T_β also exhibits similar characteristics when optimizing from the top of the control domain downwards.

3) Constraint: Since the space vector diagram is not a rectangle, the voltage vector corresponding to the intersection of the $V_{\alpha opt}$ and $V_{\beta opt}$ does not always exist. As shown in Fig. 5(a), $\boldsymbol{V}_{opt}$ falls outside the space vector diagram, which does not exist, so further consideration of constraints is required.

According to the monotonicity analysis above, it can be inferred that the optimal voltage vector must reside at the boundary of the space vector diagram. Therefore, as shown in Fig. 5(b), it is necessary to further evaluate the cost values of the three voltage vectors V_{17}, V_{16}, and V_{15}. It should be noted that the overall cost function of the α and β components needs to be evaluated, and it can be expressed as follows:

$$T_{\alpha\beta} = T_\alpha + T_\beta. \tag{23}$$

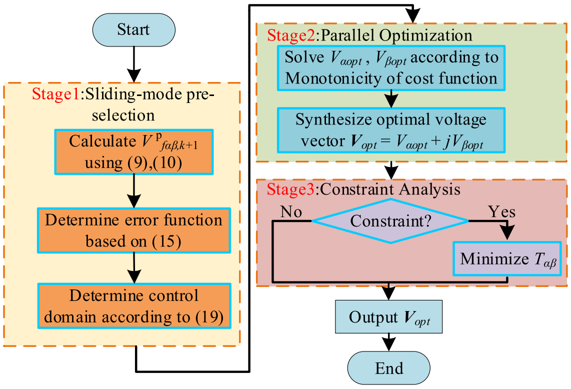
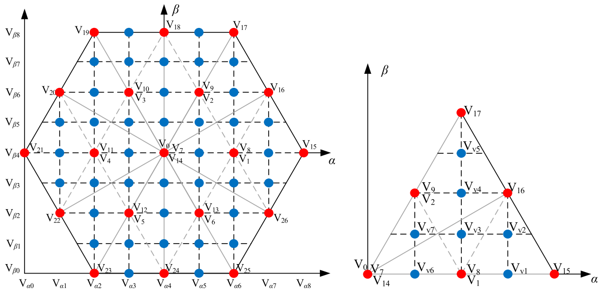


Fig. 6. Flowchart of the proposed parallel optimization algorithm.



(a) (b)

Fig. 7. Proposed voltage vector distribution diagram. (a) Real voltage vectors and VVVs. (b) Voltage vectors in large sector I.

In summary, the implementation process of the proposed parallel optimization strategy based on sliding-mode theory is depicted in Fig. 6.

Considering the delay compensation of MPC, the values of the output voltage and inductive current at (k)th instant in the above analysis can be replaced by the predicted values at (k+1)th instant. Since the output current is a slow-changing process with respect to the inductor current, it can be approximated by the value at (k)th instant [14].

D. VVVs and NP Balancing

According to the above analysis, different from the traditional method, the optimization strategy proposed in this article does not depend on the number of voltage vectors, but on the number of α and β components. As shown in Fig. 2, the number of α and β components in the real space vector diagram is only 5, which will bring large output ripple.

1) VVVs: It is feasible to expand the number of candidates for the α and β components by setting the VVVs.

In this article, one candidate component is added to the midpoint of each pair two α or β components. Simultaneously, the VVV is positioned at the intersection point of the α and β components, resulting in an expansion of candidate α or β components from 5 to 9. As depicted in Fig. 7(a), the red dots signify the real voltage vectors, while the blue dots represent the generated VVVs.

It is worth mentioning that further augmenting the candidate components can also further improve the control performance.

TABLE I
CLASSIFICATION OF REDUNDANT SMALL VOLTAGE VECTORS

Type	i_o	V_p&V_n	Small voltage vectors
P-type	$i_o < 0$	V_n increase V_p decrease	(1 0 0) (1 1 0) (0 1 0) (0 1 1) (0 0 1) (1 0 1)
N-type	$i_o > 0$	V_p increase V_n decrease	(0 -1 -1) (0 0 -1) (-1 0 -1) (-1 0 0) (-1 -1 0) (0 -1 0)

However, it is essential to acknowledge that such augmentation comes at the cost of an increased computational burden.

2) NP Voltage Balance: For 3P-3L VSIs, NP voltage balance is also crucial. Since the proposed optimization method only considers the "Tracking cost", if the "NP cost" can be eliminated from the cost function, $\boldsymbol{V}_{opt}$ can be used as the optimal voltage vector.

The NP voltage has been integrated into the system model, associating its variation with the NP current i_{o}. Consequently, the impact on the NP voltage is confined to the redundant small voltage vectors [28], which can be categorized as P-type and N-type according to i_{o}, as outlined in Table I. It is essential to note that the two small voltage vectors at each node exert opposing effects on the NP voltage, while maintaining a consistent influence on the output voltage [29].

In fact, the VVVs can be defined as the composition of the real voltage vectors, which can be expressed as follows:

$$\begin{cases} V_{Vz} = \frac{1}{T_s} \sum\limits_{i=1}^{N} t_i V_i \\ T_s = \sum\limits_{i=1}^{N} t_i \end{cases} \tag{24}$$

where V_i denotes the real voltage vector and t_i denotes the operation time of the corresponding real voltage vector.

When V_{Vz} contains at least one small voltage vector, the V_{Vz} can select different output modes according to the NP voltage. For example, as shown in Fig. 7(b), V_{V3} can be expressed as

$$V_{V3} = \underbrace{\frac{1}{4}\left(V_9 + V_{16} + 2V_8\right)}_{textP-Type} = \underbrace{\frac{1}{4}\left(V_2 + V_{16} + 2V_1\right)}_{textN-Type}. \tag{25}$$

When synthesized with V_9, V_{16} and V_8, V_{V3} belongs to the P-type. Conversely, when synthesized with V_2, V_{16}, and V_1, it belongs to the N-type. This principle extends to all other candidate voltage vectors that incorporate small voltage vectors.

In summary, the introduction of the VVVs achieves a dual objective: reduction of output ripple and elimination of the weighting factor in the cost function.

E. Determination of Optimal Voltage Vector Considering Excessive ΔV

The determination of the optimal voltage vector illustrated in Fig. 6 overlooks the potential for excessive ΔV. Therefore, a constraint analysis on excessive ΔV will be further conducted in this section.

First of all, since the VVVs are synthesized from adjacent voltage vectors, applying either the virtual or real voltage vector in one control cycle will not cause excessive ΔV. During the adjacent control cycle, the optimal voltage vector should either

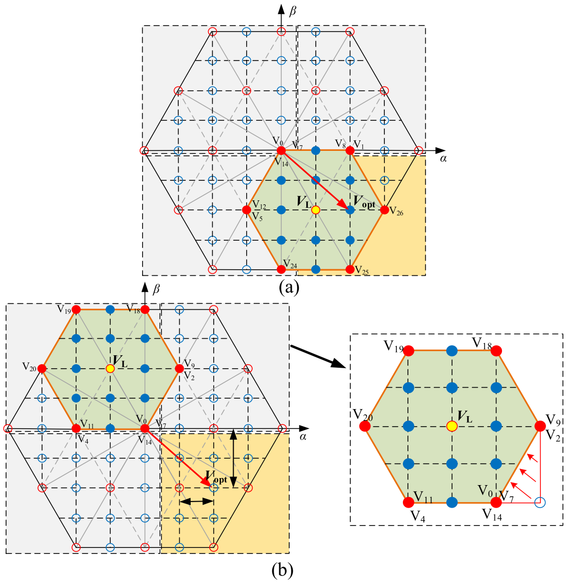


Fig. 8. Constraint on excessive ΔV. (a) V_{opt} is connected to V_{L}. (b) V_{opt} is not connected to V_{L}.

connect to or be the same as the voltage vector utilized in the preceding control cycle. [25].

As shown in Fig. 8, V_L represents the voltage vector applied in the preceding control cycle, while V_{opt} represents the optimal voltage vector obtained through the parallel optimization solution proposed in this article, which minimizes the tracking error. Based on the above analysis, it is evident that the voltage vectors that avoid excessive ΔV should lie within the green area depicted in Fig. 8, denoted by solid points. Furthermore, their α and β components must satisfy the following conditions:

$$\begin{cases} V_{\Delta V-\alpha} \in \left[V_{L-\alpha} - \frac{V_{dc}}{3}, V_{L-\alpha} + \frac{V_{dc}}{3}\right] \\ V_{\Delta V-\beta} \in \left[V_{L-\beta} - \frac{\sqrt{3}}{6}V_{dc}, V_{L-\beta} + \frac{\sqrt{3}}{6}V_{dc}\right] \end{cases}$$
$$\text{s.t.} \begin{cases} V_{L-\alpha} - \frac{V_{dc}}{3} \geq -\frac{2}{3}V_{dc} \qquad V_{L-\alpha} + \frac{V_{dc}}{3} \leq \frac{2}{3}V_{dc} \\ V_{L-\beta} - \frac{\sqrt{3}}{6}V_{dc} \geq -\frac{\sqrt{3}}{3}V_{dc} \quad V_{L-\beta} + \frac{\sqrt{3}}{6}V_{dc} \leq \frac{\sqrt{3}}{3}V_{dc} \end{cases} \tag{26}$$

$V_{\Delta V-\alpha}$ and $V_{\Delta V-\beta}$ cannot be on the border at the same time.

Then, the relationship between V_L and V_{opt} can be divided into two categories as follows.

1) If the α and β components of V_{opt} satisfy formula (26), then V_{opt} will not introduce excessive ΔV, as demonstrated in Fig. 8(a). In such a case, V_{opt} will be selected as the optimal voltage vector for the final output.
2) If the α and β components of V_{opt} fail to satisfy formula (26), the control system should prioritize avoiding excessive ΔV. According to the monotonicity, the solid point nearest to V_{opt} should be selected as the final output voltage vector, as shown in Fig. 8(b). Similarly, the α and β components nearest to V_{opt} in the green area can still be identified, respectively. The optimization and constraint procedures are similar to those in Section III-C and will not be reiterated here. Although the selected output voltage vector lies outside the control domain, the resulting tracking error remains controllable, constrained by the dc voltage.

The analysis above suggests that constraining excessive ΔV can be viewed as a simplified version of the parallel optimization method proposed in this article, thereby reducing algorithmic complexity.

TABLE II
Parameters of the System

Variable	Description	Numeric Value
V_{dc}	Dc voltage	200[V]
T_s	Sampling and control period	62.5[us]
C_1, C_2	Dc-link Capacitors	500[uF]
$R_{a,b,c}$	Linear load	30[Ω]
L_f	Filter inductance	3[mH]
C_f	Filter capacitor	20[uF]
f	Rated output frequency	50[Hz]

F. Comparison and Extension

An extended model predictive-sliding mode control (EMP-SMC) based on sliding-mode theory preselection has been proposed in [34]. Specifically, the space vector diagram is divided into 12 sectors, and the voltage vector to be evaluated is preassigned based on the location of the grid voltage. However, the preselection scheme proposed in this article reconstructs the coordinate system according to the output voltage and then determines the control domain. In comparison with EMP-SMC in [34], the optimization process of the proposed method is dynamic and more flexible. Additionally, the proposed parallel optimization strategy can further reduce computational complexity.

It is worth mentioning that, to further enhance robustness, the proposed method can be augmented with well-established robust optimization strategies, such as parameter identification and gradient methods [30], [31], [32], [33].

G. System Overall Control

Based on the preceding analysis, the complete control block diagram of the ESM-PC proposed in this article is illustrated in Fig. 9.

IV. Experimental Results

Experiments were conducted to validate the superiority and adaptability of the proposed ESM-PC in this article. As shown in Fig. 10, a T-type 3P-3L VSI experiment platform was built based on Texas Instruments DSP chip (TMS320F28374S), where inductor current ($i_{fa,b,c}$) and output current ($i_{oa,b,c}$) are sampled by VAC current sensors, and output voltage ($V_{oa,b,c}$) and NP voltage ($V_{p,n}$) are sampled by LEM voltage sensors. The DSP executed control algorithms. Essential parameters are detailed in Table II.

At the same time, four algorithms are implemented and compared on the experimental platform, each defined as follows.

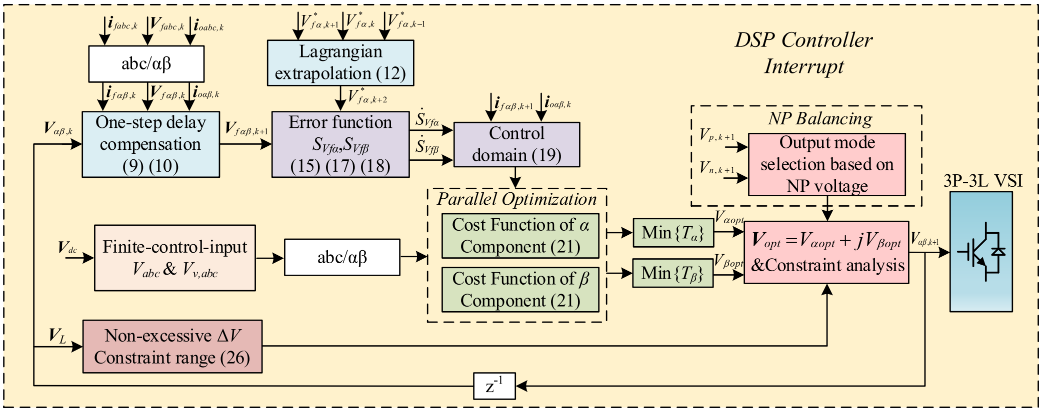


Fig. 9. Control block diagram of the proposed ESM-PC.

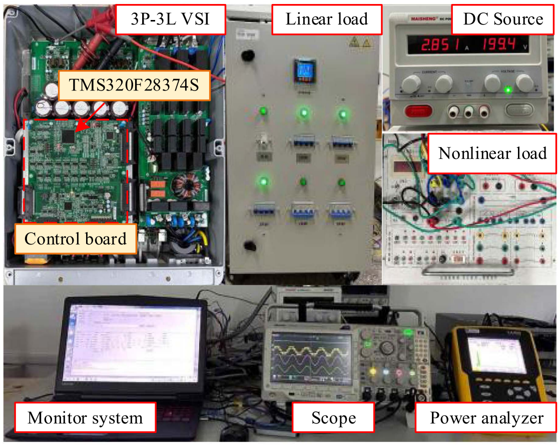


Fig. 10. System experiment platform.

Traditional PID: The traditional PID control follows the classical double-loop control structure, with the outer loop controlling the capacitor voltage and the inner loop regulating the inductor current. The balance of the NP voltage is achieved by injecting zero sequence voltage components.

Traditional MPC: The MPC algorithm proposed in [15] is regarded as the traditional MPC. The cost function is designed as (11), the weighting factor is used to achieve NP voltage balance, and the optimal voltage vector is obtained by evaluating 27 voltage vectors.

DB-MPC: The MPC algorithm proposed in [18] applies three voltage vectors in one switching cycle, and the operation time inversely proportional to the cost value. The adjustment of redundant small voltage vectors is performed to eliminate the weighting factors, and computational efficiency is optimized through the integration of DB control.

ESM-PC: The proposed MPC algorithm.

A. *Execution Time*

First of all, the time complexity of the four methods was compared using a DSP-TMS320F28374S with a crystal frequency of 200 MHz and a sampling period of 62.5 μs.

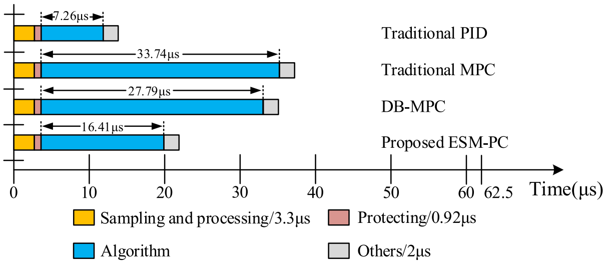


Fig. 11. Comparison of time complexity of different algorithms.

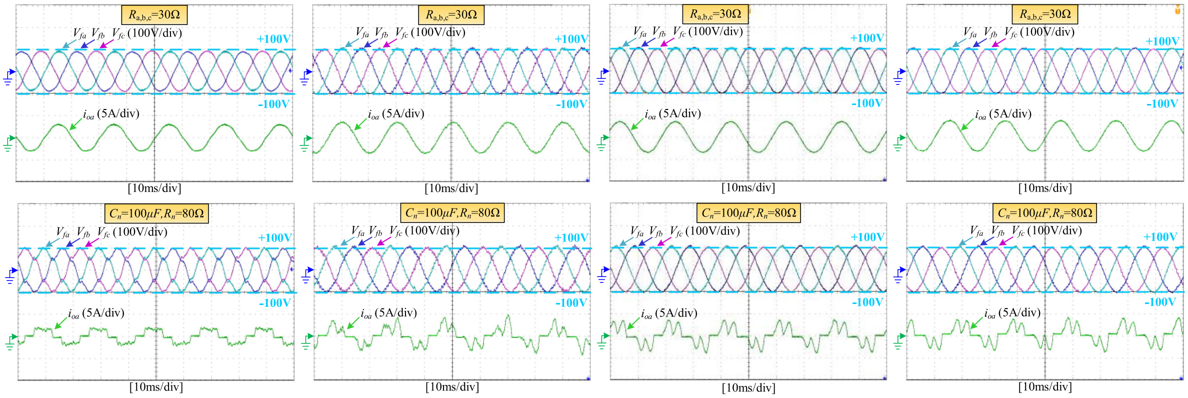
Specifically, the execution time of A/D conversion, system protection and other tasks is about 6.22 μs, and the remaining is the execution time of algorithms. Notably, in the proposed method, the number of voltage vectors to be evaluated in each control cycle is variable. When evaluating the computation time, the most complex condition is considered, involving the evaluation of cost values for all α and β components, along with constrained cases.

The experimental results are depicted in Fig. 11. The traditional PID control, with its simple structure, exhibits a computation time of only 7.26 μs. For MPC algorithms, it is evident that the computation time for traditional MPC is 33.74 μs, for DB-MPC is 27.79 μs, and for the proposed ESM-PC is only 16.41 μs. In comparison to traditional MPC, the computation time is reduced by approximately 51.3%, and compared with DB-MPC, the computation time is reduced by about 40.9%.

The experimental results demonstrate that the proposed parallel optimization strategy significantly reduces the computational burden.

B. *Steady-State Performance Evaluation*

In Fig. 12, the steady-state experimental waveforms of the four algorithms under both linear and nonlinear loads are depicted. The waveforms encompass the three-phase output voltage ($\boldsymbol{V}_{fa,b,c}$) and the phase-A output current (i_{oa}). Notably, due to the linear nature of traditional PID control, it exhibits significant distortion when confronted with nonlinear loads. In contrast, MPC-based methods effectively track the reference



(a) (b) (c) (d)

Fig. 12. Steady-state experimental waveforms with linear loads and nonlinear loads. (a) Traditional PID. (b) Traditional MPC. (c) DB-MPC. (d) Proposed ESM-PC.

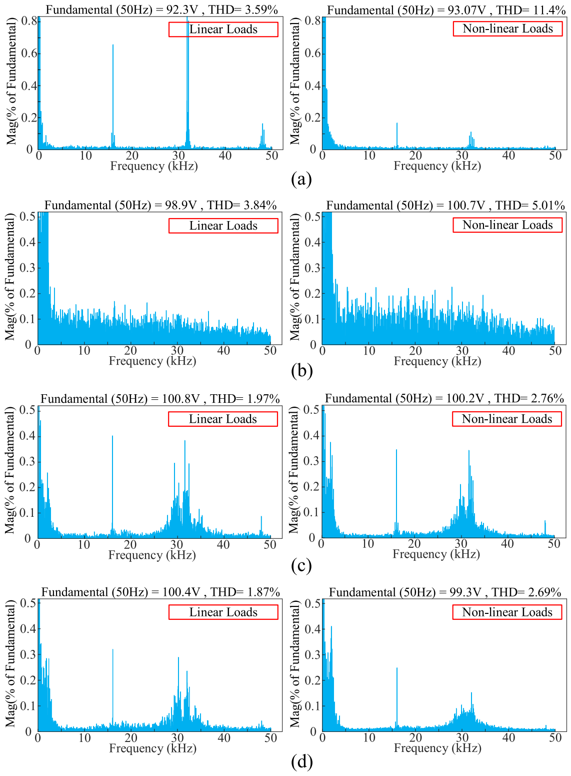


Fig. 13. FFT analysis of steady-state experiments. (a) Traditional PID. (b) Traditional MPC. (c) DB-MPC. (d) Proposed ESM-PC.

voltage, indicating their capability to provide sinusoidal voltage output to loads more stably than traditional PID control.

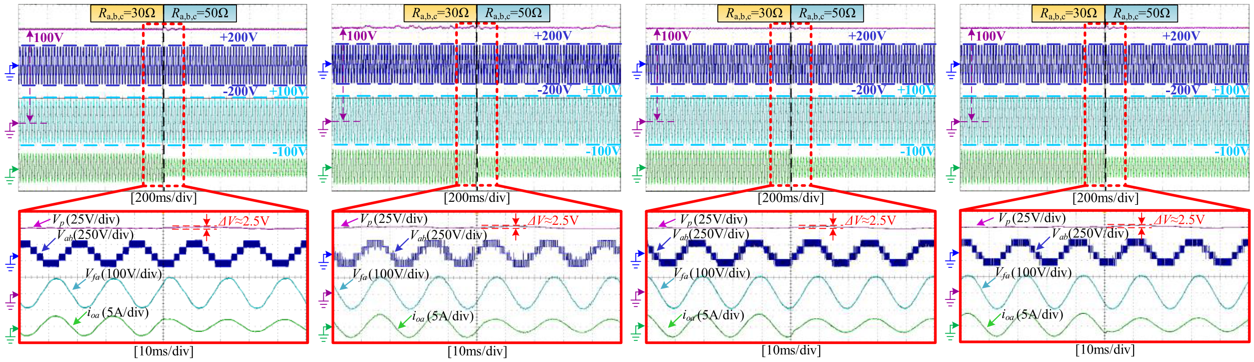
Furthermore, Fig. 13 presents the harmonic spectra of the output voltage, generated using MATLAB/Simulink with experimental data acquired from the oscilloscope. The experimental results reveal that, regardless of the linear or nonlinear loads, the proposed algorithm exhibits the lowest total harmonic distortion (THD). This suggests that the proposed method attains optimal steady-state performance when compared to traditional PID, traditional MPC and DB-MPC. Particularly, the traditional MPC, with a single switching action per control cycle, exhibits a scattered spectrum distribution. In contrast, the other three methods maintain a constant switching frequency, offering advantages for filter design and EMI suppression.

C. Dynamic Performance Evaluation

To evaluate the dynamic performance of the proposed ESM-PC, Figs. 14 and 15 illustrate the waveforms of phase-A output voltage (V_{fa}), phase-A output current (i_{oa}), inverter output line voltage (V_{ab}), and the upper capacitor voltage (V_p) of the four methods, respectively.

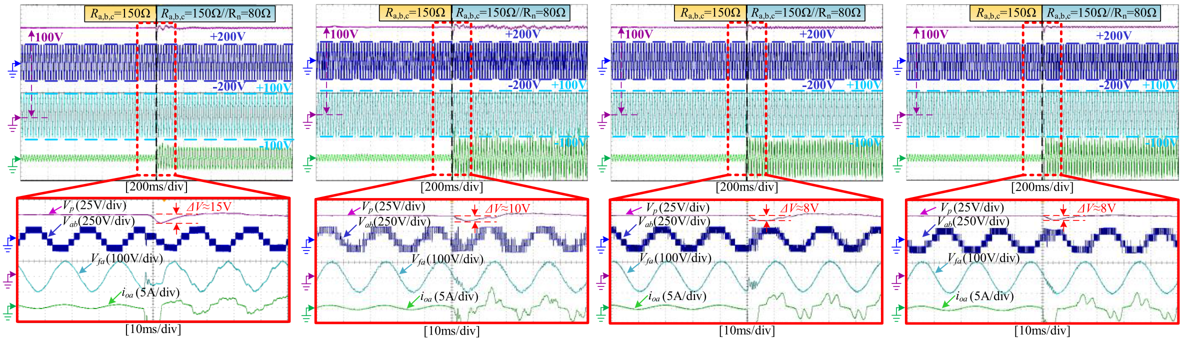
In Fig. 14, the dynamic waveform illustrates linear loads step from 30 Ω to 50 Ω. The four methods exhibit similar dynamic characteristics, with the output voltage remaining almost unchanged. Simultaneously, at the step instant, the NP voltage fluctuations for all four methods are approximately 2.5 V. This observation suggests that the four methods demonstrate a superior dynamic response to changes in linear loads.

Additionally, in Fig. 15, the waveforms depict the transition from linear loads to both linear and nonlinear loads in parallel. Similar to the results under linear loads stepping, all four methods maintain a constant voltage output. However, compared with the MPC-based methods, the output voltage waveform of traditional PID control exhibits greater distortion and longer recovery time. Furthermore, due to the restriction of excessive ΔV by the proposed ESM-PC, the waveform of the proposed method appears smoother at the moment of switching compared to the other three methods. The experimental waveforms of phase and line-to-line voltage jumps at switching transient are shown in Fig. 16. It can be seen that both traditional MPC and DB-MPC exhibit excessive ΔV, whereas the proposed ESM-PC effectively suppresses the excessive ΔV. In terms of NP voltage balance, the upper capacitor voltage pulsation for the traditional PID control is approximately 15 V, for the traditional MPC is approximately 10 V, while for DB-MPC and the proposed ESM-PC is around 8 V. Consequently, the proposed ESM-PC and DB-MPC exhibit better suppression of NP voltage fluctuation when the load is disrupted.



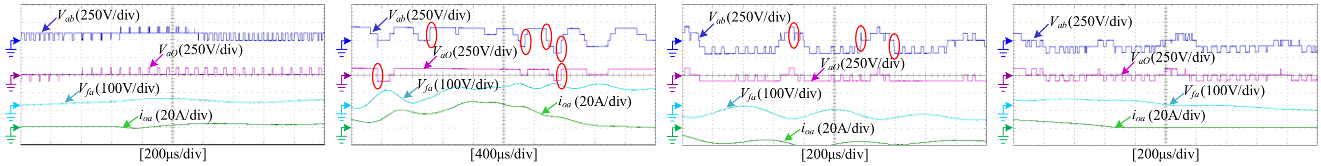
(a) (b) (c) (d)

Fig. 14. Dynamic experimental waveforms with linear loads stepped from 30 Ω to 50 Ω. (a) Traditional PID. (b) Traditional MPC. (c) DB-MPC. (d) Proposed ESM-PC.



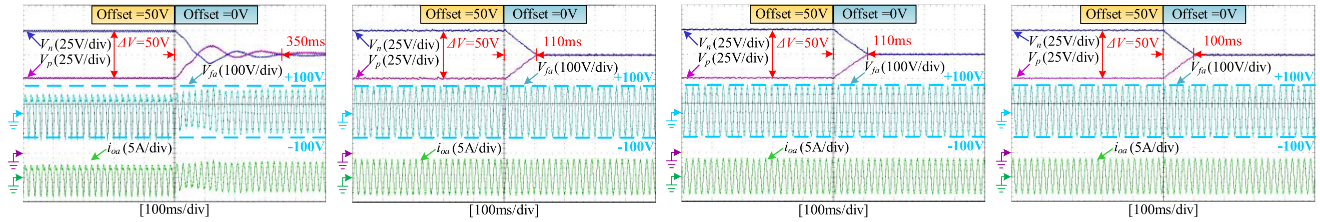
(a) (b) (c) (d)

Fig. 15. Dynamic experimental waveform from linear loads to linear loads in parallel with nonlinear loads. (a) Traditional PID. (b) Traditional MPC. (c) DB-MPC. (d) Proposed ESM-PC.



(a) (b) (c) (d)

Fig. 16. Experimental waveforms of phase and line-to-line voltage jumps at switching transient. (a) Traditional PID. (b) Traditional MPC. (c) DB-MPC. (d) Proposed ESM-PC.



(a) (b) (c) (d)

Fig. 17. Experimental waveforms of NP voltage balance. (a) Traditional PID. (b) Traditional MPC. (c) DB-MPC. (d) Proposed ESM-PC.

D. NP Voltage Balancing Experiments

To further evaluate the NP voltage balancing capabilities of the four methods, a 50 V dc OFFSET is initially added to the sampling signal to simulate the NP voltage imbalance condition. Subsequently, the OFFSET is removed, and the recovery time for balance among the four algorithms is compared. The experimental results are shown in Fig. 17.

From the experimental results, it is evident that the recovery time of NP voltage adjusted by the PID control is about

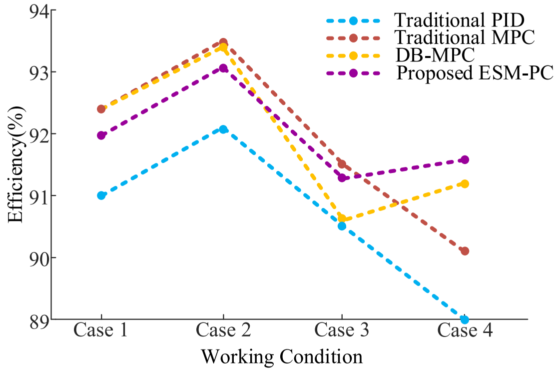


Fig. 18. System efficiency under different working conditions.

350 ms, and the output voltage waveform experiences significant distortion when the NP voltage is unbalanced. In contrast, for MPC-based methods, the recovery time is better than that of traditional PID. The traditional MPC and DB-MPC exhibit a balance recovery time of approximately 110 ms, while the proposed method achieves a recovery time of around 100 ms. This indicates a slightly better performance compared to the first two methods. Thus, it can be concluded that ESM-PC demonstrates superior NP voltage balancing ability compared to the traditional methods.

E. System Efficiency Evaluation

To study the system efficiency, the four algorithms are compared under various working conditions. The system efficiency is defined as

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \tag{27}$$

where P_{out} is the output power of the ac side and P_{in} is the input power of the dc side.

Four different working conditions are defined as follows.

Case 1: Linear loads with $R_{a,b,c} = 50\ \Omega$.
Case 2: Linear loads with $R_{a,b,c} = 30\ \Omega$.
Case 3: Nonlinear loads with $C_n = 100\ \mu F, R_n = 80\ \Omega$.
Case 4: Linear loads paralleled with non-linear loads with $R_{a,b,c} = 150\ \Omega, C_n = 100\ \mu F, R_n = 80\ \Omega$.

The experimental results measured by the power analyzer are shown in Fig. 18. It can be observed that the efficiency of the MPC-based methods is consistently above 90% across all four working conditions, surpassing the efficiency of the traditional PID control. Consequently, the system efficiency of the proposed method in this article is commendable.

F. Model Parameter Mismatch Experiments

In practice, model parameter mismatch is inevitable due to various disturbances. In this section, the parameter sensitivity of three MPC methods is evaluated by changing the inductance L_f and capacitance C_f, where the change rate ΔL and ΔC are defined as

$$\begin{cases} \Delta L = \frac{\tilde{L} - L_r}{L_r} \times 100\% \\ \Delta C = \frac{\tilde{C} - C_r}{C_r} \times 100\% \end{cases} \tag{28}$$

where $\tilde{L}$ and $\tilde{C}$ are the inductance and capacitance values used in the experiments, respectively. L_r and C_r are the real inductance and capacitance values, respectively.

TABLE III
Analysis of Parameters Sensitivity

Mismatch	Traditional MPC	DB-MPC	Proposed ESM-PC
	THD	THD	THD
——	3.84%	1.97%	1.87%
ΔL = 50%,ΔC = 0%	6.03%	3.26%	2.68%
ΔL = −50%,ΔC = 0%	4.37%	2.59%	2.24%
ΔL = 0%,ΔC = 50%	4.76%	2.72%	2.48%
ΔL = 0%,ΔC = −50%	3.47%	2.06%	1.94%

The experimental results, as presented in Table III, indicate that the traditional MPC exhibits the weakest model mismatch capability compared to DB-MPC and the proposed ESM-PC. However, even in the presence of parameter mismatches, the proposed ESM-PC still demonstrates the lowest THD, showcasing superior robustness.

V. Conclusion

This article develops a novel ESM-PC scheme for 3P-3L VSIs with *LC*-filter. The performance of the proposed ESM-PC is evaluated by experiment and compared with traditional MPC and existing optimization algorithms. Based on the theoretical analysis and experimental findings, the following conclusions can be drawn.

1) The proposed ESM-PC exhibits superior steady-state performance, showcasing a THD of less than 3% under both linear and nonlinear loads. Compared with the traditional MPC, ESM-PC maintains a constant switching frequency.
2) The proposed preselection scheme based on sliding-mode theory fully considers the dynamic characteristics of the output voltage and has good robustness.
3) The proposed VVVs design method is simple and easy expandable, which effectively suppresses the output ripples. Combined with redundant small voltage vectors, the weighting factor can be eliminated, thereby reducing the complexity of the algorithm.
4) Compared with the traditional MPC, the proposed parallel optimization strategy enhances computational efficiency, reducing computation time by at least 51.3%.

Thus, the proposed ESM-PC shows promising and practical applications in multilevel inverters.

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