A Dynamic Current Sharing Model of Multichip Parallel SiC MOSFETs Considering Layout-Dominated Mutual Inductance Coupling

Zexiang Zheng, Cai Chen, *Member, IEEE*, Jianwei Lv, Yiyang Yan, Jiaxin Liu, and Yong Kang, *Fellow, IEEE*

***Abstract*—Dynamic current imbalance of parallel SiC MOSFETs can lead to uneven losses and even thermal runaway. Unbalanced parasitic parameters dominated by layout are one of the main causes of unbalanced dynamic currents. However, a current sharing model that comprehensively considers all inductances and mutual inductances is still lacking. Aiming at the problem, a quantitative model is proposed to analyze the dynamic current sharing mechanism and performance considering all inductances and mutual inductances. The phenomenon that the high-side dynamic currents are more balanced than the low-side currents is explained from a new perspective in a baseline module. Furthermore, more accurate judgment coefficients (JCs) than existing models are obtained to evaluate the dynamic current sharing performance. When JCs = 0, balanced currents are achieved. The connection points of bonding wires are adjusted to validate the model through simulation and experiments, and this method yields better results due to the consideration of mutual inductance coupling. Finally, to further describe the contribution of the model, a model-based layout optimization by adjusting mutual inductances is discussed and presented.**

***Index Terms*—Dynamic current sharing model, multichip sic power modules, mutual inductance coupling, package layout.**

I. Introduction

RECENTLY, silicon carbide (SiC) MOSFETs have been widely used in high-power applications such as electric vehicles and electrical aircraft due to higher switching speed, operating temperature, and voltage than Si IGBT. This is mainly due to the high critical electric field strength, band gap energy, electron velocity, melting point, and thermal conductivity of SiC material [1], [2], [3], [4], [5]. However, limited by the manufacturing costs and the thermomechanical stress of SiC dies, the effective area of the single die is relatively small [6]. The rated currents of most commercial 1200 V SiC MOSFET bare dies are below 150 A [7]. Therefore, SiC MOSFETs are often paralleled in power modules to enhance the current capacity [8].

However, unbalanced parameters of the paralleled chips and the unbalanced parasitic inductances can cause unbalanced currents during the switching transient. The dynamic current imbalance will lead to uneven power loss, further leading to uneven junction temperatures on paralleled chips [1]. The chips with larger transient currents have higher junction temperatures. The threshold voltage (V_{th}) of SiC dies decreases with the increase in junction temperature leading to a larger dynamic current, which in turn increases the losses of this chip. It may eventually lead to thermal runaway of the power module [9]. Therefore, it is necessary to investigate the dynamic current sharing mechanism of multichip power modules. It has a guiding significance for researching the dynamic current balancing method.

The circuit of paralleled SiC MOSFETs can be divided into non-Kelvin connection and Kelvin connection according to the connection mode of the driving loop. The paralleled SiC MOSFETs with Kelvin connection is a popular method to fully exploit the advantages of high switching speed and low switching losses of SiC MOSFETs [10], [11], [12]. Much research investigated the dynamic current sharing mechanism in the Kelvin-connected power module [9], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. The dynamic current imbalance caused by unbalanced parameters of chips with Kelvin connection was investigated in [13] and [14]. They reveal that mismatched V_{th} of paralleled SiC MOSFETs can cause unbalanced dynamic currents. Meanwhile, the influence of unbalanced parasitic inductances with Kelvin connection on current sharing was analyzed. Zhao et al. [15] analyzed the effects of drain influence point, gate influence point, auxiliary source influence point, and power source influence point (PSCP) on transient current imbalance. It shows that the PSCP significantly influences the transient current imbalance. In [9], [12], [16], [17], [18], [19], [20], [21], and [22], the current sharing mechanism due to asymmetric layout and different junction temperatures under the Kelvin connection was analyzed. It is concluded that the matching degree of the power source parasitic inductances is the main factor affecting the dynamic current sharing performance. Zeng et al. [23] and [24] proposed general mathematical and graphical models to reveal the current sharing mechanism affected by networked parasitic impedances. Some general design guidelines for the multichip power module are

Manuscript received 3 April 2024; accepted 19 May 2024. Date of publication 24 May 2024; date of current version 16 July 2024. This work was supported by the National Natural Science Foundation of China under Grant 52077094. Recommended for publication by Associate Editor J. Popovic-Gerber. *(Corresponding author: Cai Chen.)*

The authors are with the State Key Laboratory of High Density Electrical Energy Conversion, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: zzx_huster@hust.edu.cn; caichen@hust.edu.cn; jianweil@hust.edu.cn; yanyiyang@hust.edu.cn; liujx711@hust.edu.cn; ykang@hust.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3404969.

Digital Object Identifier 10.1109/TPEL.2024.3404969

presented. In [25], in-depth mathematical models are created to reveal the electrothermal mechanisms of the imbalance currents considering device parameters, parasitic inductances, and junction temperatures.

In addition, the judgment conditions for dynamic current balance were researched in multichip power modules [19], [24], [26], [27], [28]. In [19], the current balancing equation considering the power source self-inductances among four paralleled SiC MOSFETs was derived. In [24], based on the matrices of parasitic impedances, common coefficients are proposed to assess the current sharing performance. Nondiagonal elements of the proposed parasitic matrices should be symmetric to balance the coupling of loops, and diagonal elements should be equal to guarantee balance loops. Zhao et al. [26] obtained the judgment basis of the dynamic current balance considering power source, drive source, and gate parasitic inductances. Lv et al. [27] revealed the key parameter affecting dynamic current sharing. The value of the key parameter determines the degree of dynamic current balance of paralleled chips. Wang et al. [28] showed a Cu clip-bonding method for current balancing. A current sharing judgment equation is derived and used as the optimizing target for clip design.

All the research above is based on the impact of self-inductances on the dynamic current sharing performance, neglecting the impact of the mutual inductance coupling. In some layouts, the mutual inductance coupling among power loops and between power loops and driving loops can cause a non-negligible impact on the dynamic current sharing performance [26], [29], [30], [31]. Zhao et el. [26] and Yan et al. [29] pointed out that the mutual inductances between the power source branches affect the dynamic current sharing. Zhao [30] revealed that the mutual inductances between the power source branches and the mutual inductances between the drain and source branches can affect the current sharing performance. However, the above research ignores mutual inductances between the power loops and the drive loops. In [31], two dynamic current balancing equations considering the mutual inductances between the paralleled branches of the high-side MOSFETs were proposed. However, the mutual inductances between switches on different sides and the unbalanced mutual inductances between parallel branches are ignored.

In general, there are still several issues that need to be addressed.

1) Some important mutual inductance coupling is ignored, leading to model accuracy issues.
2) Moreover, existing models that consider mutual inductance coupling are mainly used to analyze several layouts qualitatively, lacking a more quantitative model.
3) The mechanism of the influence of mutual inductance coupling on dynamic current sharing performance is not clear.
4) How to specifically use a multivariable model that considers mutual inductance coupling to optimize the dynamic current sharing performance has not yet been solved.

In response to the above issues, the article further researches the dynamic current mechanism and more accurately guides dynamic current sharing design. The innovation and contributions of the article are as follows.

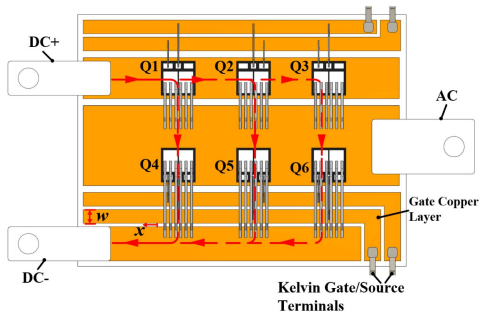

Fig. 1. Block diagram of the baseline power module.

1) A dynamic current sharing quantitative model is established considering all inductances and mutual inductances. The mechanism of the effects of unbalanced self-inductances and mutual inductances is analyzed.
2) Furthermore, a quantitative evaluation index with higher accuracy and applicability than existing models is proposed. Subsequently, the high accuracy and linearity of the quantitative model are verified by adjusting the connection points of bonding wires, and the adjustment optimization achieves better results compared to previous research.
3) Finally, to further describe the contribution of the model, a model-based quantitative layout optimization and an optimization idea by adjusting mutual inductances are demonstrated and discussed, which can guide more current sharing optimization designs in future works.

The rest of this article is organized as follows. In Section II, the impact of mutual inductance coupling on dynamic current sharing performance is introduced first through the phenomenon that unbalanced high-side inductances lead to balanced high-side dynamic currents. In Section III, an analytical model was established to effectively explain this phenomenon by considering all self-inductances and mutual inductances. In Sections IV–VI, the proposed model is verified by adjusting the connection points of bonding wires and compared with an existing model. In Section VII, a model-based layout optimization is presented to improve the current sharing performance by adjusting mutual inductance coupling. Finally, Section VIII concludes this article.

II. Baseline Module Structure and Dynamic Current Sharing Analysis

The baseline SiC power module is shown in Fig. 1, whose layout and terminals are similar to 1200 V/300 A full-SiC EconoDUAL power modules from ROHM [32]. For the convenience of analysis, three 1200 V/136 A SiC MOSFETs (S4651 from ROHM) are paralleled in each switch to analyze the dynamic current sharing. The blocking characteristics of the body diode of SiC MOSFETs are very close to the SiC Schottky barrier diode [33]. Therefore, there is no need for additional paralleled freewheeling diodes. The high-side SiC MOSFETs are denoted as Q1–Q3, and the low-side SiC MOSFETs are denoted as Q4–Q6.

First, the parasitic inductance network, including various self-inductances and mutual inductances at 20 MHz of the baseline

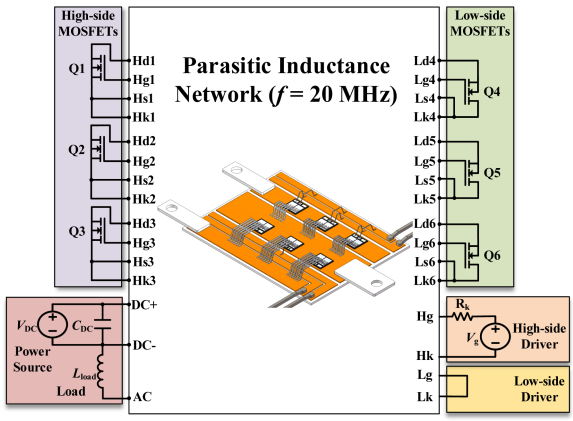

Fig. 2. Electromagnetic coupling simulation topology for high-side MOSFETs of the baseline module based on ANSYS Q3D and LTSIPCE.

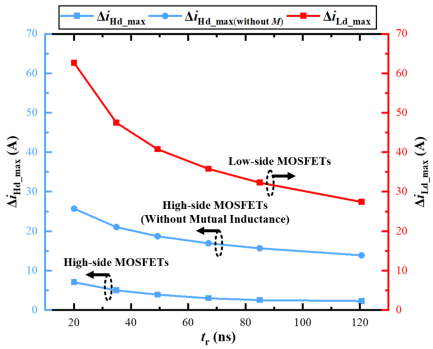

Fig. 3. Maximum current difference of high-side MOSFETs, low-side MOSFETs, and high-side MOSFETs without mutual inductance under different switching times.

module, is extracted by ANSYS Q3D Extractors. Based on the parasitic inductance network, LTSIPCE is used to simulate the dynamic current of the high-side and low-side MOSFETs under 180 A I_{load}. The electromagnetic coupling simulation topology for the high-side MOSFETs of the baseline module is shown in Fig. 2.

The comparison of the current imbalance degree between the high side and the low side under different switching times is shown in Fig. 3. It shows that under different switching speeds, the current imbalance degree on the low side is always much larger than that on the high side. Specifically, under the same switching time, the comparison of high-side and low-side transient currents is shown in Fig. 4. The maximum dynamic current difference between Q1, Q2, and Q3 is $\Delta i_{1\_2} = i_{\mathrm{d1}} - i_{\mathrm{d2}} =$ 2.32 A. However, the maximum difference between Q4, Q5, and Q6 is $\Delta i_{4\_6} = i_{\mathrm{d4}} - i_{\mathrm{d6}} = 27.42$ A, which is 11.8 times that of the high side. The maximum difference of the power source self-inductances between Q1–Q3 is 1.82 nH, and the maximum difference value between Q4–Q6 is 4.94 nH, which is 2.7 times that of the high side. With the same order of magnitude difference in source inductances, the current imbalance degree between the high side and the low side is hugely different. Unbalanced high-side source inductances cause balanced high-side dynamic

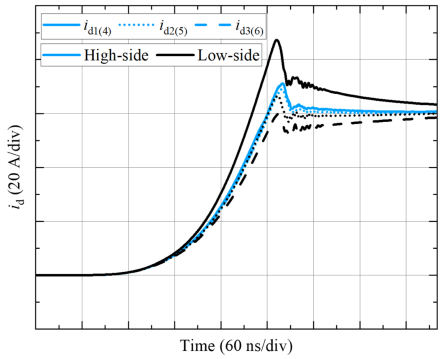

Fig. 4. Comparison of high-side and low-side transient currents.

currents. Therefore, the impact of mutual inductance coupling should be considered.

To directly verify the impact of mutual inductance coupling on dynamic current sharing performance, high-side electrical simulations were performed with all mutual inductance coupling removed. The results are shown in Fig. 3. After the mutual inductances are removed, the high-side currents are more unbalanced than before it was removed. It shows that mutual inductance coupling significantly affects the high-side dynamic current sharing performance. Therefore, to more clearly explain the mechanism of the phenomena and more accurately assess dynamic current sharing performance, a model considering all inductances and mutual inductances is proposed.

III. Current Sharing Model With Mutual Inductance Coupling and Current Sharing Mechanism Analysis

In this section, a dynamic current sharing model is established considering various mutual inductance couplings to reveal the mechanism of dynamic current sharing more clearly. Based on the model, the mechanism of different current sharing performances of the high-side and low-side paralleled SiC MOSFETs are analyzed, respectively.

A. Simplification of Parasitic Circuit Model and Dynamic Current Sharing Model

Considering the symmetry of the high-side and low-side MOSFETs, this section only analyzes the dynamic current sharing model of high-side Q1–Q3. The parasitic circuit model of the baseline module, including self-inductances and mutual inductances between the circuit branches, is shown in Fig. 5. The current sharing performance of paralleled SiC MOSFETs depends on the voltage of power source, gate, and driving source inductances. Therefore, for simplicity, only the coupling from other branches to the power source, gate, and driving source branches of Q1 is marked in Fig. 5. The other mutual inductances are not marked, which is also considered in the model. The mutual inductance between the x and y branches is expressed as M_{xy}. For example, M_{Ls1Ld4} represents the mutual inductance between L_{s1} and L_{d4}. The red, yellow, and green arrows indicate the mutual inductance couplings from power source inductance

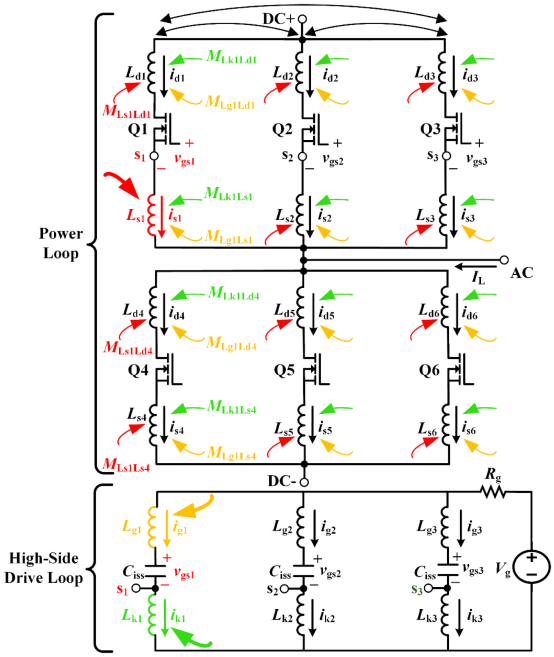

Fig. 5. Parasitic circuit model based on self-inductances and mutual inductances.

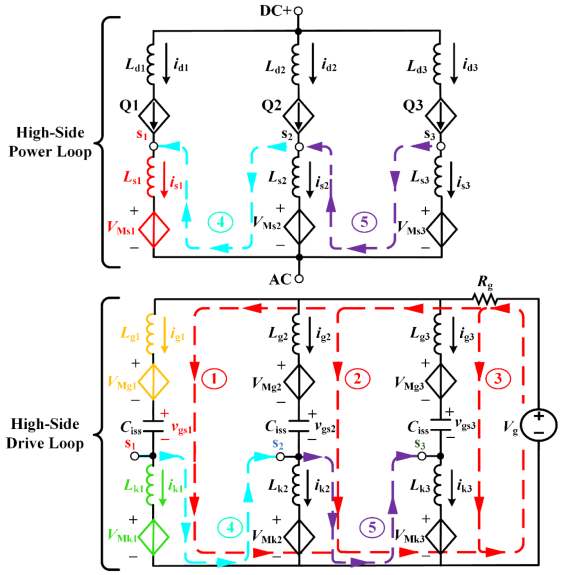

Fig. 6. Equivalent parasitic circuit model of the high-side MOSFETs in switching dynamics.

L_{s1}, gate inductance $L_{g1,}$ and drive source inductance L_{k1} of Q1 to other parasitic inductances.

Dynamic current balance occurs during switching transients. During the switching transients, SiC MOSFETs work in the saturation region. Therefore, SiC MOSFETs can be equivalent to current sources controlled by the gate-source voltage v_{gs}. The drain-source parasitic capacitance C_{ds} of MOSFETs can be ignored [26]. The paralleled gate-drain capacitance C_{gd} and gate-source capacitance C_{gs} are merged into input capacitance C_{iss}, which is equal to the sum of C_{gd} and C_{gs}.

The influence of the mutual inductance between two conductors can be regarded as induced voltage sources determined by the conductors' currents and mutual inductances. Then, the circuit in Fig. 5 can be equivalent to the circuit in Fig. 6 including 9 induced voltage sources representing mutual inductance couplings. V_{Ms1}, V_{Ms2}, and V_{Ms3} are the induced voltage sources in the high-side power source branches caused by the magnetic coupling from other power branches. V_{Mg1}, V_{Mg2}, and V_{Mg3} are the induced voltage sources in the high-side gate branches caused by the magnetic coupling from other power branches. V_{Mk1}, V_{Mk2}, and V_{Mk3} are the induced voltage sources in the high-side driving source branches caused by the magnetic coupling from other power branches. The induced voltages in the power circuit caused by the drive currents can be ignored since the gate currents i_g and the driving source currents i_k are much smaller than the power loop currents.

When the paralleled Q1–Q3 achieve dynamic current balance, it can be considered that

$$\begin{cases} i_{d1} = i_{d2} = i_{d3} = i_{Hd} \\ i_{s1} = i_{s2} = i_{s3} = i_{Hs} \end{cases} \tag{1}$$

where i_{Hd} and i_{Hs} are the drain current and power source current of a single high-side MOSFET. To simplify the analysis, it is assumed that the currents of Q4–Q6 are equal. Equation (2) is derived

$$\begin{cases} i_{d4} = i_{d5} = i_{d6} = i_{Ld} \\ i_{s4} = i_{s5} = i_{s6} = i_{Ls} \end{cases} \tag{2}$$

where i_{Ld} and i_{Ls} are the drain current and power source current of a single low-side MOSFET. Meanwhile, the specific expressions of V_{Mg1}, V_{Mg2}, V_{Mg3}, V_{Ms1}, V_{Ms2}, and V_{Ms3} are shown in (3) and (4) shown at the bottom of the next page

The KVL equation is derived from the driving loops 1, 2, and 3 in Fig. 6 and can be expressed by

$$\begin{cases} V_g = L_{g1}\frac{di_{g1}}{dt} + L_{k1}\frac{di_{k1}}{dt} + v_{gs1} + V_{Mg1} + V_{Mk1} \\ \quad +R_g(i_{g1} + i_{g2} + i_{g3}) \\ V_g = L_{g2}\frac{di_{g2}}{dt} + L_{k2}\frac{di_{k2}}{dt} + v_{gs2} + V_{Mg2} + V_{Mk2} \\ \quad +R_g(i_{g1} + i_{g2} + i_{g3}) \\ V_g = L_{g3}\frac{di_{g3}}{dt} + L_{k3}\frac{di_{k3}}{dt} + v_{gs3} + V_{Mg3} + V_{Mk3} \\ \quad +R_g(i_{g1} + i_{g2} + i_{g3}). \end{cases} \tag{5}$$

According to (5), the gate-source voltage difference Δv_{gs12} between Q1 and Q2 and the difference Δv_{gs23} between Q2 and Q3 can be derived that

$$\begin{cases} \Delta v_{gs12} = v_{gs1} - v_{gs2} \\ = L_{g2}\frac{di_{g2}}{dt} - L_{g1}\frac{di_{g1}}{dt} + L_{k2}\frac{di_{k2}}{dt} - L_{k1}\frac{di_{k1}}{dt} + V_{Mg2} \\ \quad -V_{Mg1} + V_{Mk2} - V_{Mk1} \\ \Delta v_{gs23} = v_{gs2} - v_{gs3} \\ = L_{g3}\frac{di_{g3}}{dt} - L_{g2}\frac{di_{g2}}{dt} + L_{k3}\frac{di_{k3}}{dt} - L_{k2}\frac{di_{k2}}{dt} \\ \quad +V_{Mg3} - V_{Mg2} + V_{Mk3} - V_{Mk2}. \end{cases} \tag{6}$$

The KVL equation is derived from power loop 4 and loop5 in Fig. 6 and can be expressed by

$$\begin{cases} L_{s2}\frac{di_{s2}}{dt} - L_{s1}\frac{di_{s1}}{dt} + V_{Ms2} - V_{Ms1} = L_{k2}\frac{di_{k2}}{dt} \\ \quad -L_{k1}\frac{di_{k1}}{dt} + V_{Mk2} - V_{Mk1} \\ L_{s3}\frac{di_{s3}}{dt} - L_{s2}\frac{di_{s2}}{dt} + V_{Ms3} - V_{Ms2} = L_{k3}\frac{di_{k3}}{dt} \\ \quad -L_{k2}\frac{di_{k2}}{dt} + V_{Mk3} - V_{Mk2}. \end{cases} \tag{7}$$

During the switching transient, the gate currents are much smaller than the power source currents. Therefore, by combining (6) and (7), it can be deduced that

$$\begin{cases} \Delta v_{gs12} = V_{Mg2} - V_{Mg1} + V_{Ms2} - V_{Ms1} \\ \quad +L_{s2}\frac{di_{s2}}{dt} - L_{s1}\frac{di_{s1}}{dt} \\ \Delta v_{gs23} = V_{Mg3} - V_{Mg2} + V_{Ms3} - V_{Ms2} \\ \quad +L_{s3}\frac{di_{s3}}{dt} - L_{s2}\frac{di_{s2}}{dt}. \end{cases} \tag{8}$$

By solving (1)-(4) and (8), it can be deduced that

$$\begin{cases} \Delta v_{gs12} = M_{Hd1\_2}\frac{di_{Hd}}{dt} + M_{Hs1\_2}\frac{di_{Hs}}{dt} + M_{Ld1\_2}\frac{di_{Ld}}{dt} \\ \quad +M_{Ls1\_2}\frac{di_{Ls}}{dt} \\ \Delta v_{gs23} = M_{Hd2\_3}\frac{di_{Hd}}{dt} + M_{Hs2\_3}\frac{di_{Hs}}{dt} + M_{Ld2\_3}\frac{di_{Ld}}{dt} \\ \quad +M_{Ls2\_3}\frac{di_{Ls}}{dt} \end{cases} \tag{9}$$

The specific expressions of mutual inductance coefficients (MICs: $M_{\mathrm{Hd1\_2}}$, $M_{\mathrm{Hs1\_2}}$, $M_{\mathrm{Ld1\_2}}$, $M_{\mathrm{Ls1\_2}}$, $M_{\mathrm{Hd2\_3}}$, $M_{\mathrm{Hs2\_3}}$, $M_{\mathrm{Ld2\_3}}$, and $M_{\mathrm{Ls2\_3}}$) are shown in (10) and (11) shown at the bottom of the next page, which are composed of two parts: 1) power-source self-inductances and mutual inductance coupling between power branches and power-source branches (M_{Ppower}); 2) mutual inductance coupling between the power branches and the driving gate branches (M_{Pdrive}).

The basic meanings of the MICs in (9) are analyzed below through Q1 and Q2, taking $M_{\mathrm{Hd1\_2}}$ as an example. The expression of $M_{\mathrm{Hd1\_2}}$ is divided into four terms. The first two items of $M_{\mathrm{Hd1\_2}}$ are the mutual inductances between the high-side drain branches and power source branches of Q1 and Q2. The last two items of $M_{\mathrm{Hd1\_2}}$ are the mutual inductances between the high-side drain branches and gate branches of Q1 and Q2. Therefore, $M_{\mathrm{Hd1\_2}}$ represents the influence of the magnetic couplings from high-side drain branches on the current sharing of Q1 and Q2. Similarly, $M_{\mathrm{Ld1\_2}}$ and $M_{\mathrm{Ls1\_2}}$ reveal the influence of the magnetic coupling from low-side drain and power source branches on the current sharing of Q1 and Q2. Specifically, $M_{\mathrm{Hs1\_2}}$ not only includes the influence of the magnetic coupling from the high-side power source branches on the current sharing of Q1 and Q2 but also includes the influence of power source self-inductances of Q1 and Q2. The conclusion can be drawn that each branch affects the current sharing through the mutual inductance couplings between the branch to the power source and gate branches of the paralleled SiC MOSFETs.

In summary, $M_{\mathrm{Hd1\_2}}$, $M_{\mathrm{Hs1\_2}}$, $M_{\mathrm{Ld1\_2}}$, and $M_{\mathrm{Ls1\_2}}$ can be used to evaluate the influence of the high-side power source self-inductances, and the magnetic couplings from high-side drain branches, high-side source branches, low-side drain branches, and low-side source branches on the dynamic current sharing of Q1 and Q2 qualitatively. The positive or negative signs of

$$\begin{bmatrix} V_{Ms1} \\ V_{Ms2} \\ V_{Ms3} \end{bmatrix} = \begin{bmatrix} M_{Ls1Ld1}+M_{Ls1Ld2}+M_{Ls1Ld3} & M_{Ls1Ls2}+M_{Ls1Ls3} & M_{Ls1Ld4}+M_{Ls1Ld5}+M_{Ls1Ld6} & M_{Ls1Ls4}+M_{Ls1Ls5}+M_{Ls1Ls6} \\ M_{Ls2Ld1}+M_{Ls2Ld2}+M_{Ls2Ld3} & M_{Ls2Ls1}+M_{Ls2Ls3} & M_{Ls2Ld4}+M_{Ls2Ld5}+M_{Ls2Ld6} & M_{Ls2Ls4}+M_{Ls2Ls5}+M_{Ls2Ls6} \\ M_{Ls3Ld1}+M_{Ls3Ld2}+M_{Ls3Ld3} & M_{Ls3Ls1}+M_{Ls3Ls2} & M_{Ls3Ld4}+M_{Ls3Ld5}+M_{Ls3Ld6} & M_{Ls3Ls4}+M_{Ls3Ls5}+M_{Ls3Ls6} \end{bmatrix} \times \begin{bmatrix} \frac{di_{Hd}}{dt} \\ \frac{di_{Hs}}{dt} \\ \frac{di_{Ld}}{dt} \\ \frac{di_{Ls}}{dt} \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} V_{Mg1} \\ V_{Mg2} \\ V_{Mg3} \end{bmatrix} = \begin{bmatrix} M_{Lg1Ld1}+M_{Lg1Ld2}+M_{Lg1Ld3}+M_{Lg1Ls6} & M_{Lg1Ls1}+M_{Lg1Ls2}+M_{Lg1Ls3} & M_{Lg1Ld4}+M_{Lg1Ld5}+M_{Lg1Ld6} & M_{Lg1Ls4}+M_{Lg1Ls5} \\ M_{Lg2Ld1}+M_{Lg2Ld2}+M_{Lg2Ld3}+M_{Lg2Ls6} & M_{Lg2Ls1}+M_{Lg2Ls2}+M_{Lg2Ls3} & M_{Lg2Ld4}+M_{Lg2Ld5}+M_{Lg2Ld6} & M_{Lg2Ls4}+M_{Lg2Ls5} \\ M_{Lg3Ld1}+M_{Lg3Ld2}+M_{Lg3Ld3}+M_{Lg3Ls6} & M_{Lg3Ls1}+M_{Lg3Ls2}+M_{Lg3Ls3} & M_{Lg3Ld4}+M_{Lg3Ld5}+M_{Lg3Ld6} & M_{Lg3Ls4}+M_{Lg3Ls5} \end{bmatrix} \times \begin{bmatrix} \frac{di_{Hd}}{dt} \\ \frac{di_{Hs}}{dt} \\ \frac{di_{Ld}}{dt} \\ \frac{di_{Ls}}{dt} \end{bmatrix}. \tag{4}$$

MICs indicate the promotion or inhibition of current sharing. The closer MICs are to 0, the smaller influence on the dynamic current sharing of Q1 and Q2 is. Therefore, the effect of each part's mutual inductance coupling on dynamic current sharing can be analyzed by MICs. This has a strong guiding significance for the dynamic current balancing design of the power module.

To further simplify the design guidance of dynamic current balance, (9) is simplified below. The driving source currents i_{k} is much smaller than the drain currents and the source currents. Then, it can be deduced that

$$\begin{cases} i_{\boldsymbol{Hd}} = i_{\boldsymbol{Hs}} \\ i_{\boldsymbol{Ld}} = i_{\boldsymbol{Ls}}. \end{cases} \tag{12}$$

Meanwhile, the KCL equation for the ac point in the transient process is as follows:

$$i_{\boldsymbol{Hs}} = i_{\boldsymbol{Ld}} - \frac{I_{\boldsymbol{L}}}{3}. \tag{13}$$

Solving (9), (12), and (13), it can be deduced that

$$\begin{cases} \Delta v_{\boldsymbol{gs12}} = (M_{\boldsymbol{Hd1\_2}} + M_{\boldsymbol{Hs1\_2}} + M_{\boldsymbol{Ld1\_2}} + M_{\boldsymbol{Ls1\_2}}) \frac{di_{\boldsymbol{Hd}}}{dt} \\ \Delta v_{\boldsymbol{gs23}} = (M_{\boldsymbol{Hd2\_3}} + M_{\boldsymbol{Hs2\_3}} + M_{\boldsymbol{Ld2\_3}} + M_{\boldsymbol{Ls2\_3}}) \frac{di_{\boldsymbol{Hd}}}{dt}. \end{cases} \tag{14}$$

During the transient period of turn-ON and turn-OFF, the relationship between the drain currents of the high-side MOSFETs and v_{gs} is as follows:

$$\begin{cases} i_{\boldsymbol{d1}} = g(v_{\boldsymbol{gs1}} - V_{\boldsymbol{th}})^2 \\ i_{\boldsymbol{d2}} = g(v_{\boldsymbol{gs2}} - V_{\boldsymbol{th}})^2 \\ i_{\boldsymbol{d3}} = g(v_{\boldsymbol{gs3}} - V_{\boldsymbol{th}})^2 \end{cases} \tag{15}$$

where g is the transconductance of the SiC MOSFETs. Both g and V_{th} depend on MOSFETs themselves. This model only considers the dynamic current imbalance caused by the asymmetric layout. Therefore, it is assumed that the device parameters of paralleled chips are consistent. Therefore, in order to make the dynamic currents of the three MOSFETs fully balanced, (16) needs to be satisfied

$$\begin{cases} \Delta v_{\boldsymbol{gs12}} = 0 \\ \Delta v_{\boldsymbol{gs23}} = 0. \end{cases} \tag{16}$$

Therefore, in order to satisfy (16), according to (14), it can be deduced that

$$\begin{cases} M_{\boldsymbol{1\_2}} = M_{\boldsymbol{Hd1\_2}} + M_{\boldsymbol{Hs1\_2}} + M_{\boldsymbol{Ld1\_2}} + M_{\boldsymbol{Ls1\_2}} = 0 \\ M_{\boldsymbol{2\_3}} = M_{\boldsymbol{Hd2\_3}} + M_{\boldsymbol{Hs2\_3}} + M_{\boldsymbol{Ld2\_3}} + M_{\boldsymbol{Ls2\_3}} = 0. \end{cases} \tag{17}$$

In (17), M_{1_2} and M_{2_3} are the dynamic current balancing judgment coefficients (JCs) of Q1, Q2, and Q2, Q3, respectively. When JCs are close to 0, Q1, Q2, and Q3 can realize fully balanced dynamic currents. Therefore, JCs can be used as a design guide for dynamic current balancing under the consideration of various mutual inductance effects.

B. Dynamic Current Sharing Analysis Based on the Current Sharing Model

The current sharing model considering various mutual inductance couplings can be utilized to analyze the different dynamic current sharing mechanisms of the high-side and low-side MOSFETs, respectively.

Based on the parasitic inductance matrix extracted by Q3D Extractors, MICs between Q1, Q2, and Q3 can be calculated,

$$\begin{cases} M_{\boldsymbol{Hd1\_2}} = -(M_{\boldsymbol{Ls1Ld1}} + M_{\boldsymbol{Ls1Ld2}} + M_{\boldsymbol{Ls1Ld3}}) + (M_{\boldsymbol{Ls2Ld1}} + M_{\boldsymbol{Ls2Ld2}} + M_{\boldsymbol{Ls2Ld3}}) \\ \quad -(M_{\boldsymbol{Lg1Ld1}} + M_{\boldsymbol{Lg1Ld2}} + M_{\boldsymbol{Lg1Ld3}}) + (M_{\boldsymbol{Lg2Ld1}} + M_{\boldsymbol{Lg2Ld2}} + M_{\boldsymbol{Lg2Ld3}}) \\ M_{\boldsymbol{Hs1\_2}} = -(L_{\boldsymbol{s1}} + M_{\boldsymbol{Ls1Ls2}} + M_{\boldsymbol{Ls1Ls3}}) + (M_{\boldsymbol{Ls2Ls1}} + L_{\boldsymbol{s2}} + M_{\boldsymbol{Ls2Ls3}}) - (M_{\boldsymbol{Lg1Ls1}} \\ \quad + M_{\boldsymbol{Lg1Ls2}} + M_{\boldsymbol{Lg1Ls3}}) + (M_{\boldsymbol{Lg2Ls1}} + M_{\boldsymbol{Lg2Ls2}} + M_{\boldsymbol{Lg2Ls3}}) \\ M_{\boldsymbol{Ld1\_2}} = -(M_{\boldsymbol{Ls1Ld4}} + M_{\boldsymbol{Ls1Ld5}} + M_{\boldsymbol{Ls1Ld6}}) + (M_{\boldsymbol{Ls2Ld4}} + M_{\boldsymbol{Ls2Ld5}} + M_{\boldsymbol{Ls2Ld6}}) \\ \quad -(M_{\boldsymbol{Lg1Ld4}} + M_{\boldsymbol{Lg1Ld5}} + M_{\boldsymbol{Lg1Ld6}}) + (M_{\boldsymbol{Lg2Ld4}} + M_{\boldsymbol{Lg2Ld5}} + M_{\boldsymbol{Lg2Ld6}}) \\ M_{\boldsymbol{Ls1\_2}} = \underbrace{-(M_{\boldsymbol{Ls1Ls4}} + M_{\boldsymbol{Ls1Ls5}} + M_{\boldsymbol{Ls1Ls6}}) + (M_{\boldsymbol{Ls2Ls4}} + M_{\boldsymbol{Ls2Ls5}} + M_{\boldsymbol{Ls2Ls6}})}_{M_{\boldsymbol{Ppower}}} \\ \underbrace{-(M_{\boldsymbol{Lg1Ls4}} + M_{\boldsymbol{Lg1Ls5}} + M_{\boldsymbol{Lg1Ls6}}) + (M_{\boldsymbol{Lg2Ls4}} + M_{\boldsymbol{Lg2Ls5}} + M_{\boldsymbol{Lg2Ls6}})}_{M_{\boldsymbol{Pdrive}}} \end{cases} \tag{10}$$

$$\begin{cases} M_{\boldsymbol{Hd2\_3}} = -(M_{\boldsymbol{Ls2Ld1}} + M_{\boldsymbol{Ls2Ld2}} + M_{\boldsymbol{Ls2Ld3}}) + (M_{\boldsymbol{Ls3Ld1}} + M_{\boldsymbol{Ls3Ld2}} + M_{\boldsymbol{Ls3Ld3}}) \\ \quad -(M_{\boldsymbol{Lg2Ld1}} + M_{\boldsymbol{Lg2Ld2}} + M_{\boldsymbol{Lg2Ld3}}) + (M_{\boldsymbol{Lg3Ld1}} + M_{\boldsymbol{Lg3Ld2}} + M_{\boldsymbol{Lg3Ld3}}) \\ M_{\boldsymbol{Hs2\_3}} = -(M_{\boldsymbol{Ls2Ls1}} + L_{\boldsymbol{s2}} + M_{\boldsymbol{Ls2Ls3}}) + (M_{\boldsymbol{Ls3Ls1}} + M_{\boldsymbol{Ls3Ls2}} + L_{\boldsymbol{s3}}) \\ \quad -(M_{\boldsymbol{Lg2Ls1}} + M_{\boldsymbol{Lg2Ls2}} + M_{\boldsymbol{Lg2Ls3}}) + (M_{\boldsymbol{Lg3Ls1}} + M_{\boldsymbol{Lg3Ls2}} + M_{\boldsymbol{Lg3Ls3}}) \\ M_{\boldsymbol{Ld2\_3}} = -(M_{\boldsymbol{Ls2Ld4}} + M_{\boldsymbol{Ls2Ld5}} + M_{\boldsymbol{Ls2Ld6}}) + (M_{\boldsymbol{Ls3Ld4}} + M_{\boldsymbol{Ls3Ld5}} + M_{\boldsymbol{Ls3Ld6}}) \\ \quad -(M_{\boldsymbol{Lg2Ld4}} + M_{\boldsymbol{Lg2Ld5}} + M_{\boldsymbol{Lg2Ld6}}) + (M_{\boldsymbol{Lg3Ld4}} + M_{\boldsymbol{Lg3Ld5}} + M_{\boldsymbol{Lg3Ld6}}) \\ M_{\boldsymbol{Ls2\_3}} = \underbrace{-(M_{\boldsymbol{Ls2Ls4}} + M_{\boldsymbol{Ls2Ls5}} + M_{\boldsymbol{Ls2Ls6}}) + (M_{\boldsymbol{Ls3Ls4}} + M_{\boldsymbol{Ls3Ls5}} + M_{\boldsymbol{Ls3Ls6}})}_{M_{\boldsymbol{Ppower}}} \\ \underbrace{-(M_{\boldsymbol{Lg2Ls4}} + M_{\boldsymbol{Lg2Ls5}} + M_{\boldsymbol{Lg2Ls6}}) + (M_{\boldsymbol{Lg3Ls4}} + M_{\boldsymbol{Lg3Ls5}} + M_{\boldsymbol{Lg3Ls6}})}_{M_{\boldsymbol{Pdrive}}}. \end{cases} \tag{11}$$

TABLE I
MICS AND JCS VALUES OF HIGH-SIDE MOSFETS

Q1, Q2 20 MHz	M_{1_2}	M_{Hd1_2}	M_{Hs1_2}	M_{Ld1_2}	M_{Ls1_2}	Δi_{1_2}
simulated value	0.32	0.52	-0.17	0.22	-0.25	2.32 A
Q2, Q3 20 MHz	M_{2_3}	M_{Hd2_3}	M_{Hs2_3}	M_{Ld2_3}	M_{Ls2_3}	Δi_{2_3}
simulated value	-0.04	0.25	-0.66	0.60	-0.23	-1.59 A

TABLE II
MICS AND JCS VALUES OF LOW-SIDE MOSFETS

Q4, Q5 20 MHz	M_{4_5}	M_{Hd4_5}	M_{Hs4_5}	M_{Ld4_5}	M_{Ls4_5}	Δi_{4_5}
simulated value	1.93	-0.01	0.02	-0.01	1.93	20.9 A
Q5, Q6 20 MHz	M_{5_6}	M_{Hd5_6}	M_{Hs5_6}	M_{Ld5_6}	M_{Ls5_6}	Δi_{5_6}
simulated value	0.87	-0.01	0.02	-0.03	0.89	6.52 A

as shown in Table I. For Q1 and Q2, $M_{1\_2} = 0.32$ and $\Delta i_{1\_2} = 2.32$ A, and for Q2 and Q3, $M_{2\_3} = -0.04$ and $\Delta i_{2\_3} = -1.59$ A. When JCs are close to 0, the dynamic current of Q1, Q2, and Q3 is well balanced. Taking Q1 and Q2 as an example, the current sharing mechanism of the high-side MOSFETs is analyzed. According to the positive and negative signs of MICs in Table I, it is concluded that the influence of the magnetic couplings from the high-side and low-side drain branches (reflected by M_{Hd1_2} and M_{Ld1_2}) cancels the influence of the power source self-inductances of Q1 and Q2 and the magnetic couplings from the high-side power source branches (reflected by m_{Hs1_2}). However, the influence of the magnetic couplings from the low-side source branches (represented by M_{Ls1_2}) gains the influence of the source self-inductances and the magnetic couplings from the high-side source branches (reflected by m_{Hs1_2}). In general, the power source self-inductances of Q1 and Q2 and various mutual inductance couplings jointly affect the dynamic current sharing, resulting in a good balancing performance.

Due to the symmetry of the high-side and low-side MOSFETs, MICs ($M_{Hd4\_5}, M_{Hs4\_5}, M_{Ld4\_5}, M_{Ls4\_5}, M_{Hd5\_6}, M_{Hs5\_6}$, M_{Ld5_6}, and M_{Ls5_6}) and JCs (M_{4_5} and M_{5_6}) between the low-side MOSFETs can be derived and calculated, as shown in Table II. For Q4 and Q5, $M_{4\_5} = 1.93$ and $\Delta i_{4\_5} = 20.9$ A, and for Q5 and Q6, $M_{5\_6} = 0.87$ and $\Delta i_{5\_6} = 6.52$ A. It shows that the dynamic current is poorly balanced when JCs have a large deviation from 0. Taking Q4 and Q5 as an example, M_{Ls45} is much larger than other MICs in Table II. It indicates that the influence of the power source self-inductances of Q4 and Q5 and the magnetic couplings from the low-side source branches (reflected by M_{Ls4_5}) on the current balance of Q4 and Q5 is dominant, leading to poor dynamic current balancing. Other mutual inductance effects (reflected by M_{Hs4_5}, M_{Hd4_5}, and M_{Ld4_5}) are small and can be neglected. Therefore, based on the proposed model, the different dynamic current sharing phenomena on the high side and low side are well explained taking into account all unbalanced inductances and mutual inductances.

IV. SIMULATION VERIFICATIONS

As illustrated in Section III, JCs can assess the dynamic current sharing performance of paralleled SiC MOSFETs. In the industrial production process, the shape and connection points of the bonding wires are easily adjusted by adjusting the parameters of the bonding machine. Therefore, the connection points of the power source bonding wires of the paralleled MOSFETs are adjusted, achieving different values of JCs, to verify the proposed model and optimize the dynamic current sharing performance, JCs with different connection points are calculated by (10), (11), and (17). Meanwhile, LTSIPCE is used to simulate the switching transient currents under different connection points. Comparing the relationship between JCs and current peak differences under different current sharing conditions, the accuracy of JCs can be verified. Finally, the proposed model is compared with an existing model.

A. Simulation Verification of Dynamic Current Balancing Criterion JCs

The current peak differences with different JCs between Q1, Q2, and Q3 are shown in Fig. 7. The relationships of the current peak differences and JCs are linearly fitted, where the fitting coefficient R^2 of the fitting lines in Fig. 7(a) and (b) are 0.9819 and 0.9826, respectively. It shows that the current peak difference has a good linear relationship with JCs. The intercept of the fitting line indicates the dynamic current difference when JCs = 0. The intercept of the fitting line of Q1 and Q2 is −0.339 A, and the intercept of Q2 and Q3 is −1.489 A. It can be judged that the dynamic current of paralleled MOSFETs is balanced well when JCs = 0.

Two sets of special data (see S2 and S3 in Fig. 7) are selected for illustration. The high-side power source self-inductances of S2 are equal, and the high-side current balance of S3 is achieved. The schematic diagrams of the power modules of S2 and S3 are shown in Fig. 8. In S2, the difference in power source self-inductances between Q1 and Q2 is 0.05 nH, and the difference value between Q2 and Q3 is 0.18 nH. However, $M_{1\_2} = 0.98$ and $M_{2\_3} = 0.81$. The differences in peak current are $\Delta i_{1\_2} = 9.17$ A and $\Delta i_{2\_3} = 4.13$ A, as shown in Fig. 9. Although the differences between L_{s1}, L_{s2}, and L_{s3} are very small, the effect of the dynamic current balance is not ideal. In S3, the difference in power source self-inductances between Q1 and Q2 is 1.05 nH, and the value between Q2 and Q3 is 0.60 nH. However, $M_{1\_2} = 0.19$, $M_{2\_3} = -0.12$. $\Delta i_{1\_2} = 0.89$ A, $\Delta i_{2\_3} = -2.09$ A, as shown in Fig. 10. The high-side dynamic current is balanced well because the influence of various mutual inductances cancels the influence of power source self-inductances on the dynamic current sharing. It is shown that JCs considering self-inductances and various mutual inductances can obtain more accurate results when evaluating the dynamic current balancing degree.

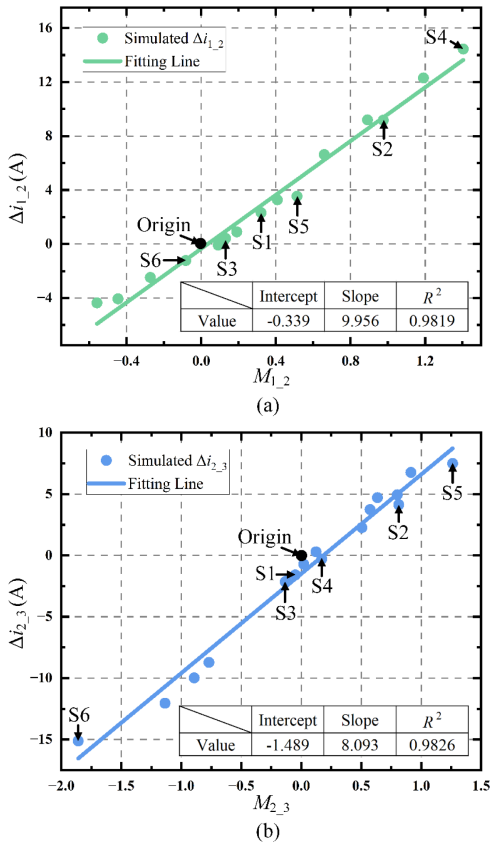

Fig. 7. Relationship between current peak differences and JCs of Q1–Q3. (a) Graph of Δi_{1_2} versus M_{1_2}. (b) Graph of Δi_{2_3} versus M_{2_3}.

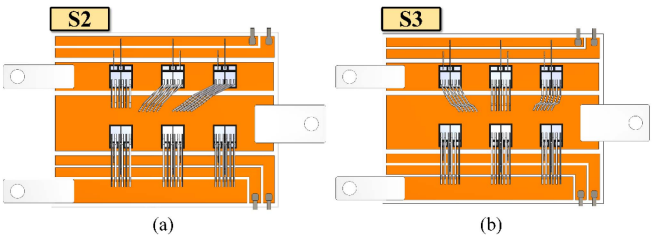

Fig. 8. Schematic diagrams with different connection points of the high-side bonding wires. (a) S2 with equal power source inductances. (b) S3 with balanced dynamic currents.

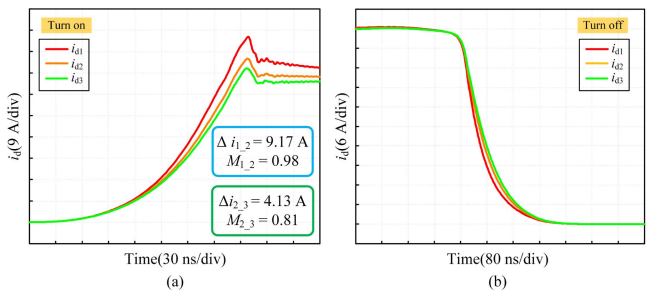

Fig. 9. Dynamic current of S2 simulated for Q1–Q3. (a) Turn-ON current of S2. (b) Turn-OFF current of S2.

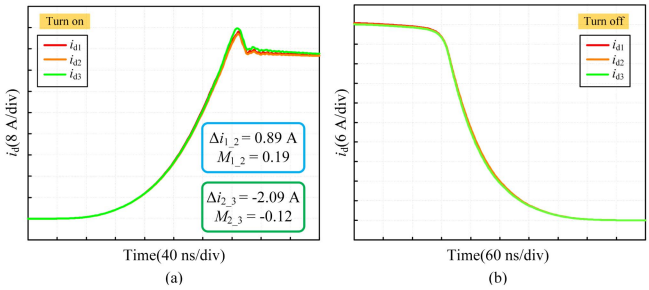

Fig. 10. Dynamic current of S3 simulated for Q1–Q3. (a) Turn-ON current of S3. (b) Turn-OFF current of S3.

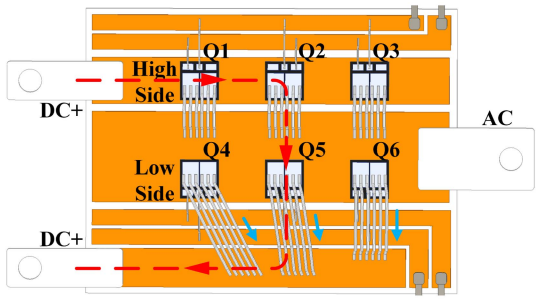

Fig. 11. Structure diagram of Module LE with current balancing low-side MOSFETs.

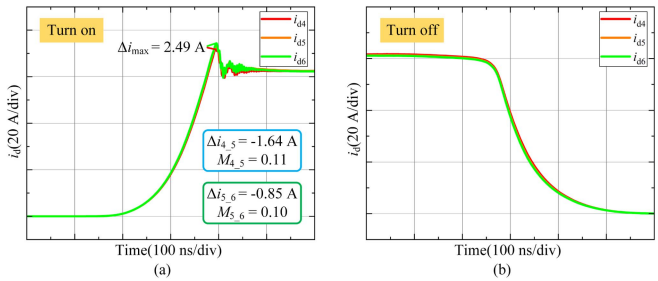

Fig. 12. Dynamic current waveform of optimized low-side MOSFETs. (a) Turn-ON current. (b) Turn-OFF current.

The accuracy of the model has been validated with the high-side MOSFETs. Therefore, only two data points are used to compare and illustrate the model's performance with the low-side MOSFETs.

Based on the proposed model, the power modules with optimized low-side MOSFETs (referred to as Module LE) are depicted in Fig. 11. The maximum dynamic current difference is $\Delta i_{4\_6} = -2.49$ A, as shown in Fig. 12. Meanwhile, $M_{4\_5} = 0.11$, $M_{5\_6} = 0.10$. $\Delta i_{4\_5} = -1.64$ A, $\Delta i_{5\_6} = -0.85$ A. In Module LE, JCs approach 0 when dynamic current balance is achieved. It indicates that the proposed model is also applicable to the low-side MOSFETs.

B. Comparison of the Existing Model

To verify the improvement of the proposed model, a comparison was made between the proposed model and the reference model in [31]. The parameters $M_{\mathrm{pp1\_2}}$, $M_{\mathrm{pg1\_2}}$, $M_{\mathrm{pp2\_3}}$, and

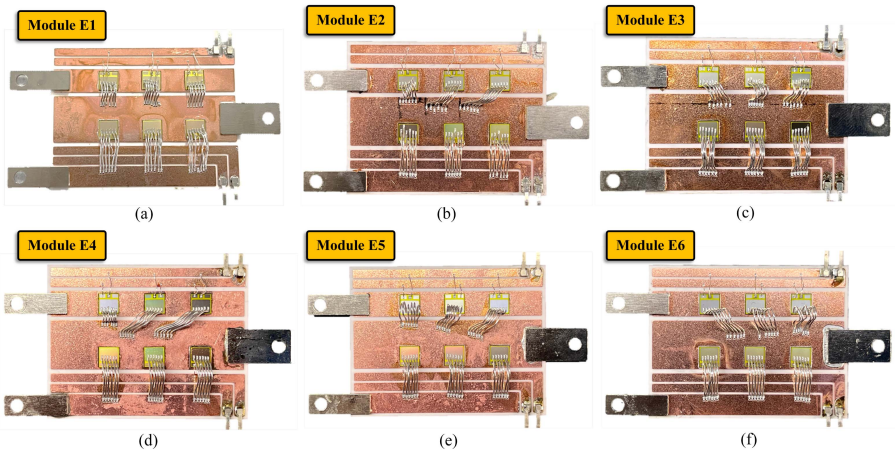

Fig. 13. Fabricated power modules. (a) Module E1. (b) Module E2. (c) Module E3. (d) Module E4. (e) Module E5. (f) Module E6.

TABLE III
COMPARISON OF PROPOSED MODEL AND REFERENCE MODEL

Module S3	Reference model		Proposed model
	M_{pp}	M_{pg}	M
Q1, Q2	0.12	0.13	0.19
Q2, Q3	0.03	-0.12	-0.12
Module LE	**Reference model**		**Proposed model**
	M_{pp}	M_{pg}	M
Q4, Q5	0.46	-1.01	0.11
Q5, Q6	0.11	0.98	0.10

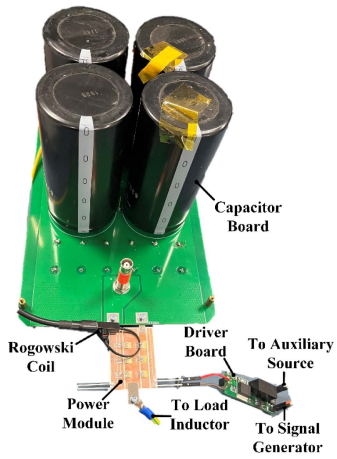

Fig. 14. Double pulse experimental test bench.

$M_{\mathrm{pg2\_3}}$ are defined in the Appendix. In the reference model, when $M_{\mathrm{pp1\_2}} = M_{\mathrm{pg1\_2}} = 0$, Q1 and Q2 achieve the current 0 balance. When $M_{\mathrm{pp2\_3}} = M_{\mathrm{pg2\_3}} = 0$, Q2 and Q3 achieve the current balance. For the low-side MOSFETs, $M_{\mathrm{pp4\_5}}$, $M_{\mathrm{pg4\_5}}$, $M_{\mathrm{pp5\_6}}$, and $M_{\mathrm{pg5\_6}}$ are similar.

For Module S3 (see Fig. 8) with balanced high-side currents and Module LE (see Fig. 11) with balanced low-side currents, comparative model results are presented in Table III. Both models are accurate in the current sharing assessment of Module S3. However, for the current sharing evaluation of Module LE, there is a non-negligible error in the reference model. It shows that the proposed model can achieve higher accuracy in some layouts. It has great significance for the effectiveness of dynamic current sharing optimized design.

V. EXPERIMENTAL VERIFICATION

To further verify the accuracy of JCs, the wire-bonding power modules E1–E6 (corresponding to S1–S6 in Fig. 7) with the different connection points of the high-side bonding wires are fabricated and tested, as depicted in Fig. 13. Among Modules E1–E6, Module E1 is the initial state module. The high-side power source inductances of Module E2 are equal (corresponding to S2), and the high-side current is balanced in Module E3 (corresponding to S3). A double-pulse test bench is built to measure the switching dynamic current of paralleled SiC MOSFETs, as shown in Fig. 14. 120 A/30 MHz Rogowski coils are used as current sensors to measure the current on each SiC MOSFETs. The switching waveforms are measured when the bus voltage is 400 V, the load inductance is 100 μH, the driving resistance is 10 Ω, and I_{load} is 180 A.

A. Experimental Verification of the High-Side and Low-Side Dynamic Current of the Baseline Module

The turn-ON and turn-OFF transient currents waveforms of the high-side and low-side MOSFETs in Module E1 obtained by the experimental measurement are shown in Figs. 15 and 16. The maximum turn-ON current difference of the high-side MOSFETs is $\Delta i_{1\_2} = 3.6$ A. The maximum turn-ON current difference of the low-side MOSFETs is $\Delta i_{4\_6} = 11.7$ A. Consistent with the simulation, the high-side dynamic current is well balanced due

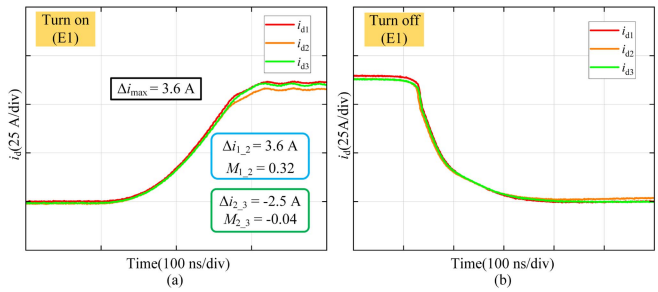

Fig. 15. Transient current of the high-side Q1–Q3 of the baseline Module E1. (a) Turn-ON transient current. (b) Turn-OFF transient current.

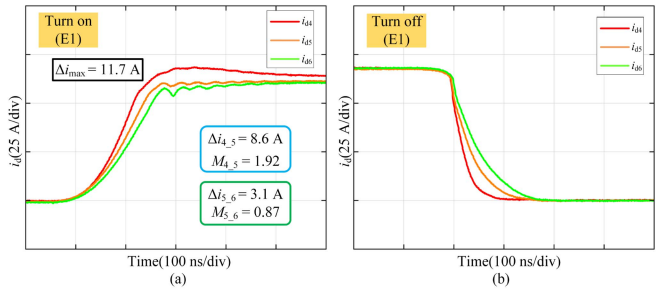

Fig. 16. Transient current of the low-side Q4–Q6 of the baseline Module E1. (a) Turn-ON transient current. (b) Turn-OFF transient current.

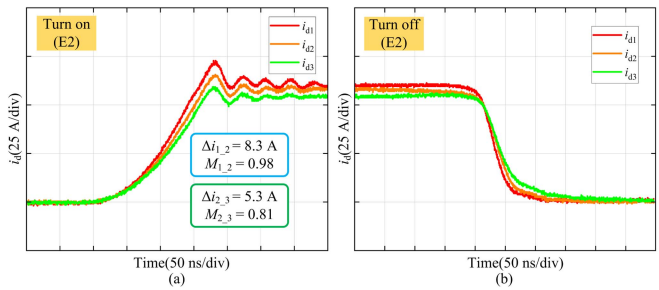

Fig. 17. Transient current of the high-side Q1–Q3 of the Module E2. (a) Turn-ON transient current. (b) Turn-OFF transient current.

to the influence of various mutual inductance couplings, which cancels the influence of source self-inductances. However, the low-side dynamic current is poorly balanced due to the small suppression effect of the mutual inductances on the influence of power source self-inductances.

B. Experimental Verification of Dynamic Current Balancing Criterion JCs

The switching waveforms of Module E2 and Module E3 are shown in Figs. 17 and 18. In Module E2, the current peak difference between Q1 and Q2 is 8.3 A when $M_{1\_2} = 0.98$, and the difference value between Q2 and Q3 is 5.3 A when $M_{2\_3} = 0.81$. The high-side dynamic current of Module E2 is imbalanced, and its JCs have a large deviation from 0. However, in Module E3, the current peak difference between Q1 and Q2 is 0.5 A when $M_{1\_2} = 0.19$, and the value between Q2 and Q3 is -1.4 A when $M_{2\_3} = -0.12$. The high-side dynamic

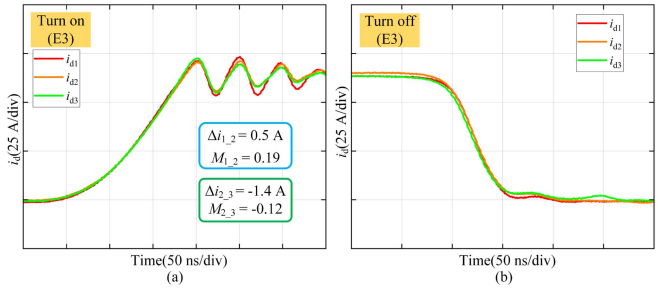

Fig. 18. Transient current of the high-side Q1–Q3 of the Module E3. (a) Turn-ON transient current. (b) Turn-OFF transient current.

current of Module E3 is balanced well, and its JCs are close to 0. Their results are consistent with those of S1 and S2. It can also indirectly prove the effect of mutual inductance coupling on dynamic current sharing performance.

To further substantiate the linearity between the current difference and JCs as depicted in Fig. 7, the turn-ON currents of Module E4–E6 were measured, as shown in Fig. 19. Consequently, the relationship between the experimentally measured current differences Δi_{1_2}, Δi_{2_3} and M_{1_2}, M_{2_3} of Module E1–E6 is shown in Fig. 20. The relationships of the current peak differences and JCs are linearly fitted, with fitting coefficients R^2 of 0.9946 and 0.9993 for the fitting lines in Fig. 20(a) and (b), respectively. The results confirm that the current peak difference exhibits a linear relationship with JCs. The intercept of the fitting line indicates the dynamic current difference when JCs $= 0$. For the fitting line of Q1 and Q2, the intercept is -1.755 A, and for Q2 and Q3, it is -1.256 A. This suggests that when JC $= 0$, the parallel MOSFETs essentially achieve the current balance. The experiment further validates that this model can accurately assess the degree of dynamic current balance. This discovery provides more robust guidance for the design of current-sharing layouts in power modules. The mismatched parameters of paralleled SiC MOSFETs and the error of the bonding wires played by the bonding machine may lead to slight differences between simulations and experiments. However, the accuracy and linearity of JCs can still be verified.

VI. Application in Different Layout

To further verify the effectiveness of the model in power modules with different layouts, a multichip module with a new layout from Cree is optimized in this section [34]. The layout of the power module is shown in Fig. 21(a), where 3 SiC MOSFETs are paralleled. Due to the symmetry of the analysis, only low-side MOSFETs are analyzed.

In the initial state, the dynamic current balance of the low-side MOSFETs is suboptimal, as shown in Fig. 22(a). The differences in peak current are $\Delta i_{4\_5} = 13.3$ A and $\Delta i_{5\_6} = 0.08$ A, respectively. Simultaneously, M_{4_5} and M_{5_6} are 1.31 and 0.19, respectively. The connection points of the bonding wires for low-side MOSFETs are then modified, as shown in Fig. 21(b). Subsequently, the differences in peak current are $\Delta i_{4\_5} = -0.30$ A and $\Delta i_{5\_6} = 0.33$ A, as shown in Fig 22(b).

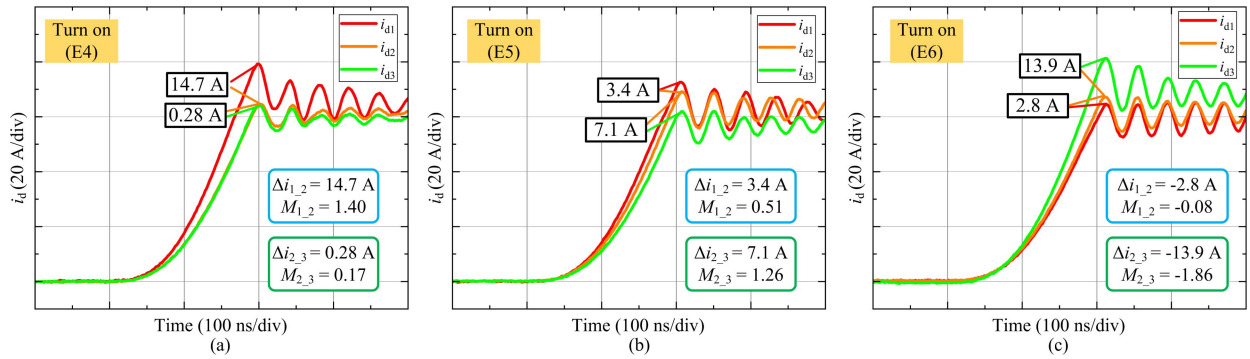

Fig. 19. High-side turn-ON current waveforms of Module E4–E6. (a) Module E4. (b) Module E5. (c) Module E6.

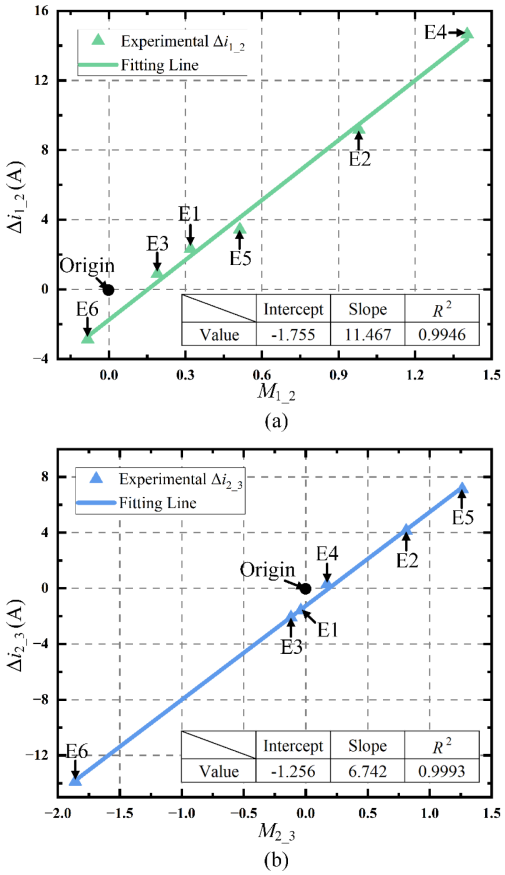

Fig. 20. Experimental relationship between current peak differences and JCs of Q1–Q3. (a) Graph of Δi_{1_2} versus M_{1_2}. (b) Graph of Δi_{2_3} versus M_{2_3}.

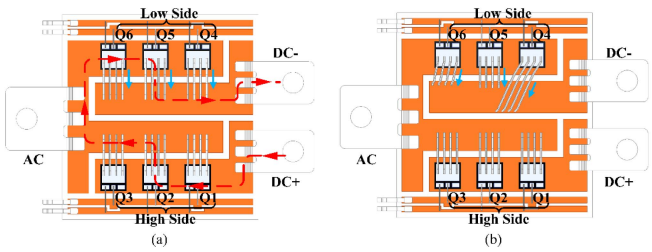

Fig. 21. Multichip SiC power module with new layout. (a) Initial module. (b) Optimized module.

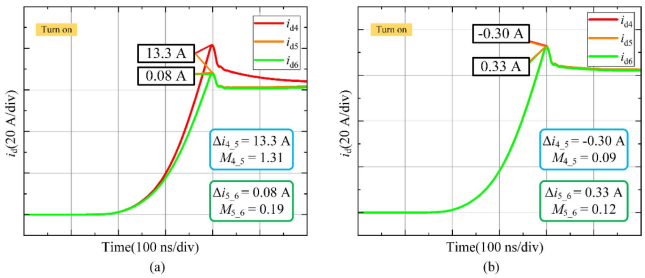

Fig. 22. Dynamic current of new layout. (a) Low side of initial module. (b) Low side of optimized module.

M_{4_5} and M_{5_6} are 0.09 and 0.12, respectively. It demonstrates that when the judgment coefficient is close to 0, the dynamic current balance is effectively achieved in the module with the new layout. The effectiveness of the proposed model in power modules with different layouts is verified.

VII. Application of the Model in Layout Optimization of Multichip Power Module

Previous models that considered mutual inductance coupling only analyzed several layouts [29], [30], [31], and dynamic current sharing optimization considering mutual inductance coupling has not yet been proposed. Passive dynamic current sharing methods in [18], [19], [20], [26], [27], and [28] are primarily based on balanced self-inductances. However, according to Section III, dynamic current sharing performance is not only affected by the internal self-inductances and mutual inductances of the power loops (M_{Ppower}) but also the mutual inductances coupling between the power loops to the driving gate loops (M_{Pdrive}). To further describe the contribution of this article, a model-based dynamic current sharing layout optimization considering mutual inductance coupling is presented below.

As shown in Fig. 1, for low-side MOSFETs, dynamic current sharing performance can be improved by optimizing the width (w) of the low-side gate copper trace and the distance (x) between the gate and the power source copper trace to adjust M_{Pdrive}. The flowchart of the model-based layout optimization is shown in Fig. 23. In Q3D, w and x are set as variables, and the proposed

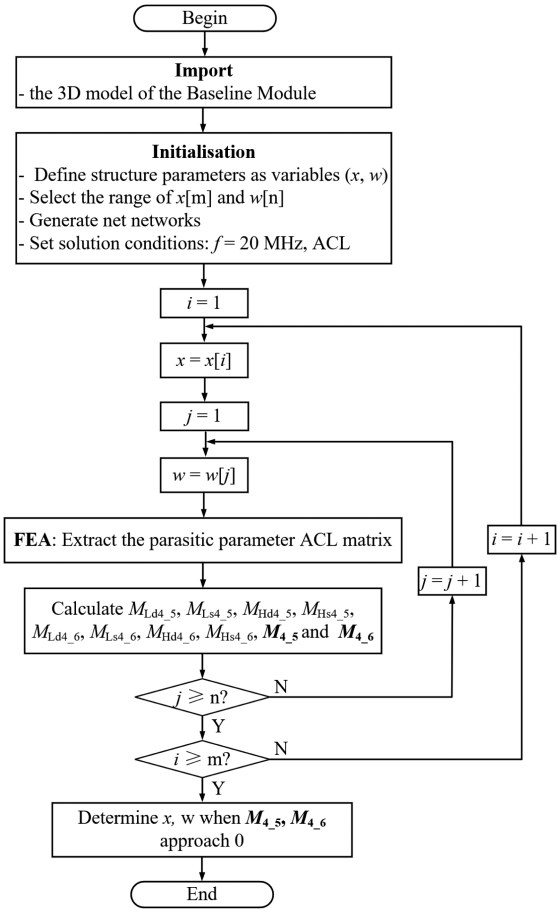

Fig. 23. Layout optimization flowchart based on the proposed model.

JCs are set as output variables. The variable range for w is from 0.1 mm to 2 mm, and for x is from 0.1 mm to 0.9 mm.

The source inductance imbalance ΔL_s and JCs versus w and x is shown in Fig. 24. As shown in Figs. 24(a) and (b), imbalanced power source inductances ΔL_s change very little. This is mainly because the power loops have not been changed. However, JCs decrease as x and w decrease, as shown in Fig. 24(c) and (d). It shows that as the gate copper trace is adjusted, the impact of the mutual inductances between the power branches and the gate branches further offsets the impact of other inductances and mutual inductances.

Considering the manufacturing process limitations of DBC, $w = 0.3$ mm and $x = 0.3$ mm were selected as $M_{4\_5} = 1.28$ and $M_{5\_6} = 0.56$, which are smaller than the origin JCs ($M_{4\_5} = 1.92$ and $M_{5\_6} = 0.88$). Before and after optimization, the turn-ON waveform is shown in Fig. 25. By simple adjustments of the gate copper trace, the maximum current difference is reduced by 42.3%, from 27.4 to 15.8 A.

Although completely balanced currents are not achieved, a model-based optimization idea for adjusting mutual inductance coupling is presented. Based on this idea, more dynamic current sharing optimization methods can be proposed in the future and more balanced current sharing can be achieved by simultaneously adjusting the power loop inductances and various mutual inductances, which can be future research works.

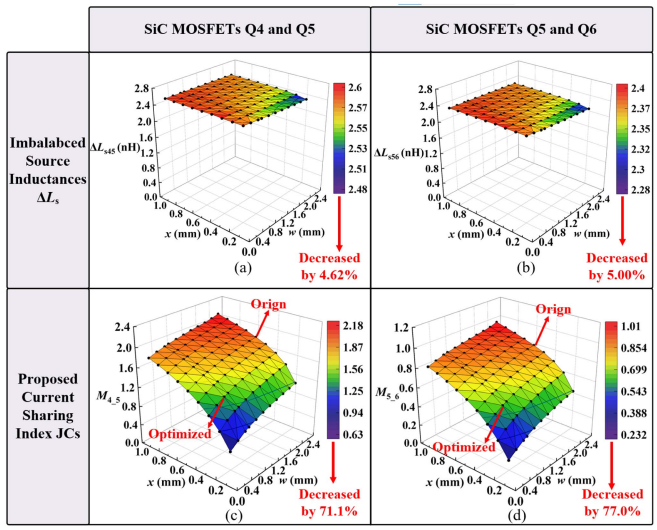

Fig. 24. Surface diagrams of various parameters versus x and w. (a) ΔL_{s45}. (b) ΔL_{s56}. (c) M_{4_5}. (d) M_{5_6}.

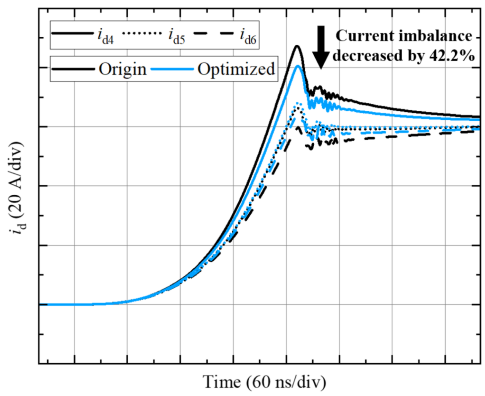

Fig. 25. Transient current comparison of low-side MOSFETs before and after layout optimization.

VIII. Conclusion

This article presents a dynamic current sharing model considering all parasitic inductances and parasitic mutual inductances. Based on this model, the dynamic current sharing mechanism about unbalanced inductances and mutual inductance is analyzed. The phenomenon that unbalanced high-side source inductances cause balanced high-side dynamic currents is explained. Furthermore, a more accurate dynamic current sharing access index is obtained compared to the existing model. When JCs = 0, the dynamic currents are balanced well and JCs and the current differences remain linear. Simulations and experiments have both validated the accuracy and linearity of JCs by power modules with different connection points of bonding wires, and the model also guides the optimization design of the connection points. Moreover, a model-based layout optimization is presented based on adjusting mutual inductances. By adjusting the shape and position of the gate copper trace, the dynamic current imbalance is improved.

The contributions of the model in the current sharing optimization design are discussed as follows. First, the mechanisms of various unbalanced inductances and mutual inductances can be used to guide design. In actual designs of multichip power modules, current sharing performance can be improved not only by adjusting self-inductances but also by adjusting the mutual inductances. Based on this idea, many new current sharing optimization methods can be proposed, such as those shown in Section VII. Furthermore, a more accurate dynamic current evaluation index than existing models can improve the effectiveness of various optimization methods. For example, in the presented connection points optimization, more balanced currents can be obtained, due to considering mutual inductances. Furthermore, the model can also be applied in current sharing Clip structural design and layout optimization. It can be researched in future work.

APPENDIX

For the high-side MOSFETs, the parameters $M_{\mathrm{pp1\_2}}$, $M_{\mathrm{pg1\_2}}$, $M_{\mathrm{pp2\_3}}$, and $M_{\mathrm{pg2\_3}}$ are derived [31]

$$\begin{cases} M_{\mathbf{pp1\_2}} = L_{\mathbf{d1}} + L_{\mathbf{s1}} + 2M_{\mathbf{Ld1Ls1}} - L_{\mathbf{d2}} - L_{\mathbf{s2}} \\ \quad -2M_{\mathbf{Ld2Ls2}} \\ M_{\mathbf{pp2\_3}} = L_{\mathbf{d2}} + L_{\mathbf{s2}} + 2M_{\mathbf{Ld2Ls2}} - L_{\mathbf{d3}} - L_{\mathbf{s3}} \\ \quad -2M_{\mathbf{Ld3Ls3}} \end{cases} \tag{A1}$$

$$\begin{cases} M_{\mathbf{pg1\_2}} = M_{\mathbf{Ld1Lg1}} + M_{\mathbf{Ld1Lk1}} + M_{\mathbf{Ls1Lg1}} + M_{\mathbf{Ls1Lk1}} \\ \quad - M_{\mathbf{Ld2Lg2}} - M_{\mathbf{Ld2Lk2}} - M_{\mathbf{Ls2Lg2}} - M_{\mathbf{Ls2Lk2}} \\ M_{\mathbf{pg2\_3}} = M_{\mathbf{Ld2Lg2}} + M_{\mathbf{Ld2Lk2}} + M_{\mathbf{Ls2Lg2}} + M_{\mathbf{Ls2Lk2}} \\ \quad - M_{\mathbf{Ld3Lg3}} - M_{\mathbf{Ld3Lk3}} - M_{\mathbf{Ls3Lg3}} - M_{\mathbf{Ls3Lk3}}. \end{cases} \tag{A2}$$

Similarly, for the low-side MOSFETs, the parameters $M_{\mathrm{pp4\_5}}$, $M_{\mathrm{pg4\_5}}$, $M_{\mathrm{pp5\_6}}$, and $M_{\mathrm{pg5\_6}}$ are as follows:

$$\begin{cases} M_{\mathbf{pp4\_5}} = L_{\mathbf{d4}} + L_{\mathbf{s4}} + 2M_{\mathbf{Ld4Ls4}} - L_{\mathbf{d5}} - L_{\mathbf{s5}} \\ \quad -2M_{\mathbf{Ld5Ls5}} \\ M_{\mathbf{pp5\_6}} = L_{\mathbf{d5}} + L_{\mathbf{s5}} + 2M_{\mathbf{Ld5Ls5}} - L_{\mathbf{d6}} - L_{\mathbf{s6}} \\ \quad -2M_{\mathbf{Ld6Ls6}} \end{cases} \tag{A3}$$

$$\begin{cases} M_{\mathbf{pg4\_5}} = M_{\mathbf{Ld4Lg4}} + M_{\mathbf{Ld4Lk4}} + M_{\mathbf{Ls4Lg4}} + M_{\mathbf{Ls4Lk4}} \\ \quad - M_{\mathbf{Ld5Lg5}} - M_{\mathbf{Ld5Lk5}} - M_{\mathbf{Ls5Lg5}} - M_{\mathbf{Ls5Lk5}} \\ M_{\mathbf{pg5\_6}} = M_{\mathbf{Ld5Lg5}} + M_{\mathbf{Ld5Lk5}} + M_{\mathbf{Ls5Lg5}} + M_{\mathbf{Ls5Lk5}} \\ \quad - M_{\mathbf{Ld6Lg6}} - M_{\mathbf{Ld6Lk6}} - M_{\mathbf{Ls6Lg6}} - M_{\mathbf{Ls6Lk6}}. \end{cases} \tag{A4}$$

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Zexiang Zheng received the B.S. degree in electrical and electronic engineering in 2023 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include wide-bandgap devices modeling, packaging, and high power density inverters.

Cai Chen (Member, IEEE) received the B.S. and Ph.D. degrees in electrical and electronic engineering from Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2014, respectively.

He is an Associate Research Fellow with Huazhong University of Science and Technology. From March to December 2013, he was an Intern with GE Global Research Center, Shanghai, China. From 2014 to 2016, he was the Advanced Semiconductor, Packaging and Integration Lab, Huazhong University of Science and Technology, Wuhan, China, as a Postdoctoral Researcher. From 2016 to 2017, he was a visiting scholar with the Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. From 2017 to 2018, he was a visiting scholar with the College of Engineering, University of Arkansas, Fayetteville, AR, USA. In 2019, he was with the Huazhong University of Science and Technology, Wuhan, China, as an Associate Research Fellow. His research interests include WBG devices packaging, integration, packaging EMI issues, packaging reliability, and high-density applications.

Jianwei Lv received the B.S. degree in electrical and electronic engineering in 2020 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include WBG devices modeling, packaging, and integration.

Yiyang Yan received the B.S. degree in functional material and electrical and electronic engineering from Huazhong University of Science and Technology, Wuhan, China, in 2018, and the M.S. degree in electrical engineering from the School of Electrical and Electrical Engineering, Huazhong University of Science and Technology, in 2021. He is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology.

His current research interests include wide-bandgap devices double-sided cooling package, high power density inverters, and package thermal modeling.

Jiaxin Liu was born in Liaoning, China, in 1995. She received the B.S. degree in material processing engineering from the School of Materials Science and Engineering, Northeastern University, Shenyang, China, in 2018, and the Ph.D. degree in mechanical manufacturing and automation from the School of Mechanical Science and Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2023.

From 2023, she was with the Advanced Semiconductor, Packaging, and Integration Laboratory, Huazhong University of Science and Technology, as a Postdoctoral Researcher. Her research interests include wide-bandgap device packaging, micro/nano low-temperature bonding technology, and electronic packaging reliability.

Yong Kang (Fellow, IEEE) was born in Hubei Province, China, in 1965. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan China, in 1988, 1991, and 1994, respectively.

In 1994, he was with Huazhong University of Science and Technology as a Lecturer and was promoted to Associate Professor in 1996 and to Full Professor in 1998. He has authored more than 60 technical papers. His research interests include power electronic converter, ac drivers, electromagnetic compatibility, their digital control techniques, WBG device packaging, and applications.