Synthesis and Classification of Boost/Buck Structures for Getting Transformerless Hybrid Bidirectional DC–DC Converters

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***Abstract*—In this article a synthesis, comparative analyses, and architecture classification of the family of bidirectional boost/buck power converters is done taking into account the low voltage dc bus as input and high voltage as output. The classification can be input/output as series or parallel, where the series characteristic is the voltage division between the modules, while the parallel characteristic presents the current division feature. Also, in this article, an architecture is shown, which presents the characteristics of both, the parallel and series approach, at the same time. The theoretical analyses about voltage and current stresses, as well as voltage gain is carried out and validated through experimental results for nine prototypes that were built in the laboratory. The efficiency curves was extracted from 500 W to 1 kW.**

***Index Terms*—Bidirectional dc–dc converter, boost, buck, classification.**

I. Introduction

IN RECENT years, with the growing demand for more efficient and sustainable solutions in the transportation sector, electrification has become increasingly popular [1]. This way, many studies have evaluated approaches to synthesis and derivation of converter topologies [2], [3], [4], [5]. These surveys allow new topologies to be created and establish evaluation criteria. Usually, these factors include voltage gain, voltage and current stress on the components, efficiency and losses on the components, volume, power density, cost and others. Overall, this allows to choose the best topology and application that can be applied [2], [3]. In applications such as electric vehicles, uninterruptible power supply (UPS), renewable integrations, and microgrid, there is a need to use converters to step-up or step-down the voltage levels provided by the systems. Since in these applications there are energy storage systems, bidirectional dc–dc converters are required to guarantee a good performance [4], [5].

In this sense, nonisolated bidirectional dc–dc converters have become attractive for such applications. Since these converters have lower cost and complexity of operation, in addition to being more efficient. For systems where galvanic isolation is not required, the bidirectional dc–dc boost/buck converter stands out, Fig. 1(a). This converter is composed by two switches (S_{in1} and S_{in2}), one inductor (L_1) and two capacitors (C_L and C_H) which represents the low (V_L) and high (V_H) dc bus voltage, respectively. This converter can work to interface both buses in a way robust and simple, which allows the dual power flux. However, the switches voltage stress is equal to the high dc bus voltage (V_H), which implies high voltage stress and require switches with high static drain-to-source ON-resistance ($R_{DS(ON)}$). Also, the inductor L_1 supports all low dc current (I_L). This set of factors increases the conduction losses which compromises the efficiency of the converter.

Considering the above aspects, several topologies of bidirectional dc–dc converters have been proposed. In [6], the standard boost/buck dc–dc converter is combined with the ladder of switched capacitor cell. This approach allows to increase the voltage gain of the converter and reduce the voltage stress on semiconductors. However, this converter may suffer high current stress due to the switched capacitors cell. A well-known technique is the coupled inductor which is used in [7]. By adjusting the turns ratio (N) of coupled inductor, high voltage gain can be achieved. This technique is simple in terms of operation and control. In the meantime, due to leakage inductance (L_k) of the coupled inductor, voltage spikes across the semiconductors increase which increase the switching losses. To get around this, resonant cell can be used [8], [9], [10]. This approach allows the converter to reach high voltage gain with soft-switching. However, the operation and control complexity of this type of converter is high. To sum up, in recent years, there has been growing interest in bidirectional dc–dc converter, this way some research demonstrates a literature review of these approach [11], [12]. However, in a general manner, these converters have been proposed in an isolated way, which makes it difficult to assess which one is better or worse.

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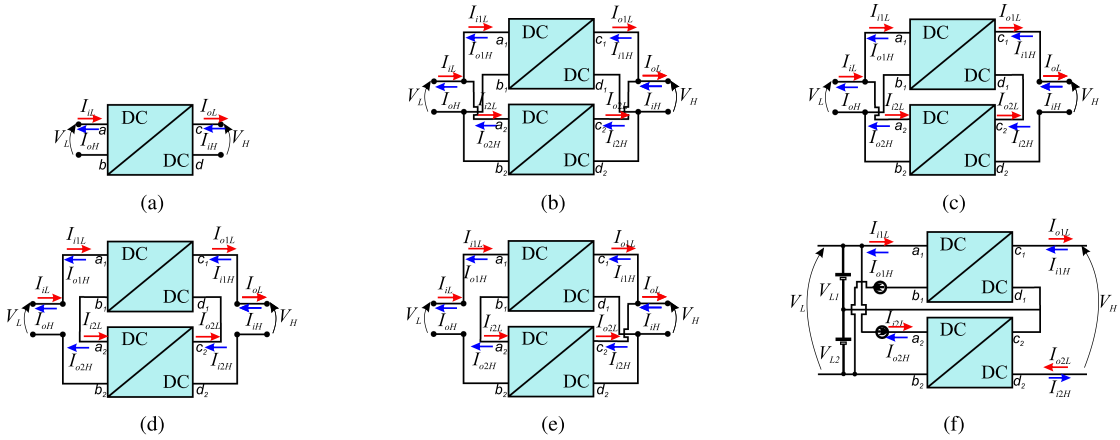

Fig. 1. Topological architecture of the family of boost/buck bidirectional nonisolated power converters. (a) Standard. (b) Parallel Input Parallel Output (PIPO). (c) Parallel Input Series Output (PISO). (d) Series Input Series Output (SISO). (e) Series Input Parallel Output (SIPO). (f) Hybrid Series and Parallel Input Series Output (SPISO).

To provide a concise assessment, this article suggests a synthesis approach to understand the creation of bidirectional dc–dc converter topologies based on the standard boost/buck converter. This methodology provides insight into well-known circuits techniques which can be applied in different applications. These circuits can be classified as standard, series, or parallel. In addition, a detailed comparison of the topologies is carried out.

The rest of this article is organized as follows. The classification of the family of bidirectional boost/buck dc–dc converters is presented in Section II. In Section III, a static analysis about component count, voltage gain, voltage, and current stresses is done, while the experimental validation are presented in Section IV. Finally, Section V concludes this article.

II. Classification of the Bidirectional Converters

The classification of the bidirectional power converters will be given taking into account the V_L bus as input and V_H bus as output. Fig. 1 shows the circuits blocks formed by PWM dc–dc converters structures, while the family of bidirectional boost/buck power converters are shown in Fig. 2. These structures and the converters that can be generated are detailed below.

A. Standard Structure

The standard structure diagram is shown in Fig. 1(a). This structure is composed of a single converter. Usually, this topology is a classical converter proposed in the literature. In general, in this type of configuration, the components of this converter support all current (I_L) of the low voltage bus (V_L) and also support the bus voltage (V_H). It is evident that the current and voltage stress of this type of configuration are high. This will imply that the losses are high and consequently, the efficiency tends to be low.

The classical buck/boost converter [13] belongs to this class. This converter presents simplicity of operation, low components count, and facility of control. However, the components show high current and voltage stresses across semiconductor devices.

In this work, the classical bidirectional boost/buck converter serves as a module for the synthesis of the others. In Fig. 1(a), the points a and b are used to denote the input ports, while c and d denote the output ports of a single module. By connecting these points of two or more single modules, it is possible to achieve series and parallel characteristics, both at the input and output, thus, generating the family of bidirectional boost/buck converters, demonstrated in this article.

B. PIPO Structure

PIPO structure diagram is shown in Fig. 1(b). To synthesize the totally parallel connection, basically, two single modules are combined in parallel on both the V_L side and the V_H side, connecting the points a_1 with a_2; b_1 with b_2; c_1 with c_2; and d_1 with d_2. One of the advantages is the reduction of the current stress since the current I_L of the low voltage bus V_L is shared between the topologies and conduction power losses are decreased and a higher power density can be achieved [14]. Besides that, phase shift strategy allows to decrease the current ripple in V_L bus [15]. However, there is no increase in voltage gain and the components still support the V_L bus voltage. Also, a complex control system is required as due the nonidealities the parallel modules present current unbalance [16].

Fig. 1(b) shows the simplified diagram of PIPO bidirectional converters, where it is shown the paralleling of the modules. Some of PIPO converters founded in the literature are the PBB [17], presented in Fig. 2(b), which present the same voltage gain of the classical module. Due to its entirely parallel characteristic, this converter may exhibit an inverse efficiency feature, with its efficiency being lower at lower power and increasing efficiency as power increases. Rearranging the components is possible to achieve higher voltage gain with the BB-SI [18], shown in Fig. 2(c).

C. PISO Structure

PISO structure is shown in Fig. 1(c). In this configuration the input section of the single modules is connected in parallel while their outputs are in series [19]. In structure terms, the parallel characteristic is created by connecting points a_1 with a_2 and b_1 with b_2, while the series characteristic is created by connecting

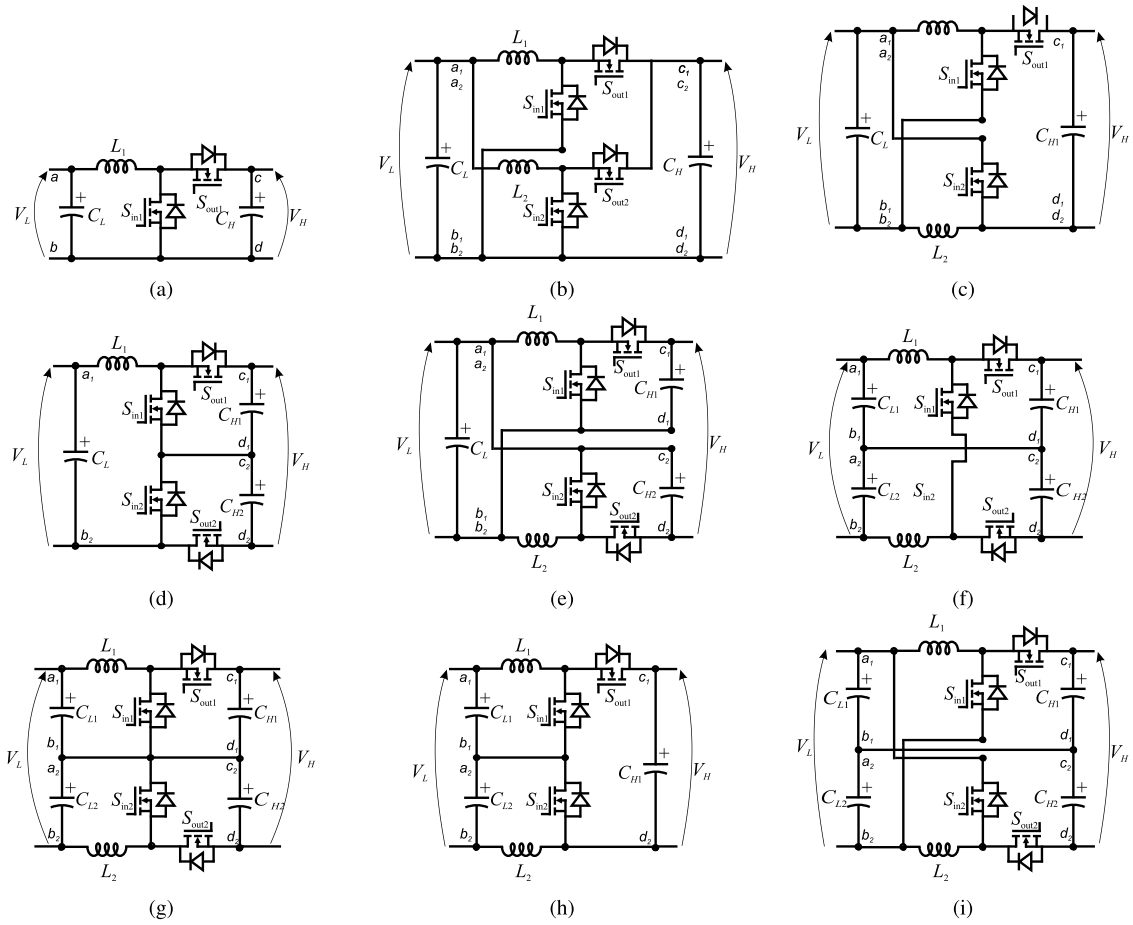

Fig. 2. Topological architecture of the family of boost/buck bidirectional nonisolated power converters. (a) Classical. (b) Parallel buck/boost (PBB). (c) Buck/boost based in switched inductor (BB-SI). (d) Single inductor double boost (SIDB). (e) Boost/buck based in switched inductor with differential output (BB-SID). (f) Single boost dual buck (SBDB). (g) Dual boost dual buck (DBDB). (h) Dual boost single buck (DBSB). (i) Dual stacked buck/boost (DSBB).

points d_1 with c_2. Therefore, points c_1 and d_2 are used as the output ports of these structures. The high current from V_L bus and the high voltage from V_H are divided between the modules. In this way low current stresses at the input and low voltage stress at the output is achieved. The parallel characteristic allows decreasing the conduction power losses [24] and decrease the switching frequency when a phase shift PWM is used [20]. Besides that, since the output section are in stacked connection, the voltage gain of the topology is increased.

In this way, the converter SIDB [21] is presented in Fig. 2(d). As can be seen, this converter has only one inductor. So, this inductor presents high current stress which it is not desirable for this configuration. On the other hand, to decrease the current stress, BB-SID [22] is shown in Fig. 2(e). However, this converter presents higher voltage stress across semiconductor devices.

D. SISO Structure

SISO structure diagram is shown in Fig. 1(d). SISO systems are used to achieve low voltage stress across semiconductor devices as it is clamped by fractions of V_L and V_H [23]. To synthesize this structure from single modules, points a_1 and b_2 are used as input ports. Points b_1 and a_2 are connected together to create the series characteristic at the input. At the output, this characteristic is achieved by connecting points d_1 and c_2, while points c_1 and d_2 serve as the output ports of these structures.

This topology can achieve high voltages due to the stacked connection of the output capacitors of each converter [24]. Some topologies belonged to this class present voltage unbalance between the modules which affect the efficiency [25]. This voltage unbalance brings stability problems and hence make these converters needs a special control systems [26].

The converter SBDB is shown in Fig. 2(f). This converter presents the same voltage gain of classical boost/buck. Besides that, at least one switch achieves higher voltage stress. To improve the voltage stress in all of the switches, keeping the same voltage gain, the converter DBDB [27] is presented in Fig. 2(g).

E. SIPO Structure

SIPO structure diagram is shown in Fig. 1(e). In this configuration, the input section of the converters is connected in series while the output section are in parallel. To create this structure, points a_1 and b_2 are used as input ports. Points b_1 and a_2 are connected together to create the series characteristic at the input. The parallel characteristic at the output is created by connecting

points c_1 with c_2 and d_1 with d_2. Each module support only a fraction of V_H voltage [28]. Besides that, phase shift can be used in order to decrease the current ripple of V_L bus voltage [29]. Usually, this topology is recommended when high voltage is required at V_L and high current at V_H [24].

The converter DBSB [27] is presented in Fig. 2(h). In this converter, the input switches achieve low voltage stress, while the output switch present high voltage stress.

F. SPISO Structure

SPISO structure diagram is shown in Fig. 1(f). In general, this class presents all advantages of other classes. This means, the voltage is divided in series while the current in parallel on the components.

To create this special structure, the parallel portion of the input is obtained by connecting points a_1 with a_2 and b_1 with b_2. The series portion of the input is obtained externally by connecting points d_1 with c_2 to the node created by the parallel connection. The series part of the output is obtained by connecting points d_1 with c_2 and using points c_1 and d_2 as output ports.

In this way, low voltage and current stresses across the semiconductors devices can be achieved. Besides that, the capacitors of the converters are in stacked connection which increases the voltage gain of the topology.

There is only one bidirectional converter known belonged to this class, the DSBB [30] shown in Fig. 2(i). The topology presented in Fig. 2(i) is based on active switched inductor cell, where the inductors are magnetized in parallel with V_L bus creating the parallel characteristic. To create a switching phase shift the capacitors C_{L1}, C_{L2}, C_{H1}, and C_{H2} are added and hence, the switches are clamped by these capacitors creating the series characteristic at input.

III. Comparison Analysis

The bidirectional dc–dc converters present distinct features. So, in this section, these converters are compared in terms of static gain, voltage stress, current stress, current ripple, component count, estimated losses, and efficiencies.

A. Static Voltage Gain

The static voltage gain is obtained using volt-second balance on the inductors for step-up and step-down mode. For clarity, below is presented the voltage gains of the converters for each mode. For step-up mode, the converters shown in Fig. 2(a), (b), (d), (f), (g), and (h), their voltage gain are given by

$$\frac{V_H}{V_L} = \frac{1}{1-D} \tag{1}$$

while, the converters shown in Fig. 2(c), (e), and (i), their voltage gain are given by

$$\frac{V_H}{V_L} = \frac{1+D}{1-D}. \tag{2}$$

Fig. 3(a) shows the static gain for step-up mode of the converter as function of duty cycle (D). As can be observed, the converter represented by the green curve has higher voltage gain.

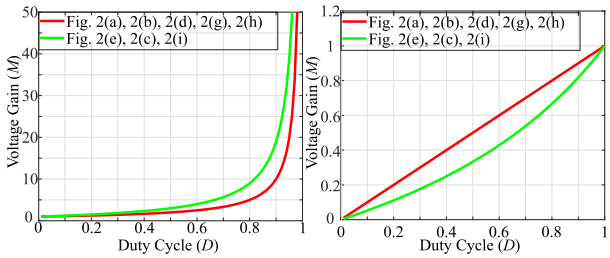

Fig. 3. Static gain for: (a) Step-up mode. (b) Step-down mode.

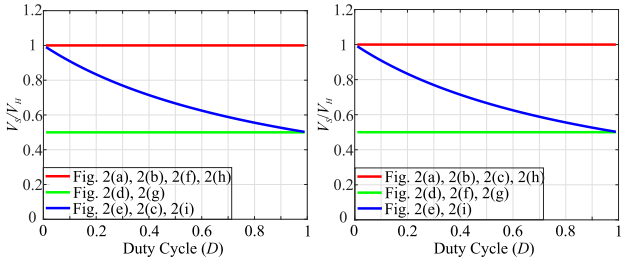

Fig. 4. Normalized voltage stress on (a) Switches of V_L side. (b) Switches of V_L side.

For step-down mode, the converters shown in Fig. 2(a), (b), (d), (f), (g), and (h), their voltage gain are given by

$$\frac{V_L}{V_H} = D \tag{3}$$

while, the converters shown in Fig. 2(c), (e), and (i), their voltage gain are given by

$$\frac{V_L}{V_H} = \frac{D}{2-D}. \tag{4}$$

Fig. 3(b) shows the static gain for step-up mode of the converter as function of duty cycle (D). As can be observed, the converter represented by the green curve has lower voltage gain. In this way, it can be highlighted that the configurations PISO, PIPO, and SPISO present better characteristics in relation to the static gain.

B. Voltage Stresses

The voltage stress on the semiconductor devices is the same for step-up and step-down operation. They are presented in Table I in terms of V_L and V_H voltages. In Fig. 4(a) and (b), the behavior of the voltage stress on the switches normalized by the V_H is presented. Both converters, Fig. 2(d) and (g), present the lower voltage stress on the switches. So, this topologies can be used switches with lower $R_{DS(ON)}$. In this way, it can be highlighted that the configurations PISO and SISO present better characteristics in relation to voltage stress.

C. Current Stress

The mathematical expression for the current through the semiconductors devices are presented in Table I. Fig. 5(a) and (b) shows the current of the switches normalized by the I_L. The

TABLE I
CONVERTERS COMPARATIVE TABLE

Converter	Maximum voltage stress on input switches	Maximum voltage stress on output switches	I_{Sin}	I_{Sout}	I_L/I_H Current ripple	Switches count	Inductors count	Capacitors count
Fig. 2a	V_H	V_H	$I_L\sqrt{D}$	$I_L\sqrt{1-D}$	Low/High	2	1	2
Fig. 2b	V_H	V_H	$\frac{I_L}{2}\sqrt{D}$	$\frac{I_L}{2}\sqrt{1-D}$	Low/Low	4	2	2
Fig. 2c	$\frac{V_H+V_L}{2}$	V_H	$\frac{I_L}{1+D}\sqrt{D}$	$\frac{I_L}{1+D}\sqrt{1-D}$	Medium/High	3	2	2
Fig. 2d	$\frac{V_H}{2}$	$\frac{V_H}{2}$	$I_L\sqrt{D}$	$I_L\sqrt{1-D}$	Medium/High	4	1	3
Fig. 2e	$\frac{V_H+V_L}{2}$	$\frac{V_H+V_L}{2}$	$\frac{I_L}{1+D}\sqrt{D}$	$\frac{I_L}{1+D}\sqrt{1-D}$	Low/High	4	2	3
Fig. 2f	V_H	$\frac{V_H}{2}$	$I_L\sqrt{D}$	$I_L\sqrt{1-D}$	Low/High	3	2	4
Fig. 2g	$\frac{V_H}{2}$	$\frac{V_H}{2}$	$I_L\sqrt{D}$	$I_L\sqrt{1-D}$	Low/High	4	2	4
Fig. 2h	$\frac{V_H}{2}$	V_H	$I_L\sqrt{D}$	$I_L\sqrt{1-D}$	Low/High	3	2	3
Fig. 2i	$\frac{V_H+V_L}{2}$	$\frac{V_H+V_L}{2}$	$\frac{I_L}{1+D}\sqrt{D}$	$\frac{I_L}{1+D}\sqrt{1-D}$	Medium/High	4	2	4

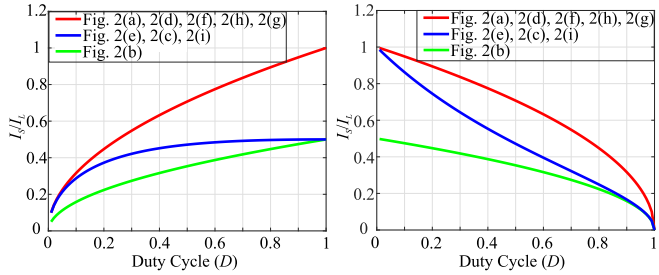

Fig. 5. Normalized current stress on (a) Switches of V_L side. (b) Switches of V_L side.

converter presented in Fig. 2(b), PIPO structure, presents better characteristics in relation to the current stress. Furthermore, this structure allows achieving better input and output current ripple characteristics, as can be seen in the Table I.

D. Component Count

In Table I is presented the component count. The converters from Fig. 2(g) and (i) present the most number of component, followed by Fig. 2(e), (f), (b), (d), (h), (c), and (a).

E. Estimated Losses and Efficiencies

In order to select the best structure/topology in efficiency terms, in this section the estimated theoretical losses and efficiencies are presented. It assumes that the converters operate with the parameters presented in Table II. The used methodology to obtain the efficiency and the losses distribution is presented in [31] and consist of the use mathematical model to get power losses in the components.

The switches present two kind of losses as follows: 1) ohmic and 2) switching losses. The ohmic losses are deduced using the parasitic ON resistance ($R_{DS}(\text{ON})$), while the switching depends of the rise (t_{ON}) and fall (t_{OFF}) times. The complete deduction of

TABLE II
EXPERIMENTAL PARAMETERS

Symbol	Parameter	Value
P_o	Output power	1 kW
V_H	High side voltage	400 V
V_L	Low side voltage	144 V
f_s	Switching frequency	50 kHz
S_{in1}, S_{in2} S_{out1}, S_{out2}	Switches of converter in Fig. 2(a), 2(b), 2(c), 2(f) and 2(h)	IRFP450 (540 V, 14 A, 0.38 Ω)
S_{in1}, S_{in2}, S_{out1}, S_{out2}	Switches of converter in Fig. 2(d), 2(e), 2(g) and 2(i)	IRFP4868 (300 V, 75 A, 32 mΩ)
L_1	Inductor of converter in Fig. 2(a)	530 uH (0.79 Ω)
L_1, L_2	Inductors of converter in Fig. 2(b)	1.5 mH (2.62 Ω)
L_1, L_2	Inductors of converter in Fig. 2(c), 2(d), 2(e), 2(f), 2(g), 2(h) and 2(i)	270 μH (0.4 Ω)
C_{L1}, C_{L2}, C_{H1}, C_{H2}	Capacitors	470 μF (0.29 Ω)

power losses coming from the switches are presented in

$$P_S = \underbrace{I^2_{S(RMS)} R_{DS(\text{ON})}}_{\text{Ohmic}} + \underbrace{0.5 F_s V_{DS} I_S (t_{\text{ON}} + t_{\text{OFF}})}_{\text{Switching}} \quad (5)$$

where $I_{S(RMS)}$, $R_{DS(\text{ON})}$, t_{ON}, and t_{OFF} are respectively the the RMS value of the current crossing through the switch, the resistance between drain and source, the turn ON time and the turn OFF time, all of these information can be get in the MOSFET datasheet.

The inductors perform Ohmic and magnetic losses, which is presented in

$$P_L = \underbrace{r_L {I_{L(rms)}}^2}_{\text{Ohmic}} + \underbrace{\left(a {B_{pk}}^b {f_s}^c\right) A_e l_e}_{\text{Magnetic}} \quad (6)$$

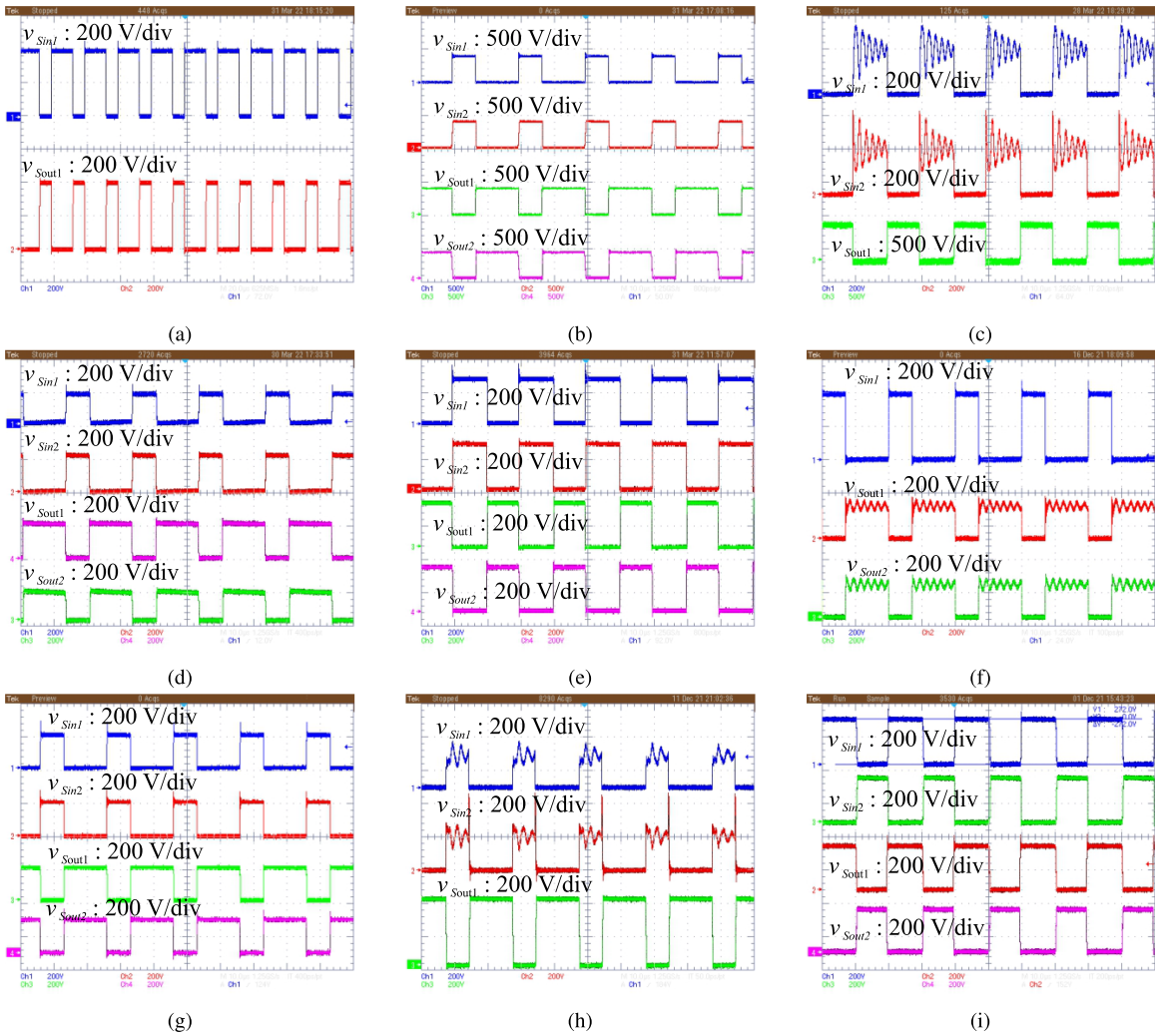

Fig. 6. Voltage across the semiconductor devices for converter in (a) Fig. 2(a). (b) Fig. 2(b). (c) Fig. 2(c). (d) Fig. 2(d). (e) Fig. 2(e). (f) Fig. 2(f). (g) Fig. 2(g). (h) Fig. 2(h). (i) Fig. 2(i).

where $I_{L(rms)}$ is the RMS current of the inductor; r_L is copper resistance; B_{pk} is the ac magnetic flux density for the magnetic device core; a, b, and c are constants determined from the curve fitting of the core; l_e is the core medium path length (MPL); and A_e is the transversal core area, provided in the manufacturing core part number datasheet.

The capacitors present only ohmic losses, as can be seen in

$$P_C = ESRI_{C(rms)} \tag{7}$$

where ESR is the series resistance of the capacitors, and $I_{C(rms)}$ is the RMS value of the current flowing through the capacitor.

The efficiency (η) of the converter can be determined as follows:

$$\eta = \frac{P_{\text{output}}}{P_{\text{losses}} + P_{\text{output}}} \tag{8}$$

where P_{losses} is the summation of all power losses in the components and P_{output} is the nominal output power.

Given the methodology, the theoretical losses distribution and efficiencies of evaluated converters are show in Fig. 9. The classical converter reaches 68.88 W of losses and 93.56% of efficiency, as depicted in Fig 9(a). The most part of the losses coming from the inductor due to its higher inductance and hence higher resistance. The converter PBB, a totally parallel modularization (PIPO) of the classical converter. This converter has the losses presented in 9(b), where it achieves a efficiency of 92.05% and power losses of 86.41 W. The converter BB-SI achieves one of the highest efficiencies. As shown in Fig. 9(c), it perform 96.39% of efficiency with only 37.49 W of losses. This elevated value of efficiency is due the PIPO characteristic allied with the high voltage gain, which allow to reduce the duty cycle and hence decreases the conduction losses. The PISO structure reaches a efficiency of 93.24% with 72.45 W of losses with the converter SIDB, as presented in Fig. 9(d). To become better the efficiency of SIPO class, the BB-SID converter decreases the duty cycle, having the losses depicted in Fig. 9(e), achieving 95.8% of efficiency with 42.95 W of losses. The SBDB converter, belonged to the SISO structure, have an efficiency of 92.45% with 81.61 W of losses, as mentioned in Fig 9(f). In SISO class, it can be improved by DBDB converter due it stacked connection of the input switches, allowing achieve low voltage

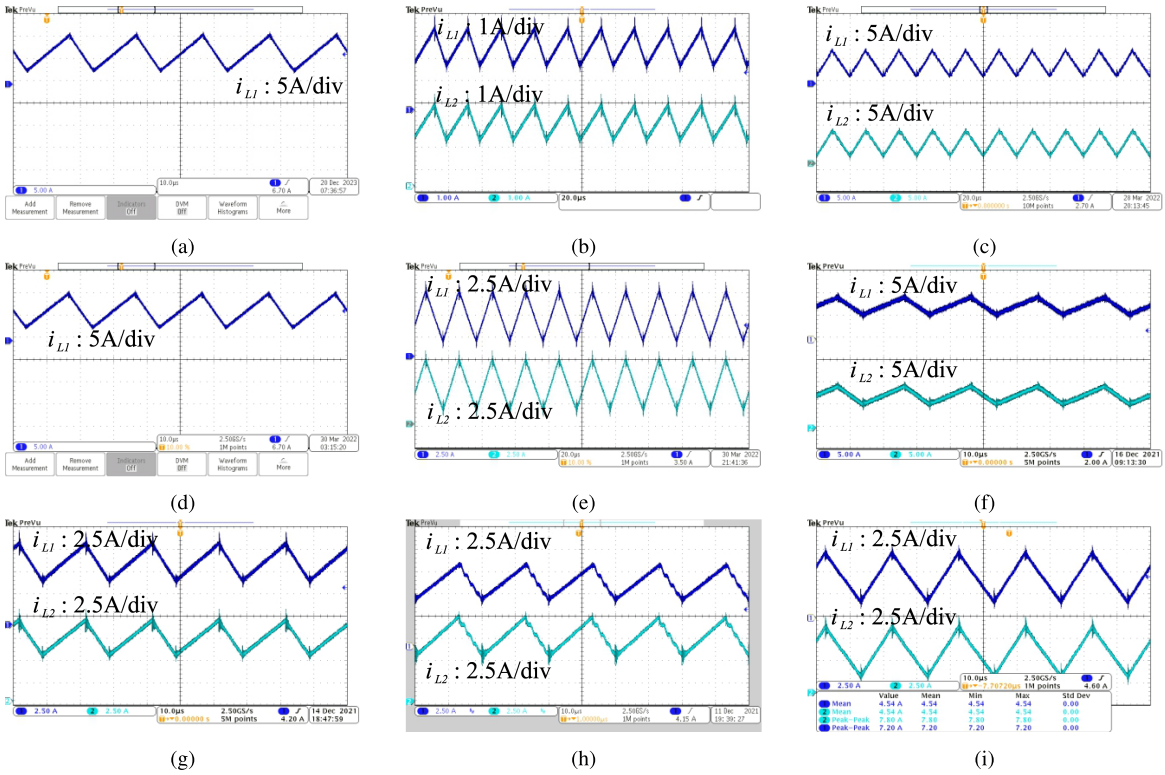

Fig. 7. Current through the inductors for converter in (a) Fig. 2(a). (b) Fig. 2(b). (c) Fig. 2(c). (d) Fig. 2(d). (e) Fig. 2(e). (f) Fig. 2(f). (g) Fig. 2(g). (h) Fig. 2(h). (i) Fig. 2(i).

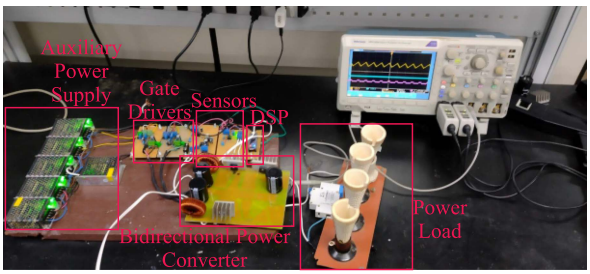

Fig. 8. Experimental setup.

stress and hence, low parasitic resistance in the semiconductor devices, this characteristic make the converter perform 94.73% of efficiency with 55.68 W of losses, as presented in Fig. 9(g). The SIPO structure is represented by the DBSB converter, achieving 94.4% of efficiency with 59.32 W of losses, as the features in Fig. 9(h). The hybrid structure (SPISO) performs the best efficiency between all of the structures/converters, it is possible owing this class demonstrate both series and parallel connection, decreasing at same time the voltage and current stresses across the semiconductors devices. The SPISO structure achieved 96.85% of efficiency and 32.47 W of losses, as shown in Fig. 9(i).

IV. Experimental Validation

In order to verify the effectiveness of the topologies, the converters presented in Table I were built in laboratory with parameters presented in Table II. In Fig. 8, the experimental setup can be seen, highlighting one of the bidirectional converters, auxiliary power supply, gate drivers, DSP, and power load. All of these converters were evaluated under the same power conditions. Furthermore, in their references, a switching frequency range of 35–70 kHz is mentioned. Therefore, was selected the intermediate point of 50 kHz for the converters operation. To establish the low and high voltage source (V_L and V_H), a Keysight N8762 A dc voltage source was used in the experimental converters. A STM32F411 Digital Signal Processor was implemented to provide the PWM signal. Finally, a Yokogawa WT1800 power meter was used to measure the efficiency.

A. Voltage Stress

In Fig. 6 is presented the experimental results of the voltage stress on the semiconductor devices. The converters in Fig. 2(a), (b), (d), (e), (g), and (i) have a natural clamping system, therefore, there are no over voltage or resonance process in it switches, then, the practical voltage stress matched exactly with the static analysis. However, converters from Fig. 2(c) and (h) does not have a natural clamping system, thus, presenting over voltage due the resonance process caused by the switches parasitic capacitance with the PCB parasitic inductance. This process also occurs to converter in Fig. 2(f), but in this case the over voltage is minimum, being possible ignore it.

B. Current Stress

As the current of all switches is reflected in the inductors current, the Fig. 7 present the inductors current. The inductors

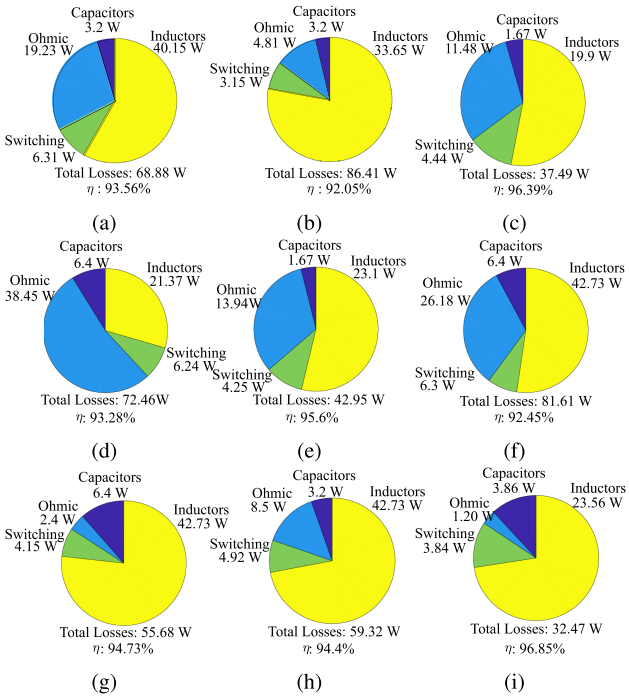

Fig. 9. Losses distribution and efficiencies for converters (a) Classical. (b) PBB. (c) BB-SI. (d) SIDB. (e) BB-SID. (f) SBDB. (g) DBDB. (h) DBSB. (i) DSBB.

were designed to have a very close relationship of the type (Δ_{IL}/IL_{AVG}) in all converters, always ensuring to maintain operation in continuous conduction mode (CCM). For converters in Fig. 2(a) and (b) to work in CCM is necessary high value of inductances to achieve it, for this, was used 530 μH and 1.5 mH, respectively, all of the others converters was used 270 μH. The converters from Fig. 2(a) showed a current ripple of 8 A. Converter in Fig. 2(b) perform a ripple of 1.8 A. The converters in Fig. 2(d), (f), (g), and (h) demonstrate a current ripple of 5, 8, 6, and 5 A, respectively. For the converters in Fig. 2(c), (e), and (i) shows a current ripple of 5, 4, and 6 A, in the same sequence.

C. Efficiency

The practical efficiency curves, extracted using the power meter, is shown in Fig. 10, where the positive power flux represent step-up mode and negative power flux represent step-down mode.

For nominal power (1 kW) step-up mode the converter presented in Fig. 2(i) achieved the highest efficiency (95,4%), followed by Fig. 2(e) (95.38%), Fig. 2(g) (94.1%), Fig. 2(d) (92.92%), Fig. 2(f) (91.315%), Fig. 2(h) (91%), Fig. 2(a) (87.5%), and Fig. 2(b) (86.11%).

For nominal power (1 kW) step-down mode the converter presented in Fig. 2(e) (96,3%) achieve the best efficiency, followed Fig. 2(i) (96.07%), 2(h) (96%), Fig. 2(d) (94,34%), Fig. 2(g) (93.03%), Fig. 2(b) (91.25%), Fig. 2(a) (89.6%), Fig. 2(c) (87.84%), and Fig. 2(f) (85.8%).

In terms of architecture classification, as expected the single module [Fig. 2(a)] presented one of the worst efficiency,

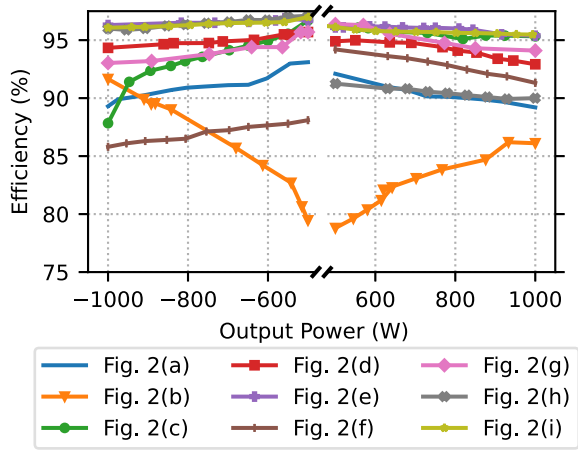

Fig. 10. Experimental output power versus efficiency.

TABLE III
ESTIMATED VS EXPERIMENTAL EFFICIENCIES FOR $P_o = 1$ KW

Converter	Estimated (%)	Experimental (%)
Fig. 2(a)	93.56	87.5
Fig. 2(b)	92.05	91.65
Fig. 2(c)	93.39	95.33
Fig. 2(d)	93.28	92.92
Fig. 2(e)	95.6	95.38
Fig. 2(f)	92.45	91.32
Fig. 2(g)	94.73	94.1
Fig. 2(h)	94.4	91
Fig. 2(i)	96.85	95.4

while converter with parallel architectures at the input presented the higher efficiencies. Besides that, the hybrid architecture (SPISO), which present series and parallel characteristic at input performed between the best efficiencies.

D. Comparison Between Estimated and Experimental Efficiency

In Table III, the estimated and experimental efficiencies of the converters studied in this research are presented considering the nominal power of $P_o = 1$ kW. It is noteworthy that there is an average error of approximately 2.05% between the estimated and experimental efficiencies. This error can be explained by system resonances, minor inaccuracies in the measurement equipment, and parametric variations in the converters.

V. CONCLUSION

This article presents a review of the architecture classification and make a complete comparative analyses of the family of bidirectional boost/buck dc–dc power converters and its main characteristics. This family is considered due to its low component number, facility of operation, high efficiency, low voltage and current stresses, and facility to control. Besides that, this family of nonisolated converter are the most used in microgrid systems and electrical vehicles.

The architecture classification was done taking into account the V_L bus as input and V_H bus as output and the input/output

are classified as series or parallel. The main advantage of series connection is the voltage division between the modules, which present low voltage stress in the switch devices, but this connection may present high current stress. While the parallel connection advantage is the current division between the modules, but this connection presents high voltage stress in the switches. The hybrid architecture presents all advantages without the disadvantages of the other architectures, such as: low voltage and current stresses, facility of operation, and simple control technique.

In terms of general efficiency, topologies that present parallel feature at input and/or series characteristic at output have higher efficiency. However, these topologies usually have more component count, specially switches count. The hybrid architecture (SPISO) due to demonstrate both characteristics of parallel and series, present one of the highest efficiency.

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