Study of the Influence of Different Gate Oxide Traps on Threshold Voltage Drift of SiC MOSFET Based on Transient Current

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***Abstract*—With the aim of resolving the threshold voltage drift problem of the silicon carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET), which is caused by traps, this article presents a study of the laws for the different traps that affect threshold voltage drift and also clarifies the details of the trap that leads to the SiC MOSFET threshold voltage drift. First, based on use of the transient current method for trap characterization, we eliminate the interference from the SiC bulk traps, and the time constant spectrum of the gate oxide trap is then obtained accurately. Second, the effects of the different traps on the threshold voltage are studied by filling or releasing the charges from traps with different time constants. The main trap time constant that leads to the SiC MOSFET threshold voltage drift is revealed to be 300 ms, whereas the other trap only affects the current and hardly contributes to the threshold voltage drift. Finally, based on the activation energies of the different traps, it is inferred that the trapping mechanism of the traps are the trap-assisted tunneling effect and the hot electron emission effect, and the corresponding trap types are identified as the oxide trap and the interface trap, respectively.**

***Index Terms*—Reliability, silicon carbide metal-oxide-semiconductor field-effect transistor (SiC MOSFET), threshold voltage, transient current method, trap characterization.**

I. Introduction

Silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) and their modules have characteristics that include small size, high temperature resistance, high operating frequencies, and low switching losses. These devices have a wide range of potential applications in fields with high power conversion requirements, including aerospace equipment, military weapon systems, power conversion systems, new energy vehicles, and industrial drives [1], [2], [3].

At present, the design and processing aspects of SiC MOSFETs are basically mature, and the biggest drawback that is restricting wider application of these devices stems from product reliability. The reliability of the gate oxide, which can cause threshold voltage (V_{th}) drift, is the main factor that is currently limiting long-term use of SiC MOSFETs. When compared with Si-based devices, the interface state density (D_{it}) at the SiC/SiO_2 interface is two orders of magnitude higher, and the SiC conduction-band energy level is closer to the trap energy level at the SiC/SiO_2 interface. Therefore, the V_{th} drift problem is mainly caused by trapped charges, including the charges in gate oxide traps and interface traps. Several studies have been conducted on both the V_{th} drift mechanism and measurement of the trap density of the SiC MOSFET.

With respect to the V_{th} drift, a dc scanning method has been used to investigate the causes of the V_{th} instability by George Mason University. They found that the interface traps and near-interface traps capture electrons when positive stress is applied to the device gate and then release these electrons under application of negative stress [4]. Jiang et al. [5] found that under switching conditions, the main driving force behind the V_{th} drift was the gate oxide electric field between the trap and the interface, which drives the carriers to tunnel out from or into the trap. In a bipolar gate switch, the gate oxide electric field is enhanced locally. Lelis et al. [6], [7] analyzed V_{th} drift at different test times and the correspondence of the drift to the oxide trap tunnel model, and then speculated that the main process that affects V_{th} drift is the direct tunneling mechanism. This mechanism causes charging of the oxide layer traps. However, their method only calculated the approximate oxide trap concentration, and no more detailed trap information was provided.

With regard to trap characterization, Terao et al. [8] studied and calculated the oxide trap concentration in SiC, but their trap characterization method was based on different material levels, and the time constant and the activation energy of the trap could not be obtained. Berens et al. [9] and Uranwala et al. [10] determined the D_{it} distribution in the band gap using the thermal dielectric relaxation current (TDRC) method. Deep level transient spectroscopy (DLTS) is another widely used trap characterization method and can measure the peak and activation energies of traps [11], [12]. However, the test conditions required for both TDRC and DLTS are very harsh. The equipment must be placed in a low temperature environment and be able to withstand a wide range of temperature changes, which places high performance requirements on the experimental instrumentation.

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The transient current method is a new trap characterization method that can represent the time constants of traps accurately. To date, this method has been verified via application to the GaN high-electron-mobility transistor [13], [14], [15] and the SiC MOSFET [16]. However, there is little research published in the literature that can show a clear correspondence between the SiC MOSFET device traps and the threshold voltage drift.

In summary, the current research focus on the V_{th} drift of SiC MOSFETs is still at the stage of characterization of the phenomenon, and most of the existing works are combined with reliability tests to explore the long-term effects of temperature stress or electrical stress on V_{th}. At the same time, only a general conclusion that the trap affects the V_{th} drift is usually drawn, but more specific trap information (including the trap time constant, activation energy, and type) is rarely mentioned. This is because the current ability to characterize the gate oxide traps in SiC MOSFETs still only works in terms of the concentration distribution and cannot provide more information about the traps that are causing the V_{th} shift.

Therefore, it is necessary to identify the effects of different types of trap on the V_{th} shift, along with the specific trap parameters (e.g., time constant, activation energy) that cause the V_{th} shift in SiC MOSFETs. To solve this problem, this paper combines the transient current method with a precondition method for V_{th} testing. After the influence of the SiC bulk traps has been excluded, the Bayesian deconvolution method [17], [18], [19] is used to better determine the trap time constant. Subsequently, the effects of the different traps on the device V_{th} are studied by filling or releasing the charges of traps with different time constants. When combined with the test results acquired for V_{th} under the same conditions, the time constant of the trap that leads to the SiC MOSFET V_{th} drift is determined. Identify the influence of different traps on V_{th} drift. Finally, the transient curves of the drain current variations versus time are recorded under various temperature conditions and constant test conditions, and the trap activation energy is determined by combining the curves with the Arrhenius equation. A combination of the time constant and the activation energy is used to locate the trap position, and the trap types that affect V_{th} drift can be characterized, which may then provide suggestions to improve the reliability of SiC MOSFETs in the future. The rest of this article is organized as follows. Section II introduces the experimental principle of the transient current method used to characterize the traps and test V_{th} by preconditioning. In Section III, the effects of different experimental conditions on the trapping behavior are evaluated, along with the correspondence of the results obtained with the actual V_{th} test results. The initial trap positions in the SiC MOSFET are studied and the traps that affect the device V_{th} drift are characterized. Finally, Section IV concludes this article.

II. Methodology

The experiments in this article comprise two main parts: 1) trap characterization and 2) V_{th} testing.

First, the experimental principles of the trap characterization process are explained. As shown in Fig. 1(a), when the gate filling voltage (V_{GF}) is applied, the trap captures charge until it

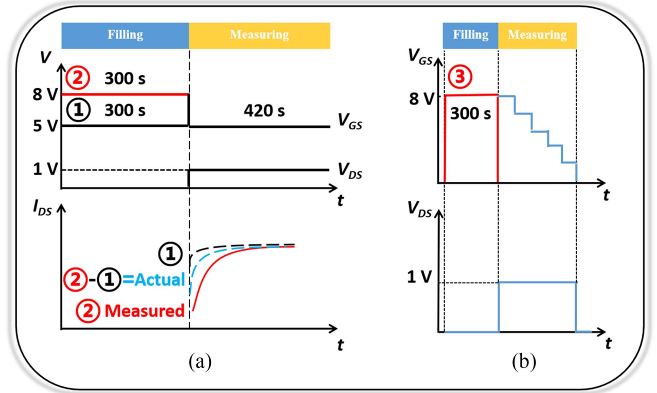

Fig. 1. Test timing diagram. (a) Transient current method test trap. (b) Test V_{th} drift under the same filling conditions.

becomes saturated, and V_{th} increases gradually up to saturation with continuous charge capture. During the test phase, when the test gate voltage (V_{GM}) is lower than V_{GF}, the charges that have been captured by the different traps are released gradually, V_{th} also decreases gradually as the test time increases, and the transient drain-source current (I_{DS}) increases gradually. Theoretically, after the trap charge is filled stably during the filling stage, the gate electric field does not change during the test stage, the binding force to the gate oxide trap will remain consistent, and I_{DS} should not change. Because some SiC bulk traps also exist simultaneously, these SiC bulk traps also capture charge during the test and, thus, affect the test current. Therefore, we set up a reference group to eliminate the interference from the bulk traps, set both V_{GF} and V_{GM} to 5 V, did not apply the filling drain-source voltage (V_{DF}), and applied the test drain-source voltage (V_{DM}) of 1 V to test the value of I_{DS}. To avoid the bulk traps, which are caused by current fluctuations and cause errors in the experimental results, the subsequent experimental results are then calculated as the differences between the test results and the reference group's results, as illustrated in the lower part of Fig. 1(a). When the experimental conditions were subsequently changed, the conditions of the reference group remained unchanged to ensure that the oxide trap is completely filled, so as to avoid the fluctuation of the test curve of the reference group by the oxide trap, and only the influence of the bulk trap is excluded. The time constant spectrum (TCS) is then used to analyze the transient current, thus allowing the different trap types to be characterized and distinguished.

In this study, Rohm's trench gate SiC MOSFET (SCT30-80ALHR) was used as the experimental test device. The I_{DS} characteristics were measured under various gate bias voltages using the Keysight B1505A parameter analyzer and the Keysight N1265A fast switch. The test timing diagram is shown in Fig. 1(a), where curve ① is the reference group mentioned above. Curve ② represents the measured transient change curve of I_{DS} versus time and shows an increase in V_{GF} from 5 V to 8 V. The real gate oxide trap's detrapping transient is then determined by subtracting the two curves above, as shown in Fig. 1(a), and this approach avoids the error caused by the SiC bulk traps. The filling time and the test time are based on a

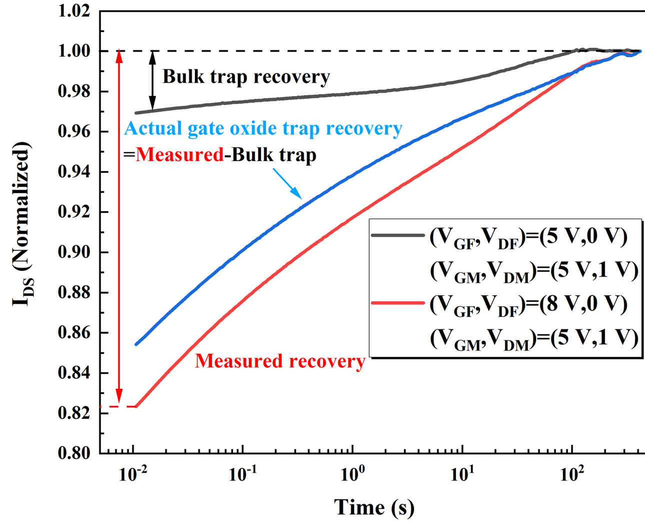

Fig. 2. Actual detrapping curve for gate oxide trap.

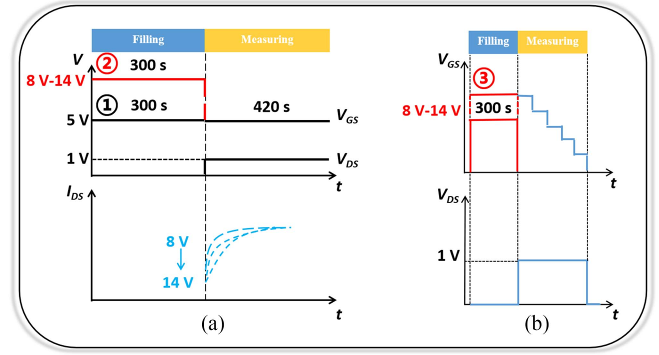

Fig. 3. Test timing diagram for different V_{GF} values.

process of selection after several tests. The filling time of 300 s ensures trap charge filling stability, and the initial V_{th} used for the test does not change with changes in the filling time. The test time of 417 s ensures that the trap releases its charge completely (while ensuring that all bulk traps are excluded), the final curve remains flat, and the trap captures and releases charge in a dynamic balance state. The actual test results are shown in Fig. 2. By dividing all data points along the entire curve by the last measured data point (the maximum value of the data), the curve can, then, be normalized. This process allows the ends of the curves that were measured under the various test conditions to coincide, thus making the previous trend more intuitive. The test curves that are presented for subsequent experiments are all based on the results after the difference and normalization processes (e.g., the blue curve in Fig. 2).

Next, the V_{th} test principle is explained. In this work, a gate voltage scanning method with preconditioning was used. According to [20] and [21], the direction required for the scanning gate voltage is determined to be downward scanning. The initial gate voltage value is consistent with the filled gate voltage, and test errors caused by sudden changes in the filled gate voltage and the test gate voltage are reduced. Because the research objective of this article is to explore the relationship between the V_{th} drift and the effects of the traps, the preconditions for the V_{th} test are the same as those used for the transient current method for filling the trap. The relevant values are a V_{GF} of 8 V and a filling time of 300 s (the time is not limited to this value), as shown in the upper part ③ of Fig. 1(b). The value of V_{DM} during the test was also 1 V. V_{th} is then determined via the threshold current method, and the gate voltage (V_{GS}) that corresponds to I_{DS} = 10 mA was selected as V_{th} (the selection of this I_{DS} value was based on the value that was commonly used in the datasheet).

In the following experiments, by filling traps with different time constants, the filling time for each trap test is shown to be consistent with that for the V_{th} test (i.e., ② and ③ are the same), and the changes in V_{th} are then measured under the different filling conditions. When charge is trapped by the gate oxide trap, V_{th} is affected, the gate transconductance controls the current through the voltage, and I_{DS} has an amplified effect on that. Therefore, the effect of the gate oxide trap on I_{DS} is greater than that of a bulk trap. The V_{th} value of the device is then read using the transfer curve. The transient current method test curve is I_{DS} versus time t, and the transfer curve is I_{DS} versus V_{GS}. The value of V_{GS} does not change when the transient current curve is tested, and switching of V_{GS} only occurs during filling and testing. When V_{th} is measured, V_{GS} is a scanning step voltage, and the change in the current caused by the gate oxide trap occurs more frequently than the transient current curve. Therefore, the gate oxide trap is absolutely a factor in the change in I_{DS}, the V_{th} test is different from the transient current curve test, and the effects of the bulk traps can be ignored. By comparing the changes in the influence of the trap on the current with the drift in V_{th}, it then becomes possible to determine the trap type that has the greatest effect on the V_{th} drift.

III. Experimental

A. Effect of V_{GF} on the Trap

To avoid any parameter drift being caused by temperature changes, all tests were conducted in a constant temperature environment, and the temperature condition for this experiment was selected to be 40 °C (it is not limited to this value). The test timing sequence is, as shown in Fig. 3, and the initial test conditions were (V_{GF}, V_{DF}) = (8 V, 0 V) and (V_{GM}, V_{DM}) = (5 V, 1 V). Under these conditions, I_{DS} is less than 100 mA and the power dissipation is no more than 0.1 W, which allows the effects of self-heating on the transient curve for I_{DS} to be avoided. V_{GF} was set to be within the 8–14 V range and the transient change curve for I_{DS} was acquired under these test conditions, with results, as shown in Fig. 4(a). After each test, a negative gate voltage (−5 V) was applied to the device to reduce V_{th}, thus counteracting the increase in V_{th} caused by the positive gate voltage pre-conditioning and producing a consistent initial state for the device. This also prevented the repeated measurements from having any effects on the trap state, and this will also be the case in the subsequent experiments.

In Fig. 4(b), the TCS of the trap under application of different V_{GF} values is plotted and shows a transient current curve that is generated based on a Bayesian deconvolution algorithm [16],

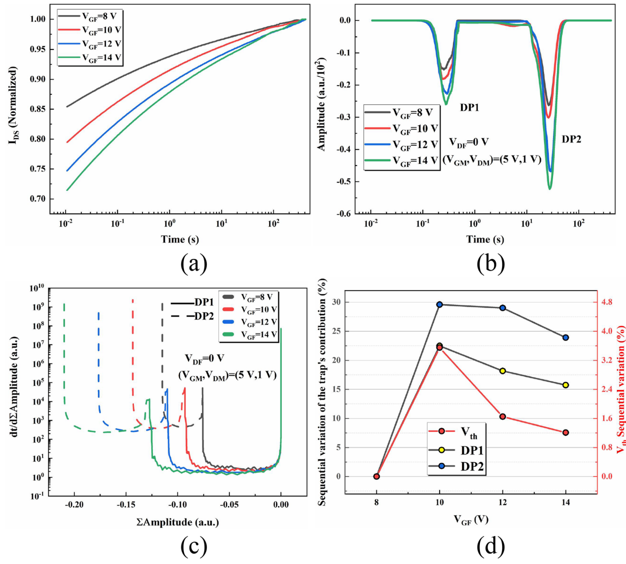

Fig. 4. Test results acquired at different values of V_{GF}. (a) Transient current curve. (b) Time constant spectrum. (c) Corresponding DAS. (d) Trap effects on the sequential changes in I_{DS} and the sequential changes in V_{th}.

[22]. The two most obvious time constant peaks can, then, be extracted from the transient current curve and these traps, which have different time constants, are termed DP1 and DP2. At the same time, many other time constant traps are present in the device, but their amplitudes are small and they are submerged in this coordinate system, which has little effect on the current. In this article, only the two traps (DP1 and DP2) that have the most obvious effects on the current are studied. The time constant of DP1 is approximately 300 ms and the time constant of DP2 is approximately 30 s. Because the transverse coordinate of the TCS is logarithmic and each trap peak width is different, it is both inappropriate and inaccurate to use the longitudinal value of the peak point alone to represent the full effect of the trap on the channel current. To resolve this problem, the differential amplitude spectrum (DAS) [23] is used to characterize the degree of influence that the trap has on the current, where the DAS represents an additional operation of the TCS. The points near the peak value are added up and the horizontal coordinate range contained in each arc represents the degree of influence of the trap on the current. A positive value for the horizontal coordinate of the DAS represents the reduction in the current caused by trapping of electrons by the trap, and a negative value represents an increase in the current caused by detrapping of the electrons from the trap; these values correspond to the positive and negative values of the vertical coordinate in the TCS, respectively. This characterization method, which takes the peak shape into account, offers greater accuracy when solving the trap amplitude problem and can also pave the way toward the subsequent calculation of the variation. The test results are presented in Fig. 4(c).

As Fig. 4(a) shows, when V_{GF} increases, the initial I_{DS} value decreases, and the increases in the actual transient current curve show a regular increasing trend. This occurs because when V_{GF} increases, the gate electric field also increases, and the number of trapped electrons increases; then, the V_{th} of the device increases and the initial I_{DS} also decreases. When V_{GF} is converted into the test gate voltage, the gate electric field strength is weakened, V_{th} is reduced gradually because of the release of electrons by the trap, and I_{DS} gradually increases with increasing test time. As shown in Fig. 4(b), the time constants of traps DP1 and DP2 remain almost unaffected by the differences in V_{GF}, and the amplitudes of the two trap peaks both increase significantly with increasing V_{GF}. The constant time constants for DP1 and DP2 indicate that the experimental conditions did not activate the new trap. The amplitudes of traps DP1 and DP2 increase with increasing V_{GF}, which indicates that the numbers of electrons captured by traps DP1 and DP2 increase with increments in the filling electric field. Comparison of the trapped charge in the trap to the charging state of a capacitor using $C = Q/V$ shows that when the time constant of the trap itself does not change and the value of capacitor C does not change, Q will also increase as the filling gate voltage (V) rises. Therefore, the amplitude of the time constant spectrum will also change with changes in the test conditions.

The same filling conditions are applied to test V_{th} and the temperature during the test is also maintained at 40 °C. The sequential change in the value of V_{th} is calculated using

$$\Delta V_{th} = \frac{|V_{th} - V_{th'}|}{V_{th}} \times 100\% \tag{1}$$

where V_{th} is the threshold voltage test result measured under the current test conditions and $V_{th'}$ is the threshold voltage test result obtained under the previous test conditions. For example, when calculating the sequential change in V_{th} at $V_{GF} = 12$ V, the V_{th} value for $V_{GF} = 12$ V is subtracted from the V_{th} value for $V_{GF} = 10$ V and is then divided by the V_{th} for $V_{GF} = 12$ V, before the final value can, then, be calculated.

The same calculation method is used again here. Based on the DAS, the sequential changes in the effects of traps DP1 and DP2 on the current under the different V_{GF} conditions were calculated, and the calculation results obtained are shown in Fig. 4(d).

It can, thus, be concluded here that both traps are affected by the gate voltage and that they are both located near the gate. Based on the measured trap time constant, the experimental conditions continued to be changed in the subsequent experiments to further distinguish the effects of the two traps on the V_{th} drift.

B. *Effects of Different Filling Times on the Trap*

In this section, the influence of the filling time ($t_{_con}$) on the test results for the transient current and V_{th} is studied. Based on the two trap time constants obtained in Experiment A, with the other test conditions remaining unchanged, the $t_{_con}$ ranges were set to be from 0–1 s and from 10–300 s (where the reference group was kept at 300 s and the filling time was completely excluded from the effects of the bulk traps to avoid errors being caused by its own fluctuations). The test sequences are shown in Fig. 5.

The experimental conditions are divided into two parts. The $t_{_con}$ range for the first part is 0–1 s. Because the peak for DP1

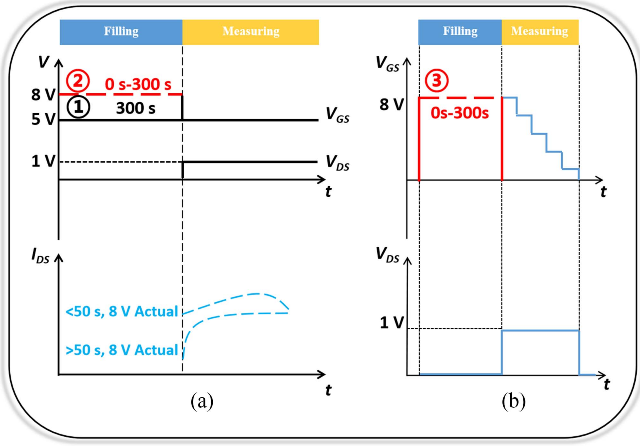

Fig. 5. Test timing diagrams for the different $t_{_con}$ values. (a) Results of characterization of the traps via the transient current method. (b) Test V_{th} characteristics acquired under the same filling conditions.

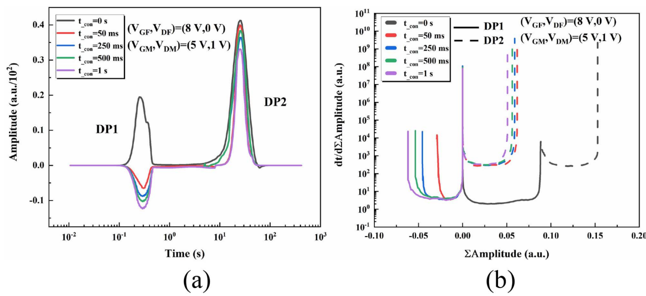

Fig. 6. Test results acquired at different values of $t_{_con}$ (0–1 s). (a) TCS. (b) Corresponding DAS.

appears at approximately 300 ms and ends at approximately 1 s, this filling stage is mainly intended to observe the relationship between the change in DP1 in the TCS and the V_{th} drift. The TCS is generated after the bulk traps are excluded from the transient current curve and the influence of the trap on the current is then characterized by the DAS. The test results for the TCS and the DAS are shown in Fig. 6.

When $t_{_con}$ is 0 s, the trap is not filled. During the test phase, the trap captures electrons, thus causing V_{th} to rise and I_{DS} to decrease with time. With increasing $t_{_con}$, the peak value of DP1 is flipped, and the trap then changes from the state where it is capturing electrons to the state where it is releasing electrons during the test. Because the time constant of DP2 is approximately 30 s, the maximum $t_{_con}$ of 1 s is much smaller than the time constant, which has little impact on it. DP2 is almost not filled at all during the filling stage, which means that the trap is not occupied by electrons during the filling stage. Upon entry to the test stage, the time is 417 s, which is much higher than the time constant of DP2. Because electrons have not been captured during the filling stage, DP2 it is always in the state where it is capturing electrons during the test stage. In this filling stage, the degree of change in DP1 is significantly higher than that in DP2.

The $t_{_con}$ range for the second part of the experiment is 10–300 s. Since the peak of DP2 appears at approximately 30 s

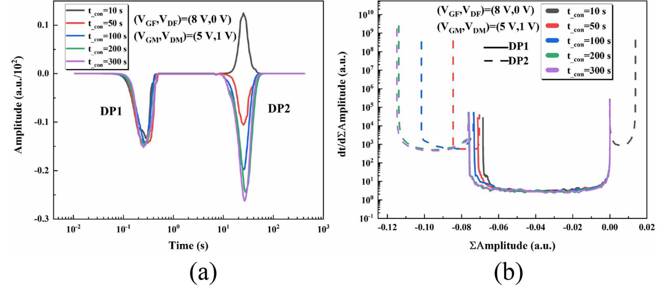

Fig. 7. Test results at different values of $t_{_con}$ (10–300 s). (a) TCS. (b) Corresponding DAS.

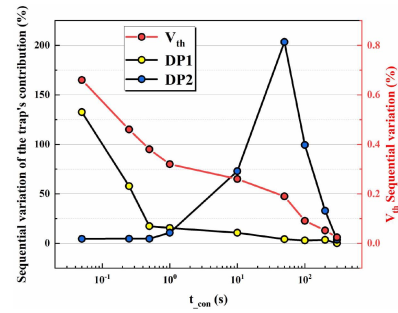

Fig. 8. Different values of $t_{_con}$, the traps affect the sequential changes in I_{DS} and the sequential changes in V_{th}.

and ends at approximately 100 s, the main aim in this part is to observe the relationship between the change in DP2 in the TCS and the V_{th} drift. DAS was also used to characterize the changes in the effects of the traps on the current at different values of $t_{_con}$ and the test results obtained are shown in Fig. 7.

Because the time constant of DP1 is approximately 300 ms, the shortest $t_{_con}$ during this stage is 10 s, which is dozens of times the time constant of DP1. Under the same electric field intensity, the trap has been filled completely. Therefore, the amplitude of DP1 hardly changes with increasing filling time. At this stage, the peak value of DP2 is flipped, and when the filling time is 10 s, it is still less than the time constant of DP2. In the filling stage, the trap is not filled, so it continues to capture electrons during the test. When the filling time exceeds 50 s, it exceeds the time constant of DP2 can enable filling of DP2, which shows a state where it is releasing electrons during the test. During this filling stage, the degree of change in DP2 is significantly higher than that in DP1.

The same filling conditions are also applied to test V_{th}, and the sequential changes in V_{th} are calculated using (1). The same calculation method used above is used again here. Based on the DAS, the sequential changes in the effects of traps DP1 and DP2 on the current under different $t_{_con}$ conditions were calculated, and the calculation results are shown in Fig. 8.

According to the results shown in Fig. 8, the sequential change trend for V_{th} is consistent with the sequential change trend for the DP1 influence on the current, both of which are decreasing monotonically. However, the sequential change trend for DP2's influence on the current initially increases and then decreases. The stage with the largest change for DP1 occurs when $t_{_con}$ is in

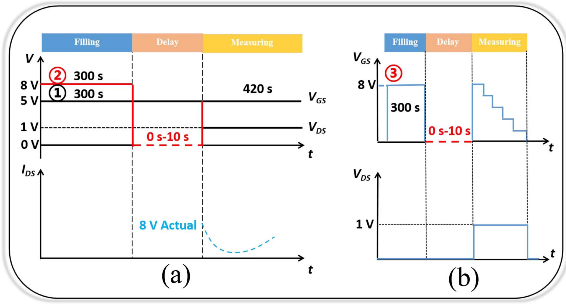

Fig. 9. Different $t_{_float}$ test timing diagrams. (a) Characterization of traps using the transient current method. (b) Test V_{th} values acquired under the same filling conditions.

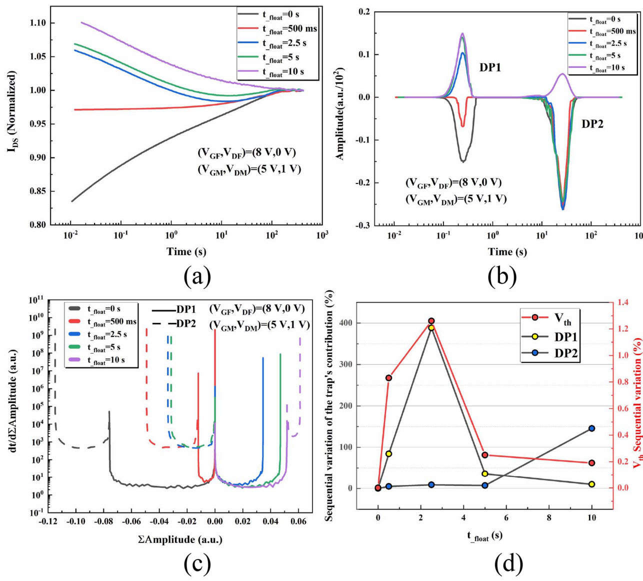

Fig. 10. Test results acquired at different values of $t_{_float}$. (a) Transient current curves. (b) TCS. (c) Corresponding DAS. (d) Trap effects on the sequential changes in I_{DS} and on the sequential changes in V_{th}.

the 0–1 s range, and the V_{th} drift in this stage is 1.82%. The stage with the largest variation in DP2 is when $t_{_con}$ is in the 10–300 s range and the peak value appears at 50 s. The corresponding V_{th} drift during this stage is 0.617%, which is much smaller than that during the stage where $t_{_con}$ was 0–1 s. Therefore, it is concluded preliminarily here that DP2 has little influence on the V_{th} drift.

C. Effects of Different Interval Times on the Trap

This section studies the influence of the interval time ($t_{_float}$) on the transient current and the V_{th} test results. With the other test conditions remaining unchanged, the $t_{_float}$ range was set to be 0–10 s (and was not imposed by the reference group) and the test timing was, as shown in Fig. 9.

The change in I_{DS} versus time was tested according to the given experimental conditions and the TCS was generated, as shown in Fig. 10(a) and (b). The DAS was used to characterize the influence of the trap on I_{DS}, with results, as shown in Fig. 10(c). The same filling conditions were then applied to test V_{th}, and the sequential changes in V_{th} are still calculated according to (1). The same calculation method is also used to calculate the sequential changes in the effects of traps DP1 and DP2 on the current at different values of $t_{_float}$. The test results are shown in Fig. 10(d).

The results in Fig. 10(b) and (c) show that when $t_{_float}$ is within 5 s, DP1 is strongly affected by $t_{_float}$, whereas DP2 remains almost unaffected by $t_{_float}$. When $t_{_float}$ is greater than 5 s, the influence of DP2 on the current changes, whereas the influence of DP1 on the current tends to remain stable.

The reason for this stability is that the $t_{_con}$ of 300 s has been experienced entirely before the test, and the trap has been filled completely without changing the magnitude of the bias stress. The $t_{_float}$ in this case is equivalent to application of a gate filling voltage (V_{GF}) of 0 V; the trap that was previously fully filled will release charges at $t_{_float}$ and the trap with the small time constant at the beginning of the test will be affected by $t_{_float}$. The peak value of DP1 gradually decreases to show a reversing trend and the corresponding transient current curve changes from rising to falling with increasing test time, as shown in Fig. 10(a). This behavior occurs because, with increasing $t_{_float}$, V_{th} decreases gradually at the beginning of the test, and V_{th} then continues to rise as a result of the influence of the trap charge during the test, which means that I_{DS} decreases with increasing test time. At the same time, the time constant of DP2 is long, and the trap's behavior in capturing and releasing charge is unaffected by the longest $t_{_float}$ of 5 s, which means that the amplitude of DP2 does not change with increasing $t_{_float}$. When $t_{_float}$ increases from 5 s to 10 s, DP1 has almost completely released the charge captured during the filling stage, and recapture has started during the test stage; therefore, the influence of the trap on the current during this stage remains almost unchanged with increasing $t_{_float}$. In addition, with increasing $t_{_float}$, the charge that was captured by DP2 during the filling stage also produces a certain degree of release, and the related time constant spectrum also produces a flip.

According to the results presented in Fig. 10(d), the sequential change trend in V_{th} is still consistent with the sequential change trend in DP1 that affects the current. In the $t_{_float}$ range from 0–5 s, the influence of DP1 on the current changes strongly, and the total shift in V_{th} during this stage is 2.34%. At this time, the sequential change trend for DP2's influence on the current is relatively gentle. The stage with the larger change occurs after $t_{_float}$ reaches 5 s, and the total drift in V_{th} at this stage is 0.19%, which is much smaller than that during the stage before $t_{_float}$ reached 5 s. Therefore, the conclusions drawn from this verification are that DP1 is the main trap that affects the V_{th} drift and that DP2 has little influence on the V_{th} drift.

D. Activation Energy Characterization

In this section, the changes in the trap time constant that occur at different ambient temperatures are analyzed, the activation energy of the deep level trap is extracted using the Arrhenius equation, and the trap location is estimated with respect to the different time constants.

The temperature is set to be within the 30–60 °C range with intervals of 10 °C, and the I_{DS} and the TCS of the device are tested

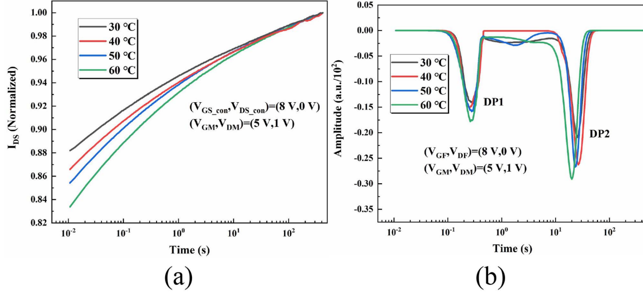

Fig. 11. Test results acquired under different temperature conditions. (a) Transient current curves. (b) Time constant spectra.

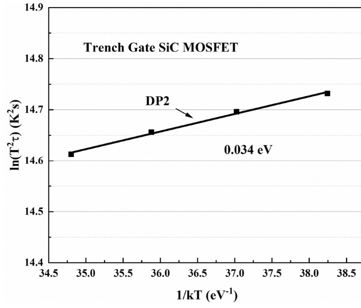

Fig. 12. Activation energy characteristic for DP2.

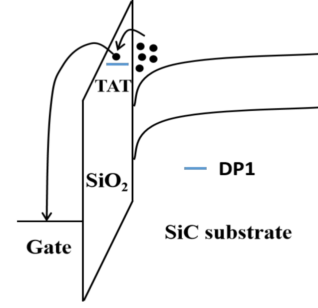

Fig. 13. Schematic diagram of the electron tunneling mechanism.

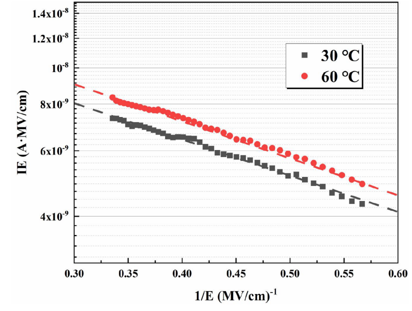

Fig. 14. TAT characteristics of electron injection for devices operating at different temperatures.

at each temperature. The test conditions are still $(V_{GF}, V_{DF}) =$ (8 V, 0 V) and $(V_{GM}, V_{DM}) =$ (5 V, 1 V). The transient I_{DS} curves caused by the trap state at various temperatures are shown in Fig. 11(a). Because the device V_{th} decreases with increasing temperature and the test gate voltage remains constant, the initial I_{DS} increases with increasing temperature. The time constant spectra that were recorded at different temperatures are shown in Fig. 11(b). The peak amplitudes for DP1 and DP2 increase with increasing temperature, which indicates that more charges are injected into the traps as the temperature increases. Among these characteristics, the time constant of DP1 remains almost unchanged, but the time constant of DP2 decreases gradually with increasing temperature.

Combining the change in the time constant with the Arrhenius equation [24] allows (2) to be obtained as follows:

$$\ln\left(\mathrm{T}^2\tau_{\mathrm{n}}\right) = \mathrm{E}_{\mathrm{a}}\frac{1}{\mathrm{kT}} - \ln\left(\gamma_{\mathrm{n}}\sigma_{\mathrm{n}}\right) \quad (2)$$

where T is the applied temperature, τ_{n} is the trap time constant, E_{a} is the trap activation energy, k is the Boltzmann constant, γ_{n} is the material correlation constant, and σ_{n} is the trap density. In addition, $\frac{1}{\mathrm{kT}}$ is the ordinate, $\ln\left(\mathrm{T}^2\tau_{\mathrm{n}}\right)$ is the abscissa, and the slope of the curve obtained at the different temperatures represents the trap activation energy.

The activation energy for DP2 was calculated to be 0.034 eV using the Arrhenius equation and the results are shown in Fig. 12. Since the time constant of DP1 does not shift with temperature, its activation energy cannot be calculated.

Because the time constant of DP1 is independent of the temperature, the trapping process may be related to the tunneling effect without energy levels [25], [26], [27]. The tunneling mechanism varies under the different electric field strengths. According to previous studies, the field strength for the gate oxide layer of 5 MV/cm acts as the dividing line [28], and when the field strength is greater than 5 MV/cm, the amount of Fowler–Nordheim tunneling increases exponentially with increasing field strength. Within the 0–5 MV/cm range, trap-assisted tunneling (TAT) is the main tunneling mechanism [29], and in a nonideal insulator, TAT may result in large leakage currents passing through thicker dielectric layers [30], [31]. The carriers are initially captured by the oxide trap, which is in a charged state, and these carriers are subsequently released and tunnel out of the oxide layer, as illustrated in Fig. 13.

According to the capacitance-voltage test results, the flat-band voltage of the SiC MOSFET used in the experiments here is approximately −3.5 V. When the test gate voltage is 8 V, the electric field intensity generated reaches 2.3 MV/cm. The resulting tunneling current is shown in [32]

$$J_{\mathrm{TAT}} = \frac{2qN_tC_t\exp\left[\left(-D/E\right)\phi_t^{3/2}\right]}{3E} \quad (3)$$

$$ln\left(JE\right) = \left(-D\phi_t^{3/2}\right)\left(1/E\right) + ln\left(\frac{2}{3}N_tC_t\phi_t\right). \quad (4)$$

From (4), it can be determined that there is an approximate linear relationship between $ln(JE)$ and $(1/E)$ when TAT is generated, and the experimental results are shown in Fig. 14.

As shown in Fig. 14, the relationship between $ln(JE)$ and $(1/E)$ is approximately linear within the electric field intensity range of 1.8–3 MV, and thus, the tunneling effect is mainly TAT under low electric field intensities.

Because the spatial environment in which the near-interface oxide traps are located is an interface transition layer that contains a large structural change, the time constants of the captured and emitted carriers from the oxide traps at the different positions are different. Overall, the near-interface oxide trap time constant distribution is very wide (ranging from 10^{-6}–10^{5} s) [33]. Fundamentally, this distribution occurs because the trap capture cross section associated with the thermal activation process is distributed widely. The time constant of DP1 conforms to the time constant range for the oxide trap.

The temperature correlation coefficient of the barrier height at the SiC/SiO_2 interface is -7.6 meV/°C [28]. Because the barrier height temperature coefficient is negative, the electron barrier height will decrease slightly when the temperature increases under the same applied electric field intensity. The probability of electron tunneling then increases slightly. As shown in Fig. 11(b), the amplitude of DP1 increases only slightly. The amplitude variation in DP2 is significantly greater than that which occurs in DP1 because DP2 is a trap caused by hot carrier injection. As the temperature increases, increasing numbers of hot carriers are excited and injected, which results in a significant amplitude change.

DP2 is an interface state trap with an activation energy of less than 0.1 eV [34], [35]. According to [36], other ultrashallow and ultradeep defects are present after NO nitridation, thus providing further confirmation of the existence of traps with activation energies of less than 0.1 eV in the device.

When an interface trap is present, the carrier is captured or released by the interface trap; this process is similar to that of a capacitor charging and discharging, and can be considered to be equivalent to a trap capacitance (C_{it}). The process of carrier capture and release is accompanied by energy loss, which can then be equivalent to a trap resistance (R_{it}) [37]. The time constant of a series resonant loop composed of a trap capacitance and a trap resistance is given by

$$\tau = R_{it} C_{it} . \quad (5)$$

As the test temperature increases, the leakage current (I_{gss}) increases and R_{it} decreases. C_{it} remains constant, which means that the time constant decreases with increasing temperature. Therefore, the time constant of DP2 decreases with increasing temperature, but the time constant of DP1 remains unchanged.

Combining the results from experiments A–D leads to the conclusions that DP1 is an oxide trap and DP2 is a SiC/SiO_2 interface state trap. Therefore, under the gate bias conditions near room temperature, the main mechanism that causes the V_{th} drift is the charging of the near-interface oxide traps through the tunneling mechanism, whereas the contribution of the interface traps to the V_{th} drift is relatively small. To reduce the V_{th} drift of SiC MOSFET devices further and thus improve the device reliability, it will be necessary to solve for an oxide trap effect with a time constant of approximately 300 ms.

IV. Conclusion

This article proposes a method to characterize the trap information that affects V_{th} instability in SiC MOSFETs. Based on the transient current method of Bayesian deconvolution, the time constants of the different traps were determined preliminarily. By using these trap time constants and varying the experimental conditions, the trap changes that occurred with the different time constants were related to the V_{th} drift individually, and the traps that affected the V_{th} drift were then analyzed.

1) The test conditions were set and the reference group for the I_{DS} curve with time was established (V_{GF} is the same as the test gate voltage). After the influence of the SiC bulk traps was eliminated, an accurate transient current curve was obtained.
2) Based on the Bayesian deconvolution method, the transient current curve was then processed. Two traps, designated DP1 and DP2, in the SiC MOSFET were analyzed. The time constants of these traps were approximately 300 ms and 30 s, respectively. By varying V_{GF} in combination with the changes in the trap in the time constant spectrum, the trap positions were determined preliminarily. Both DP1 and DP2 are located between the gate and the source.
3) By changing the values of $t_{_con}$ and $t_{_float}$, the variations in the degree of influence of each trap on the current were observed, and these changes corresponded to the V_{th} drift results acquired under the same filling conditions. It was found that the trap type that mainly affected the V_{th} drift of the SiC MOSFET was trap DP1, which had a time constant of approximately 300 ms, and trap DP2 made a lesser contribution to the V_{th} drift.
4) Repeated detrapping experiments performed at different temperatures indicated that the activation energy for DP2 was 0.034 eV. However, we cannot calculate the activation energy for DP1, which is inferred to be based on the TAT effect. By combining the results obtained here with previous experimental information, it was determined that DP1 was an oxide trap and DP2 was a SiC/SiO_2 interface trap. By improving the process used to eliminate the gate oxide trap DP1 with a time constant of 300 ms, both V_{th} drift and overall device reliability can be improved.

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