Robust Sequential Model-Free Predictive Control of a Three-Level T-Type Shunt Active Power Filter

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***Abstract*—Three-level T-type shunt active power filter (3LT^2-SAPF) has been widely used to improve the power quality of power grid under nonlinear load, and their harmonic compensation performance and reliability have been widely noticed. Model predictive control (MPC) offers the advantage of convenient multiobjective optimization, quick response and a simple principle. However, once the parameter mismatch occurs due to some reasons (e.g., temperature change, noise from the sensors, etc.), the output performance of MPC system will be seriously deteriorated, sometimes may even endanger the system stability. Moreover, for cases when the circuit relation is unknown, the prediction model of the control object could not be established, rendering the traditional model-based MPC (TMPC) inapplicable. To address these challenges and enhance the robustness of the 3LT^{2}C SAPF system, a linearly fitting sequential model free predictive control method is proposed. First, the principle of linear fitting method for current prediction is briefly analyzed. Second, a current difference matrix for each switch sequence has been established, which is utilized for harmonic current tracking. Finally, the cost functions for neutral-point voltage and dc-bus voltage are designed. Numerous experimental results under different scenarios verify the correctness and effectiveness of the proposed method.**

***Index Terms*—Neutral-point voltage balance, sequential control, sequential model-free predictive control (SMFPC), shunt active power filter (SAPF).**

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I. Introduction

NOWADAYS, harmonic pollution is becoming overwhelmingly serious due to the increasing number of nonlinear loads in the power system, such as diode rectifiers, switching power supply systems, and battery charging systems for electric vehicles. As a result, the power quality of the grid has drawn great attention. To address the issues of harmonic and reactive power compensation, shunt active power filters (SAPF) are widely used. SAPF can automatically determine the reference compensation current in real-time and achieve harmonic compensation [1], leading to a significant improvement in the power quality of the grid and ensuring electricity safety.

To suppress harmonic current, various power circuit topologies are applied in SAPF for current compensation. Among these converters, the three-level T-type converter (3LT^{2}C) has drawn great attention due to its high efficiency and controllability in low-voltage applications [2] because of its lower output current ripple [3], higher overall efficiency [4], etc. Also, to meet grid standards and reduce the impact of harmonic currents, *LCL* filters have been widely adopted. They can effectively filter out high-order current harmonics with smaller volume. By using a 3LT^{2}C converter interfaced with an *LCL* filter, the quality of SAPF compensation current can be improved and the total harmonic distortion of the grid current can be further reduced [5].

There are several methods for APF control, including support vector machines and genetic algorithms [6], proportional-integral-derivative (PID) control [7], robust control [8], and artificial intelligence methods [9], etc. At present, model predictive control (MPC) has been widely applied due to its ability to reduce the impact of control delay and generate control first. However, MPC heavily relies on the modeling accuracy of the object and its performance is severely affected by thechanges in model parameters.

Recently, the harmonic compensation performance of power converters under different operating conditions has become a widespread research focus [10], [11], [12]. One way to improve the overall performance is to establish a model-free predictive control (MFPC) method that achieves harmonic compensation without prior knowledge of model parameters. In addition, MFPC does not require establishing the state-space equation of the system. Therefore, the same model can be used for different topologies, avoiding parameter mismatch caused by aging or errors in the manufacture process, which deteriorates

SAPF performance. Currently, different MFPC methods such as neural networks and hyper-local models are proposed and have been widely used by scholars in motor control [13], [14], [15]. Similar ideas can also be applied to MPC in power electronic networks. But the above methods still have certain problems. In [16], the ultralocal model method was proposed, which can achieve normal operation of the power grid but still requires some circuit models and parameters, and could not achieve complete model-free control. The continuous fractional-order sliding mode controller based on a developed output feedback feature selection neural network proposed in [17] could compensate for harmonic currents in the power grid, but it has a high computational burden and is not easy to implement.

Due to the need for neutral-point (NP) voltage balance and a simpler method for the T-type three-level shunt active power filter circuit, a new linear fitting MFPC strategy is proposed. It predicts the future state variables by establishing a current difference matrix. An optimization problem is then constructed by assigning cost functions to directly output the required switching sequence for the converter. Meanwhile, as MFPC in SAPF is associated with the multiobjective optimization, it involves the selection of the optimal weighting factor for each subcost function. Previous approaches for selecting weighting factors are usually involved with trial and error, which is time-consuming [18], [19]. Sequential MFPC (SMFPC) can effectively address this issue, thus it has been extensively validated in motors [20], [21], [22]. This method transforms multiobjective optimization problem into multiple cascaded single-objective optimization problems, thereby avoiding time-consuming optimal weighting factor selection. This concept is also applicable to SMFPC of SAPF. In general, the main contributions of this article are summarized as follows.

1) A linear fitting SMFPC strategy is proposed, which can ensure the harmonic compensation performance of SAPF remains unaffected by model parameter mismatch or the need to establish the prediction model of SAPF.
2) SMFPC is applied to mitigate the impact of improper weight factor selection on the performance of SAPF.
3) The experimental results verify the effectiveness of the proposed method under various working scenarios.

The rest of this article is organized as follows. Section II provides an overview of the preliminary research on 3LT^{2}C SAPF, including circuit topology, control objectives and the MPC method. Section III introduces the proposed SMFPC method, covering its working principles, harmonic current suppression, NP voltage balance control and DC bus voltage stability. Section IV mainly discusses the design of the SMFPC. In Section V, experimental results under different scenarios are presented to validate the effectiveness of the proposed method. Finally, Section VI concludes this article.

II. Preliminary of 3LT^{2}C SAPF Converter

A. Circuit Topology

Fig. 1 shows the topology of a 3LT^{2}C SAPF. The dc bus side consists of two series-connected capacitors. The voltages of the upper capacitor C_1 and lower capacitor C_2 are expressed as v_p and v_n. Because there is no dc power supply, the dc voltage v_{dc} is provided by the ac grid via an *LCL* filter. The 3LT^{2}C converter consists of six horizontal NP switches and six vertical half-bridge switches. Its parameters include the converter-side inductance L_1, grid-side inductance L_2, and filter capacitor C_f. R_1 and R_2 represent the parasitic resistances of L_1 and L_2, and R_C is the passive damping resistance. i_{np} represents the NP current. v_i, i_1, i_2, v_C, i_g, v_g and i_l are the converter-side voltage, converter-side current, SAPF output current, filter-capacitor voltage, grid current, grid voltage, and load current. The output current i_2 compensates for the harmonic component of the load current i_l, thereby improving the quality of the grid current.

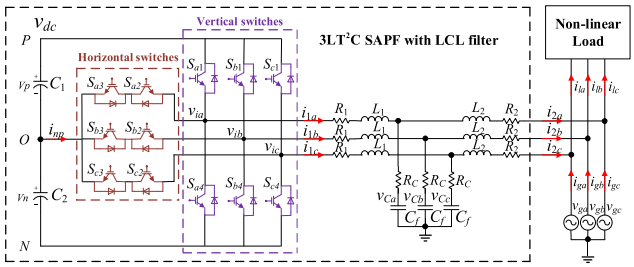

Fig. 1. Topology of a 3LT^{2}C SAPF with an *LCL* filter.

B. Control Targets

In traditional model-based predictive control (TMPC) of SAPF, several parameters are typically used as the main control targets. First, the output current of the power grid should be sinusoidal to ensure the grid power quality. This can be achieved by controlling the SAPF terminal to generate harmonic compensation current that is opposite to the harmonics. Therefore, the primary control target is the output current. Second, to prolong the lifespan of the entire system, it is necessary to maintain equal voltage across the two series-connected dc-link capacitors, namely, the NP voltage should be kept as lower as possible. Finally, the dc-bus voltage should be maintained stable.

C. Problem for TMPC

Although the aforementioned MPC method is effective, it still has many limitations. First, in practical applications, factors such as temperature and humidity are constantly changing, which may lead to changes in circuit parameters, especially, filters. Second, as devices are pronged used, parameters of *LCL* filters will inevitably experience some changes. Finally, it is unavoidable that there may be manufacture errors of the filters, leading to model mismatch between the real value and desired value. In this case, TMPC can result in a significant reduction in control performance.

On the other hand, multiobjective optimization of TMPC requires weighting factor design, which often relies on the experience of engineers and is time-consuming [18], [19]. This poses a great challenge for engineers and is not conducive to system stability. To address these issues, a linear fitting SMFPC method is proposed.

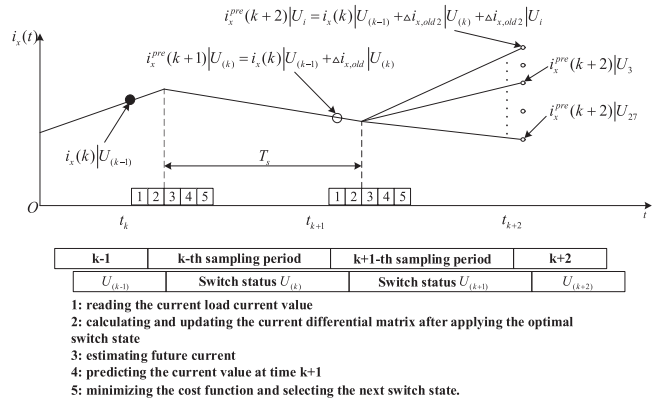

Fig. 2. Working principle for linear fitting MFPC.

III. Proposed Linear Fitting SMFPC

A. Basic Idea of Linearly Fitting SMFPC

Fig. 2 illustrates the principle of linear fitting the current operation. Through analyzing current variances, SMFPC does not need any prior knowledge of circuit parameters or models. The calculations of current differences involve simple addition and subtraction operations, thereby alleviating the computational burden. It directly regulates electronic devices by considering voltage and current values over a specific timeframe to ensure their continuity in following established patterns.

Due to its high sampling frequency (over 15 kHz) and the utilization of only one switching state per control cycle, it can be inferred that the converter-side current linearly fluctuates during every control cycle. Therefore, by calculating the difference and sampling the current values, it becomes feasible to predict the converter-side current. To compensate the control-delay in implementation, a two-step prediction method is applied [23].

In Fig. 2, the segments labeled as 1, 2, 3, 4, and 5 represent distinct sequence segments, each with specific operations marked. U denotes different switching sequences. As the current $i_x(k)$ is required for selecting the switch sequences at $k+1$, there exists a delay between the current and switch sequences, quantified as a unit of "1". $i_x(k)|U_{(k-1)}$ represents the current at k under the influence of the switching sequence at $k-1$. $i_{x,old}|U_i$ represents the prior current difference under the switching sequences U_i. Throughout the entire process, the circuit topology remains constant. Hence, the current difference under $U_{(k)}$ at k should be approximately equal to that generated after the last selection of switch sequence $U_{(k)}$. According to the linear fitting theory, it can be inferred that the predictive value for $i_x(k+1)$ will be written as:

$$\begin{aligned} i_x^{pre}(k+1)\ U_{(k)} &= i_x(k)\ U_{(k-1)} + i_{x,old}\ U_{(k)} \\ i_x^{pre}(k+2)|U_i &= i_x(k)\ U_{(k-1)} + i_{x,old}\ U_{(k)} \\ &\quad + i_{x,old}|U_i\ . \end{aligned} \tag{1}$$

The computational procedure described above is iterated sequentially to derive the predicted values for different switching states. During the calculation process, it is crucial to acquire the current differential values under different switching sequences and establish the current differential matrix.

B. Grid Current Prediction for MFPC

1) Theoretical Analysis: The principle of MFPC is illustrated in Fig. 2. Taking the A-phase of the 3LT^{2}C SAPF in Fig. 1 as an example, the current difference at k can be expressed as follows:

$$\begin{aligned} i_{1m}(k) &= i_{1m}(k)\ U_{(k-1)} \quad i_{1m}(k-1)\ U_{(k-2)} \\ i_{1m}(k+1) &= i_{1m}(k+1)\ U_{(k)} \quad i_{1m}(k)\ U_{(k-1)} \end{aligned} \tag{2}$$

where $i_{1m}(m = d, q)$ represents the dq-axis difference of the grid current, and U represents the switching vector.

However, the current difference at $k+1$ cannot be obtained at k. Under the condition that the sampling time T_s is fixed and short enough, any two consecutively calculated current differences under the same voltage vector are close to each other. So, the previous value can be used instead. The substituted current difference is approximated as follows:

$$i_{1m}(k+1) \quad i_{1m,old}\ U_{(k+1)}\ , U_{(k+1)} \quad \{U_1, \ldots, U_{27}\} \tag{3}$$

where the subscript "old" represents the previous current difference stored in the memory of the microprocessor.

Thus, by combing (2) and (3), the current prediction equation of MFPC can be derived as follows:

$$\begin{aligned} i_{1m}^{pre}(k+2)\ U_j &= i_{1m}(k) + i_{1m,old}\ U_{(k)} + i_{1m,old}|U_j \\ U_j &\quad \{U_1, \ldots, U_{27}\}\ . \end{aligned} \tag{4}$$

The cost function of MFPC for the grid current tracking can be expressed as follows:

$$\begin{aligned} J_{i_1} = i_{1d}(k+1) &\quad i_{1d}^{pre}(k+2)\ U_j| + i_{1q}(k+1) \\ &\quad i_{1q}^{pre}(k+2)\ U_j| \end{aligned} \tag{5}$$

where $i_{1m}(k+1), (m = d, q)$ represents the current reference of i_1 at $k+1$.

It can be observed that the crucial aspect of achieving current tracking MFPC lies in setting up and updating the data table. Due to the symmetry among the three phases, the relationship between the current of the three phases is shown as follows:

$$i_{1a} + i_{1b} + i_{1c} = 0. \tag{6}$$

When the data table is not updated within several sampling periods, the reliability of (5) will decrease, leading to what is known as the MFPC update stagnation problem. To solve this problem, a synchronous updating method is designed.

First, the composition of the current difference is analyzed as

$$\begin{aligned} i_{1d}(k+1) &= (1 - \tfrac{R_1 T_s}{L_1}) i_{1d}(k) + \tfrac{T_s}{L_1}(e_d(k) \\ &\quad u_{1d}(k)) + T_s i_{1q}(k) \\ i_{1q}(k+1) &= (1 - \tfrac{R_1 T_s}{L_1}) i_{1q}(k) + \tfrac{T_s}{L_1}(e_q(k) \\ &\quad u_{1q}(k)) - T_s i_{1d}(k) \end{aligned} \ . \tag{7}$$

TABLE I
OUTPUT OF THE T-TYPE CONVERTER

Switching state	V_{out}	S_{n1}	S_{n2}	S_{n3}	S_{n4}
[P]	$0.5V_{dc}$	on	on	off	off
[O]	0	off	on	on	off
[N]	$-0.5V_{dc}$	on	off	on	on

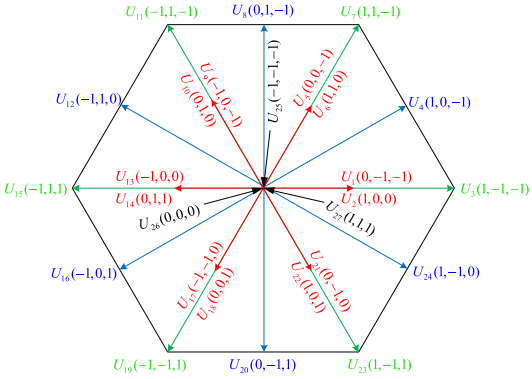

Fig. 3. Switching vector distribution of 3LT^{2}C SAPF.

Thus, the current difference caused by different voltage vectors can be expressed as follows:

$$\begin{aligned} i_{1d}|U_j &= i_{1d0} + i_{1d}|U_j \\ i_{1q}|U_j &= i_{1q0} + i_{1q}|U_j \end{aligned} \tag{8}$$

where

$$\begin{aligned} i_{1d0} &= \frac{T_s}{L_1}(e_d - R_1 i_{1d}) + T_s i_{1q} \\ i_{1q0} &= \frac{T_s}{L_1}(e_q - R_1 i_{1q}) - T_s i_{1d} \\ i_{1d}\ U_j &= \frac{T_s}{L_1} u_{1d}|U_j \\ i_{1q}\ U_j &= \frac{T_s}{L_1} u_{1q}|U_j \end{aligned} \tag{9}$$

where i_{1d0} and i_{1q0} represent the natural attenuation of the *dq*-axis current caused by zero vector. e_d and e_q represent the ideal grid voltage under the *dq*-axis. $i_{1d}|U_j$ and $i_{1q}|U_j$ represent the enforced responses of current caused by a nonzero vector. $u_{1d}|U_j$ and $u_{1q}|U_j$ represent the input voltages that vary along with the switching vector U_j.

2) Establishment of Current Differential Matrix: Equation (9) demonstrates that the current difference can be divided into two components: natural attenuation caused by the zero vector and enforced response caused by the nonzero vector. Based on the working states of the four switching devices in each phase, the output voltage exhibits three voltage levels, as given in Table I, where $n = a, b, c$. Each phase of the 3LT^{2}C includes three switching states: [*P*]; [*O*]; and [*N*]. Thus, the 3LT^{2}C has 27 switching states, which can be interpreted as candidate voltage vectors for MFPC.

In addition, Fig. 3 demonstrates that the input voltage evoked by distinct nonzero vectors is correlated.

Therefore, as given in Table II, the 27 switching vectors can be divided into 7 categories, where in-phase and anti-phase vectors are considered as the same category.

TABLE II
SWITCHING VECTOR TABLE

Category	Switching Vectors
1	$U_1, U_2, U_3, U_{13}, U_{14}, U_{15}$
2	U_4, U_{16}
3	$U_5, U_6, U_7, U_{17}, U_{18}, U_{19}$
4	U_8, U_{20}
5	$U_9, U_{10}, U_{11}, U_{21}, U_{22}, U_{23}$
6	U_{12}, U_{24}
7	U_{25}, U_{26}, U_{27}

In Table II, the seventh category is zero vector, and the current differences caused by them are solely due to natural attenuation. On the other hand, the remaining vectors induce an enforced response in addition to the natural attenuation, and the enforced response is dependent on the phase and amplitude presented in Fig. 3. The update mechanism for categories 1, 3, and 5 current differences is analogous, while categories 2, 4, and 6 follow a similar updating pattern. Once the natural attenuation and the current difference resulting from any switching vector within the category are known, the current difference i_{1m} caused by other switching vectors in this category is deduced as follows:

$$\begin{aligned} &i_{1m}|U_2 = i_{1m}|U_1,\quad i_{1m}|U_6 = i_{1m}|U_5, \\ &\quad i_{1m}|U_{22} = i_{1m}|U_{21} \\ &i_{1m}|U_{16} = i_{1m}|U_4,\quad i_{1m}|U_{20} = i_{1m}|U_8 \\ &i_{1m}|U_{24} = i_{1m}|U_{12} \\ &i_{1m}|U_{14} = i_{1m}|U_{13} = (i_{1m}|U_1 - i_{1m0}) + i_{1m0} \\ &i_{1m}|U_{10} = i_{1m}|U_9 = (i_{1m}|U_{21} - i_{1m0}) + i_{1m0}. \\ &i_{1m}|U_{18} = i_{1m}|U_{17} = (i_{1m}|U_5 - i_{1m0}) + i_{1m0} \\ &i_{1m}|U_3 = i_{1m}|U_3 = 2(i_{1m}|U_1 - i_{1m0}) + i_{1m0} \\ &i_{1m}|U_7 = i_{1m}|U_{19} = 2(i_{1m}|U_5 - i_{1m0}) + i_{1m0} \\ &i_{1m}|U_{23} = i_{1m}|U_{11} = 2(i_{1m}|U_{21} - i_{1m0}) + i_{1m0} \\ &i_{1m}|U_{25} = i_{1m}|U_{26} = i_{1m}|U_{27} = i_{1m0} \end{aligned} \tag{10}$$

Equation (10) provides the specific values for each current difference, while (11) shows the current difference matrix for all 27 switching sequences

$$i_{1m} = \begin{matrix} i_{1m}|U_1 & i_{1m}|U_2 & i_{1m}|U_3 \\ i_{1m}|U_4 & i_{1m}|U_5 & i_{1m}|U_6 \\ i_{1m}|U_7 & i_{1m}|U_8 & i_{1m}|U_9 \\ i_{1m}|U_{10} & i_{1m}|U_{11} & i_{1m}|U_{12} \\ i_{1m}|U_{13} & i_{1m}|U_{14} & i_{1m}|U_{15} \\ i_{1m}|U_{16} & i_{1m}|U_{17} & i_{1m}|U_{18} \\ i_{1m}|U_{19} & i_{1m}|U_{20} & i_{1m}|U_{21} \\ i_{1m}|U_{22} & i_{1m}|U_{23} & i_{1m}|U_{24} \\ i_{1m}|U_{25} & i_{1m}|U_{26} & i_{1m}|U_{27} \end{matrix}. \tag{11}$$

3) Harmonic Current Extraction: The harmonic current of the nonlinear load should be extracted and used as the reference. The widely used i_p-i_q method [24], [25], [26], [27] is employed here (see Fig. 4). Initially, Clarke and Park transformations are performed on the three-phase load currents. Subsequently, the load current components i_{ld} and i_{lq} are filtered via a low-pass filter with a 20-Hz cut-off frequency, to remove the ac

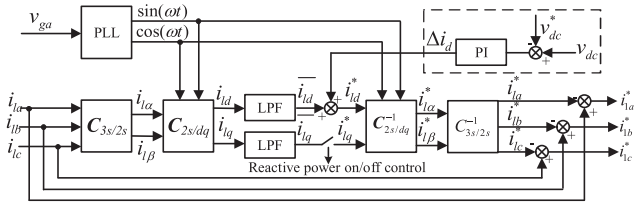

Fig. 4. Harmonic extraction diagram implementing i_p-i_q method.

components. Finally, the fundamental component of the three-phase load current is derived via the inverse Clarke and Park transformations of the filtered current. The reference harmonic currents i_{1a}, i_{1b}, and i_{1c} are the results of the load currents minus the fundamental currents. Additionally, the dc-bus voltage regulation block is constructed by introducing an active power reference signal i_d to the *d*-component.

C. MFPC for NP Voltage Balance

Based on the previous analysis, the NP voltage, denoting the voltage at the midpoint of the dc capacitor labeled "O" in Fig. 1, should be close to 0 V. It can be assumed that the reference value for the NP voltage is 0 V. By collecting the voltage and current on both sides of the dc bus capacitor, different NP voltage predictions under different switching vectors can be obtained. The predictive NP voltage and the cost function are given as follows:

$$V_{np}^{pre}(k+1) = \frac{V_p(k)}{2i_p(k)} \quad i_{1a}(k) \quad i_{1b}(k) \quad i_{1c}(k) \quad U_j(k \quad 1) \quad (V_n(k) \quad V_p(k)) \tag{12}$$

$$J_{np} = \quad 0 \quad V_{np}^{pre}(k+1) \tag{13}$$

where V_p is the voltage of the upper capacitor, V_n is the voltage of the lower capacitor, V_{np}^{pre} is the prediction value for NP voltage, and i_p is the capacitor current.

D. MFPC for DC-Bus Voltage

The dc-bus voltage should be maintained stable. According to the literature review and practical engineering requirements, it can be found that the dc-bus voltage should be kept around 800 V to ensure the normal operation of SAPF [28], [29]. Therefore, a proportional-integral controller is used for the external dc-bus voltage. The time response of the dc-bus voltage controller is significantly slower than the output current using MFPC controller in the inner loop, thereby avoiding interference between them. The predicted and reference values for the dc-bus voltage are calculated as follows:

$$\begin{aligned} V_{dc}^{pre}(k+1) &= V_{dc}(k) \quad \frac{V_p(k)}{2i_p(k)} \bullet i_{1a}(k) \quad i_{1b}(k) \quad i_{1c}(k) \\ &\quad \bullet U_j(k \quad 1) \\ V_{dc}(k+1) &= V_{dc}(k) + 0.25 \times [800 \quad V_{dc}(k)] \end{aligned} \tag{14}$$

$$J_{dc} = V_{dc}(k+1) \quad V_{dc}^{pre}(k+1) \tag{15}$$

where V_{dc}^{pre} is the predicted voltage and V_{dc} is the reference for dc-link voltage.

IV. Design of SMFPC

A. Block Diagram of SAPF With SMFPC

Once the control objectives are determined, the optimal solution can be selected by evaluating the cost functions and weighting factor. However, the optimal weighting factor selection can be quite time-consuming. To overcome this drawback, sequential method is employed in this case. Furtherly, SMFPC is proposed, which combines the sequence method with MFPC and determine the order of the three-stage screening through priority arrangement to get the optimal switching vector.

The complete control block diagram of 3LT^{2}C SAPF with SMFPC is illustrated in Fig. 5. The entire SMFPC system involves the control of NP voltage, dc-bus voltage, and converter-side current. First, voltage and current sensors are used to sample the voltage values (V_p, V_n), current values (I_p, i_{1m}) and switch states ($U_1(k)$, $S_1(k)$), which are used for state variable estimation.

Subsequently, the measured V_p, I_p, and V_n are used as inputs to calculate the predicted value of V_{np} under different switching sequences. The cost functions of different sequences are calculated and a group of n_1 sequences with the smaller cost function is selected to form the switching sequence W_1 after the initial sequential selection. The measured i_{1m}, $U_1(k)$, and $S_1(k)$ from sensors are used as inputs. $i_{1m}(k \quad 1)$ is updated by $i_{1m}(k)$ and the predicted values of i_{1m} under different switch states are calculated. The harmonic extraction method is applied to obtain the reference current of $i_1(k+1)$. The cost functions with different sequence are then calculated. From the switch sequences obtained in the previous step, n_2 sequences with the smaller cost function are selected from W_1, and the switching sequence W_2 is formed after the second sequential selection. By employing the harmonic extraction method, the reference dc-bus voltage (V_{dc}) is obtained. Considering the dc-bus voltage, the cost function of each switch sequence in W_2, is directly calculated and the switching sequence with the minimum cost function is selected.

The switching sequence is converted into different status of converters according to Table I to directly control 3LT^{2}C SAPF, subsequently influencing the *LCL* filter and ultimately compensating for the harmonic components due to the nonlinear load, thus maintaining the high-quality grid current. Additionally, the current, voltage, and switching status at $k \quad 1$ are sampled to get the switching state at time instant k.

B. Priority Analysis

For the NP voltage, due to its mathematical expression [in (12)], J_{np} remains identical when certain switching vectors are applied. $V_{np}(k+1)$ remains unchanged regardless of whether $U_j(k \quad 1)$ equals 100 or $\quad 100$ (where 1, 0, $\quad 1$ represent [*P*], [*O*], and [*N*] in Table I, respectively.). This implies that 100 and $\quad 100$ have an equivalent control effect on NP voltage. Thus, the 27 switching vectors of J_{np} are divided into 8 groups, where all switching vectors within each group have the same control effect, as given in Table III.

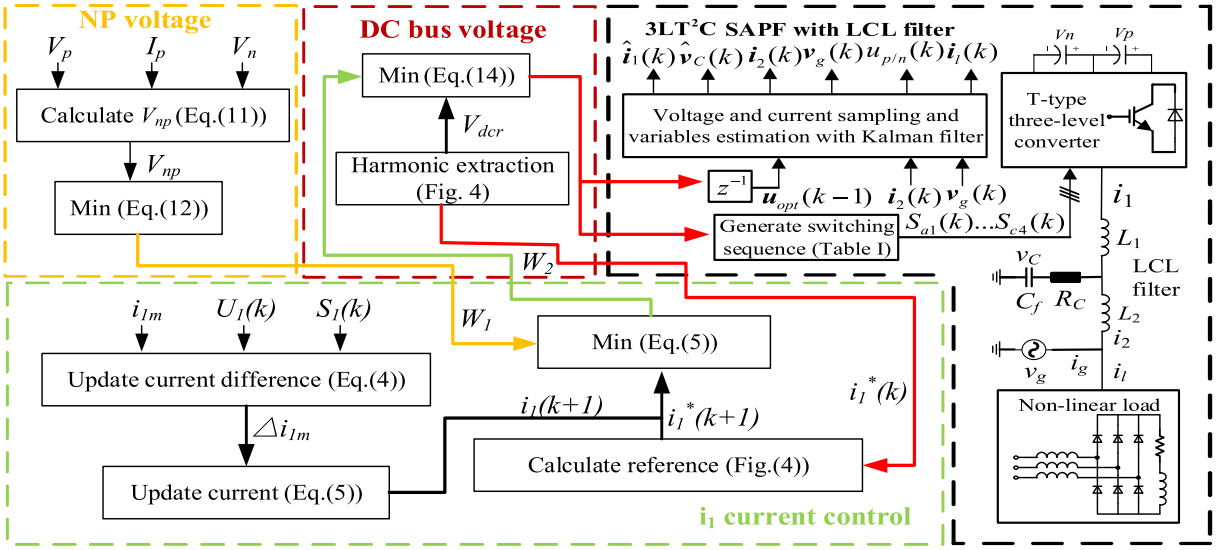

Fig. 5. Implementation block diagram of SMFPC for 3LT^2 C SAPF.

TABLE III
SWITCHING VECTORS OF J_{np}

Switching Vectors	Group
000	G_{np1}(000)
001,00-1	G_{np2}(001)
010,0-10	G_{np3}(010)
100, -100	G_{np4}(100)
011,0-1-1,01-1,0-11	G_{np5}(011)
101, -10-1, -101,10-1	G_{np6}(101)
110, -1-10, -110,1-10	G_{np7}(110)
111, -1-1-1, -111,1-11,11-1, -1-11,1-1-1,1-1-1	G_{np8}(111)

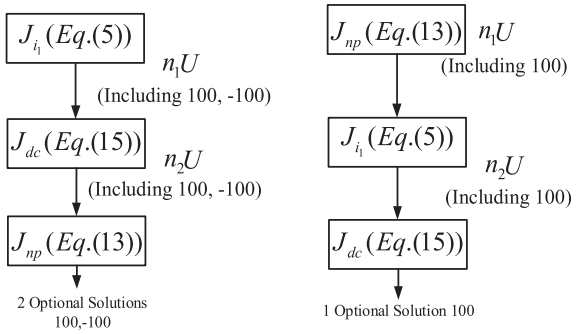

Fig. 6. Example of J_{np} at different sequences.

When exhaustively calculating the optimal or suboptimal solution for J_{np}, only eight switching vectors are substituted instead of 27 switching vectors. So, if J_{np} is in the final layer, there may exist more than one optimal solution.

For example, when 100 is identified as the optimal solution for J_{np}, based on Table III, 100 would also be considered optimal. In such cases, there is no definitive basis for selecting between the two switching vectors, as illustrated in Fig. 6. But if J_{np} is positioned in the initial layer, dividing the switching vectors into distinct groups can efficiently reduce the number of

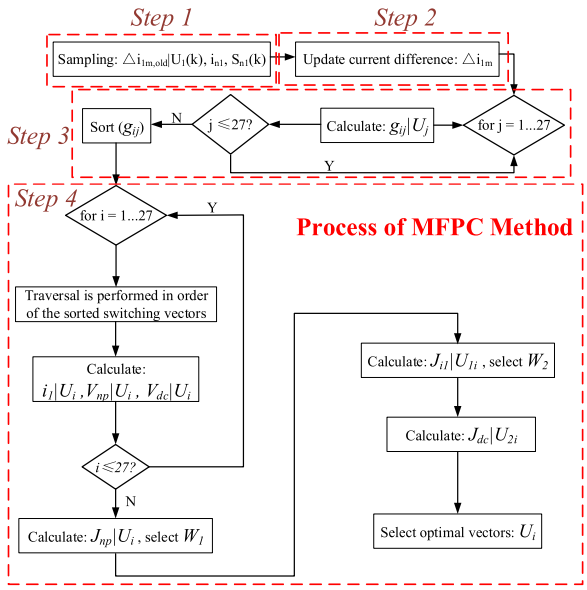

Fig. 7. Implementation block diagram of the proposed SMFPC.

vectors evaluated, thus saving time and enhancing effectiveness in the process.

As for i_1 and dc-bus voltage, i_1 holds greater significance as the APF is primarily utilized for direct harmonic compensation of the grid current. Conversely, a certain degree of fluctuation in the dc-bus voltage around 800 V is permissible. So i_1 should be controlled in ahead of dc-bus voltage.

C. Implementation Steps of SMFPC

The implementation of SMFPC is shown in Fig. 7 and is explained as follows.

Step 1: The grid current i_{g1}, dc-side capacitor voltage and current at time instant k are sampled by the voltage and current

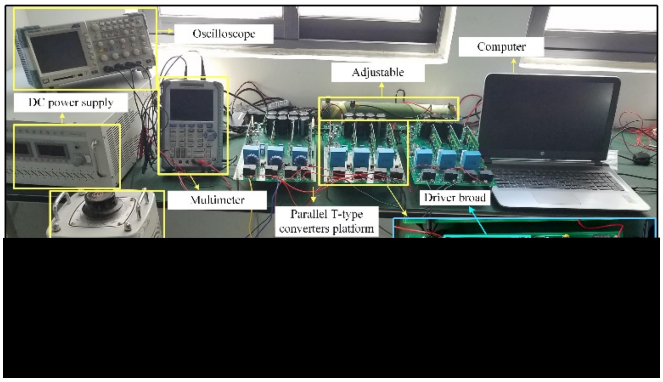

Fig. 8. Experimental setup.

sensors. Based on the sampled dc capacitor voltage, the NP voltage deviation $V_1(k)$ is calculated. Subsequently, the switching state $S_{n1}(k)$ can be obtained using the optimal switching vector predicted at k 1 stored in the data table. Additionally, the difference in grid current on the *dq*-axis $i_{1m}|U(k)$ can be computed by substituting the grid current sampled at time k 1 from the data table and the grid current sampled at k into (2).

Step 2: Based on the switching state and current difference at time k, the current difference resulting from each switching vector can be determined and updated.

Step 3: The updated current difference and (10) are used to compute the current difference caused by different switching vectors. Subsequently, the sorted order of switching vectors is recorded. The current reference is derived from the previously mentioned harmonic extraction.

Step 4: The fundamental principle for selecting the optimal solution involves the traversal method. The switching vector order is arranged based on the current difference. During the sorting process, the switching vector that satisfies NP voltage balance is initially selected. Specifically, arrange the values of J_{np} in ascending order, select the top n_1 groups of switch vectors to form the switching vector matrix W_1. Subsequently, W_1 is traversed and the values of the cost function J_{i_1} for current tracking are recorded. Arrange the values of J_{i_1} in ascending order, select the top n_2 groups of switch vectors to form the switching vector matrix W_2. Finally, W_2 is traversed and J_{dc} for the dc-bus voltage PID controller is recorded. Consequently, arrange the values of J_{dc} in ascending order and the first set of switching vectors is selected as the optimal switching sequence.

V. Experimental Results

A. Hardware Setup

To validate the effectiveness of the proposed strategy, a three-phase 3LT^{2}C LCL-type SAPF with a rated power of 10 kW was constructed in the laboratory. Fig. 8 shows the experimental setup, wherein the 3LT^{2}C consists of six FUZI 1MBH50D-060 IGBTs and six FUZI 2MBI150U2A-060 IGBTs. Six Hall current sensors (HCS-LTS-06A) were used to measure the converter current and grid current. A fundamental frequency transformer was employed to facilitate voltage matching between the control effect is minimally impacted by the model parameters. The proposed SMFPC and TMPC method is implemented in TMS320F28379D digital-signal-processor from Taxus instrument, USA. Therefore, there is no necessity to explicitly define the parameters of the model. During the experiment, both SMFPC and TMPC methods were employed, the parameter specification of the TMPC system is given in Table IV.

TABLE IV
Parameter Specifications

Parameter	Description	Values
$C_1(\mu F)$	DC-link capacitance	500
$L_1(mH)$	Converter-side inductance	6
$L_2(\mu H)$	Grid-side inductance	10
$C(\mu F)$	Filter capacitance	10
$R_1(\Omega)$	Converter-side resistance	0.1
$R_2(\Omega)$	Grid-side resistance	0.1
$R_C(k\Omega)$	Resonance damping resistance	1
$V_g(V)$	Grid voltage (RMS)	$200\sqrt{2}$
$\omega(rad/s)$	Grid frequency	314.16
$f_s(kHz)$	Sampling frequency	20
K_p	Proportion coefficient	0.05
K_i	Integral coefficient	0.2
$R_n(\Omega)$	Load resistance	20
$L_n(mH)$	Load inductance	8

To evaluate the computation burden of different control methods, namely, SMFPC and TMPC algorithm, two breakpoints are set in the program debugging environment CCS10.1 for the TMS320F28379D, the time difference between the two breaking points are the calculation time. The results indicate that, the calculation time for SMFPC takes about 45 μs, compared with 38 μs with TMPC methods. TMPC method has the lowest calculation time because it does not need the linear fitting function for current prediction.

B. Error Rate Definition for Analysis of Experimental Results

To evaluate the tracking performance, the error rate k_x^{err} is defined as

$$\begin{aligned} i_x^{err} &= |i_x \quad i_x| \\ k_x^{err} &= \frac{i_x^{err}}{i_x} \quad 100\% \end{aligned} \tag{16}$$

where i_x^{err} represents the tracking error for different variables, i_x represents the references, i_x represents the predicted value, and k_x^{err} represents the tracking error rate for each control object.

C. Experimental Results Under Unbalanced Nonlinear Load

To evaluate the proposed SMFPC under nonlinear unbalanced loads, the transition from balanced loads Z_n to unbalanced loads (an additional load with $R = 20$ and $L = 8$ mH in phase-A, which is marked as Z_w) by opening switch S_w is shown as Fig. 9.

Fig. 10 illustrates the experimental results for each control objective. Fig. 10(a) displays the waveforms of the output current of SAPF and its reference, along with the tracking errors. Fig. 10(b) shows the waveforms of the grid current and its reference, as well as their tracking errors. Meanwhile, the NP voltage in Fig. 10(c) fluctuated around 0.5 V, with a maximum value of 2.2 V, indicating successful control of the NP voltage.

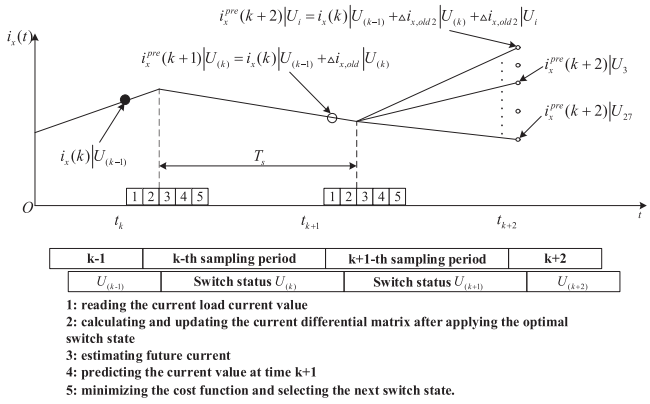

Fig. 2. Working principle for linear fitting MFPC.

III. Proposed Linear Fitting SMFPC

A. Basic Idea of Linearly Fitting SMFPC

Fig. 2 illustrates the principle of linear fitting the current operation. Through analyzing current variances, SMFPC does not need any prior knowledge of circuit parameters or models. The calculations of current differences involve simple addition and subtraction operations, thereby alleviating the computational burden. It directly regulates electronic devices by considering voltage and current values over a specific timeframe to ensure their continuity in following established patterns.

Due to its high sampling frequency (over 15 kHz) and the utilization of only one switching state per control cycle, it can be inferred that the converter-side current linearly fluctuates during every control cycle. Therefore, by calculating the difference and sampling the current values, it becomes feasible to predict the converter-side current. To compensate the control-delay in implementation, a two-step prediction method is applied [23].

In Fig. 2, the segments labeled as 1, 2, 3, 4, and 5 represent distinct sequence segments, each with specific operations marked. U denotes different switching sequences. As the current $i_x(k)$ is required for selecting the switch sequences at $k+1$, there exists a delay between the current and switch sequences, quantified as a unit of "1". $i_x(k)|U_{(k-1)}$ represents the current at k under the influence of the switching sequence at $k-1$. $i_{x,\,old}|U_i$ represents the prior current difference under the switching sequences U_i. Throughout the entire process, the circuit topology remains constant. Hence, the current difference under $U_{(k)}$ at k should be approximately equal to that generated after the last selection of switch sequence $U_{(k)}$. According to the linear fitting theory, it can be inferred that the predictive value for $i_x(k+1)$ will be written as:

$$\begin{aligned} i_x^{pre}(k+1)\,U_{(k)} &= i_x(k)\,U_{(k-1)} + i_{x,old}\,U_{(k)} \\ i_x^{pre}(k+2)|U_i &= i_x(k)\,U_{(k-1)} + i_{x,old}\,U_{(k)} \\ &\quad + i_{x,old}|U_i\,. \end{aligned} \tag{1}$$

The computational procedure described above is iterated sequentially to derive the predicted values for different switching states. During the calculation process, it is crucial to acquire the current differential values under different switching sequences and establish the current differential matrix.

B. Grid Current Prediction for MFPC

1) Theoretical Analysis: The principle of MFPC is illustrated in Fig. 2. Taking the A-phase of the 3LT^{2}C SAPF in Fig. 1 as an example, the current difference at k can be expressed as follows:

$$\begin{aligned} i_{1m}(k) &= i_{1m}(k)\,U_{(k-1)} - i_{1m}(k-1)\,U_{(k-2)} \\ i_{1m}(k+1) &= i_{1m}(k+1)\,U_{(k)} - i_{1m}(k)\,U_{(k-1)} \end{aligned} \tag{2}$$

where $i_{1m}(m = d, q)$ represents the dq-axis difference of the grid current, and U represents the switching vector.

However, the current difference at $k+1$ cannot be obtained at k. Under the condition that the sampling time T_s is fixed and short enough, any two consecutively calculated current differences under the same voltage vector are close to each other. So, the previous value can be used instead. The substituted current difference is approximated as follows:

$$i_{1m}(k+1) \quad i_{1m,old}\,U_{(k+1)}\,, U_{(k+1)} \quad \{U_1, \ldots, U_{27}\} \tag{3}$$

where the subscript "old" represents the previous current difference stored in the memory of the microprocessor.

Thus, by combing (2) and (3), the current prediction equation of MFPC can be derived as follows:

$$\begin{aligned} i_{1m}^{pre}(k+2)\,U_j &= i_{1m}(k) + i_{1m,old}\,U_{(k)} + i_{1m,old}|U_j \\ U_j &\quad \{U_1, \ldots, U_{27}\}\,. \end{aligned} \tag{4}$$

The cost function of MFPC for the grid current tracking can be expressed as follows:

$$\begin{aligned} J_{i_1} = &\; i_{1d}(k+1) - i_{1d}^{pre}(k+2)\,U_j| + i_{1q}(k+1) \\ &- i_{1q}^{pre}(k+2)\,U_j| \end{aligned} \tag{5}$$

where $i_{1m}(k+1)$, $(m = d, q)$ represents the current reference of i_1 at $k+1$.

It can be observed that the crucial aspect of achieving current tracking MFPC lies in setting up and updating the data table. Due to the symmetry among the three phases, the relationship between the current of the three phases is shown as follows:

$$i_{1a} + i_{1b} + i_{1c} = 0. \tag{6}$$

When the data table is not updated within several sampling periods, the reliability of (5) will decrease, leading to what is known as the MFPC update stagnation problem. To solve this problem, a synchronous updating method is designed.

First, the composition of the current difference is analyzed as

$$\begin{aligned} i_{1d}(k+1) &= \left(1 - \frac{R_1 T_s}{L_1}\right) i_{1d}(k) + \frac{T_s}{L_1}\left(e_d(k) - u_{1d}(k)\right) + T_s i_{1q}(k) \\ i_{1q}(k+1) &= \left(1 - \frac{R_1 T_s}{L_1}\right) i_{1q}(k) + \frac{T_s}{L_1}\left(e_q(k) - u_{1q}(k)\right) - T_s i_{1d}(k) \end{aligned}\,. \tag{7}$$