Parallel Capacitive-Link Universal Converters With Low Current Stress and High Efficiency

Junhao Luo, *Student Member, IEEE*, Khalegh Mozaffari, *Senior Member, IEEE*, Brad Lehman, *Fellow, IEEE*, and Mahshid Amirabadi, *Senior Member, IEEE*

***Abstract*—Series capacitive-link universal converters are a relatively new class of single-stage power converters that offer numerous advantages including high reliability, high power density, and high efficiency. However, one of the limitations of these converters is high current stress of the switches, which lowers their efficiency especially in high current applications. In this article, a new class of soft-/hard-switched parallel capacitive-link converters is introduced to address this limitation of the series capacitive-link universal converter while keeping its advantages. Apart from providing bidirectional power transfer, the proposed ac–ac converter can implement voltage stepping up/down as well as frequency transformation. A small film capacitor, which is placed in parallel with the input and output switch bridges, is responsible for transferring the power from input towards output. A small inductor can be placed in series with the link capacitor to realize zero-current-switching for all the switches under any load conditions, which lowers the switching losses and reduces electromagnetic interference (EMI). The proposed parallel capacitive-link converter is expected to offer an enhanced efficiency and reduced current stress compared to the series capacitive-link universal converters. In this article, principles of the operation of the proposed converter are presented, and its performance and advantages are verified by simulation and experiment.**

***Index Terms*—Current stress, efficiency, parallel capacitive-link converter, series capacitive-link converter, universal converter, zero current switching (ZCS).**

I. Introduction

AC–AC power converters are widely utilized in industrial applications including variable-speed drive systems, solid-state transformer, and wind power generation systems, where high power density, high reliability, high efficiency, and low cost are preferred.

The ac–ac converters can be classified as direct and indirect types. The traditional two-level back-to-back indirect converter, which is composed of a pulse width modulation (PWM) rectifier and a PWM inverter decoupled by a capacitor forming the dc-link, is the most widely utilized ac–ac converter in low voltage systems. Control flexibility as well as simple topology are the main advantages of this converter. However, a large capacitor is required in the two-level back-to-back converter to decouple the inverter and rectifier [1], resulting in a low power density. Depending on the switching frequency, this capacitor may be of electrolytic type, which is sensitive to temperature and the prominent cause of failure in power converters.

Direct PWM ac–ac converters [2], [3], [4], [5] are another type of converters, which are developed from their dc–dc counterparts. In [2], several three-phase PWM ac–ac converter topologies derived from buck, boost, buck–boost, Ćuk, and flyback are introduced. A three-phase Z-source ac–ac converter employing bidirectional switches capable of both stepping up and stepping down the voltage is proposed in [3]. In [4], a three-phase ac–ac converter with switched capacitor settings and voltage stepping up/down capability is proposed. The distinct feature of this topology lies in the elimination of all magnetic components, which leads to smaller volume and a higher power density. However, 12 bidirectional switches are required in this topology and the voltage gain is limited. Most of the direct converters discussed here are subjected to a common commutation problem [5] due to inherent overlap or dead time in the gate signals, which affects the reliability of the system. Besides, the direct PWM ac–ac converters are mostly hard-switching, and suffer from high-switching losses, high-switching stresses, and electromagnetic interference (EMI) problems.

Matrix converters [6], [7], [8], [9], [10], [11], [12] are another candidate for single-stage ac–ac power conversion. In matrix converters the power transfer is realized directly by bidirectional switches rather than any energy storage components. Simultaneous voltage amplitude and frequency control can be realized in these converters. The conventional ac–ac matrix converters have a high requirement on the number of switches. In [7], a series of three-phase ac–ac matrix converters, named sparse, very-sparse and ultrasparse converter with reduced number of switches is proposed to solve the problem. However, the power transfer direction, the phase shift, the voltage, and current transfer ratios are limited in these converters.

Several high-frequency ac-link topologies have also been proposed. Multiple resonant ac-link power converter topologies that benefit from soft-switching are presented in [15], [16], [17], [18], and [19]. However, these converters suffer from high

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Junhao Luo, Brad Lehman, and Mahshid Amirabadi are with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115 USA (e-mail: luo.ju@northeastern.edu; lehman@ece.neu.edu; m.amirabadi@northeastern.edu).

Khalegh Mozaffari is with the Enphase Energy Inc., Fremont, CA 94538 USA (e-mail: kmozaffari@enphaseenergy.com).

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reactive rating of the link elements, increased conduction-loss, and higher voltage and current ratings of the switches and diodes. Moreover, there are restrictions for some load conditions as a result of potential oscillation as well as instability issues [19], [20].

Universal power converters are another category of single-stage power converters. These topologies can be designed with any number of phases and any type of source and load. The input and output voltage amplitudes, frequencies as well as power factors, can vary in a wide range. Unlike two-level back-to-back indirect converters, universal converters do not need to decouple the input side and output side switches, and a small capacitor or inductor is utilized for transferring the power from input to output. This eliminates the requirement of large electrolytic capacitors that have high failure rates. Universal power converters are, in general, categorized as inductive-link and capacitive-link.

In inductive-link universal converters with soft-switching, the link is composed of an inductor placed in parallel with a small capacitor. The inductor acts as the primary power transfer component, and capacitor only facilitates soft-switching. Series and parallel inductive link universal converters were presented and studied in [21], [22], [23], [24], [25], [26], [27], and [28]. However, the switches in these topologies may experience high voltage and current stress as well as high power loss as a result of the discontinuous currents. To address this issue, several series inductive-link converters with multifunction control, which can notably decrease the link current peak, are proposed in [29] and [30]. Since inductive-link universal converters employ the bidirectional blocking, unidirectional conducting switches, which is usually realized by an IGBT/MOSFET with a series diode, conduction loss is higher than topologies that employ unidirectional blocking switches. A Zeta-based universal converter using an inductive-capacitive link is presented in [31]. However, this topology needs two power transferring elements and its control is more complex.

Capacitive-link universal converters presented in [32], [33], [34], [35], [36], and [37] are another class of universal converters. This type of converter is derived from a dc–dc Ćuk converter, and the link capacitor transfers power from the input to the output. The capacitive-link universal converters can be configured to offer soft-switching through the addition of a small inductor placed in series with the link capacitor. A family of series capacitive-link universal converters in which the link voltage can be both positive and negative, are presented in [32] and [33]. However, four-quadrant switches are required in this converter, resulting in 24 switches for three phase ac–ac application, and the control is complex. To lower the number of switches and reduce the cost, modified topologies using two-quadrant switches and the corresponding control strategy are introduced in [34], [35], and [36]. The hard-switching series capacitive-link three-phase ac–ac converters with fixed and variable switching frequencies are proposed and analyzed in [37]. Series capacitive-link converter, as shown in Fig. 1, provides numerous merits. It offers high reliability due to using a very small link capacitor, even in high power applications, which can be of film type rather than electrolytic type. This converter has a high-power density due to using small link capacitors and the possibility of using high frequency transformers for providing galvanic

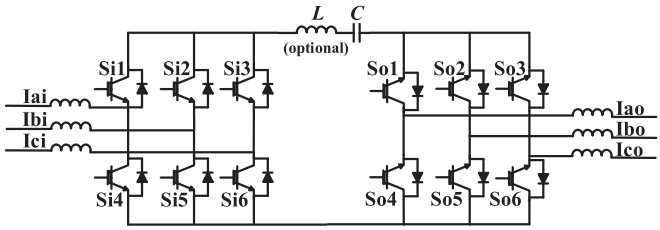

Fig. 1. Series capacitive-link three-phase AC–AC converter with soft-switching.

isolation. Despite all these advantages, the series capacitive link universal converters suffer from high current stress across the switches/diodes. In [38], a dc-to-three-phase inverter employing a small dc-link capacitor in parallel with the input and output switch bridges is introduced. This inverter is hard switching and requires an idle interval since the converter will enter the next active mode automatically.

In this article, an innovative class of soft-switching single-stage parallel capacitive-link universal converters are proposed to address the shortcomings of series capacitive-link universal converters. The high-frequency ac link, which is formed by a small film capacitor with an optional series inductor, is placed in parallel with the input and output switch bridges in this bidirectional topology. The link capacitor is responsible for power transfer from source(s) to load(s). The link inductor can realize partial resonances to facilitate zero current switching (ZCS) for all the switches, which reduces switching losses and EMI. In the series capacitive link universal converters, the input currents go through the output switches/diodes when charging the link capacitor, and the output currents flow through the input switches/diodes when discharging the link capacitor. This leads to increased current stress of the switches/diodes. In the proposed parallel capacitive link universal converters, the current path of the input and output currents are separated. This feature reduces the current stress and the conduction loss compared to series capacitive-link universal converters while preserving the benefits. The proposed parallel capacitive-link converter requires only 12 bidirectional conducting-unidirectional blocking switches, maintaining the same number of switches as the traditional PWM back-to-back dc-link converters. In comparison to traditional dc-link converters, a higher power density and a longer lifespan can be acquired in the proposed converter since the link capacitor is much smaller. Moreover, the proposed ac–ac converter can offer voltage stepping up/down as well as frequency transformation. The operation principles of the proposed parallel capacitive-link converters were analyzed, and the features were validated by simulation in [39]. This article presents operation principles, switching patterns, control strategies, and design considerations of the proposed converters in detail, and evaluates the performance by both simulations and experiments.

The rest of this article is organized as follows. Section II presents the proposed three-phase ac–ac converter and its operation principles. Section III describes the corresponding control scheme as well as the specific design process. Section IV evaluates the performance and feature of the proposed converter by

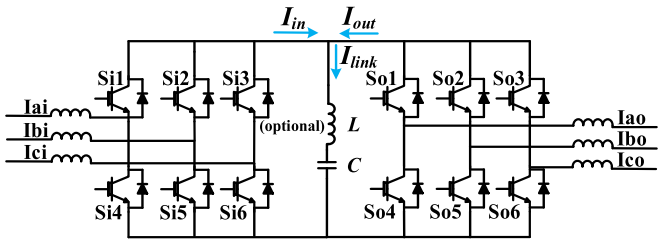

Fig. 2. Proposed parallel capacitive-link three-phase AC–AC converter.

simulation and experiment, and compares it with other converters. Finally, Section V concludes this article.

II. Proposed Topology and Principles of Operation

Fig. 2 depicts the proposed three-phase ac–ac converter. Unlike the series capacitive link, as shown in Fig. 1, the ac link is placed in parallel with the input and output switch bridges in this topology, and the direction of the switches at the output is opposite to that of series-link configuration. The link in hard-switching configuration contains only a small ac capacitor C. Capacitor C in series with a small ac inductor L can form the high-frequency LC tank for soft-switching operation. The link capacitor is responsible for transferring power from source(s) to load(s). The link inductor realizes partial resonances to facilitate soft-switching operation. The input and output switch bridges each require 6 bidirectional conducting and unidirectional blocking switches. Therefore, an IGBT or MOSFET with an antiparallel diode can be employed as a switch in this converter.

In series and parallel capacitive link converters, the link capacitor is first charged from input sources, and then it is discharged into loads. Since the sources and loads are three-phase systems, the charging mode and the discharging mode each can be split into two modes.

It should be noted that the proposed three-phase ac–ac configuration is a parallel capacitive link converter with an optional small inductor for soft-switching operation, which is different from conventional PWM ac–dc–ac converter even though both have a parallel capacitor link between input and output switch bridges. The main differences are as follows.

1) *Control strategy*: The conventional PWM ac–dc–ac converter is two-stage, and the inverter and rectifier stages are controlled individually and independently using well-known modulation techniques. However, the proposed converter is single-stage, and the input-side and output-side switches are controlled simultaneously by turning ON/OFF switches according to input and output zones and modes.
2) *Capacitor type*: Regardless of the switching frequency and power level, the proposed converter utilizes a small film capacitor, which is usually less than several μF and has a longer lifetime compared to electrolytic capacitors [40], while the conventional PWM ac–dc–ac converter typically uses a large capacitor to decouple the inverter and rectifier forming a dc voltage at the link. This capacitor typically needs to be an electrolytic capacitor, which has a shorter lifetime.
3) *Soft switching*: A small inductor can be added to the link of the proposed converter to realize ZCS for all the switches under any load conditions, while the link inductor does not exist in conventional PWM ac–dc–ac converter, which is a hard-switching topology. The addition of the link inductor in the proposed converter minimizes the switching losses and reduces EMI.
4) Link voltage is typically dc in the conventional PWM ac–dc–ac converter; however, in the proposed converter the voltage across the link capacitor is controlled to be at the boundary of continuous conduction and discontinuous conduction modes. Therefore, the link capacitor has a very high voltage ripple in the proposed converter.

The link current and link voltage in the proposed three-phase ac–ac topologies are illustrated for soft-switching and hard-switching operations in Fig. 3(a) and (b), respectively. Each switching cycle in the soft-switching configuration contains four energy transferring modes (the odd modes) and four partial resonance modes (the even modes). There is no partial resonance mode in hard-switching configuration, as shown in Fig. 3(b).

To control this converter the highest, second-highest, and lowest reference currents and reference line–line voltages, which are defined by the absolute values, need to be determined first. For example, if $|V^*_{abi}| > |V^*_{cai}| > |V^*_{bci}|$, then V^*_{abi}, V^*_{cai}, V^*_{bci} are considered the highest, second-highest, and lowest reference line–line voltages, respectively. Fig. 4. illustrates the highest, the second-highest, and the lowest reference line–line voltages in a full line cycle. Although in a line cycle there are two sections having the same highest line–line reference voltage, as displayed in Fig. 5, the polarities of these line–line voltages are reversed. The same principle applies to the reference currents. The converter is controlled such that the lowest and second-highest line–line voltages are regulated, then the highest line–line voltage will be regulated automatically.

Each input and output line cycle will be divided into 12 zones to determine the specific switching pattern for the converter. The input and output zone determination are based on the absolute values of the line-to-line voltages and phase currents, as shown in Fig. 5. Fig. 5(a) depicts the zone determination for the input side, when the power factor is unity, and Fig. 5(b) represents the output zone determination when the power factor is not unity. The power factors for the input and output can vary over a wide range. The line–line voltage and current shown in each zone of Fig. 5 denote the highest line–line voltage and the maximum phase current in the corresponding zone. The phase pair and phase associated with the highest line–line voltage and the maximum phase current change as the zone changes. For instance, the line–line voltage of phase pair ABI is the highest input line–line voltage for zones 1 and 2, while the current of phase A is the maximum input phase current for zones 2 and 3. The sign $*$ at the right top of the voltage or current implies that they are reference values rather than measured values. The negative sign near the voltage or current specifies the negative polarity of the voltage or current. When negative sign is not included, the voltage or current is positive. For example, in zone

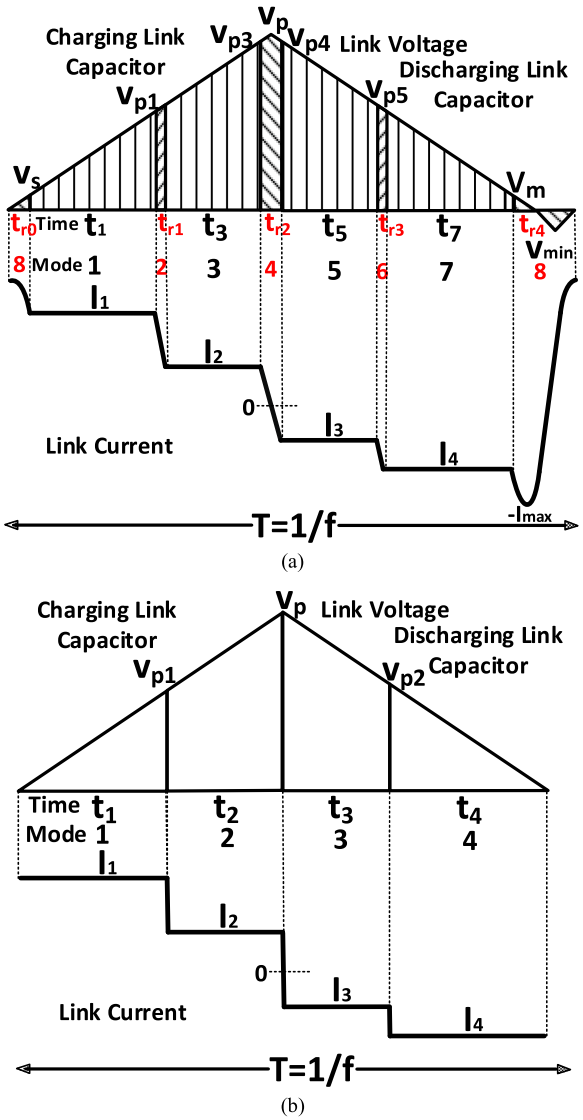

Fig. 3. Link voltage and current of the proposed converter. (a) Soft-switching operation. (b) Hard-switching operation.

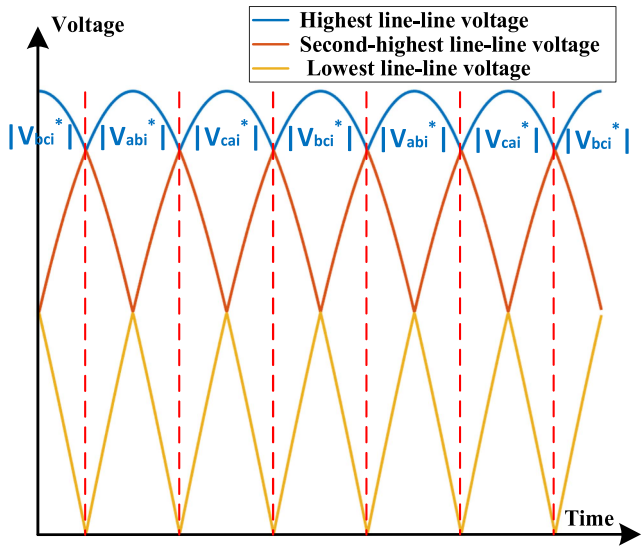

Fig. 4. Reference line-line voltages in a full line cycle.

1 of Fig. 5(a), V^*_{abi} is the reference input line–line voltage with the highest absolute values and it is positive. I^*_{bi} is the reference input phase current with the maximum absolute values and it is negative. It is assumed that the current flowing from left to right to be positive.

In this part, the operation of the proposed soft-switching converter is presented. The behavior of the converter during each mode is shown in Figs. 6 and 7. Modes 1 and 3 are the charging modes, and modes 5 and 7 are the discharging modes. Modes 2, 4, 6, and 8 are the resonant modes. Modes 2, 4, and 6 will be very short and mode 8 will be the longest resonant mode, as shown in Fig. 6. For hard-switching converter, there will be only four modes. Mode and zone are the two factors that determine the switches to be turned ON/OFF in the proposed converter. The input and output zones do not necessarily need to be the same, since the voltage and current references for the input and output do not necessarily have the same frequency and/or phase angle.

Additionally, the starting zone is decided based on the initial phase angle of the reference line–line voltages.

Fig. 6 represents the voltage across the parallel link capacitor (V_{link}), the link inductor current (I_{link}), unfiltered line-to-line voltages for the input (V_{ABI}, V_{BCI}, and V_{CAI}), and unfiltered line-to-line voltages for the output (V_{ABO}, V_{BCO}, and V_{CAO}) during a switching period including 8 operation modes. The current paths and the active elements in each mode are depicted in Fig. 7. It is assumed that for the time interval considered in Figs. 6 and 7 the converter is in zone 2 at the input side and zone 8 at the output side. During this period, the reference of voltage across input phase pair ABI is the maximum line-to-line input voltage, and it is positive. Also, the reference of the voltage across the output phase pair ABO has the maximum line-to-line output voltage and it is negative. Referring to Figs. 4 and 5, the second-highest and the lowest reference line–line voltages are associated with phase pairs *CAI and BCI* for the input, and phase pairs *CAO and BCO* for the output. Even though the input and output references are sinusoidal and vary over a cycle, their values can be considered constant in one switching cycle, since the input and output frequencies are much lower than the switching frequency.

Mode 1 (Charging): As shown in Fig. 7(a), no input switches are turned ON in mode 1 and currents only flow through the antiparallel diodes at the input side. In input zone 2, which is considered in Figs. 6 and 7, I_{ai} has the highest phase current value at the input, as depicted in Fig. 5. During mode 1, the antiparallel diode of switch Si1, which corresponds to the phase carrying the highest input phase current, conducts to charge the link capacitor. The input current flows through the link. While in series capacitive-link universal converters, the input current needs to flow through the link and the output antiparallel diodes, leading to increased conduction losses and higher current stress for the switches/diodes.

During the first charging mode, the link voltage increases. As seen in Fig. 7(a), $V_{\text{ABI}} = -V_{\text{CAI}} = V_{\text{link}}$. The objective

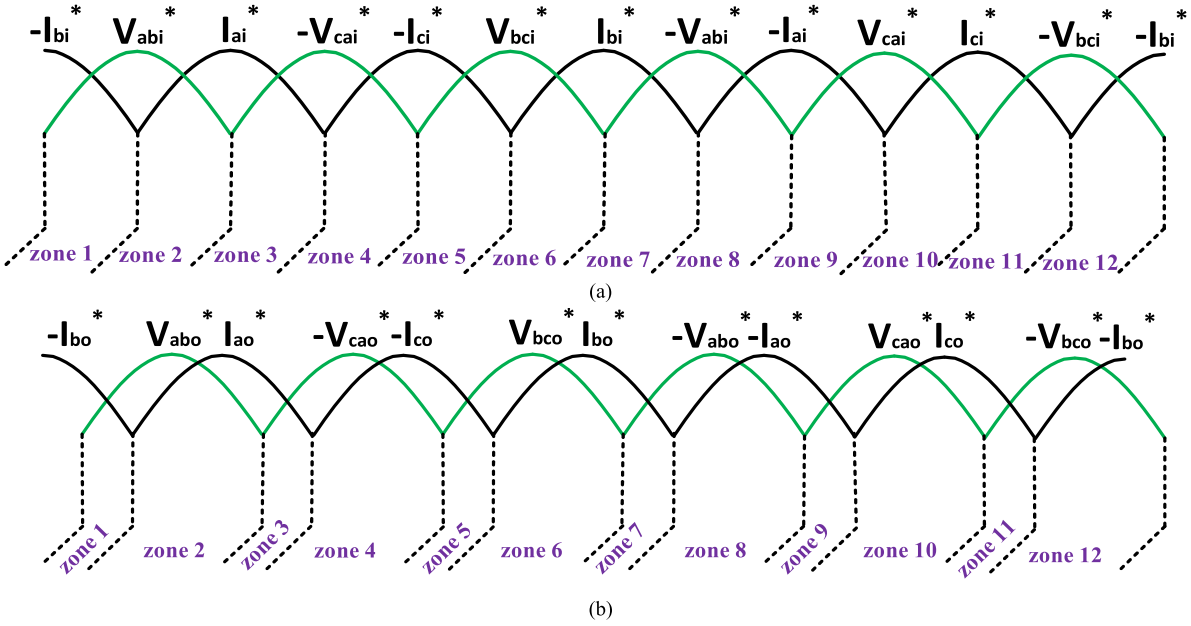

Fig. 5. Zone determination of the proposed converter. (a) Input side. (b) Output side.

in mode 1 is to establish the second-highest line-to-line input voltage (V_{CAI} in Figs. 6 and 7), while also partially building up the highest line-to-line input voltage (V_{ABI} in Figs. 6 and 7). This mode ends by turning on switch Si3 when the average of the unfiltered second-highest line-to-line voltage $V_{\rm CAI}$ meets its reference V^*_{cai}.

Mode 2 (Resonating): In the first partial resonance mode, the input switch Si3 is ON, and the antiparallel diodes of input switches Si1, Si5, and Si6 continue to conduct. Therefore, the link capacitor and the link inductor form a short circuit loop. The conduction of the switches/diodes at the output side remains the same as mode 1. During mode 2, the parallel *LC* link resonates to facilitate soft switching. The link current, which is equal to current of phase A at the beginning of mode 2, decreases and when it becomes equal to the current of input phase B, the current of antiparallel diode of switch Si6 is reduced to zero and its conducting ends under ZCS.

Mode 3 (Charging): The second charging mode aims to regulate the unfiltered lowest input line-to-line voltage, which is associated with phase pair *BCI*, by charging the link capacitor with second-highest input phase current ($I_{\rm bi}$). The link voltage keeps increasing during this mode. The current of input phase B still flows through the antiparallel diode of switch Si5, and the current of input phase C flows through the input switch Si3. The voltage across input switches Si3, Si4, Si6, and output switches So4, So5, So6, which are OFF in mode 3, is equal to $V_{\rm link}$. Thus, the maximum voltage stress on input and output switches is equal to the link peak voltage in a full line frequency cycle. In this charging mode, the link capacitor continues to be charged until the average of unfiltered voltage across phase pair BCI meets its reference V^*_{bci}. Then input switch Si2 and output switch So4 are turned ON, and output switch So3 is turned OFF to begin mode 4. At the end of mode 3, all three input line–line voltages ($V_{\rm CAI}$, $V_{\rm BCI}$, and $V_{\rm ABI}$) are built up and regulated, as exhibited in Fig. 6.

Mode 4 (Resonating): The *LC* link is shorted to allow the *LC* pair to resonate in mode 4, and the link current will decrease from a positive value to a negative value. When the link current meets the current of output phase B, the antiparallel diode of switch So1 stops conducting, and this initiates the first discharging mode.

During the discharging modes, the output current flows only through the link. Unlike the series capacitive link universal converters, the input switches are not involved in discharging the link capacitor.

Mode 5 (Discharging): The first discharging mode targets to regulate the unfiltered lowest output line-to-line voltage ($V_{\rm BCO}$) while the second-highest output phase current ($I_{\rm bo}$) flows through the link capacitor to discharge it. Simultaneously, the highest line-to-line output voltage, which is associated with phase pair ABO in Figs. 6 and 7, will also be partially built up. As shown in Fig. 7(e), $I_{\rm link} = -I_{\rm bo} = I_{\rm ao} + I_{\rm co}$, $V_{\rm link} = -V_{\rm ABO} = +V_{\rm BCO}$, and $V_{\rm CAO} = 0$ in mode 5. During this mode the link voltage decreases until the average of the unfiltered voltage $V_{\rm BCO}$ reaches its reference V^*_{bco}. As soon as this condition is met, switch So3 is turned ON to initiate mode 6.

As seen in Fig. 7(e), input switches Si2 and Si3 are ON during mode 5. These switches are selected according to the input zone, as shown in Fig. 5(a). The specific switching pattern in different zones will be presented in Section III.

Mode 6 (Resonating): In the third partial resonance mode, the output switch So3 is turned ON, while the antiparallel diodes of output switch So6 is still conducting. As a consequence, the *LC* link is shorted and resonates. The link current will decrease until it equals to the largest output current (phase A). Once the condition is met, the conduction of antiparallel diode of switch So6 ends and the second discharging mode 7 starts.

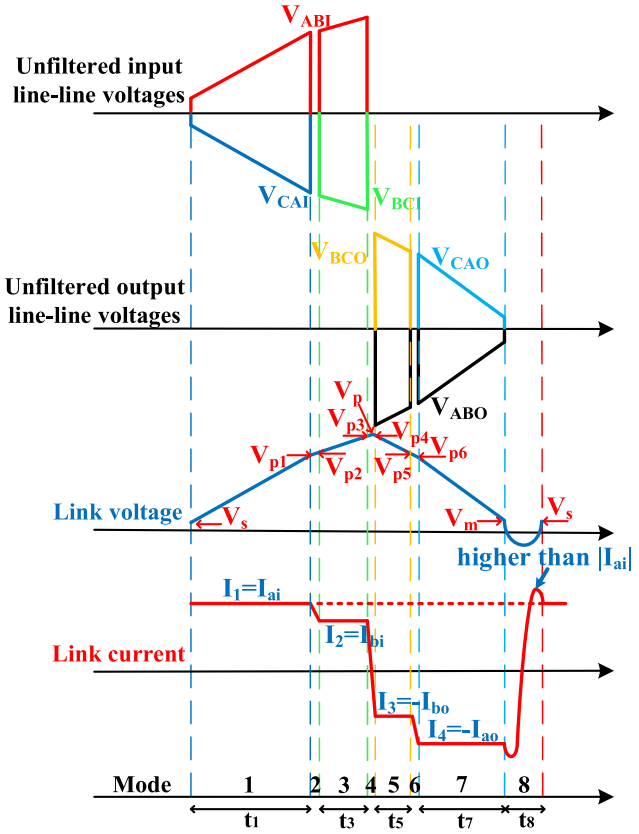

Fig. 6. Unfiltered line-to-line voltages at the input and output, link voltage, and link current in each mode.

Mode 7 (Discharging): During the second discharging mode, the highest output phase current (I_{ao}) discharges the link capacitor while forming the unfiltered second-highest output line-to-line voltage (V_{CAO}). Mode 7 will be terminated before the link capacitor is discharged to zero. At the end of this discharging mode, the energy in the link capacitor should be sufficient for the link current to swing from $-|I_{\mathrm{ao}}|$ to a positive value, which should be larger than $|I_{\mathrm{ai}}|$. Mode 7 is ended by turning on So1, Si5, and Si6 once the link voltage reaches a preset value V_{m}.

Mode 8 (Resonating): As the longest resonating mode, mode 8 can be divided into 2 stages, as shown in Fig. 8. In the first stage, the *LC* link is again shorted and forms a resonant tank to provide a zero current turn-OFF for the switches at both input side and output side, and zero voltage turn-ON for the output switches at the beginning of next cycle if the zone changes. The *LC* link continues to resonate until the polarity of the link current is reversed. When the antiparallel diodes of switches Si2, Si5, Si3, Si6, So1, and So4 get forward biased and starts to conduct, the second stage of mode 8 is initiated.

In the second stage of mode 8, the link current increases until it reaches a value higher than the input current of phase A. At this time, all the switches at the input side and switches So1 and So4 at the output side are turned off under ZCS. The link current continues increasing and reaches its peak value; then it decreases and reaches the input current value of phase A. Another link cycle will be started at this moment.

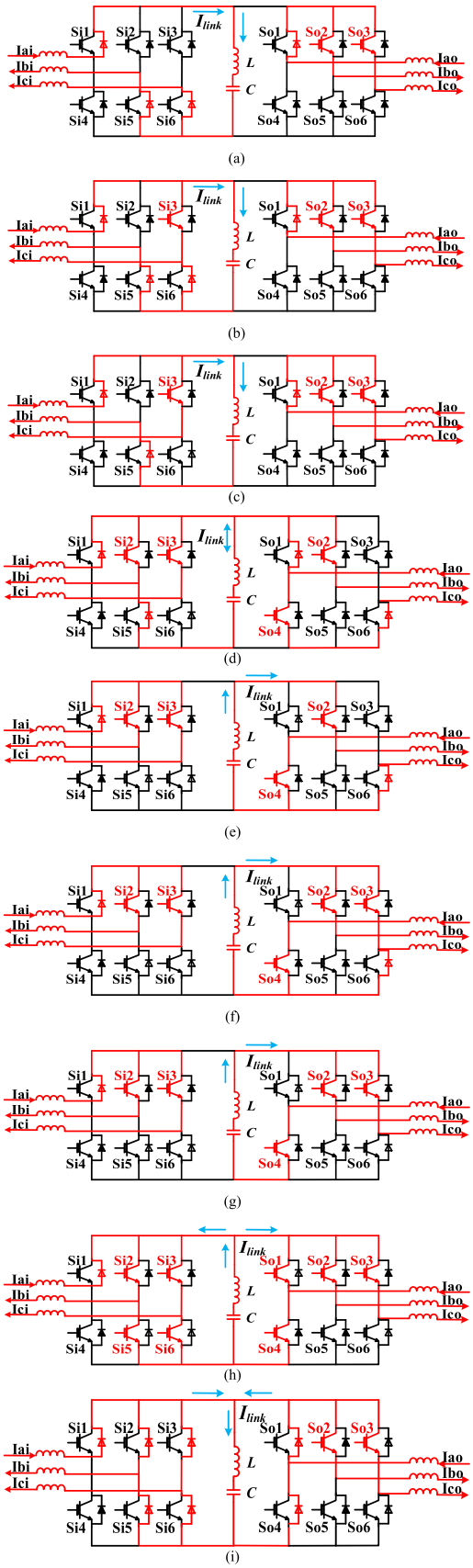

Fig. 7. Behavior of proposed three-phase AC–AC converter in different modes of operation. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8-1. (i) Mode 8-2.

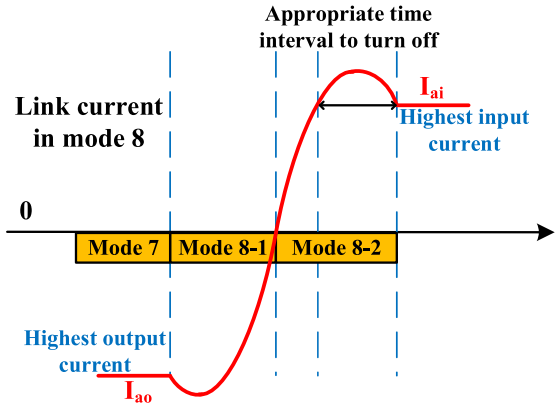

Fig. 8. Link current during mode 8.

III. Converter Control Scheme

A. Control Block Diagram

Both closed-loop and open-loop controls can be implemented for the proposed converter. This section explains the two control strategies of the proposed three-phase ac–ac converter with soft switching. As mentioned before, the switch selection is based on the operating zone for input and output sides that are independent. Figs. 9 and 10 present the flow chart of closed-loop control and open-loop control, respectively. The proposed parallel capacitive-link universal converter operates by building up the corresponding unfiltered input and output line-to-line voltages for each phase, and is indeed a voltage-controlled converter. To implement the control more effectively and accurately, the voltage references for the input and output should be determined first to ensure that the average values of the unfiltered voltages match their references.

Fig. 9 illustrates the procedure of closed-loop control strategy. Three voltage sensors measure the input source phase voltages ($V_{\rm ai}$, $V_{\rm bi}$, and $V_{\rm ci}$). The reference of the unfiltered input line-to-line voltages (V^*_{abi}, V^*_{bci}, V^*_{cai}) and the input phase current references (I^*_{ai}, I^*_{bi}, I^*_{ci}), which are typically preferred to be in phase with the input phase voltages, can be determined based on $V_{\rm ai}$, $V_{\rm bi}$, $V_{\rm ci}$, the rated power, the input filter inductance/capacitance and input frequency. The unfiltered output line-to-line reference voltages (V^*_{abo}, V^*_{bco}, V^*_{cao}) and the output phase current references (I^*_{ao}, I^*_{bo}, I^*_{co}) can also be determined according to the rated power, rated output voltage, the output filter value and output frequency. For the closed loop control, the unfiltered input line-to-line voltages ($V_{\rm ABI}$, $V_{\rm BCI}$, and $V_{\rm CAI}$) and unfiltered output line-to-line voltages ($V_{\rm ABO}$, $V_{\rm BCO}$, and $V_{\rm CAO}$) as well as the link voltage ($V_{\rm link}$) and the link current ($I_{\rm link}$) values are needed. As mentioned before, the reference line-to-line voltages can be regarded as constants in a switching cycle. In closed-loop control, the measured unfiltered voltages are averaged in one switching cycle and compared with their references to determine the start and/or termination of each mode. Although there are 8 modes in each switching cycle of the soft-switching configuration, ending resonant modes does not require any switching commands.

The corresponding switching pattern of the proposed parallel capacitive-link universal converter, which is determined according to the zones and modes, is exhibited in Table I. At the beginning of each cycle, the proper switches at the input and output sides are determined based on the voltage and current references. The input reference line-to-line voltages and currents will be sorted according to their absolute values as $V^*_{\rm Li1}$, $V^*_{\rm Li2}$, $V^*_{\rm Li3}$ ($|V^*_{\rm Li1}|>|V^*_{\rm Li2}|>|V^*_{\rm Li3}|$), representing absolute values of the highest, second-highest, and lowest reference input line–line voltages according to Fig. 4, and $I^*_{\rm i1}$, I^*_{i2}, I^*_{i3} ($|I^*_{\rm i1}|>|I^*_{i2}|>|I^*_{i3}|$), representing absolute values of the highest, second-highest, and lowest reference input phase current. The sorting is also done for the output. In this converter, the second-highest and the lowest input line-to-line voltages are built up in mode 1 and 3, respectively. Then, the maximum input line-to-line voltage will be built up during both modes. In the closed-loop control, mode 1 and mode 3 will be terminated when the average values $V_{{\rm Li}2,av}$ and $V_{{\rm Li}3,av}$ of the measured unfiltered input line-to-line voltages $V_{\rm Li2}$ and $V_{\rm Li3}$ reach their reference values, i.e., $|V_{{\rm Li}2,av}|>=|V^*_{{\rm Li}2,av}|$ and $|V_{{\rm Li}3,av}|>=|V^*_{{\rm Li}3,av}|$, where $V^*_{{\rm Li}2,av}$ and $V^*_{{\rm Li}3,av}$ are the average values of the second-highest, and lowest reference input line–line voltages during this specific switching cycle, and they can be considered equal to the instantaneous values of the corresponding references. These measured value and reference value pairs will be reset to zero for the next cycle when the corresponding mode ends. When each charging mode is ended, the corresponding input and output switches, which are listed in Table I, are turned ON or OFF. Once mode 3 is terminated, the link capacitor begins to discharge its energy to the output side and the link voltage decreases. In mode 5, the lowest output line-to-line voltage is built up. Once the absolute average of the lowest line-to-line voltage ($|V_{{\rm L}3o,av}|$) meets its reference ($|V^*_{{\rm L}3o,av}|$), mode 5 is ended, and these average values are set to 0. The last discharging mode will be ended once the link voltage reaches a preset value $V_{\rm m}$. The remaining energy in the link capacitor allows the link current to swing from $-|I^*_{\rm o1}|$ to a desired positive peak value, which should be larger than $|I^*_{\rm i1}|$.

The open-loop control can eliminate the need for sensors measuring the unfiltered input and output line-to-line voltages, link voltage, and the link current, which lowers the cost and increases power density. The process of open-loop control strategy is shown in Fig. 10. The open-loop control can directly calculate the time duration of each mode by the voltage and current references. As seen in Fig. 10, the operation time of each mode is compared with the reference values to determine when to end each mode. After the operation zones for the input and output are determined, reference duration of each mode can be calculated based on the line-to-line voltage references and the phase current references. The detailed calculation and design process are presented in Section III-B.

B. Design Consideration

To analyze and design the converter a soft-switching configuration is considered. The equations for the hard-switching

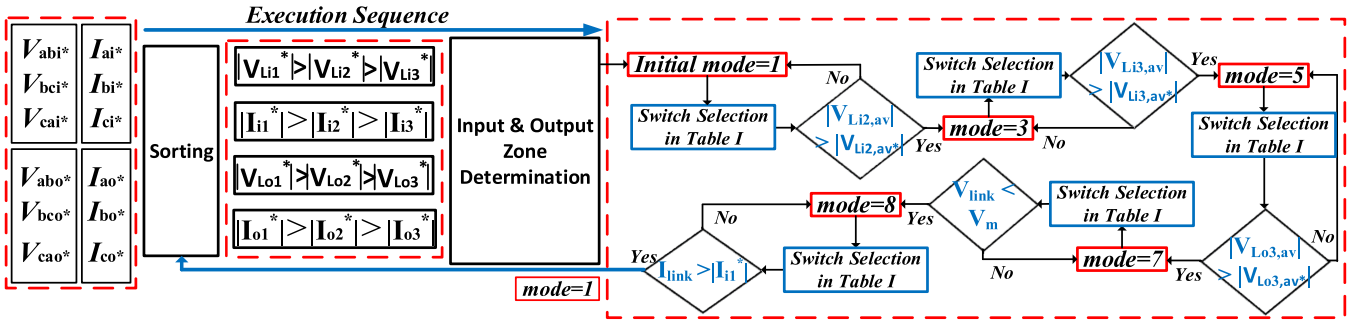

Fig. 9. Closed-loop control block diagram of the proposed converter.

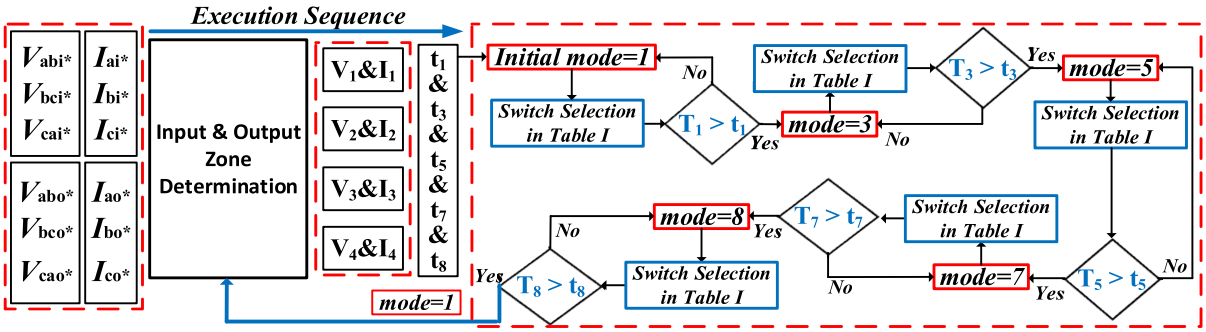

Fig. 10. Open-loop control block diagram of the proposed converter.

TABLE I
SWITCHING PATTERN OF THE PROPOSED THREE-PHASE AC–AC CONVERTER

Mode	Side	Zone 1	2	3	4	5	6	7	8	9	10	11	12
1	Input	-	-	-	-	-	-	-	-	-	-	-	-
	Output	So1 So3	So5 So6	So5 So6	So1 So2	So1 So2	So4 So6	So4 So6	So2 So3	So2 So3	So4 So5	So4 So5	So1 So3
3	Input	Si6	Si3	Si2	Si5	Si4	Si1	Si3	Si6	Si5	Si2	Si1	Si4
	Output	So1 So3	So5 So6	So5 So6	So1 So2	So1 So2	So4 So6	So4 So6	So2 So3	So2 So3	So4 So5	So4 So5	So1 So3
5	Input	Si4 Si6	Si2 Si3	Si2 Si3	Si4 Si5	Si4 Si5	Si1 Si3	Si1 Si3	Si5 Si6	Si5 Si6	Si1 Si2	Si1 Si2	Si4 Si6
	Output	So1 So5	So1 So5	So1 So6	So1 So6	So2 So6	So2 So6	So2 So4	So2 So4	So3 So4	So3 So4	So3 So5	So3 So5
7	Input	Si4 Si6	Si2 Si3	Si2 Si3	Si4 Si5	Si4 Si5	Si1 Si3	Si1 Si3	Si5 Si6	Si5 Si6	Si1 Si2	Si1 Si2	Si4 Si6
	Output	So1 So3 So5	So1 So5 So6	So1 So5 So6	So1 So2 So6	So1 So2 So6	So2 So4 So6	So2 So4 So6	So2 So3 So4	So2 So3 So4	So3 So4 So5	So3 So4 So5	So1 So3 So5
8	Input	Si1 Si3 Si4 Si6	Si2 Si3 Si5 Si6	Si2 Si3 Si5 Si6	Si1 Si2 Si4 Si5	Si1 Si2 Si4 Si5	Si1 Si3 Si4 Si6	Si1 Si3 Si4 Si6	Si2 Si3 Si5 Si6	Si2 Si3 Si5 Si6	Si1 Si2 Si4 Si5	Si1 Si2 Si4 Si5	Si1 Si3 Si4 Si6
	Output	So1 So2 So3 So5	So1 So4 So5 So6	So1 So4 So5 So6	So1 So2 So3 So6	So1 So2 So3 So6	So2 So4 So5 So6	So2 So4 So5 So6	So1 So2 So3 So4	So1 So2 So3 So4	So3 So4 So5 So6	So3 So4 So5 So6	So1 So2 So3 So5

converter can be derived in a similar way. Typically, the rated power and input and output voltages are given.

As shown in Fig. 6, the link voltage at the end of modes 1, 2, 3, 4, 5, and 6 is denoted by V_{p1}, V_{p2}, V_{p3}, V_{p4}, V_{p5}, and V_{p6}, respectively. As discussed in Section III-A, the averages of the unfiltered line-to-line voltages in one switching cycle should be equal to the corresponding references

$$V_1 = \frac{1}{2}\left(V_{p1} + V_s\right) t_1 f \tag{1}$$

$$V_2 = \frac{1}{2}\left(V_{p2} + V_{p3}\right) t_3 f \tag{2}$$

$$V_3 = \frac{1}{2}\left(V_{p4} + V_{p5}\right) t_5 f \tag{3}$$

$$V_4 = \frac{1}{2}\left(V_{p6} + V_m\right) t_7 f \tag{4}$$

where f is the switching frequency. V_1 and V_2 represent the instantaneous absolute values of the reference line-to-line voltages in mode 1 and mode 3, which are associated with the second-highest and the lowest input line-to-line voltages, respectively, as illustrated in Fig. 4. Similarly, V_3 and V_4 are the instantaneous absolute values of the reference line-to-line voltages in mode 5 and mode 7, which are associated with the lowest and the second-highest output line-to-line voltages, respectively. For example, if the converter operates in input zone 2 and output zone 8, $V_1 = |V^*_{cai}|$, $V_2 = |V^*_{bci}|$, $V_3 = |V^*_{bco}|$, $V_1 = |V^*_{cao}|$. $V_{\rm m}$ is the preset link voltage value when mode 7 is terminated, and $V_{\rm s}$ is the link voltage value when mode 8 ends. t_1–t_7 represent the time durations of modes 1–7. The relationship between the current charging or discharging the capacitor in modes 1, 3, 5, and 7 and the link voltage at the end of corresponding modes can be expressed as

$$I_1 = C\frac{V_{p1} - V_s}{t_1} \tag{5}$$

$$I_2 = C\frac{V_{p3} - V_{p2}}{t_3} \tag{6}$$

$$|I_3| = C\frac{V_{p4} - V_{p5}}{t_5} \tag{7}$$

$$|I_4| = C\frac{V_{p6} - V_m}{t_7} \tag{8}$$

where C is the link capacitance; I_1–I_4 represent the currents flowing through the link in modes 1, 3, 5, and 7, which are equal to the largest and second-largest input phase current, the second-largest and largest output phase current, respectively. For example, if the converter operates in input zone 2 and output zone 8, $I_1 = I_{\rm ai}$, $I_2 = I_{\rm bi}$, $I_3 = -I_{\rm bo}$, $I_4 = -I_{\rm ao}$, as shown in Fig. 6. The average power transferred in mode 1, 3, 5, and 7 can be obtained using (1)–(4) and (5)–(8). The energy transfer in soft switching is a bit different from hard switching due to the presence of link inductor. During mode 2, the energy is transferred from the link inductor to the capacitor due to resonance. In mode 6, the energy transfer direction is reversed. In mode 4, the energy transfer can be divided into 2 stages. During the first stage (mode 4-1), the energy of the link inductor is transferred to the link capacitor, and the link current reduces from I_2 to 0 and the link voltage reaches the maximum value $V_{\rm p}$; during the second stage (mode 4-2), the energy is transferred from the link capacitor to the link inductor, and the absolute value of link current increases from 0 to $|I_3|$ and the link voltage decreases from $V_{\rm p}$ to $V_{\rm p4}$. The average power transferred from source to load during modes 1, 3, 5, and 7 (P_1, P_3, P_5, P_7) and the power transfer between link inductor and capacitor during resonance modes (P_2, $P_{4\text{-}1}$, $P_{4\text{-}2}$, P_6, P_8) are as follows:

$$P_1 = V_1 \times I_1 = \frac{1}{2} Cf\left(V_{p1}^2 - V_s^2\right) \tag{9}$$

$$P_2 = \frac{1}{2}Lf(I_1^2 - I_2^2) = \frac{1}{2}Cf(V_{p2}^2 - {V_{p1}}^2) \tag{10}$$

$$P_3 = V_2 \times I_2 = \frac{1}{2}Cf(V_{p3}^2 - V_{p2}^2) \tag{11}$$

$$P_{(4-1)} = \left(\frac{1}{2}LI_2^2 - 0\right)f = \frac{1}{2}Cf(V_p^2 - V_{p3}^2\Big) \tag{12}$$

$$P_{(4-2)} = \left(\frac{1}{2}LI_3^2 - 0\right)f = \frac{1}{2}Cf(V_p^2 - {V_{p4}}^2\Big) \tag{13}$$

$$P_5 = V_3 \times I_3 = \frac{1}{2} Cf\left(V_{p4}^2 - V_{p5}^2\right) \tag{14}$$

$$P_6 = \frac{1}{2} Lf\left(I_4^2 - I_3^2\right) = \frac{1}{2} Cf\left(V_{p5}^2 - V_{p6}^2\right) \tag{15}$$

$$P_7 = V_4 \times I_4 = \frac{1}{2} Cf\left(V_{p6}^2 - V_m^2\right) \tag{16}$$

$$P_8 = \frac{1}{2} Lf\left(I_4^2 - I_1^2\right) = \frac{1}{2} Cf\left(V_s^2 - V_m^2\right). \tag{17}$$

Since the link capacitor is charged from the input source only in modes 1 and 3, and discharged to the output in modes 5 and 7, the total power transferred from the input or to the output in a switching cycle will be $P_{\rm rated} = P_{\rm in} = V_1 I_1 + V_2 I_2 = P_1 + P_3 = P_{\rm out} = V_3 I_3 + V_4 I_4 = P_5 + P_7$. By combining (9)–(12), the following equation can be obtained, it is the same for the output by using (13)–(16):

$$P_1 + P_2 + P_3 + P_{4-1} = P_{in} + P_2 + P_{4-1} = P_{in} + \frac{1}{2}Lf\, I_1^2 = \frac{1}{2} Cf\left(V_p^2 - V_s^2\right) \tag{18}$$

$$P_{4-2} + P_5 + P_6 + P_7 = P_{out} + P_{4-2} + P_6 = P_{out} + \frac{1}{2}Lf\, I_4^2 = \frac{1}{2} Cf\left(V_p^2 - V_m^2\right). \tag{19}$$

By combining (17), the rated power can be expressed as

$$P_{rated} = P_{in} = P_{out} = \frac{1}{2} CV_p^2 - \frac{1}{2}CV_m^2 - \frac{1}{2}Lf I_4^2. \tag{20}$$

Since $V_{\rm m}$ is much smaller than $V_{\rm p}$ and the link inductor is small, rated power can be estimated as $P_{\rm rated} = \frac{1}{2} CfV_p^2$. Thus, the link capacitance can be obtained through (20)

$$C = \frac{2P_{\rm rated}}{f \times V_p^2}. \tag{21}$$

If the resonance modes are neglected, the link peak voltage can be estimated as a function of the instantaneous values of the highest line-to-line input and output voltages ($V_{{\rm in}-ll}$ and $V_{{\rm out}-ll}$) [34]:

$$V_p = 2\left(V_{{\rm in}-ll} + V_{{\rm out}-ll}\right). \tag{22}$$

Since the values of $V_{{\rm in}-ll}$ and $V_{{\rm out}-ll}$ vary in a line cycle, which can be observed in Fig. 4, the link frequency also changes. However, the variation range is small. The design can be done

for the worst case when $V_{\text{in}-ll}$ and $V_{\text{out}-ll}$ have their maximum values, $V_{\text{in}-ll-\text{peak}}$ and $V_{\text{out}-ll-\text{peak}}$, and link frequency has its minimum value. The value of link capacitance can be determined by

$$C = \frac{P_{\text{rated}}}{2f(V_{\text{in}-ll-\text{peak}} + V_{\text{out}-ll-\text{peak}})^2}. \tag{23}$$

Since the resonating modes 2-4-6 are typically much shorter than other modes, they can be neglected in the analysis. The time duration of modes 1, 3, 5, and 7 can be obtained by (1)–(4) and (9)–(16)

$$t_1 = \frac{2V_1}{f\,(V_{p1} + V_s)} \tag{24}$$

where $V_{p1} = \sqrt{V_s^2 + \frac{2V_1 I_1}{Cf}}$

$$t_3 = \frac{2V_2}{f\,(V_{p2} + V_{p3})} \tag{25}$$

where $V_{p2} = \sqrt{V_s^2 + \frac{L(I_1^2 - I_2^2)}{C} + \frac{2V_1 I_1}{Cf}}$,
$V_{p3} = \sqrt{V_s^2 + \frac{L(I_1^2 - I_2^2)}{C} + \frac{2V_1 I_1 + 2V_2 I_2}{Cf}}$

$$t_5 = \frac{2V_3}{f\,(V_{p4} + V_{p5})} \tag{26}$$

where $V_{p4} = \sqrt{V_m^2 + \frac{L(I_4^2 - I_3^2)}{C} + \frac{2V_3 I_3 + 2V_4 I_4}{Cf}}$,
$V_{p5} = \sqrt{V_m^2 + \frac{L(I_4^2 - I_3^2)}{C} + \frac{2V_4 I_4}{Cf}}$

$$t_7 = \frac{2V_4}{f\,(V_{p6} + V_m)} \tag{27}$$

where $V_{p6} = \sqrt{V_m^2 + \frac{2V_4 I_4}{Cf}}$.

As mentioned previously, link inductor is typically small, and V_{m} and V_{s} are much smaller than V_{p}. Thus, $V_{p1} \approx V_{p2} = \sqrt{\frac{2V_1 I_1}{Cf}}$, $V_{p3} \approx V_p \approx V_{p4} = \sqrt{\frac{2V_3 I_3 + 2V_4 I_4}{Cf}} = \sqrt{\frac{2P_{\text{rated}}}{Cf}}$, $V_{p5} \approx V_{p6} = \sqrt{\frac{2V_4 I_4}{Cf}}$, and the time duration of modes 1, 3, 5, and 7 can be estimated as follows:

$$t_1 = \frac{2V_1}{f\left(\sqrt{\frac{2V_1 I_1}{Cf}} + V_s\right)} \tag{28}$$

$$t_3 = \frac{2V_2}{f\left(\sqrt{\frac{2V_1 I_1}{Cf}} + \sqrt{\frac{2P_{rated}}{Cf}}\right)} \tag{29}$$

$$t_5 = \frac{2V_3}{f\left(\sqrt{\frac{2P_{rated}}{Cf}} + \sqrt{\frac{2V_4 I_4}{Cf}}\right)} \tag{30}$$

$$t_7 = \frac{2V_4}{f\left(\sqrt{\frac{2V_4 I_4}{Cf}} + V_m\right)}. \tag{31}$$

The main requirement for V_{m}, which is the preset link voltage value when mode 7 is terminated, is to ensure that the energy in the link capacitor is sufficient for the link current to swing from $-|I_4|$ to I_{m}, which is a positive value larger than $|I_1|$. The link current reaches the peak value I_{m} during mode 8 when the voltage across the link capacitor is 0; thus, the energy balance in mode 8 can be expressed as

$$\frac{1}{2}CV_m^2 + \frac{1}{2}L\,I_4^2 = \frac{1}{2}LI_m^2. \tag{32}$$

The condition $I_{\text{m}} > I_1$ must be satisfied in (32) to assure zero current turn OFF of the switches. If the converter operates in input zone 2 and output zone 8, the minimum value for V_{m} can be determined by substituting I_4 with I_{ao} and I_{m} with an optional value slightly higher than I_{ai} in (32).

The link inductance in soft-switching configuration determines the duration of mode 8, which is the longest resonance mode and is usually confined to 10% of the switching cycle. The link inductance L can be determined by

$$\frac{3}{4} \times 2\pi\sqrt{LC} < 0.1\frac{1}{f}. \tag{33}$$

Thus, time duration of mode 8 can be obtained by

$$t_8 = \sqrt{LC}\left[2\pi - \arcsin\left(\frac{I_1}{I_m}\right) - \arcsin\left(\frac{I_4}{I_m}\right)\right]. \tag{34}$$

TABLE II
SYSTEM PARAMETERS FOR SIMULATION AND EXPERIMENT

Parameters		Value
Nominal Power		1 kW
Link Frequency		26~28.5 kHz
Link Capacitance		150 nF
Link Inductance		3.3 μH
Input L-L Voltage		150 V, 60 Hz
Output L-L Voltage		100 V, 120 Hz
Input L Filter		5 mH
Output LC Filter	**L**	2 mH
	C	3.3 μF

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

To validate the operation of the proposed converter, the simulation results corresponding to the proposed parallel capacitive-link three phase ac-to-ac configuration, as well as the simulation results of a series capacitive-link three phase ac-to-ac configuration are presented in this part and compared. Both converters are designed for a 1-kW system and are simulated in PSIM under the same conditions. The system parameters are listed in Table II. To reach a minimum switching frequency of 27 kHz at 1-kW, a 150 nF film capacitor is used at the link of the proposed converter. For a conventional back-to-back dc-link converter with the same system parameters, the minimum value of the link capacitance is 50 μF.

Fig. 11 indicates the switching frequency and duration of modes 1, 3, 5, 7, and 8 in a full 60 Hz cycle. The result shows the switching frequency varies in a narrow range between 26 kHz and 28.5 kHz. As can be seen from Fig. 11, time duration of mode

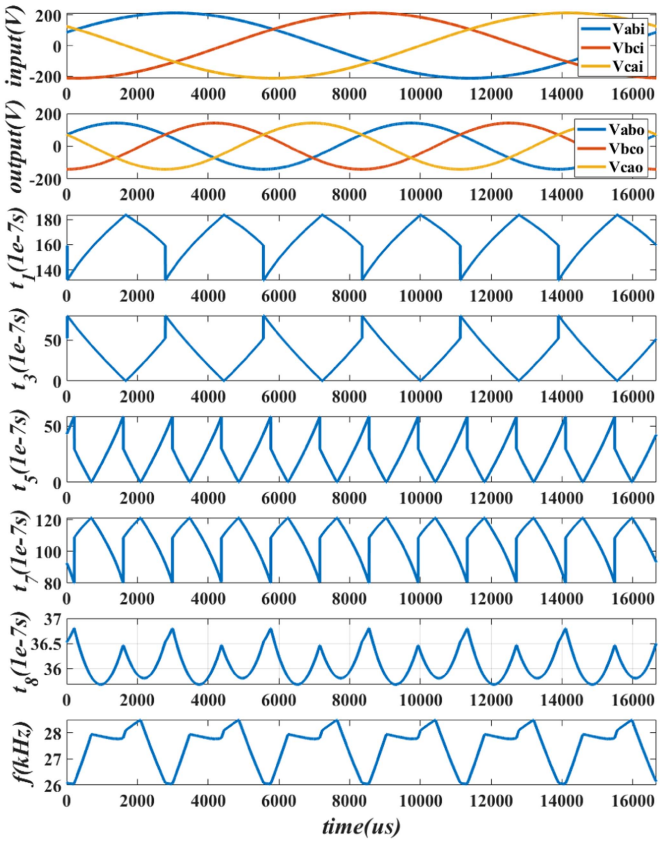

Fig. 11. Switching frequency and durations of modes 1, 3, 5, 7, and 8.

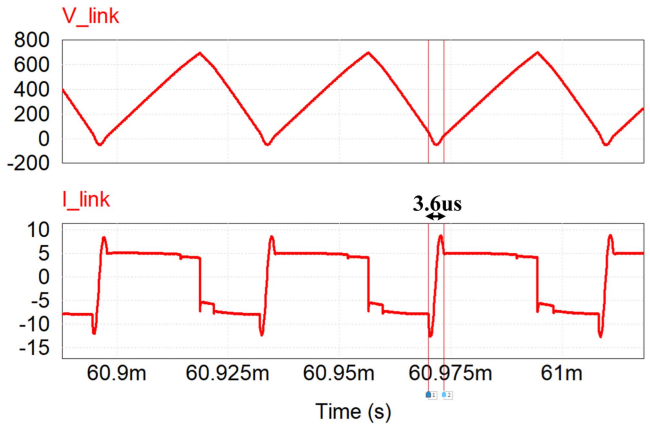

Fig. 12. Link voltage and link current of the proposed parallel capacitive-link converter.

8 is much smaller than the charging and discharging modes, and it is varying in a small range.

Fig. 12 illustrates the link voltage and link current of the proposed parallel capacitive-link converter. The link current is positive during modes 1 and 3, and during mode 4 the flowing direction is reversed. At this instant, the link voltage reaches its peak value, which is about 710 V, and this value is very close to the calculated link peak voltage 707 V based on (22). As shown

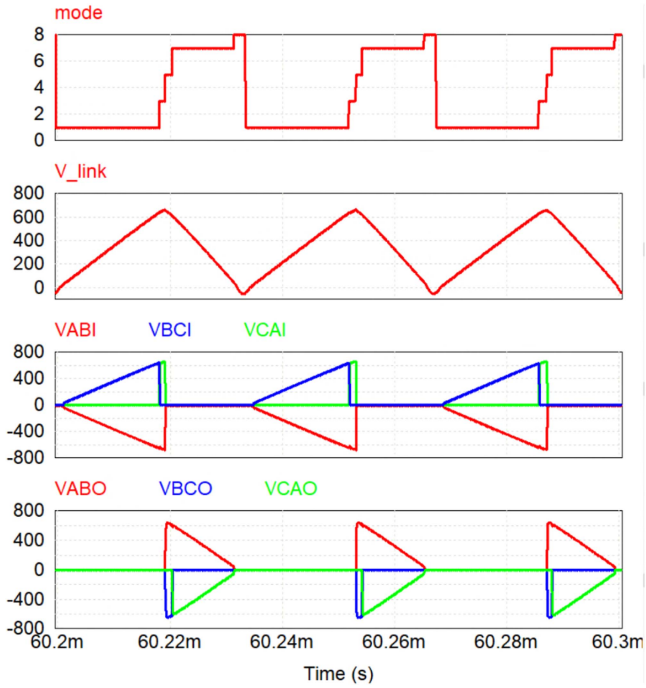

Fig. 13. Link voltage and unfiltered input and output line-to-line voltages in the proposed parallel capacitive-link converter.

in Fig. 12, the time duration of mode 8 is about 3.6 μs, which coincides with the calculated value shown in Fig. 11.

Fig. 13 presents the unfiltered input and output line-to-line voltages for the period that phase pairs ABI and ABO have the maximum absolute value of input and output line-to-line voltages. As is evident in this figure, the second-highest input line-to-line voltage V_{BCI} and the lowest input line-to-line voltage V_{CAI} are built up in modes 1 and 3, respectively. The lowest line-to-line output voltage V_{BCO} and the second-highest output line-to-line voltage V_{CAO} are built up in modes 5 and 7, respectively. It can be noted that the peak value of the line-to-line voltages is the same as the link peak voltage. Thus, the link peak voltage determines the voltage stress of the switches.

Figs. 14 and 15 depict the input current, output current as well as the current of input switch Si6 for series capacitive-link and parallel capacitive-link converters, respectively. The frequency of input current is 60 Hz, the frequency of output current is 120 Hz. It is evident that the proposed converter can realized both the voltage and frequency conversion. As seen in Figs. 14 and 15, the rms current of switch Si6 is about 4.39 A in series capacitive-link converter, which is about 4 times higher than that of the parallel capacitive-link converter (1.14 A). Figs. 14(b) and 15(b) demonstrate that the large current passes through Si6 mainly during modes 5 and 7. The simulation results verify a significant reduction in the rms currents of the switches in the proposed converter, which implies the conduction losses will be lower and the efficiency will be improved.

For a more detailed overall efficiency comparison, the power loss breakdown analyses of the two converters, which are obtained through simulations employing an accurate switch model

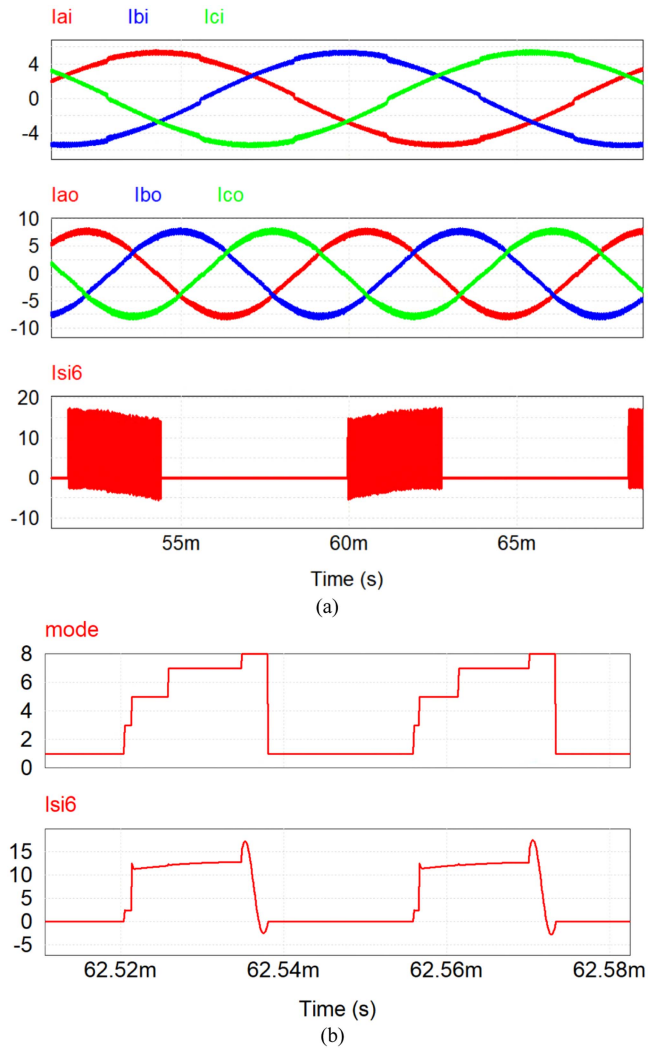

Fig. 14. Simulation results of series capacitive-link converter. (a) Input current, output current and current of switch Si6 in an input line cycle. (b) Current of switch Si6 during each mode.

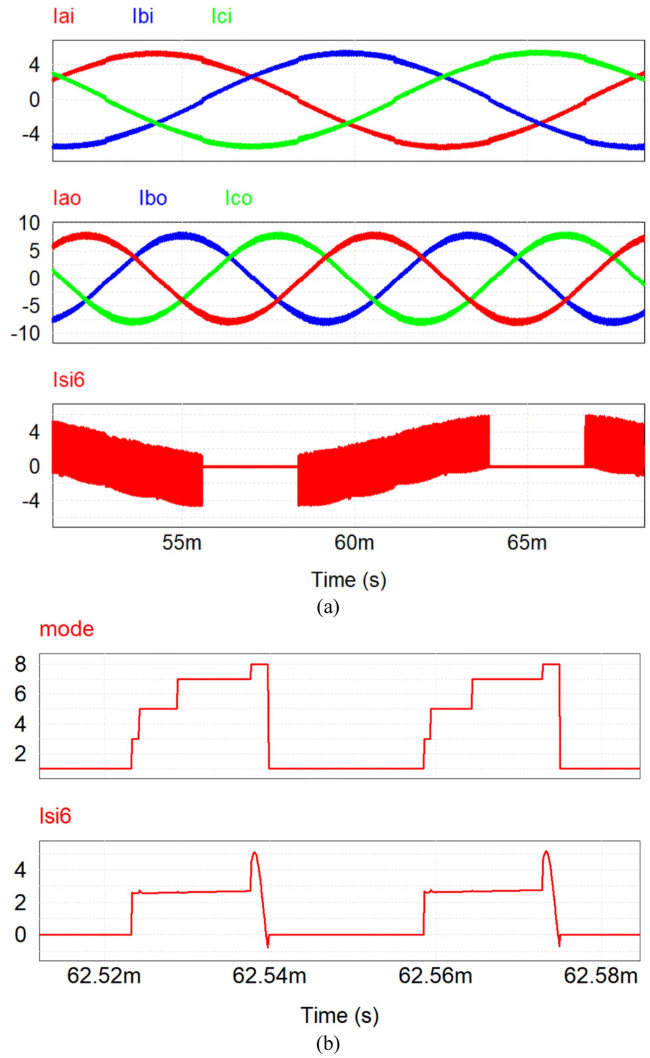

Fig. 15. Simulation results of parallel capacitive-link converter. (a) Input current, output current, and current of switch Si6 in an input line cycle. (b) Current of switch Si6 during each mode.

(level 2) within the PSIM software, are presented in Fig. 16. The results show that in the series capacitive-link converter, conduction losses make up the majority of the total losses, accounting for approximately 81% of total losses. Switching losses account for about 13% of the total losses, while the snubbers, designed according to [41], contribute only a small portion to the total losses. Compared to the series capacitive-link converter, the conduction losses of the parallel capacitive-link converter are reduced by approximately 33%, due to a lower current.

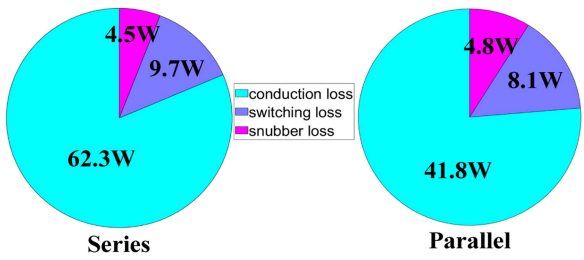

Fig. 16. Power loss breakdown comparison between the parallel and series capacitive-link universal converter.

B. Experimental Results

To further evaluate the performance of the proposed converter, a SiC-based prototype, the switching frequency of which varies between 26.5 kHz and 29.7 kHz, is fabricated, as displayed in Fig. 17. The prototype is composed of a power board and a control board. A Zync-7000 all programmable SoC core has been used to control the converter. The parameters of the prototype tested with open-loop control are listed in Table II.

The input and output phase currents of the proposed parallel capacitive-link converter are displayed in Fig. 18. Since the phase angle of the three-phase ac source at the start-up point is unknown, two sensors are placed at the input side to measure the

TABLE III
COMPARISON OF THE THREE-PHASE AC–AC TOPOLOGIES

	Proposed parallel capacitive-link	Series capacitive-link	Series inductive-link [24]	Ref. [37]	Ref. [23]	Ref. [42]	Ref. [43]	Dc-link back-to-back converter
Power rating	1 kW	1 kW	1.5 kW	1 kW	50 kW	1 kW	6 kW	-
Number of active switches/diodes	12/0	12/0	12/12 14/14	12/0	14/12	6/6	12/0	12/0
Number of energy transferring elements	1	1	1	1	1	3	1	1
Voltage step up/down capability	Yes	Yes	Yes	Yes	Yes	Yes	Limited	Limited
Frequency control capability	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Switch quadrant	2	2	2	2	2	2	2	2
Number of dc caps	0	0	0	0	0	0	1	1
Soft-switching feature	Full range	Full range	Full range	No	Full range	No	No	No
Efficiency	93.29%	91.21%	BB[1]: 90.15% BU[2]: 92.23%	90.5%	97.4%	92.5%	93.75%	-

[1]BB: Buck-boost. [2]BU: Buck.

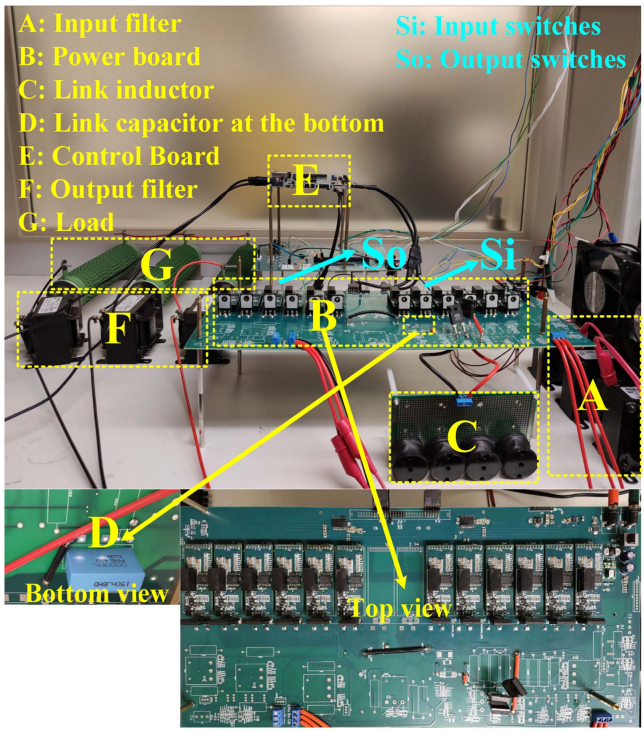

Fig. 17. Annotated photograph of the proposed converter prototype.

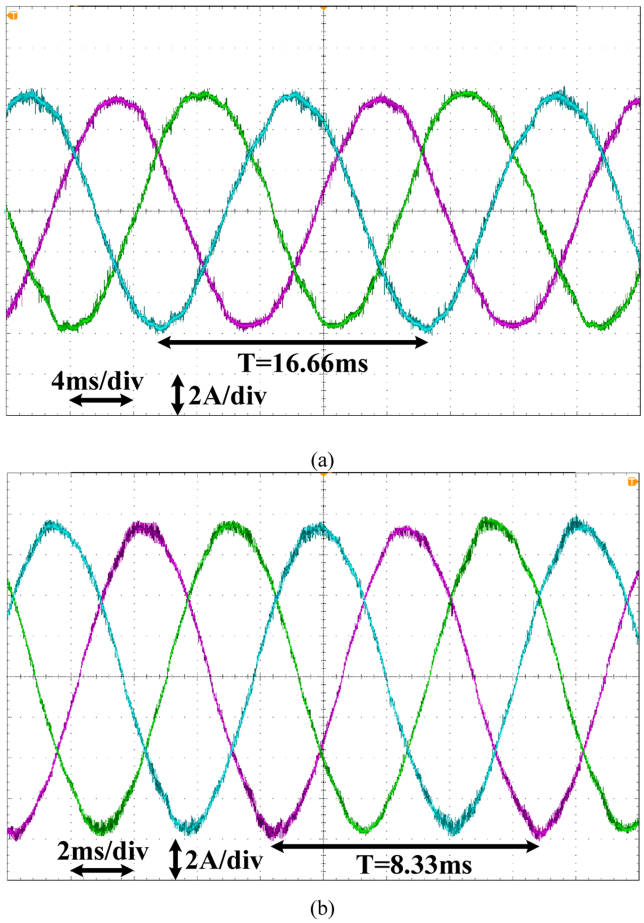

Fig. 18. Phase currents of the proposed parallel capacitive-link converter. (a) Input phase currents with frequency of 60 Hz. (b) Output phase currents with frequency of 120 Hz.

voltages of two phases of the ac source and detect the amplitude and phase angle of the input phase voltages V_{ai} and V_{bi}, and parameters of the third input phase voltage V_{ci} can be determined assuming the source is a balanced three-phase system. Then, the reference for the unfiltered input line-to-line voltages and the input phase current references can be calculated, as mentioned in Section III.

Fig. 19 represents the link voltage and link current of the proposed parallel capacitive-link converter. The link voltage reaches the peak value of 710 V, which is almost the same as the simulation result and the calculated value. Additionally, a fluke infrared thermometer gun is used to test the temperature of the link capacitor when the converter is operating, and the result shows the temperature of the link capacitor is almost the same as room temperature.

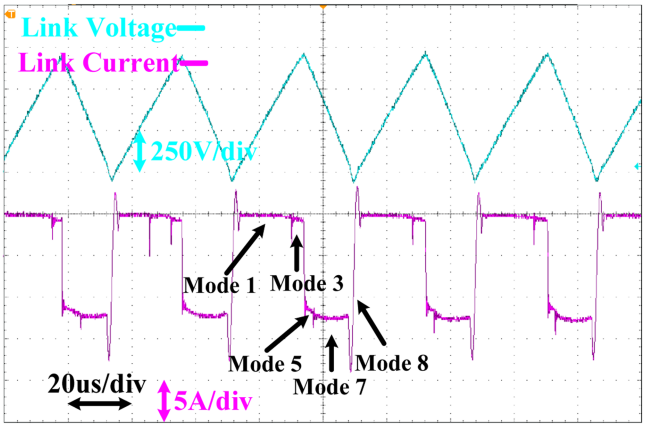

Fig. 19. Experiment result of the link voltage and link current in the proposed parallel capacitive-link converter.

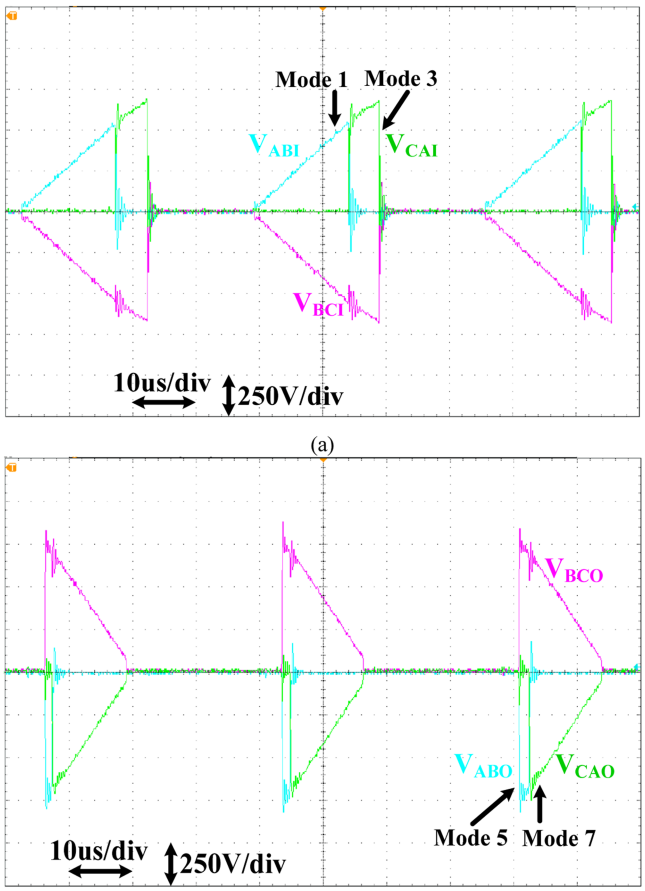

Fig. 20. Experiment results of the unfiltered line-to-line voltages. (a) Input unfiltered line–line voltages. (b) Output unfiltered line–line voltages.

Fig. 20(a) and (b) exhibits the unfiltered line–line input and output voltages in the proposed parallel capacitive-link converter, respectively. Some oscillations, which is caused by the resonance of the link inductor and the parasitic capacitance of switches/diodes, can be observed during the short transition between two active modes.

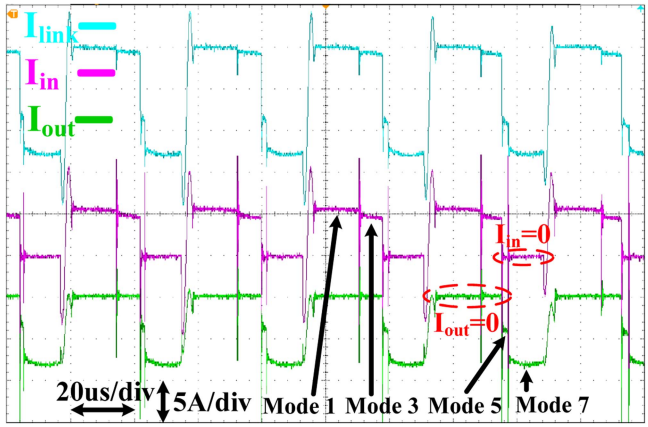

Fig. 21. Experiment results of $I_{\rm link}$, $I_{\rm in}$, and $I_{\rm out}$.

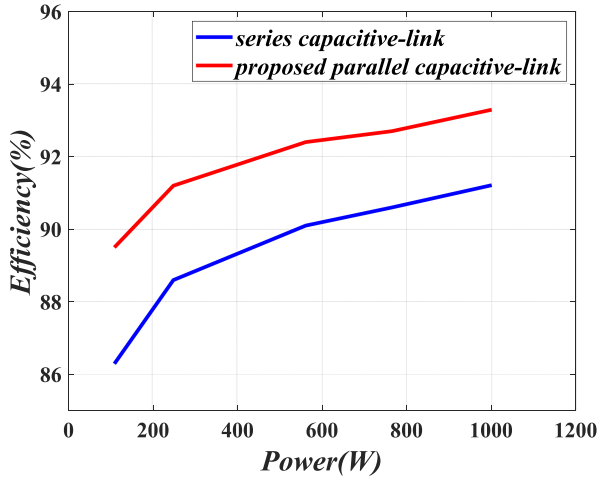

Fig. 22. Measured efficiencies of the proposed parallel capacitive-link converter and series capacitive-link converter.

Fig. 21 shows $I_{\rm link}$, $I_{\rm in}$, and $I_{\rm out}$. As specified in Fig. 2, $I_{\rm in}$ and $I_{\rm out}$ represent the currents flowing from the input side and output side to the link, respectively. In the charging modes $I_{\rm in} = I_{\rm link}$, and $I_{\rm out} = 0$, and in the discharging modes $I_{\rm out} = I_{\rm link}$, and $I_{\rm in} = 0$. The spikes on $I_{\rm in}$ and $I_{\rm out}$ are caused by the parasitic inductance of wires (as shown in Fig. 17) added for measuring these currents. The waveforms verify that the flowing path of the input and output currents are separated in the proposed parallel capacitive-link converters. Thus, the current stress on the switches/diodes are reduced compared with the series capacitive-link converter.

Fig. 22 compares the efficiency of the proposed parallel capacitive-link converter and series capacitive-link converter under the same operating condition at different power levels. The efficiency of the proposed converter can reach 93.29% at 1 kW, which is about 2% higher than the series capacitive-link converter. As the power level increases, the efficiency will be further improved. According to the simulation results, the efficiency of the proposed parallel capacitive-link converter tends to approach 97% at 10 kW.

The proposed parallel capacitive-link ac–ac converter and several existing three-phase ac–ac converter topologies are compared in Table III. As seen in this table, the proposed parallel capacitive-link converter has a high efficiency and provides a simple topology requiring only 12 two-quadrant switches.

V. Conclusion

Series capacitive-link universal converters can provide high reliability and power density. However, the current stress of the switches in this converter is relatively high. In this article, an innovative class of parallel capacitive-link converters that addresses this limitation is introduced and analyzed. The high frequency ac-link enables utilizing a small film capacitor in parallel with the input and output switch bridges as the energy elements to transfer the power from input towards output. Unlike PWM dc-link ac–ac converter, a very small film capacitor is used in the proposed converter and the need for large and unreliable electrolytic capacitors is eliminated. Besides, ZCS for all the switches can be realized by adding a small inductor in series with the link capacitor. These features notably increase the power density and reliability while reducing the cost. The advantages and promising characteristics of the proposed converter are validated through simulations and experiments. The results demonstrate that the proposed converter has a significantly lower current stress on input switches and output diodes compared to series capacitive-link universal converter; thus, improving the overall efficiency.

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Junhao Luo (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Wuhan University, Wuhan, China, in 2015 and 2018, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA.

His research interests include power electronics, design, and digital control of power converters.

Khalegh Mozaffari (Senior Member, IEEE) received the B.S. degree (first-class hons.) from Islamic Azad University, Kazerun, Iran, in 2007, the M.S. degree (first-class hons.) from University of Tabriz, Tabriz, Iran, in 2011, and the Ph.D. degree from Northeastern University, Boston, MA, USA, in 2019, all in electrical engineering.

He is currently a Staff Power Electronics Engineer with Enphase Energy Inc., Austin, TX, USA.

Brad Lehman (Fellow, IEEE) received the B.E.E. degree from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 1987, the M.S.E.E. degree from the University of Illinois at Champaign-Urbana, IL, USA, in 1988, and the Ph.D. degree in electrical engineering from Georgia Tech in 1992.

He was listed in the inaugural edition of the book *The 300 Best Professors* (Princeton Review, Framingham, MA, USA, 2012). He is currently a Professor with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA. His research interests include power electronics and renewable energy, with emphasis on the modeling, design, and control of high-density converters.

Dr. Lehman is a President of the IEEE Power Electronics Society (PELS, 2023/2024). He previously was the Editor-in-Chief of IEEE TRANSACTIONS ON POWER ELECTRONICS from 2013–2018. He has been the recipient of the 2015 IEEE (PELS) Modeling and Control Technical Achievement Award, a 2016 IEEE Standards Medallion, the 2018 IEEE Award for Achievement in Power Electronics Standards, and the 2019 IEEE PELS Harry A. Owen, Jr. Distinguished Service Award. Prior to his career as a Professor, he was the Head Coach of the varsity Georgia Tech swimming and diving team.

Mahshid Amirabadi (Senior Member, IEEE) received the B.S. degree from Shahid Beheshti University, Tehran, Iran, in 2002, the M.S. degree from the University of Tehran, Tehran, Iran, in 2006, and the Ph.D. degree from Texas A&M University, College Station, TX, USA, in 2013, all in electrical engineering.

She was the University of Illinois at Chicago, Chicago, IL, USA, in 2013, as an Assistant Professor. Since 2015, she has been with Northeastern University, Boston, MA, USA, where she is currently an Associate Professor. Her main research interests and experience include universal power converters, renewable energy systems, variable speed drives, and wireless power transfer systems.

Dr. Amirabadi was the recipient of the National Science Foundation CAREER Award in 2021. She is currently an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS and is a Member-at-Large for the IEEE Power Electronics Society Administrative Committee.