Modified Single-Edge Modulation to Decrease Common-Mode Voltage With Considering Deadtime Effects and Switching Losses for Three-Phase VSIs

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***Abstract*—As the switching frequency of power semiconductor devices increases, it is necessary to suppress the common-mode voltage (CMV) generated by the pulsewidth modulation action of the voltage-source inverters, which can produce serious electromagnetic interference (EMI) and hazards, such as motor axial current. This article proposes a modified modulation technique based on the single-edge carrier form to decrease the amplitude and frequency of CMV by selecting different combinations of active voltage vectors in different voltage vector sectors. On this basis, the method of optimizing the sequence of voltage vector action is adopted to reduce the switching losses of the inverter and designing a reasonable carrier frequency variation function based on the mathematical derivation, considering the phase angle of output current and distribution characteristics in the time domain of switching frequency, which is combined with the above-modified modulation strategy to further restrain the switching losses and differential-mode conducted EMI. Moreover, a deadtime effect correction methodology for estimating the phase current at the moment of switching action is introduced to eliminate the CMV spikes during the deadtime interval. Finally, the experimental platform is built to validate the effectiveness and practicality of the modified single-edge modulation technique.**

***Index Terms*—Common-mode voltage (CMV), deadtime effect correction, single-edge modulation, switching losses, voltage-source inverter (VSI).**

I. INTRODUCTION

IN RECENT years, three-phase two-level voltage-source inverters (VSIs) have been widely used in the fields of various motor drives, photovoltaic grid-connected power generation, and power transmission due to the advantages of high efficiency, flexibility, and ease of implementation [1], [2]. With the development of power semiconductor device performance, process technology, physical characteristics, and package form, the switching frequency of VSIs has been improved greatly, achieving better hardware performance of motor drive so that better control quality can be implemented. Increasing the switching frequency of the VSIs can significantly improve the system control bandwidth to provide high dynamic response and high steady-state accuracy for servo control and ultraprecision positioning platforms. However, it also introduces lots of high-frequency switching noise and switching losses, which will lead to severe conducted electromagnetic interference (EMI) and efficiency degradation of the whole system [3]. One of the major noise sources is the common-mode voltage (CMV) generated by the pulsewidth modulation (PWM) technique of the VSIs. It can couple with parasitic circuits of the motor-drive system to generate motor axial current, which can cause motor bearing damage and isolation breakdown [4], [5].

Many researchers have attempted to reduce the CMV generation of VSIs nowadays. Current studies are divided into two main perspectives to achieve suppression. The first one is to suppress it from the hardware topology, which is also further classified into two subcategories. The first subclass is changing the topological form of the inverters to suppress or even eliminate the CMV at the origin source [6], [7], [8], [9], [10], [11], [12]. A circuit improvement of adding bridge arms is proposed in [6], which took the form of expanding an odd number of bridge arms into an even number to eradicate CMV. Impedance-source inverters are an efficient way that they can operate in non-shoot-through and shoot-through conditions; hence, both switches of the same bridge arm can be conducted simultaneously [7], [8]. For achieving common-mode current (CMC) elimination, one power switch is added to every bridge arm and the stator windings are equivalently divided into two symmetrical groups through a synchronous switching strategy [9]. In voltage space vector modulation, the zero vectors produce the largest magnitude of CMV. Therefore, separating the bus voltage end and the inverter during the period of zero vector action is also an efficient way [10], [11]. An improved topology adopts four insulated gate bipolar transistors (IGBTs) with common-gate–common-emitter configuration to connect the middle point of the bus voltage and the bridge arm to remove the impact of zero vectors [12]. However, all of these approaches above require the use of

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extra active power devices and passive components. This results in production cost increment and complexity of the control and reduces the reliability of the whole device.

The second subcategory of modifying hardware circuits is applying common-mode EMI filters [13], [14], [15], [16]. This cancels the CMV from the propagation path, not the origin source. In the design of EMI filters, common-mode noise detection and compensation can all be divided into voltage way and current way. Among these methods, voltage detection and current compensation do not require the use of additional isolation transformers, but the other methods do. Equal amplitude cancelation of CMC is carried out by introducing common-mode impedance equivalent circuits and push–pull amplification network circuits, thereby preventing interference with other parts of the system [13], [14]. The filtering method in which the midpoint of a three-phase sinusoidal output filter is used as a CMV detection point and coupled to the conduction path using a transformer is called voltage detection and voltage compensation, as shown in [15]. But all these approaches require the introduction of additional active devices, such as op-amps and transistors. The operating bandwidth of these devices limits the actual effectiveness of the filter. And the CMV is still present in the system, it has just shifted or canceled out.

All the above strategies are based on hardware topology modification to achieve CMV reduction from the origin source or conduction path. The second major perspective is based on software approaches, which are called reduced common-mode voltage pulsewidth modulation (RCMVPWM). It is well known that the CMV is generated from the high-frequency PWM action of the inverters, so in contrast, the CMV can be solved from the source by improvement of the modulation technique [17], [18], [19], [20], [21], [22]. Since the number of the three-phase two-level VSIs bridge arms is odd, it is naturally impossible to completely eliminate the CMV for three-phase two-level VSI without changing the hardware topology. It cannot be eliminated but decreased. On the basis of traditional space vector pulsewidth modulation (SVPWM), the use of two active voltage vectors with opposite phases as zero vectors in SVPWM to participate in the modulation process can achieve the reduction of the amplitude of the CMV [19], [20]. The same effect can be achieved by taking three adjacent active voltage vectors and three separated ones to synthesize the reference voltage vector without using zero vectors [21], [22]. However, the CMV amplitude abrupt change still exists several times in a carrier period in [19], [21], and [22], so this type of method only reduces the amplitude and ignores the frequency. Taking both into account, the article [22] can remain a constant CMV output over the entire operational period, but the voltage linear modulation region is narrow. This limits its widespread use in high-power scenarios.

Therefore, on the basis of these modulation strategies based on the double-edge center-symmetrical carrier form, this article proposes a modified modulation method based on the single-edge carrier, taking into full consideration of the amplitude and frequency of the CMV generated by inverters, as well as output voltage linear modulation region and switching losses of the power devices. At the same time, the influence of the inverter deadtime effect on the proposed modified modulation is analyzed, and a method based on load characteristics combined with current estimation is recommended to realize the deadtime effect compensation (DEC). Finally, to further reduce the conducted EMI peaks and switching losses of the drive system, a reasonable carrier frequency variation function considering the phase angle of output current and distribution characteristics in the time domain of switching frequency is designed based on the detailed mathematical derivation.

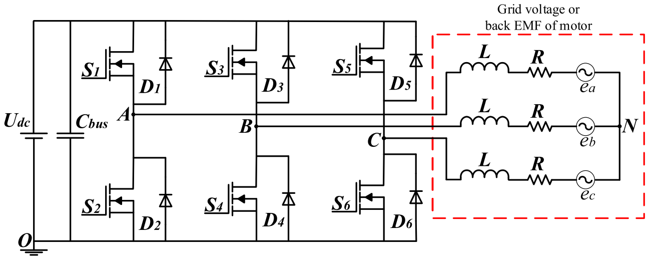


Fig. 1. Topology of general three-phase two-level VSI system.

The rest of this article is organized as follows. The traditional voltage space vector modulations will be presented in Section II to compare with the modified one. Section III will discuss the proposed modified single-edge modulation (MSEM) strategy, which contains the single-edge modulation design guidelines, DEC method, carrier frequency variation function derivation, and overall digital control system implementation block diagrams. Experiments comparing the various performance metrics of the former and novel methodologies will be shown in Section IV. Finally, Section V concludes this article.

II. REVIEW OF THE TRADITIONAL SVPWM AND RCMVPWM

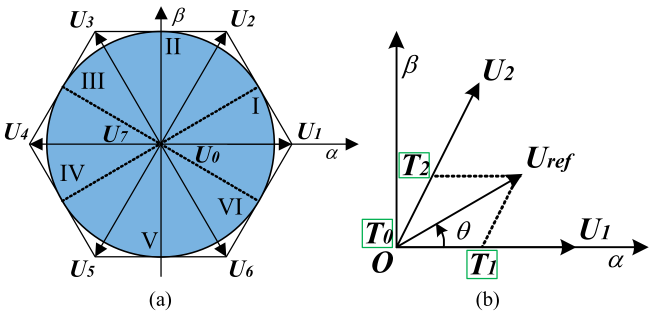
A. Traditional SVPWM

For a conventional three-phase two-level VSI system, the topological form is shown in Fig. 1. In this topology, the general expression for the CMV of the VSI is given as follows:

$$U_{\mathrm{CM}} = U_{NO} = \frac{1}{3}\left(U_{AO} + U_{BO} + U_{CO}\right) \quad (1)$$

where U_{CM} represents the CMV of the VSI system, and U_{iO} $(i = A, B, C, N)$ indicates the voltage between points i and O in Fig. 1.

The strategy SVPWM divides the voltage space vector into six sectors (I–VI). And two zero-voltage vectors (U_0 and U_7) and six active voltage vectors (U_1–U_6) are used to synthesize the reference voltage vector (U_{ref}). Fig. 2 shows the SVPWM voltage space vector distribution and vector synthesis when the U_{ref} is in Sector I, where T_1 and T_2 represent the action time of the corresponding voltage vectors, respectively. The three-phase switching state of the voltage vector at Sector I as well as phase-A voltage and CMV are displayed in Fig. 3. From the figure, it can be seen that the PWM phase voltage based on double-edge carrier form of SVPWM is centrosymmetric and the CMV jumps six times in one carrier cycle with a peak–peak value of U_{dc}. This is the common-mode noise source, which leads to severe EMI phenomena and problems, such as bearing breakage and



(a) (b)

Fig. 2. Voltage space vector distribution and synthesis of SVPWM. (a) Vector distribution. (b) Vector synthesis.

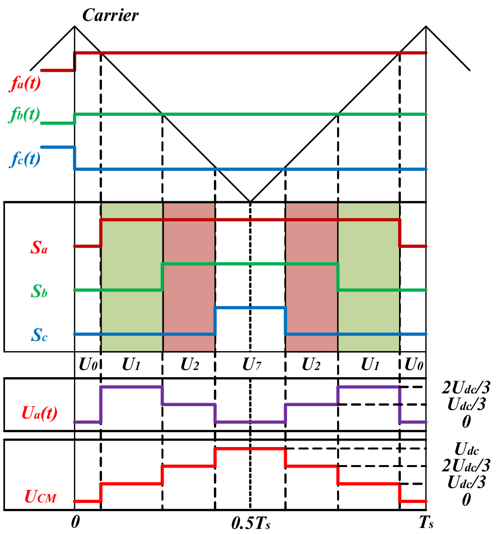


Fig. 3. Switching state, phase-A voltage, and CMV of SVPWM in Sector I.

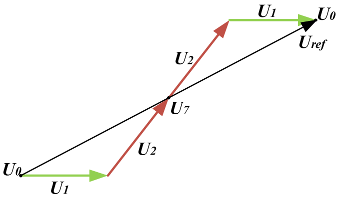
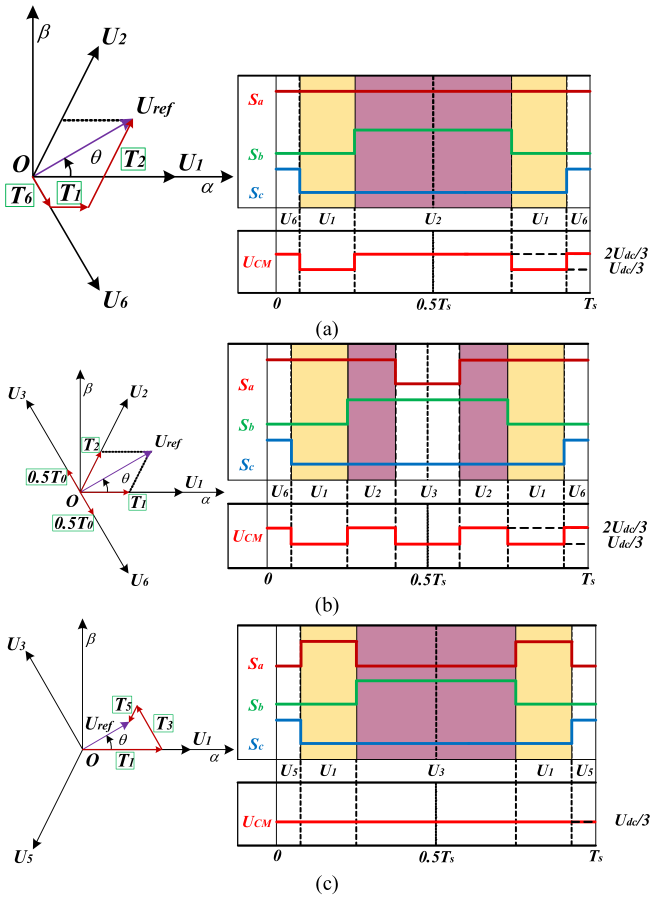


Fig. 4. Voltage vector synthesis sequence of SVPWM in Sector I.

isolation breakdown. Fig. 4 represents its corresponding voltage vector synthesis sequence. To facilitate the subsequent analysis of the CMV metrics with various modulation technologies, the variables are defined as follows.

1) Δp refers to the peak–peak value of the CMV with U_{dc} as the reference voltage.
2) Δs presents the step amplitude of the CMV with U_{dc} as the reference voltage.
3) N_L refers to the number of different levels of the CMV within a carrier cycle.
4) N_{L0} indicates the number of different levels of the CMV within a fundamental cycle.



(a) (b) (c)

Fig. 5. Vector synthesis mode, switching state, and CMV in Sector I of RCMVPWM. (a) NSPWM. (b) AZSPWM. (c) RSPWM.

5) N_T refers to the number of CMV transitions within a carrier period.
6) N_{T0} denotes the number of CMV transitions within a fundamental period.
7) A_L refers to the voltage vector amplitude in the linear modulation region with U_{dc} as the reference voltage.

Therefore, for SVPWM, the CMV metrics are described as

$$\begin{cases} \Delta p = 1, \Delta s = \frac{1}{3}, \ N_L = 4 \\ N_{L0} = 4, \ N_T = 6, \ N_{T0} = \frac{6f_c}{f_0}, A_L \in \left[0, 1/\sqrt{3}\right] \end{cases} \tag{2}$$

where f_c represents the switching frequency of VSI system, and f_0 denotes the fundamental frequency of the output phase voltage.

B. Reduced Common-Mode Voltage Pulsewidth Modulation

Several conventional RCMVPWM methods, which include near-state pulsewidth modulation (NSPWM), active zero-state pulsewidth modulation (AZSPWM), and remote-state pulsewidth modulation (RSPWM), are shown in Fig. 5. The figures all assume that the reference voltage vector U_{ref} is at Sector I. Based on the variables defined in Section II-A, the CMV metrics for these RCMVPWM methods can be summarized in Table I .

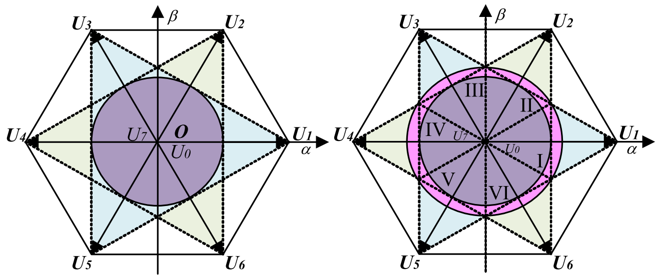
TABLE I
CMV METRICS OF RCMVPWM

	NSPWM	AZSPWM	RSPWM
Δp	1/3	1/3	0
Δs	1/3	1/3	0
N_L	2	2	1
N_{L0}	2	2	1
N_T	4	6	0
N_{T0}	$4\,f_c/f_0$	$6\,f_c/f_0$	0
A_L	$[2\sqrt{3}/9\,,1/\sqrt{3}]$	$[0,1/\sqrt{3}]$	$[0,1/3]$

f_c: switching frequency; f_0: fundamental frequency.

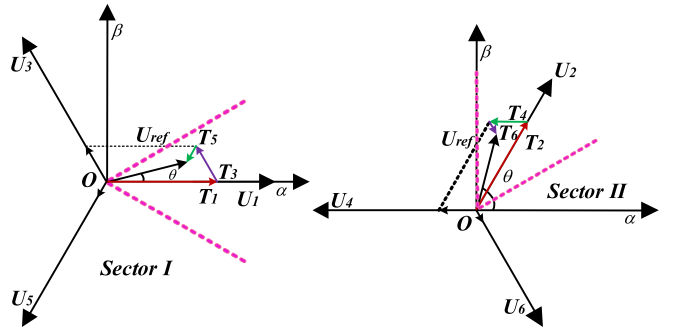
TABLE II
SECTOR DEFINITION AND VECTOR COMBINATION

Sector	Region (rad)	Vector Combination	CMV
I	$[-\pi/6\,,\pi/6]$	U_1, U_3, U_5	$U_{dc}/3$
II	$[\pi/6\,,\pi/2]$	U_2, U_4, U_6	$2\,U_{dc}/3$
III	$[\pi/2\,,5\pi/6]$	U_1, U_3, U_5	$U_{dc}/3$
IV	$[5\pi/6\,,7\pi/6]$	U_2, U_4, U_6	$2\,U_{dc}/3$
V	$[7\pi/6\,,3\pi/2]$	U_1, U_3, U_5	$U_{dc}/3$
VI	$[3\pi/2\,,11\pi/6]$	U_2, U_4, U_6	$2\,U_{dc}/3$



(a) (b)

Fig. 6. Voltage linear modulation region of (a) RSPWM and (b) proposed MSEM.



(a) (b)

Fig. 7. Voltage vector synthesis of the proposed MSEM in (a) Sector I and (b) Sector II.

III. PROPOSED MSEM TECHNIQUE

A. *Introduction of the Proposed MSEM Technique*

According to the principle of RSPWM strategy, as introduced in Section II of this article, the voltage linear modulation region of RSPWM can be obtained, as shown in the circular region in Fig. 6(a). Compared with Fig. 2(a), it can be found that, although the RSPWM has better CMV specifications, its maximum output linear voltage vector is too small. It is only suitable for light-load and low-speed motion, which is a limitation in some high-power applications or high-precision motion systems that require high speed and high acceleration. Therefore, this article proposes the modified strategy by redefining the sector distribution of voltage space vector and choosing different combinations of active voltage vectors in adjacent sectors to synthesize the reference voltage vector. It is evident to increase the maximum output linear voltage vector to some extent. The sector distribution as well as the voltage linear modulation region, which is the outer circle, are shown in Fig. 6(b). The novel sector definitions and combinations of active voltage vectors within each sector are displayed in Table II.

Defining that U_α and U_β represent the components of the reference voltage vector U_{ref} in the α and β axes. $X, Y,$ and Z are three intermediate variables, which are defined as follows:

$$\begin{cases} X = U_\alpha \\ Y = \frac{\sqrt{3}}{2}\,U_\beta - \frac{1}{2}U_\alpha \\ Z = -\frac{\sqrt{3}}{2}U_\beta - \frac{1}{2}U_\alpha. \end{cases} \tag{3}$$

Fig. 7 shows the vector composite plot of the improved strategy in Sector I and Sector II, respectively. The discussion is carried out separately to calculate the action time of each voltage vector in the above sectors.

1) Reference Voltage Vector Is Situated in Sector I: From Fig. 7(a), the following equation can be obtained according to the principle of volt-second equilibrium:

$$\begin{cases} T_s = T_1 \ + T_3 + T_5 \\ U_\alpha T_s = U_1 T_1 + U_3 \cos\left(\frac{2}{3}\pi\right) T_3 + U_5 \cos\left(-\frac{2}{3}\pi\right) T_5 \\ U_\beta T_s = U_3 \ \cos\left(\frac{1}{6}\pi\right) T_3 + U_5 \cos\left(\frac{5}{6}\pi\right) T_5 \end{cases} \tag{4}$$

where T_s represents the carrier period, and $T_1, T_3,$ and T_5 denote the action time of the corresponding voltage vectors.

By calculation, it is easy to obtain the individual vector operating time as follows:

$$\begin{cases} T_1 = \left(\frac{1}{3} + \frac{X}{U_{\mathrm{dc}}}\right) T_s \\ T_3 = \left(\frac{1}{3} + \frac{Y}{U_{\mathrm{dc}}}\right) T_s \\ T_5 = \left(\frac{1}{3} + \frac{Z}{U_{\mathrm{dc}}}\right) T_s. \end{cases} \tag{5}$$

2) Reference Voltage Vector Is Situated in Sector II: Similarly, the volt-second equilibrium equation and the action time of the corresponding voltage vectors at Sector II can be given as follows:

$$\begin{cases} T_s = T_2 \ + T_4 + T_6 \\ U_\alpha T_s = U_2 \cos\left(\frac{1}{3}\pi\right) T_2 - U_4 T_4 + U_6 \cos\left(-\frac{1}{3}\pi\right) T_6 \\ U_\beta T_s = U_2 \sin\left(\frac{1}{3}\pi\right) T_2 + U_6 \sin\left(-\frac{1}{3}\pi\right) T_6 \end{cases} \tag{6}$$

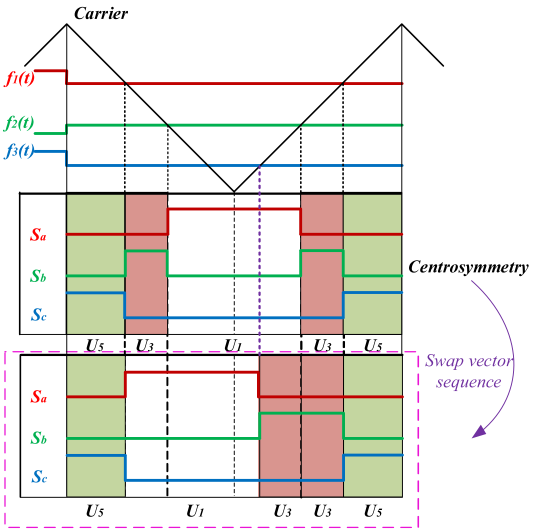


Fig. 8. Switching state of improved strategy based on the double-edge centrosymmetric carrier form in Sector I.

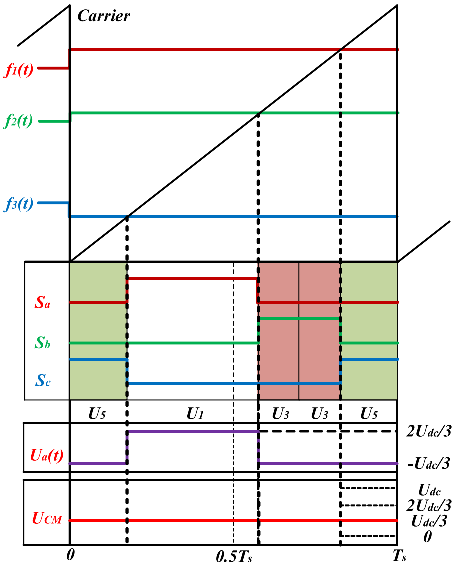


Fig. 9. Switching state, phase-A voltage, and CMV of MSEM in Sector I.

$$\begin{cases} T_2 = \left(\frac{1}{3} - \frac{Z}{U_{\mathrm{dc}}}\right) T_s \\ T_4 = \left(\frac{1}{3} - \frac{X}{U_{\mathrm{dc}}}\right) T_s \\ T_6 = \left(\frac{1}{3} - \frac{Y}{U_{\mathrm{dc}}}\right) T_s \end{cases} \tag{7}$$

where T_2, T_4, and T_6 denote the action time of the corresponding voltage vectors. The other sectors are available in the same way as the above calculations.

For the conventional modulation methods based on the double-edge carrier and PWM pulses in a centrosymmetric form, the previously mentioned improvement strategy of redefining the sector distribution and active voltage vector combinations will result in one of the three phases being switched twice in one carrier period. For example, the switching state based on the centrosymmetric and double-edge carrier form shown at the top of Fig. 8 shows that phase-B switches twice in one carrier period. This causes the inverter's switching losses to become larger, which leads to a further decrease in system efficiency. In order to avoid frequent switching of the same power device, the bridge arm that switches twice in one switching cycle from Sector I to Sector VI is selected as B-A-C-B-A-C in turn through rational planning, which realizes an even distribution of the switching frequency doubling over the three-phase bridge arms, but still does not solve the problem of the increase in switching losses at the root. This way is palliative rather than curative.

To address this problem, this article proposes an MSEM strategy based on a noncentrosymmetric single-edge carrier form. The order of the action of these voltage space vectors is modified and the centrosymmetric approach is not used. Without changing the synthesized voltage vector, the problems of switching losses are effectively reduced, and the performance of the modulation strategy is not affected. The PWM sequence, which is swapped to decrease the switching losses of VSI, is shown in the bottom of Fig. 8. As can be observed in Fig. 8, for the case when reference voltage vector is in Sector I and after swapping the voltage vector action sequence, if the double-edge centrosymmetric carrier form is still used in the digital signal processor (DSP) system, the comparative values of the modulation waveforms, which are used to compare with the carrier to produce three-phase switching signals corresponding to the rising edge of phase-A switching signal S_a, the falling edge of phase-B switching signal S_b, and the rising and falling edges of phase-C switching signal S_c, are easier to obtain. However, at this time, the comparative value of the modulation waveform corresponding to the falling edge of phase-A switching signal S_a and the rising edge of phase-B switching signal S_b and the switching action moment, is determined and influenced by the duration time of voltage vectors U_1, U_3, and U_5. As shown in Fig. 8, if the action time of U_3 is greater than that of U_1, the above-mentioned switching action moment is in the first half of one carrier period, which corresponds to the monotonically decreasing segment of the double-edge carrier signal. Conversely, it corresponds to the monotonically increasing segment of the double-edge carrier signal. And the length of action time of U_1 and U_3 is variable in real condition. Therefore, in summary, it is difficult to use double-edge carrier form to realize the strategy proposed in this article in the actual digital drive control system. So as to address the above problems, this article innovatively introduces a noncentrosymmetric single-edge carrier method to implement the above-mentioned modulation technique. This method can effectively obtain the comparison values of the three-phase modulation waveforms, greatly reducing the amount of computation and simplifying the implementation of the strategy proposed in this article. Fig. 9 displays the switching state, phase-A voltage, and CMV of the proposed MSEM in Sector I in one carrier period. Fig. 10 represents its corresponding voltage vector synthesis sequence. The order in which voltage vectors act within each sector of MSEM is detailed in Table III. Based on the above analysis, the CMV metrics of the proposed MSEM strategy are $\Delta p = 1/3$, $\Delta s = 1/3$, $N_L = 1$, $N_{L0} = 2$, $N_T = 0$, $N_{T0} = 6$, and $A_L \in [0, 2\sqrt{3}/9]$.

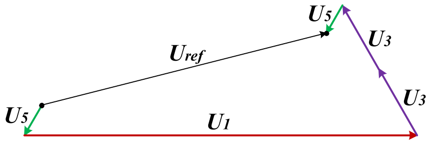


Fig. 10. Voltage vector synthesis sequence of MSEM in Sector I.

TABLE III
SEQUENCE OF VECTOR ACTION

Sector	Sequence
I	$U_5 - U_1 - U_3 - U_3 - U_5$
II	$U_6 - U_2 - U_4 - U_4 - U_6$
III	$U_1 - U_3 - U_5 - U_5 - U_1$
IV	$U_2 - U_4 - U_6 - U_6 - U_2$
V	$U_3 - U_5 - U_1 - U_1 - U_3$
VI	$U_4 - U_6 - U_2 - U_2 - U_4$

MSEM enhances the maximum voltage linear output range and the output value domain perfectly complements the NSPWM, so it can be used in combination with it in the full modulation ratio range.

B. Influence of Deadtime Effect on the Proposed MSEM

In practical engineering digital drive control systems, a certain amount of deadtime must be reserved in the drive signal to avoid the shoot-through phenomenon of the same bridge. For the proposed MSEM method, there are three switching moments in a carrier period, and each one should have two PWM actions at the same time to ensure that the CMV is constant. Consequently, when deadtime exists, the two signals should be synchronized to act asynchronously. Undesired CMV spikes are generated, and at the same time, the phase voltage is shifted and varied to some extent.

Since the deadtime effect of VSIs is closely related to the polarities of the three-phase currents, here, we discuss a theoretical analysis of the influence of the deadtime effect for a hypothetical case, which can be analyzed to the full cases. Define the polarities of three-phase currents as negative, positive, and negative when the reference voltage vector is in Sector III of MSEM. Fig. 11 shows the impact of deadtime effect on the CMV and phase-A voltage in this specific case. In this figure, T_d represents the deadtime, and the blue and green squares denote the increasing and decreasing portions, respectively. Thus, the presence of deadtime makes short pulse spikes in the CMV and introduces distortion in the output phase voltage. In the light of the phenomenon, this article adopts a method based on the load characteristics combined with current estimation to complete the DEC.

According to the topological form of the inverter used in this article, the expression for the voltage across the inductors of each phase can be obtained as follows:

$$\begin{cases} U_{aL} = U_{AO} - U_{NO} - RI_a - e_a = L\frac{dI_a}{dt} \\ U_{bL} = U_{BO} - U_{NO} - RI_b - e_b = L\frac{dI_b}{dt} \\ U_{cL} = U_{CO} - U_{NO} - RI_c - e_c = L\frac{dI_c}{dt} \end{cases} \tag{8}$$

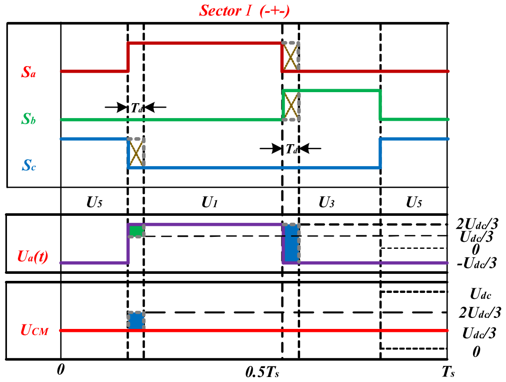


Fig. 11. Influence of deadtime effect when the polarities of the three-phase currents are negative, positive, and negative of MSEM in Sector I.

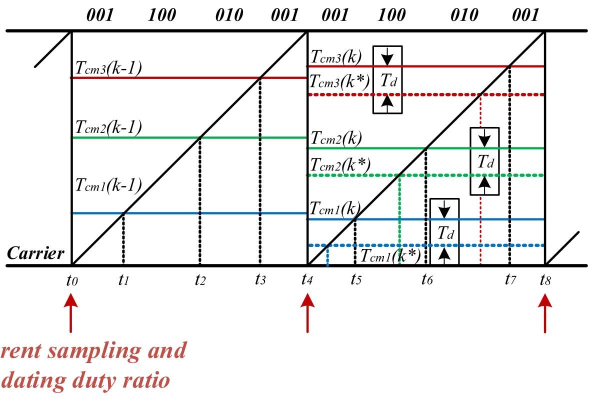


Fig. 12. Principle of the adopted DEC methodology of MSEM in Sector I.

where U_{aL}, U_{bL}, and U_{cL} are the voltages of three-phase inductors, I_a, I_b, and I_c are the three-phase currents, and e_a, e_b, and e_c are the three-phase grid voltages or back electromotive force of motor.

The conventional DEC strategies use the three-phase currents detected at the entry of a program interrupt to approximate the phase current values at each deadtime moment as a substitute, which is subject to error. In accordance with (8), the increment of inductor current during each period of voltage vectors action time can be derived, thus estimating the actual phase current values at each deadtime moment. Therefore, the estimated current values obtained at these moments can be used for the DEC strategy based on time pulsewidth correction. This method based on current estimation can achieve real-time calculation of phase currents within a carrier period, thus improving the accuracy of current polarity judgment and avoiding miscompensation where current crosses near the zero point to a certain extent. Fig. 12 shows the overall block diagram of the principle of the whole compensation strategy, where T_d represents the deadtime interval, which is set in the DSP.

The working principle of this compensation strategy is briefly described in the following text according to Fig. 12. Assuming that the reference voltage vector is in Sector I, according to the execution logic of the microprocessor, it can be known that at t_0, the software enters the interrupt and samples the three-phase currents $I_a(t_0)$, $I_b(t_0)$, and $I_c(t_0)$, followed by current loop calculations to obtain three comparison values $T_{cm1}(k)$, $T_{cm2}(k)$, and $T_{cm3}(k)$. Due to the innate latency of digital control systems, these three values must be loaded into the system at t_4. Therefore, the current estimation method is used to calculate the three-phase currents corresponding to three moments t_5, t_6, and t_7, and to determine their polarities. The following is an example of phase-A current, according to (8), we can get the formula for calculating the current increment in each period of voltage vectors as follows:

$$\Delta I_{01} = \frac{U_{01} - I_{01}(t) R - e_a}{L} \Delta t_{01} \tag{9}$$

where ΔI_{01}, U_{01}, Δt_{01}, and $I_{01}(t)$ denote the current increment value, phase voltage magnitude, time interval, and time-varying phase current variable between t_0 and t_1, respectively. To facilitate the calculation and reduce the computational bias, the Lagrange first-order interpolation method can be used to display $I_{01}(t)$, which is given as follows:

$$I_{01}(t) = \frac{I_a(t_0) + I_a(t_1)}{2} = I_a(t_0) + \frac{\Delta I_{01}}{2}. \tag{10}$$

Substituting (10) into (9) yields

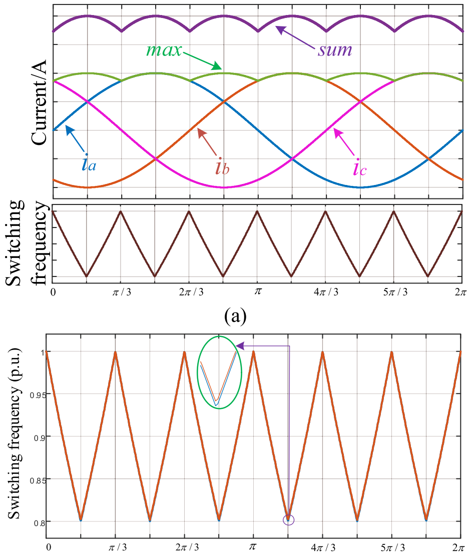
$$\Delta I_{01} = \frac{2\left(U_{01} - R I_a(t_0) - e_a\right)}{R\Delta t_{01} + 2L} \Delta t_{01}. \tag{11}$$

Thus, the value of phase-A current at t_1 can be obtained as follows:

$$\begin{aligned} I_a(t_1) &= I_a(t_0) + \Delta I_{01} \\ &= \frac{2\left(U_{01} - e_a\right)\Delta t_{01} + \left(2L - R\Delta t_{01}\right) I_a(t_0)}{R\Delta t_{01} + 2L}. \end{aligned} \tag{12}$$

Similarly, the value of the current at any moment can be estimated. The DEC method based on the combination of current estimation and time pulsewidth correction is finally implemented considering the rising and falling edges of the PWM pulse and the corresponding current polarity. The three compensated comparison values $T_{cm1}(k^*)$, $T_{cm2}(k^*)$, and $T_{cm3}(k^*)$ are finally loaded to the controller at t_4. For the MSEM strategy in Sector I, as illustrated in Fig. 12, the phase-A switching signal S_a is determined by $T_{cm1}(k)$ and $T_{cm2}(k)$, the phase-B switching signal S_b is determined by $T_{cm2}(k)$ and $T_{cm3}(k)$, and the phase-C switching signal S_c is determined by $T_{cm1}(k)$ and $T_{cm3}(k)$ without using the DEC strategy. When using the DEC method for current estimation, it is assumed that phase-A current is predicted to have the negative polarity at moments t_5 and t_6, phase-B current is predicted to have the positive polarity at moments t_6 and t_7, and phase-C current is predicted to have the negative polarity at moments t_5 and t_7. The three-phase current polarities situation at this time coincides with Fig. 11. Therefore, the three compensated comparative values can be obtained as follows:

$$\begin{cases} T_{cm1}\ (k^*) = T_{cm1}\ (k) - T_d \\ T_{cm2}\ (k^*) = T_{cm2}\ (k) - T_d \\ T_{cm3}\ (k^*) = T_{cm3}\ (k) - T_d. \end{cases} \tag{13}$$



(a)

(b)

Fig. 13. Sum of absolute values of three-phase currents and (a) desired switching frequency, and (b) function fitting of the switching frequency.

So, according to Figs. 11, 12, and the above analysis, it is easy to obtain that the phase-A switching signal S_a is determined by $T_{cm1}(k)$ and $T_{cm2}(k^*)$, the phase-B switching signal S_b is determined by $T_{cm2}(k^*)$ and $T_{cm3}(k)$, and the phase-C switching signal S_c is determined by $T_{cm1}(k^*)$ and $T_{cm3}(k)$ with using the DEC strategy. Thus, the negative impact of the deadtime effect on MSEM is eliminated to a certain extent, but it is difficult to completely compensate and offset due to the factors, such as drive delay, device variability, and parasitic parameters.

C. *Analysis of Periodic Frequency Modulation (PFM)*

While using the MSEM to reduce the common-mode noise of the system, to further decrease the peaks of conducted EMI, PFM is introduced to spread the EMI at a specific frequency point. A detailed mathematical and theoretical analysis is performed to derive the switching frequency variation function considering switching losses and distribution characteristics in the time domain of switching frequency.

The power loss of each switching device in the VSI adopted by the MSEM strategy is directly proportional to the switching frequency and current amplitude, which is expressed as

$$P_{\text{loss}} = \frac{1}{2\pi} \cdot \frac{U_{\text{dc}}\left(t_{\text{on}} + t_{\text{off}}\right)}{2} \cdot \int_0^{2\pi} f_s\left(\theta\right) \cdot f_i\left(\theta\right) d\theta \tag{14}$$

where P_{loss} denotes the power dissipated by the switching losses in one fundamental period, t_{on} and t_{off} represent the turn-on and turn-off time of power switches, and $f_s(\theta)$ and $f_i(\theta)$ are the nonnegative switching frequency function and current function of one phase. From (14), it can be said that switching losses can be reduced if the switching frequency and current can be negatively correlated. Fig. 13(a) illustrates the sum of the absolute values of the three-phase currents and the trend of the desired switching frequency function. Assuming that $f_s\ (0) = f_{cs}$ and

$f_s\left(\pi/6\right) = \ m \cdot f_{cs}$, where $m \in [0, 1]$ represents the spreading factor.

In order to extend the uniformity of the frequency bands and the EMI spikes can be distributed more evenly across it. It is, therefore, necessary to carry out a detailed mathematical theoretical derivation of the switching frequency function with the trend of the curve in Fig. 13(a) to search for the optimal variation function. From the theoretical analysis, it is clear that when the switching frequency is higher, the faster the acquisition rate is, the more acquisition points at that frequency point in the time domain. And when the absolute value of the changing rate of the switching frequency is smaller, more collection points at that frequency in the time domain will be achieved. Thus, the number of points of acquisition at a given frequency in the time domain is directly proportional to the magnitude of the switching frequency and inversely proportional to the absolute value of the changing rate of the switching frequency. So, we can deduce as follows:

$$\frac{f_s\left(\theta\right)}{\left|f'_s(\theta)\right|} = \rho\left[f_s\left(\theta\right)\right] \tag{15}$$

where $\rho[f_s(\theta)]$ represents the spreading coefficient of the switching frequency in the time domain. Further use of (15) and values constraint yields the functional expression as

$$f_s(\theta) = f_{cs} \ \cdot e^{\frac{6}{\pi}\ln(m)\cdot\theta} \tag{16}$$

To facilitate the implementation of the digital control system, the exponential function in the switching frequency function is replaced by taking the first three terms of the Taylor series expansion, at which the error is already less than 0.002, as shown in Fig. 13(b). Therefore, in accordance with (14) and (16), the switching loss power of the VSI can be calculated in one fundamental period as (17) shown at the bottom of this page. In (17), $P_{\text{loss\_VSI}}$ denotes the total switching losses of the six power devices of the VSI in one fundamental cycle. $\tilde{f}_i(\theta)$ is the sum of the absolute values of three-phase currents. I_m stands for the peak value of phase current. The variable k represents the modulation ratio of the proposed MSEM and is defined as follows: $k = 3\sqrt{3}U_{\text{ref}}/2U_{\text{dc}}$. $\varphi(m)$ is a monotonically increasing function on the variable m. Therefore, when the inverter parameters are determined, the switching loss is positively correlated with m and k. The PFM considering the phase angle of output currents not only reduces the EMI spikes but also effectively minimizes the switching losses of VSI, thus improving the efficiency of the whole system.

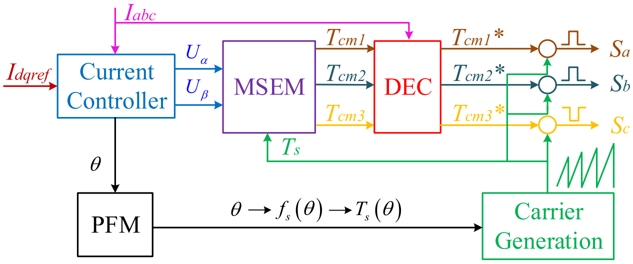


Fig. 14. Block diagram of the proposed overall strategy.

D. Implementation of the Proposed Overall Strategy

A block diagram of the proposed overall strategy is shown in Fig. 14. It can be summarized as follows. The reference current $I_{dq\text{ref}}$ generated by the outer loop and the actual sampled current I_{abc} are input to the current controller for computation to obtain U_α and U_β. And then three comparative values T_{cm1}, T_{cm2}, and T_{cm3} are obtained after going through the MSEM module proposed in this article for reducing the CMV of three-phase two-level VSIs. Subsequently, the DEC scheme adopted in this article is used to eliminate the deadtime effect on the above modulation strategy and three updated comparison values $T_{cm1}{}^*$, $T_{cm2}{}^*$, and $T_{cm3}{}^*$ are acquired. At the same time, the current phase angle θ is obtained based on the actual sampled currents of the three phases, thus gaining an updated value $T_s(\theta)$ for the switching period, which is used to generate the real-time carrier waveform. In the next control cycle, the novel comparison values and carrier values are loaded into the drive system, thus completing the digital implementation of the entire control strategy.

IV. EXPERIMENTAL VERIFICATION

A. Experimental Prototype

In order to validate the MSEM mentioned in Section III, an experimental platform was constructed. Fig. 15 shows the diagram and photographs of the experimental platform. The hardware topology of the driver is designed with a three-phase two-level VSI architecture and an 18-bit high-speed high-resolution AD

$$\begin{aligned}
P_{\text{loss\_VSI}} &= 2\cdot\frac{1}{2\pi}\cdot\frac{U_{\text{dc}}\left(t_{\text{on}}+t_{\text{off}}\right)}{2}\cdot\int_0^{2\pi} f_s\left(\theta\right)\cdot\tilde{f}_i\left(\theta\right)d\theta\\
&= 2\cdot\frac{1}{2\pi}\cdot\frac{U_{\text{dc}}\left(t_{\text{on}}+t_{\text{off}}\right)}{2}\cdot 12\cdot\int_0^{\pi/6} f_{cs}\cdot e^{\frac{6}{\pi}\ln(m)\cdot\theta}\cdot(-2)\cdot I_m\cdot\sin\left(\theta-\frac{2}{3}\pi\right)d\theta\\
&= \frac{-12\cdot f_{cs}\cdot I_m\cdot U_{\text{dc}}\cdot\left(t_{\text{on}}+t_{\text{off}}\right)}{\pi}\cdot\int_0^{\pi/6} e^{\frac{6}{\pi}\ln(m)\cdot\theta}\cdot\sin\left(\theta-\frac{2}{3}\pi\right)d\theta = \frac{8\sqrt{3}\cdot k\cdot f_{cs}\cdot U_{\text{dc}}^2\cdot\left(t_{\text{on}}+t_{\text{off}}\right)}{3\pi\cdot\sqrt{R^2+4\pi^2 f_0^2 L^2}}\\
&\quad\cdot\frac{\ln\left(m\right)\cdot\left(12m\pi-6\sqrt{3}\pi\right)+\pi^2}{72\cdot\left(\ln\left(m\right)\right)^2+2\pi^2}.
\end{aligned} \tag{17}$$

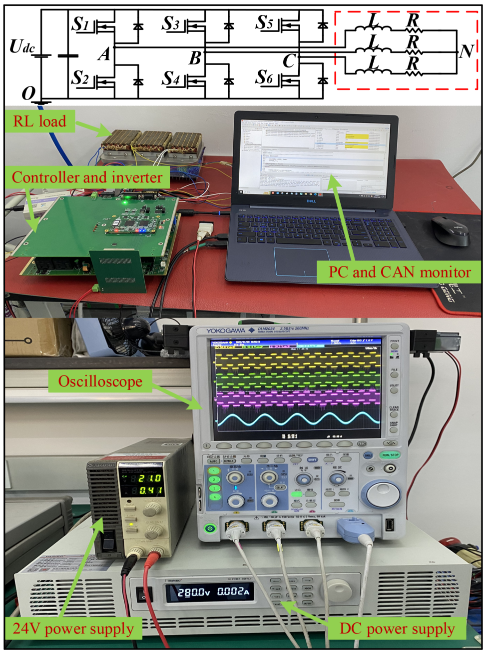


Fig. 15. Diagram and photographs of the experimental platform.

TABLE IV
SPECIFICATIONS AND PARAMETERS OF PLATFORM

Parameter	Value
DC-link Voltage	48 V
Phase Resistor	0.9 Ω
Phase Inductor	4.8 mH
Constant Switching Frequency	12.5 kHz
Fundamental Frequency	10 Hz
Deadtime Interval	2.5 μs
Reference Current	5 A

conversion chip. Therefore, the phase currents obtained are more accurate to facilitate the implementation of the DEC strategy for MSEM proposed in this article. The software is programmed based on the DSP+field programmable gate array (FPGA) dual-core CPU architecture of TI TMS320F28379D and PANGO PGL25G. The FPGA is responsible for accepting the phase currents digital quantities converted by the AD chips and transferring them to the DSP, and monitoring the abnormalities of the driver, such as overtemperature and overcurrent. The DSP is to perform the calculation of the current loop as well as the proposed MSEM, DEC, and the PFM, considering the switching losses and spreading coefficient in the time domain. And it passes the drive signals to the FPGA and then sends them out to the inverter. The DSP and FPGA interact with each other through external memory interface (EMIF) communication. The specifications and parameters of the whole experimental system are displayed in Table IV. In the experiment, 10 Hz is selected as the fundamental frequency because this article is carried out for the VSI of the drive control system for the high-speed high-precision transportation linear motors. For the determined direct-drive trajectory and velocity, the fundamental frequency of a specific frequency is directly related to the pole pitch and speed of the linear motors. In the following results, the sampling frequency of the phase voltage, phase current, and CMV for the fast Fourier transform (FFT) in an oscilloscope is 625 kHz.

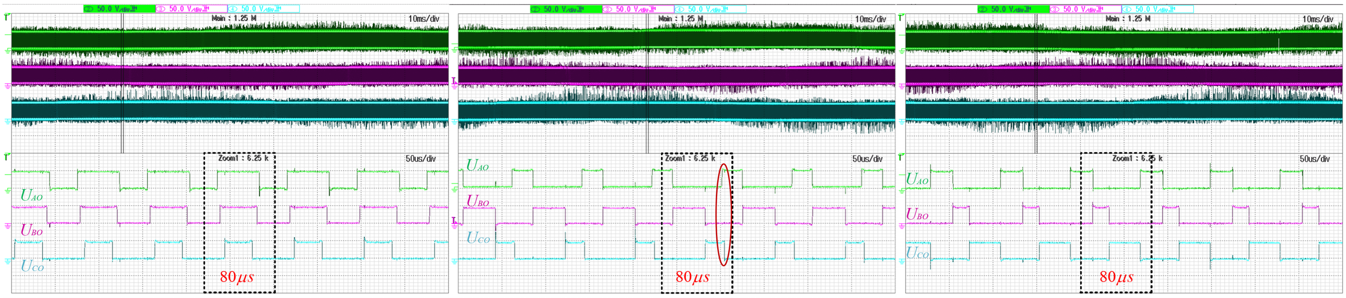
B. Experimental Results

Fig. 16 illustrates the experimental waveforms of the pole voltages of three phases for three modulation strategies SVPWM, the proposed MSEM without DEC, and the proposed MSEM with DEC. From Fig. 16(a) and (b), it can be clear that the MSEM with optimized voltage vector action sequence has the same number of switching actions in one switching period with SVPWM, thus effectively reducing the switching losses of the VSI system. In addition, there is an overlapping region of high levels of the pole voltages between phase-A and phase-C, which is marked by a red ellipse in Fig. 16(b) located in Sector III. This is introduced due to the deadtime interval in the inverter, resulting in the pole voltages of both phases not completing the simultaneous switching action. While, in Fig. 16(c), using the DEC method proposed in this article effectively eliminates the negative impact of the deadtime effect and achieves the two-by-two simultaneous switching action of the three phases.

The three-phase voltages of the SVPWM, the proposed MSEM without DEC, and the proposed MSEM with DEC are displayed in Fig. 17. The phase voltage waveform distortion brought by the deadtime effect can still be seen in Fig. 17(b), as shown by the red circle in the figure. Since both the voltage and current vectors in the figure are situated in Sector III in the space vector diagram, the polarities of three-phase currents at this time are negative, positive, and negative, respectively. This is consistent with the situation, as presented in Fig. 11. Therefore, all three-phase voltages have a downward concave short pulse, which is fully consistent with the theoretical analysis. This phase voltage distortions are effectively canceled by combining DEC, as can be shown in Fig. 17(c).

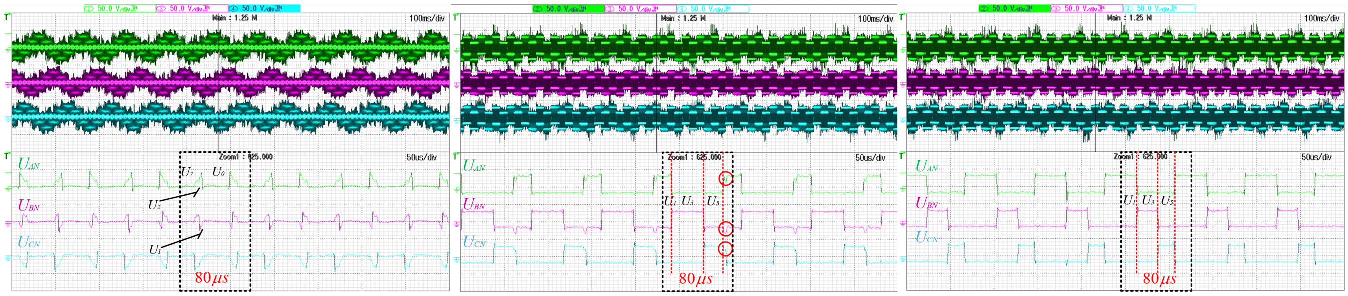
Fig. 18 exhibits the CMV waveforms for these three modulation schemes. Again, it can be noticed that there is a CMV spike in every switching period in Fig. 18(b). This is similarly due to the deadtime effect, and Fig. 18(c) solves this problem well. Comparing Fig. 18(c) with (a), it can be concluded that the peak–peak value of the VSIs CMV is reduced from U_{dc} of SVPWM to $1/3$ times, and the frequency is also decreased from $6f_c$ to $6f_0$. The effectiveness and practicality of the MSEM combined with the DEC scheme proposed in this article to reduce the amplitude and frequency of the CMV are verified.

Section III shows the time-domain characteristics of the proposed modulation method. To further verify the frequency-domain performance of the proposed modulation strategy, the data of the output phase voltage, CMV, and phase current are processed by fast Fourier transform (FFT) in the oscilloscope to obtain their spectrograms. Fig. 19 illustrates the harmonics spectrum of the phase voltage for the three strategies SVPWM, the proposed MSEM+DEC without PFM, and the proposed MSEM+DEC with PFM. Comparing Fig. 19(a) with (b), it can be deduced that the proposed MSEM combined with DEC introduces harmonic components at both the switching frequency



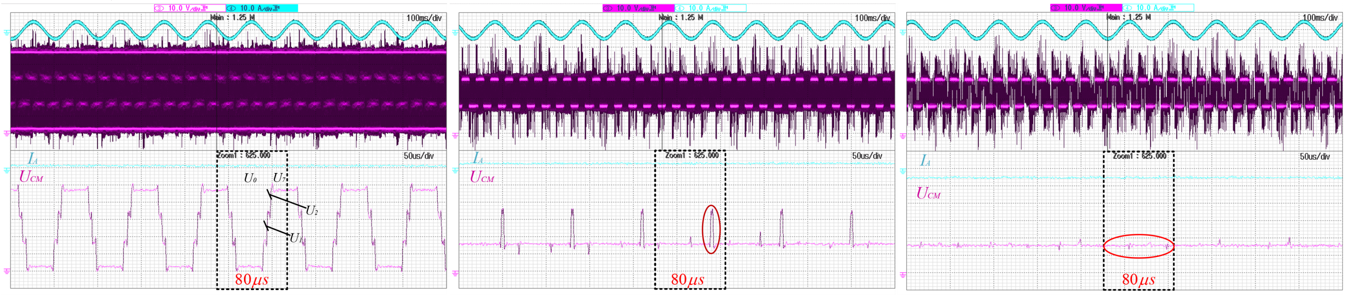
(a) (b) (c)

Fig. 16. Pole voltages with (a) SVPWM, (b) proposed MSEM without DEC, and (c) proposed MSEM with DEC in Sector III (*X*-axis: 50 μs/div and *Y*-axis: 50 V/div).



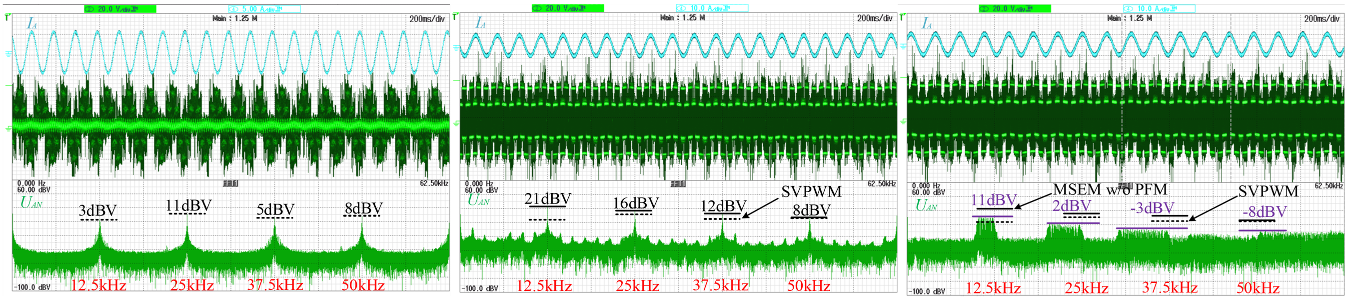
(a) (b) (c)

Fig. 17. Phase voltages with (a) SVPWM, (b) proposed MSEM without DEC, and (c) proposed MSEM with DEC in Sector III (*X*-axis: 50 μs/div and *Y*-axis: 50 V/div).



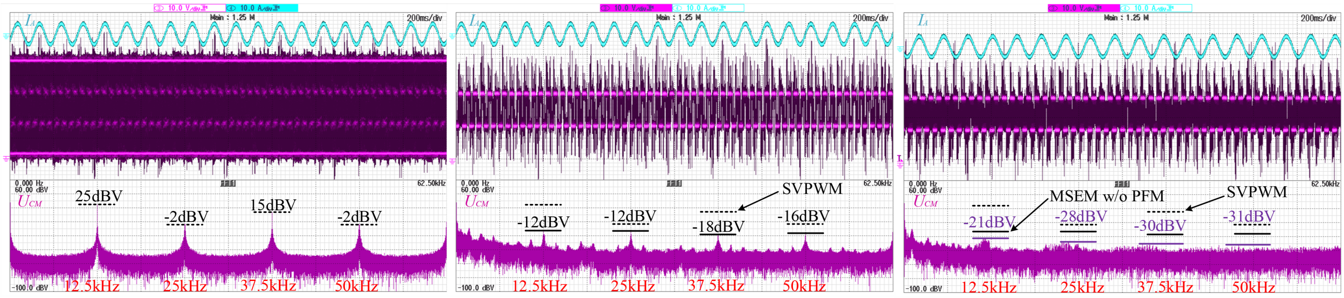
(a) (b) (c)

Fig. 18. CMVs with (a) SVPWM, (b) proposed MSEM without DEC, and (c) proposed MSEM with DEC in Sector III (*X*-axis: 50 μs/div and *Y*-axis: 50 V/div).



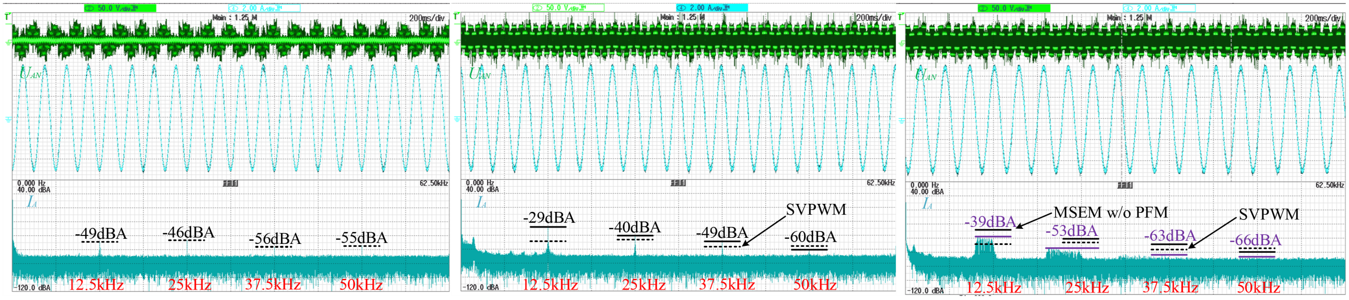
(a) (b) (c)

Fig. 19. Harmonics spectrum of phase voltage with (a) SVPWM, (b) proposed MSEM+DEC without PFM, and (c) proposed MSEM+DEC with PFM (*X*-axis: 6.25 kHz/div and *Y*-axis: 20 dBV/div).



(a) (b) (c)

Fig. 20. Harmonics spectrum of CMV with (a) SVPWM, (b) proposed MSEM+DEC without PFM, and (c) proposed MSEM+DEC with PFM (*X*-axis: 6.25 kHz/div and *Y*-axis: 20 dBV/div).



(a) (b) (c)

Fig. 21. Harmonics spectrum of phase current with (a) SVPWM, (b) proposed MSEM+DEC without PFM, and (c) proposed MSEM+DEC with PFM (*X*-axis: 6.25 kHz/div and *Y*-axis: 20 dBA/div).

TABLE V

CURRENT HARMONIC AMPLITUDES OF SWITCHING FREQUENCY AND ITS MULTIPLICATION FOR VARIOUS MODULATION STRATEGIES (MODULATION INDEX $k \approx 0.25$ FOR ALL THE EXPERIMENTS)

Value	SVPWM	MSEM+DEC	MSEM+DEC +PFM m = 0.9	MSEM+DEC +PFM m = 0.8	MSEM+DEC +PFM m = 0.7	MSEM+DEC +PFM m = 0.6	MSEM+DEC +PFM m = 0.5
f_s	−49 dBA	−29 dBA	−37 dBA	−39 dBA	−45 dBA	−47 dBA	−50 dBA
$2f_s$	−46 dBA	−40 dBA	−52 dBA	−53 dBA	−55 dBA	−58 dBA	−60 dBA
$3f_s$	−56 dBA	−49 dBA	−61 dBA	−63 dBA	−66 dBA	−66 dBA	−66 dBA
$4f_s$	−55 dBA	−60 dBA	−66 dBA	−66 dBA	−66 dBA	−66 dBA	−66 dBA

and its integer multiples of the frequency points, making the harmonic content larger than that of the SVPWM. The PFM by introducing a spreading factor in the time domain can effectively reduce the harmonic levels at the above frequency points. Fig. 19(c) shows the spectrogram of the phase voltage when the spreading factor $m = 0.8$ is taken. It can be observed that the harmonic amplitudes at once and twice switching frequencies are reduced from 21 and 16 dBV to 11 and 2 dBV.

Figs. 20 and 21 show the harmonics spectrum of the CMV and phase current, respectively. Fig. 20(c) indicates that the PFM makes the harmonic amplitudes of CMV at once and twice switching frequency reduce from -12 and -12 dBV to -21 and -28 dBV. And Fig. 21(c) displays that the PFM makes the harmonic amplitudes of phase current at once and twice switching frequency reduce from -29 and -40 dBA to -39 and -53 dBA. The detailed data for harmonic amplitude reduction of phase currents are shown in Table V. It is worth mentioning that the experimental data in Table V are also performed based on the experimental conditions and parameters in Table IV. Therefore, based on the experimental parameters in Table IV and the definition of the modulation index k, it can be deduced the modulation index of SVPWM and other modulation strategies in the experiments is given as follows:

$$k = \frac{3\sqrt{3}U_{\text{ref}}}{2U_{\text{dc}}} = \frac{3\sqrt{3}I_{\text{ref}}Z_{\text{load}}}{2U_{\text{dc}}} = \frac{3\sqrt{3}I_{\text{ref}}\sqrt{R^2 + (2\pi f_0 L)^2}}{2U_{dc}} \approx 0.25. \tag{18}$$

From Table V, as the spreading factor m decreases, the current harmonic suppression capability increases. However, selecting too small of m results in a region of spectral overlap at high frequencies, which will degrade the suppression performance. Therefore, the selection of m needs to be a tradeoff between the

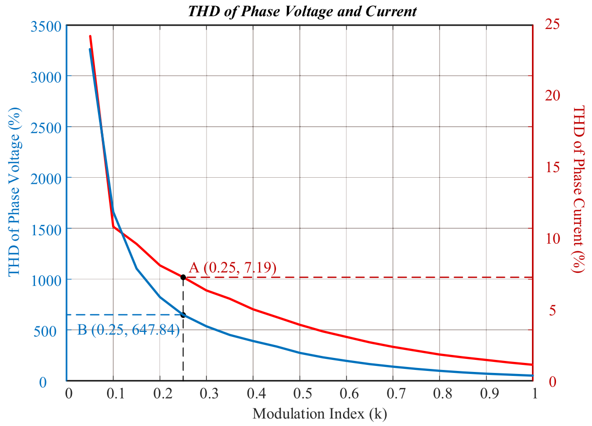


Fig. 22. THD of phase voltage and current at various modulation index k.

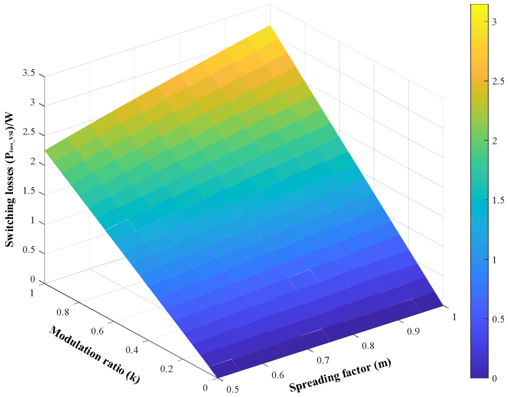


Fig. 23. Switching losses of VSI for different modulation ratios k and spreading ratios m.

harmonic suppression and the spectral overlap. Consequently, under the premise of MSEM combined with DEC, the adoption of PFM considering the time-domain spreading coefficient can significantly reduce the harmonic amplitude and reach or even outperform the harmonic level of SVPWM.

In addition, Fig. 22 illustrates the THD of the output phase voltage and current for various modulation index k. From Fig. 22, it is found that the THD of output phase voltage and phase current decreases gradually as the modulation index k increases. This is mainly due to the fact that the amplitudes of the fundamental voltage and current are also greater for large modulation index k. It is also observed that the THD of the phase voltage is very large because the phase voltage consists of a series of PWM pulse-like waveforms. It contains a large number of harmonics at the switching frequency and its multiples, where points A and B in Fig. 22 correspond to the experimental conditions in Table IV.

C. Switching Losses Analysis

The switching losses at different modulation ratios k and spreading factor m are calculated according to (17) and are shown in Fig. 23. It can be concluded that the level of switching losses decreases as m decreases. It indicates that the PFM with integrated consideration of the phase angle of phase current and spreading coefficient $\rho[f_s(\theta)]$ in the time domain cannot only reduce the harmonic amplitude of phase voltage, phase current, and CMV in the frequency domain but also effectively decrease the switching losses of the VSI, which in turn improves the efficiency level of the whole drive control system.

V. CONCLUSION

This article has proposed an MSEM strategy to decrease the CMV by considering deadtime effects and switching losses for three-phase two-level VSIs. The MSEM strategy avoids the use of zero vectors and by redefining the sector distribution of space voltage vector and choosing different combinations of active voltage vectors in adjacent sectors to synthesize the reference voltage vector. And it is possible not only to decrease the peak–peak value and frequency of the CMV but also to increase the maximum output linear voltage vector to some extent. In light of the deadtime effects on the effectiveness of CMV suppression, this article adopts a method based on the load characteristics combined with current estimation to complete the DEC. The experimental results demonstrate the capability of this strategy in suppressing the negative effects produced by deadtime. In addition, the harmonic amplitudes of phase voltage, phase current, and CMV of SVPWM and MSEM combined with DEC are compared. This leads to the introduction of the PFM strategy that considers the phase angle of phase current and spreading coefficient in the time domain. While reducing the harmonic amplitude of the MSEM+DEC method, the switching losses are effectively decreased and the system efficiency is improved. The integrated modulation scheme of MSEM combined with DEC and PFM is finally achieved. In fact, this scheme can be used not only in motor-drive systems but also in grid-connected inverter systems to reduce the CMV and harmonic amplitudes at the switching frequency and its multiplication.

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