Modeling and Analysis of Shutdown Dynamics in Flying Capacitor Multilevel Converters

Samantha Coday, *Graduate Student Member, IEEE*, Nathan Miles Ellis, *Member, IEEE*, and Robert Carl Nikolai Pilawa-Podgurski, *Fellow, IEEE*

***Abstract*—This work explores the dynamic behavior of the flying capacitor multilevel (FCML) converter during unplanned shutdown. A model for a general N-level FCML converter is developed, which captures capacitor nonlinearities, component leakage paths, and body diode behavior. This work highlights how switch voltage ratings may be exceeded during unplanned shutdown, and proposes several mitigation strategies. Using a ten-level FCML converter hardware prototype, the time-domain behavior of the model is verified, and a successful hardware mitigation strategy is demonstrated which ensures safe and rapid converter shutdown.**

***Index Terms*—Converter modeling, flying capacitor multilevel converter, shutdown dynamics.**

I. Introduction

FLYING capacitor multilevel (FCML) converters [1] have been shown to have high efficiency and power density over a wide range of applications [2], [3]; from high voltage electric aircraft drivetrains [4], to low voltage data center applications [5] and chip-scale implementations [6], [7]. The FCML converter achieves high power density through the use of flying capacitors, which can be implemented using energy dense capacitors, such as Class II multilayer ceramic capacitors (MLCCs). Moreover, the flying capacitors provide dc voltage blocking, enabling the use of low voltage power transistors with improved figures of merit, fast switching speeds, and lower conduction losses [8], [9].

While these flying capacitors enable compact and efficient designs they also present challenges, such as capacitor voltage balancing [10], [11]. If the capacitor voltages are not balanced, the voltage stress on individual switches within the FCML converter may exceed their rating, causing failures. While some control techniques have been proposed which actively balance flying capacitors during steady-state operation [12], [13], ensuring balanced operation at start-up and shutdown is particularly challenging, as all the flying capacitors must ramp up and ramp down with uniform voltages to avoid switch damage. Previous work has presented solutions to the challenge of start-up through additional auxiliary circuits [14] and sophisticated modulation techniques [15], [16]. While start-up has been the primary focus of previous work regarding the practical implementation of FCML converters, little work has been done exploring dynamics of converter shutdown, which is of great importance for practicing engineers who wish to design compact and efficient FCML converters that are also robust.

This work explores the voltage dynamics of the flying capacitors when an FCML circuit is suddenly de-energized, and investigates safe shutdown techniques in practical implementations. As demonstrated in [17], external system faults such as output short circuit transients can be mitigated through changes to the switch modulation, where the converter switches are controlled to initially counteract the fault, followed by a "ride-through" mode where the converter remains active, but not outputting any power. This work considers the different scenario where the converter is shut down immediately, either due to loss of control/logic power, controller malfunction, or due to power transistor, flying capacitor, or gate drive degradation or failure that necessitates a rapid shutdown. In such scenarios, great care must be taken through design of auxiliary circuitry to ensure that component ratings are not exceeded. Moreover, a computationally efficient dynamic model of the FCML converter during shutdown operation is proposed, and used to demonstrate how device ratings and converter failure can result from sudden loss of control power. Based on the findings of the dynamic model, several safe shutdown techniques are verified and evaluated.

This article extends an earlier conference publication [18] of this work. Here, we present more detailed analysis of shutdown dynamics including the impact of conversion ratio. Moreover, this work presents additional experimental results validating the proposed model and safe shutdown methods. The rest of this article is organized as follows. Section II introduces the relevant FCML converter component models. Section III explores the effect of input/output capacitance and conversion ratio on a generic FCML converter shutdown. In Section IV, a model is described which was developed to predict switch stress during converter shutdown. Section V describes an experimental

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The authors are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: scoday@berkeley.edu; nathanmilesellis@berkeley.edu; pilawa@berkeley.edu).

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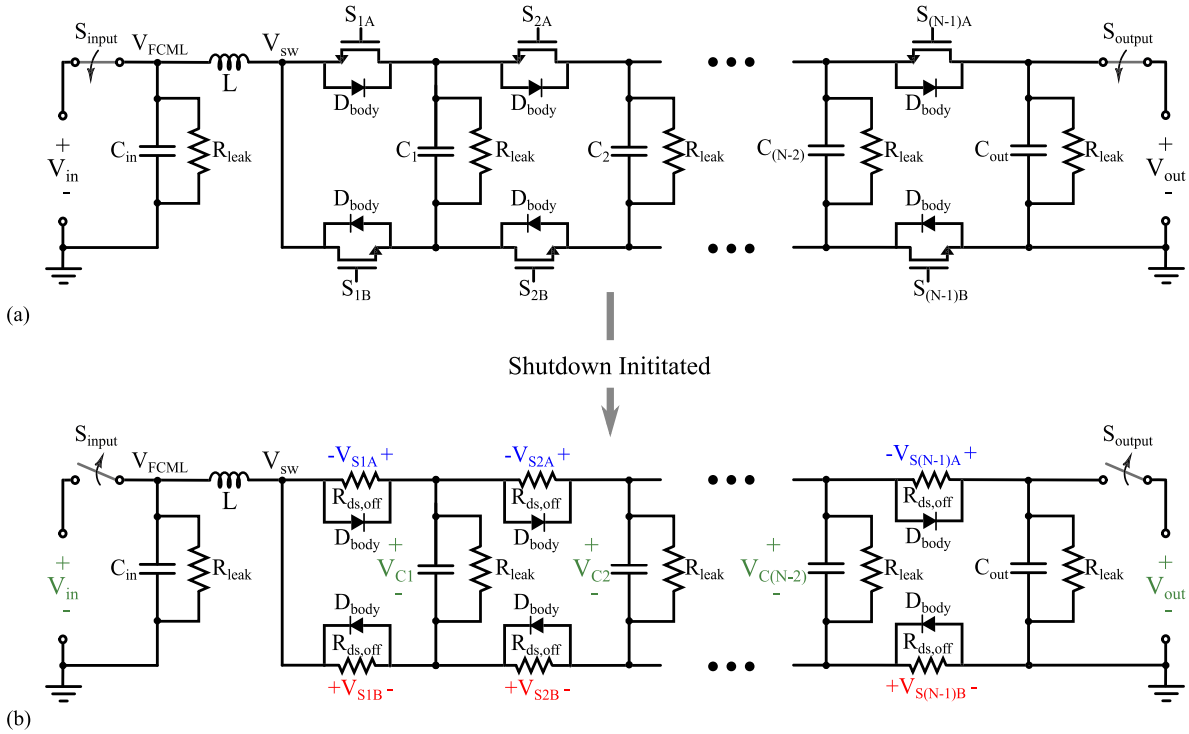

Fig. 1. (a) Circuit model of a generic N-level FCML converter [1], with input and output breakers. (b) Circuit model once shutdown is initiated, with relevant parasitic components shown. Capacitor and switch voltages are also labelled.

prototype used to validate the model. Section VI proposes three safe shutdown techniques and evaluates the performance of each. Finally, Section VII concludes the article.

II. FCML Circuit Model

A generic N-level FCML boost converter [1], [19], used to model nominal operation, is shown in Fig. 1(a). While the analysis presented here is for the boost converter, we note that due to the bi-directional nature of the FCML converter, the analysis also applies to a step-down (buck) implementation. In the model of Fig. 1(a), input and output terminals are connected through switches (S_{input} and S_{output}) that may isolate the converter from the source and load during start-up and/or shutdown. This functionality is often required in practical implementations, where relays or solid-state circuit breakers may be employed.

During nominal FCML operation, switch pairs S_{iA} and S_{iB} operate complimentary to one another, and the flying capacitors are charged to $k \times \frac{V_{out}}{N-1}$, where k is the capacitor index, as defined in Fig. 1(a). When capacitor voltages are balanced the voltage across each switch when in the OFF-state (excluding any flying capacitor voltage ripple) is $\frac{V_{out}}{N-1}$ as imposed by the two adjacent flying capacitors. However, if the capacitors are not balanced, i.e. they are not charged to their nominal voltages, then switch stress will vary and may result in overvoltage and device failure. This work investigates potential failures that stem from capacitor imbalance during the shutdown routine.

In general, converter shutdown can be either planned or unplanned. Here, we investigate the more difficult case—unplanned shutdown—stemming from a loss of control power which results in the opening of input and output switches (S_{input} and S_{output}), and the loss of gate-drive power to all FCML switches, $S_{i,A/B}$. Once shutdown has been initiated, the converter can be modelled as shown in Fig. 1(b). Since all FCML switches are open, they can be represented by their effective OFF resistance, $R_{ds,off}$ and intrinsic body diodes, D_{body}. Since the time constants associated with shutdown in practical FCML designs are typically very long (on the order of tens of seconds to over a minute), as dictated by leakage paths, the inductor can be modelled as a short. As will be shown in this work, the shutdown behavior of the FCML converter is highly dependent on component nonidealities, such as transistor body diodes and parasitic leakage paths. The following subsections describe the relevant component parasitics.

A. Switch Model

1) Body Diode: In Fig. 1, the antiparallel diodes, labelled D_{body}, correspond to body diodes in silicon MOSFET implementations. Although Gallium Nitride (GaN) transistors do not have an intrinsic body diode, their reverse conduction associated with channel inversion is also captured by the diode model. When the diodes are conducting a small forward voltage drop (less than 2 V) may also be modeled. In this work, a diode drop of 1.7 V is modeled, which was chosen to match the GaN transistor used in the experimental validation [20].

2) $R_{ds,off}$: Once the switches open, the drain-to-source leakage current can be modeled with an equivalent resistance, $R_{ds,off}$. While this resistance is typically large, it can still be an order of magnitude smaller than the leakage resistance of the

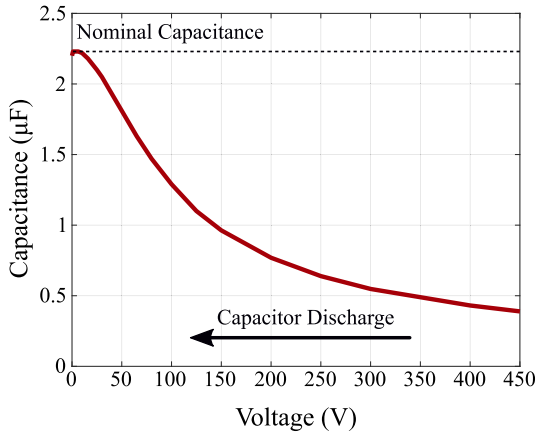

Fig. 2. Class II MLCC capacitance derating curve, as the capacitor discharges the capacitance will increase nonlinearly [21].

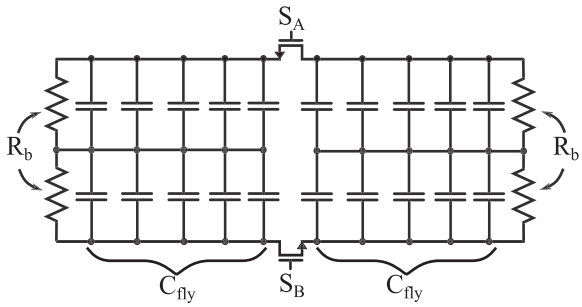

Fig. 3. Example flying capacitor implementation showing series stacked capacitors and balancing resistors, R_b, which serve to ensure uniform voltage distribution among capacitors.

flying capacitors and therefore, must be included when assessing parasitic discharge paths. In this work, it is assumed that all switches are implemented with the same device and therefore have the same $R_{ds,off}$ value. Furthermore, in this work the $R_{ds,off}$ value is estimated based on the drain-to-source leakage current reported on the manufacturer's datasheet [20].

3) C_{OSS}: Since each switching device's output capacitance, C_{OSS}, is small compared to to the flying capacitors, it has a negligible impact on shutdown dynamics. Specifically, as the time constants associated with the switch output capacitance is orders of magnitudes smaller than those associated with the flying capacitors, C_{OSS} may be safely neglected and is omitted from subsequent analysis.

B. Flying Capacitor Model

1) Capacitor Discharge: Upon entering shutdown, the flying capacitors will begin to discharge through both their internal leakage resistance and the leakage resistance of the switches. In the case where the flying capacitors are Class II MLCCs, the capacitance of the device will increase as the device discharges. An example capacitance derating curve for a Class II MLCC can be seen in Fig. 2. This creates a nonlinear function as the voltage of each flying capacitor decreases at a different rate depending on its operating voltage.

2) Leakage Resistance: Further complexity is added due to the leakage resistance which may vary between levels depending on the converter design. For the capacitor described in Fig. 2, the leakage resistance is listed as 227 MΩ on the datasheet [21]. However, this leakage resistance is not well documented and may change with operating conditions [22].

3) Balancing Resistors: In many FCML converter designs the flying capacitors are implemented with stacked MLCCs in series to increase the voltage handling capability [15], [23]. However, this introduces the possibility of unequal voltage sharing between series connected capacitors with variation in leakage resistance. To combat this uncertainty, matched balancing resistors, R_b, may be added as shown in Fig. 3. These balancing resistors decrease the effective leakage resistance to be approximately equal to R_b (assuming R_b is significantly smaller than R_{leak}) and thus, provide a well-defined voltage division between series connected capacitors. The introduction of R_b also acts to increase the discharge rate of the flying capacitors during shutdown. Here we define $R_{fly,i}$ to be the effective leakage resistance of the i^{th} flying capacitor, including the contribution of any balancing resistors.

C. Input and Output Capacitance

During nominal FCML converter operation the input and output capacitance (labelled C_{in} and C_{out} in Fig. 1) has a significant effect on capacitor balancing [24] and converter performance [25], [26], [27]. Therefore, in this work, it is assumed that these capacitance values are sized to be at least 10× the flying capacitors, as is common in practical designs. As these capacitors have much larger values than the flying capacitors they will discharge more slowly depending on associated leakage paths, potentially leading to switch overstress during shutdown.

III. General Shutdown Dynamics

Once shutdown is initiated, as shown in Fig. 1(b), the flying capacitors will begin to discharge through leakage paths. Additionally, the initial voltages stored on all capacitors, including C_{in} and C_{out}, will shape the discharge trajectory, implying that the converters conversion ratio prior to shutdown must be considered.

A. Impact of Conversion Ratio

When shutdown commences the voltage across each switch—labelled $V_{Si(A/B)}$ in Fig. 1(b)—is dictated by the voltage stored on both the input and output capacitors, which initially store V_{in} and V_{out}, respectively. Assuming that; all switches have the same leakage resistance $R_{ds,off}$, C_{OSS} is small (Section II-A3), and that all flying capacitors initially hold their nominal dc voltages when shutdown begins (neglect R_{fly}), it follows that the low-side switches will be subjected to an initial voltage stress of

$$V_{Si,B} = \frac{V_{in}}{N-1} \tag{1}$$

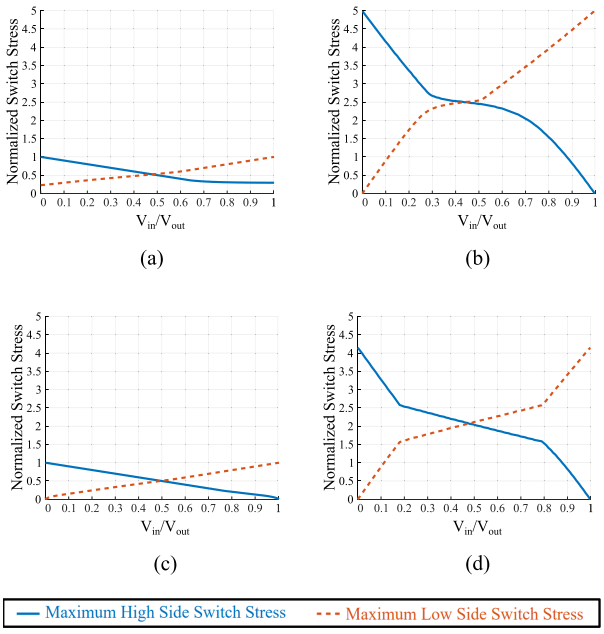

Fig. 4. Simulated switch stress during shutdown as a function of conversion ratio, normalized about the nominal steady-state blocking voltage. (a) Safe shutdown with $R_{ds,\text{off}}$ of each switch equal and with dominant impact on rate of discharge. (b) Increased switch stress observed for R_{fly} induced discharge where $C_{fly} \neq C_{\text{in/out}}$ results in mismatched RC time constants. (c) No increased switch stress is observed when RC time constants are well matched. (d) Unequal R_{fly} between cells, where R_b is implemented only for high-voltage cells.

where i is the index of the low-side switch, and the high-side switches will see

$$V_{Si,A} = \frac{V_{\text{out}} - V_{\text{in}}}{N-1}. \tag{2}$$

This results from each switch's $R_{ds,\text{off}}$ forming a resistor divider between V_{in} and ground, and V_{out} and V_{in} for low-side and high-side switches, respectively.

Considering (1) and (2), the ratio of input to output voltage will impact the initial condition of the switch voltages which will in turn affect which switches (if any) experience reverse conduction as shutdown progresses (addressed in Section III-E).

To better understand the effect of conversion ratio on capacitor discharge, a ten-level FCML converter was simulated in PLECS. In this simulation, the input and output capacitance was fixed at $10\times$ the flying capacitance. For each simulation the initial voltage on C_{in} was swept, while the initial voltage on C_{out} was kept constant. For each swept value, the maximum normalized switch voltage over the entire shutdown time was recorded, with low-side and high-side switches being recorded independently. The normalized value was found by dividing the maximum observed switch voltage by the nominal switch operating voltage, defined as $V_{\text{out}}/(N-1)$, and is helpful in showing how much the voltage increases during shutdown compared to nominal operation: in an ideal shutdown scenario the normalized switch stress would not exceed "1" (one).

The plots in Fig. 4 show the resulting normalized switch stress as a function of conversion ratio for a number of different conditions: To assess the impact of different leakage paths, the relative values of $R_{ds,\text{off}}$ and R_{fly} are varied in relation to both each other and proximal capacitive elements.

B. Dominant $R_{ds,off}$

In Fig. 4(a) the $R_{ds,\text{off}}$ of the switches was set to be 400 kΩ and the flying capacitor leakage resistance was set to be 227 MΩ, therefore indicating that switch leakage will be the dominant discharge path. Assuming that $R_{ds,\text{off}}$ is consistent across all switches, a uniform resistor divider string is formed and the capacitors will discharge at a uniform rate, without increasing the voltage stress across the switches. In this simulation, across all conversion ratios the normalized switch stress remains in a safe region, although we note that $R_{ds,\text{off}}$ is often poorly characterized and may change across devices and with voltage/temperature.

C. Dominant R_{fly}

Similarly, in Fig. 4(b), the switch resistance is increased to 4 GΩ, so that the primary discharge path for the flying capacitors will be either through their balancing resistors or their own intrinsic leakage resistance, defined collectively here as R_{fly}. The rate of discharge is determined by the capacitance value as well as R_{fly} (forming an RC time constant). If the effect of D_{body} is temporarily ignored, capacitor discharge can be described simply by

$$V_C = V_{C,init} e^{\frac{-t}{R_{fly} C_{fly}(V_C)}} \tag{3}$$

where shutdown commences at $t = 0$, $\text{V}_{C,\text{init}}$ is the initial flying capacitor voltage, R_{fly} is the effective discharge resistance defined by component leakage or balancing resistors, and C_{fly} may vary significantly with voltage (e.g., Fig. 2). In Fig. 4(b) R_{fly} is held equal across all capacitors, despite C_{in} and C_{out} being $10 \times C_{fly}$. As a result, adjacent capacitors experience differing RC time constants and will discharge at different rates thereby imposing increased (or decreased) voltage stress on neighboring switches.

Conversely, if RC time constants and the associated discharge rates of each capacitor is held equal, uniform discharge is again observed, leading to a safe shutdown without increased device stress. In Fig. 4(c) the input and output capacitors are still $10\times$ greater than the flying capacitors, but are modeled with $0.1\times$ the leakage resistance R_{fly}. As a result all the capacitors discharge at an equal rate with all switch voltages remaining at or below their nominal values.

D. Cautionary Use of Balancing Resistors

As described in Section II-B3, balancing resistors R_b are often used for high-voltage cells that construct flying capacitors using series connected low-voltage devices. This has the potential to significantly alter the effective R_{fly} seen between high-voltage and low-voltage cells, where R_b may not be included for low-voltage cells, absent of any series-connected capacitors. Without care, this may result in strongly mismatched RC discharge rates and in extreme cases lead to device overstress during shutdown. This situation is depicted in Fig. 4(d), where flying capacitors

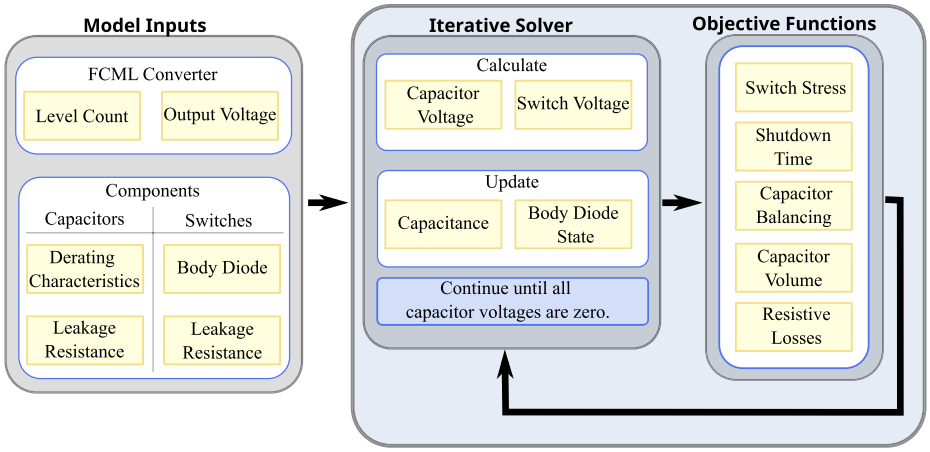

Fig. 5. Flowchart for iteratively solved MATLAB shutdown model.

C_{1-i} have $R_{fly} = 227\ M\Omega$, while capacitors $C_{(i+1)-N}$ are simulated with 2 $M\Omega$, where i is the number of low voltage cells which do not require balancing resistors, and N is the total number of levels. The resultant mismatch in RC time constants yields a voltage stress increase of over $2\times$ across all conversion ratios.

E. Effect of D_{body}

If the flying capacitors discharge nonuniformly, some switches will see a decreasing voltage stress that progresses at a faster rate than others. Subsequently, upon reaching 0 V, these switches will be subjected to a reverse bias and will begin to conduct through either their reverse body diode or as a result of $V_{GD} > V_{TH}$. Such an occurrence represents a nonlinear event in which the circuit dynamics are changed considerably: Once reverse conduction commences, associated flying capacitors form a lumped capacitance and discharge with a new RC time constant defined by the lumped capacitance and leakage resistances. This effect is captured in simulation and causes the nonlinearities observed in Fig. 4.

Additional effects such as reverse conduction voltage drop and resistance may be considered, but are assumed negligible at the voltage levels of interest.

F. Capacitor Derating

As described above, Class II MLCCs offer high energy density; however, they derate with voltage making the shutdown procedure more complicated to model. The PLECS generated results plotted in Fig. 4 include capacitor derating as shown in Fig. 2, although we note that the inclusion of capacitor derating does not significantly impact the maximum normalized switch stress.

IV. Model Description

As noted in the preceding sections, the dynamic behavior of the FCML converter involves both nonlinear passive elements, and switching circuit states due to diode turn-ON. While circuit simulations (e.g., SPICE or PLECS) can compute the behavior for a specific converter design under narrowly defined operating conditions, it becomes intractable to perform design optimization and investigation across full converter operating ranges using such an approach. To enable computationally efficient investigation and design optimization of the FCML converter at shutdown, an iterative MATLAB model for a wide range of FCML design choices was developed in this work. As described in Fig. 5, the model requires the FCML converter design parameters as inputs: The level count, the output voltage, and details of the switch and capacitor choices. Incorporating the effects discussed in Sections II and III, the model iteratively solves for capacitor discharge over time, updating the nonlinear capacitance and diode states using a specified time-step for each cycle. As a result, the switch stress and capacitor voltage limits during shutdown can be included in overall FCML design optimization, with shutdown time, balancing effects, volume, and losses accounted for. As shown in Fig. 4, the worst switch stress occurs when the input voltage equals 0 V or when the input voltage equals the output voltage. In either case the majority of the switch stress will be completely on either the high-side or low-side switches. This work focuses on the case where the input voltage is zero, however the analysis and mitigation techniques provided can be applied to other conversion ratios.

This model also allows designers to investigate alternative fault scenarios. The inputs to the model allow for flexibility, therefore specific faults such as investigating shutdown when a switch which has failed short (i.e., $R_{ds,off} = 0\ \Omega$) is simple within the existing framework. In the following sections this model is used to predict shutdown dynamics and is validated against a constructed hardware prototype.

V. Model Validation and Hardware Prototype

A. Experimental Prototype

For this work, a ten-level FCML converter with an output voltage of 750 V is considered. An annotated photograph of the hardware prototype can be seen in Fig. 6, with the input and output relays. The specifications and performance summary of the hardware prototype is shown in Table I. The nominal voltage

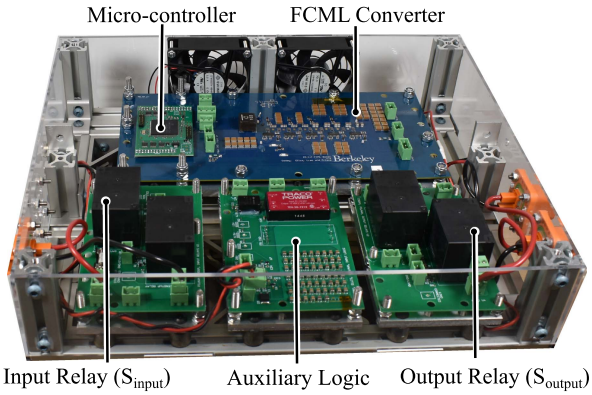

Fig. 6. Hardware prototype, showing FCML converter, input and output relays.

TABLE I
EXPERIMENTAL PROTOTYPE SPECIFICATIONS

Description	Value
Input voltage	100 – 700 V
Output voltage	750 V – 1 kV
f_{SW}	50 kHz
Effective frequency	450 kHz
Peak efficiency	99.52 %
Peak output power	2.5 kW
Specific power density	28.2 kW/kg
Volumetric power density	16.6 W/cm^3 (247 W/in^3)

TABLE II
FLYING CAPACITOR DESIGN SPECIFICATIONS

Flying Capacitor	Nominal Voltage	Nominal Capacitance	De-rated Capacitance	Series Capacitors	Parallel Resistance
C_{in}	550 V	33 μF	8.9 μF	Yes	2 MΩ
C_1	83 V	6.6 μF	3.96 μF	No	227 MΩ
C_2	167 V	6.6 μF	2.64 μF	No	227 MΩ
C_3	250 V	6.6 μF	1.98 μF	No	227 MΩ
C_4	333 V	6.6 μF	1.32 μF	No	227 MΩ
C_5	417 V	5.5 μF	1.65 μF	Yes	2 MΩ
C_6	500 V	5.5 μF	1.38 μF	Yes	2 MΩ
C_7	583 V	5.5 μF	1.20 μF	Yes	2 MΩ
C_8	667 V	5.5 μF	1.10 μF	Yes	2 MΩ
C_{out}	750 V	33 μF	6.9 μF	Yes	2 MΩ

and capacitance of each flying capacitor is shown in Table II. The derated capacitance is also shown, which is calculated based on the derating curve shown in Fig. 2. Furthermore, this converter is designed with 200 V GaNFETs (EPC2034 C), therefore it is vital that the switch stress remains below 200 V during shutdown.

B. Modeled Unsafe Shutdown

Shown in Fig. 7(a) are plots of flying capacitor and switch voltages over time for a shutdown procedure with the model parameters of Table II. Considering the prototype converter with no special consideration for shutdown, the model determines the capacitor discharge and worst case switch stress. During this shutdown the highest high-side switch ($S_{9\ A}$) experiences switch stress over 300 V, well above the rated device voltage, which would result in a device failure. The key contributor to the large switch stress is the output capacitor, which decays much slower than the flying capacitors due to its significantly larger capacitance. In addition to the required terminal voltage filtering, a sufficiently large output capacitor (in comparison to the flying capacitors) is also needed to ensure good capacitor voltage balancing during steady-state operation [24]. Thus, simply reducing the output capacitor to avoid this condition is not a feasible solution in a practical implementation. As shown in Fig. 8, this shutdown procedure was verified with hardware, to show the increased voltage stress across $S_{9\ A}$ after shutdown was initiated.

VI. SAFE SHUTDOWN TECHNIQUES

The model was used to test and validate several safe shutdown approaches. These shutdown procedures are designed with the following goals of safe shutdown.

1) Low switch stress: The switch stress should not exceed the voltage rating of the device during shutdown procedure. If the drain-to-source voltage of the switch exceeds the device rating, this in an unsafe shutdown condition as it may result is a device failure.
2) Short shutdown time: The shutdown time should remain short. If the system does not completely discharge before a subsequent start-up attempt, the capacitors may start-up nonuniformly, resulting in failure.
3) Low losses: Any additional circuitry added to the system should not incur significant losses during nominal operation.
4) Small footprint: The suggested shutdown circuitry should have a negligible impact on the overall converter volume/weight.

In the following sections, three different shutdown techniques are proposed. For each method the benefits and challenges are outlined, allowing designers to select the best technique for a specific application and constraints.

A. Normally Connected Resistive Load

The first proposed solution is to connect a resistive load during shutdown. This can be done with a normally-ON configured switch in place of S_{output}, as shown in Fig. 1(a), so that even with loss of logic power the resistive load remains connected to the output capacitance. This method effectively increases the discharge rate of the output capacitance. Fig. 7(b) shows modeled shutdown with the resistive load. With this method there is no overvoltage of the switches and the shutdown process occurs in approximately 120 ms, for the given load of 200 Ω. This shutdown procedure was verified with the experimental prototype at high voltage (750 V) and the flying capacitor voltages were measured. As shown in Fig. 9, the experimental results signify safe shutdown through uniform capacitor discharge. Note, the delay shown in Fig. 9 between the switching and input relay opening is due to the internal delay in the relay.

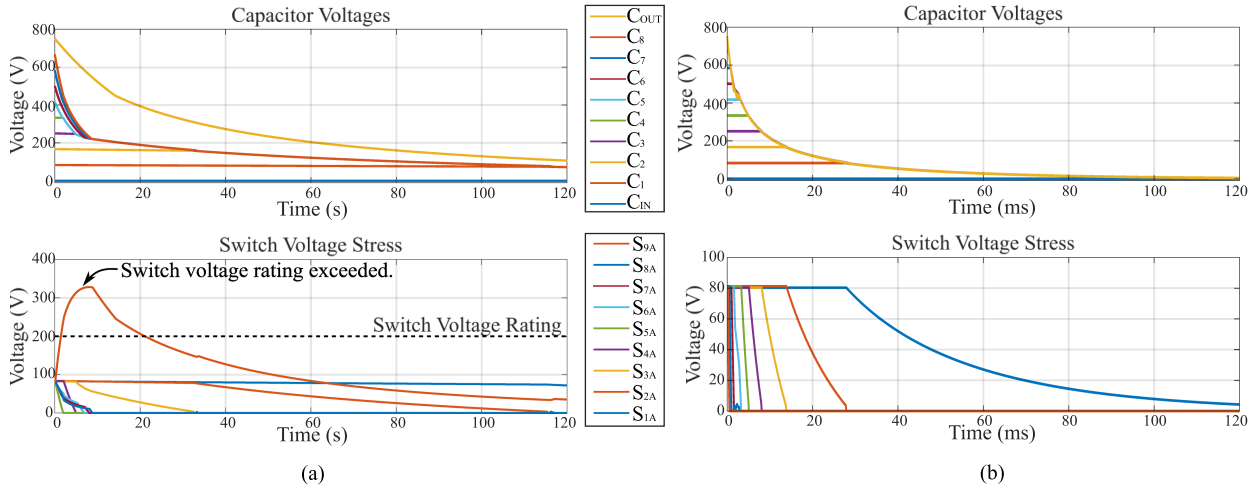

Fig. 7. (a) Modeled shutdown, where no safe shutdown techniques are implemented. The complete shutdown process takes over two minutes and the voltage rating of the switches is exceeded, resulting in an unsafe shutdown condition. (b) Modeled shutdown with resistive load. With this method complete shutdown occurs after 120 ms. All switch voltages remain under their rated voltages, therefore resulting in a safe shutdown condition.

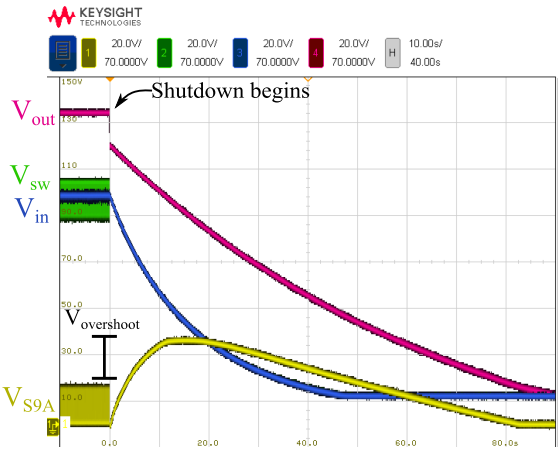

Fig. 8. Experimentally measured shutdown with no safe shutdown methods. The high side switch V_{S9A} shows increased voltage stress after the shutdown procedure begins.

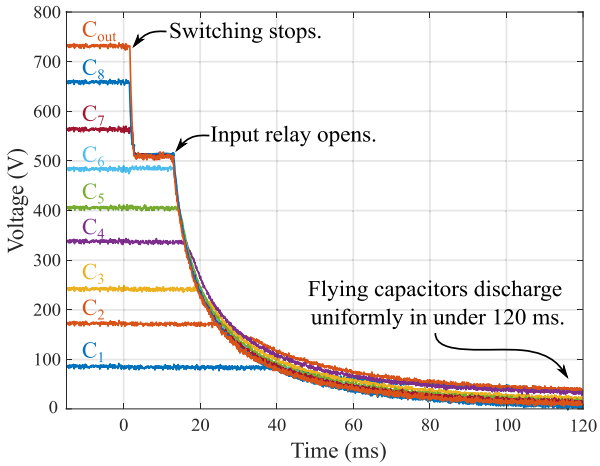

Fig. 9. Experimentally measured flying capacitor voltages during shutdown, with resistive load connected. Shutdown initiated from 750 V output steady-state operation.

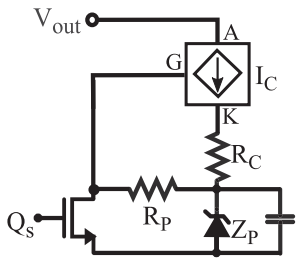

Fig. 10. Auxiliary shutdown circuit, utilizing a switchable current regulator (I_C).

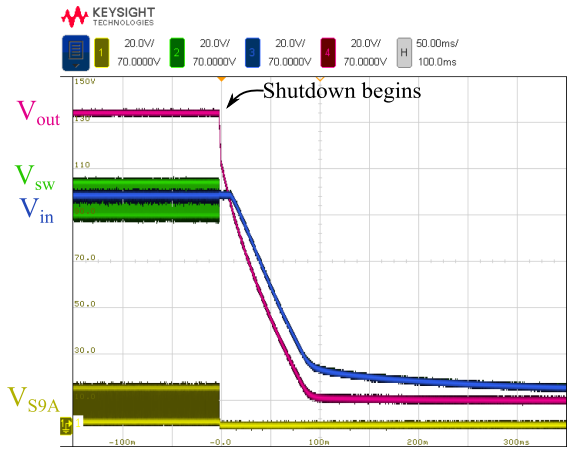

Fig. 11. Experimentally measured voltages during shutdown, while implementing the auxiliary shutdown circuit shown in Fig. 10. With this method no overshoot is observed.

While effective, it is not always feasible to keep the load connected during shutdown, which is a limitation of the suggested technique. For safety reasons it is often not desired to continue powering the load during a shutdown. Moreover, this method requires a primarily resistive load which also is dependent on system architecture. Therefore, the following sections present alternative methods which do not rely on a resistive load.

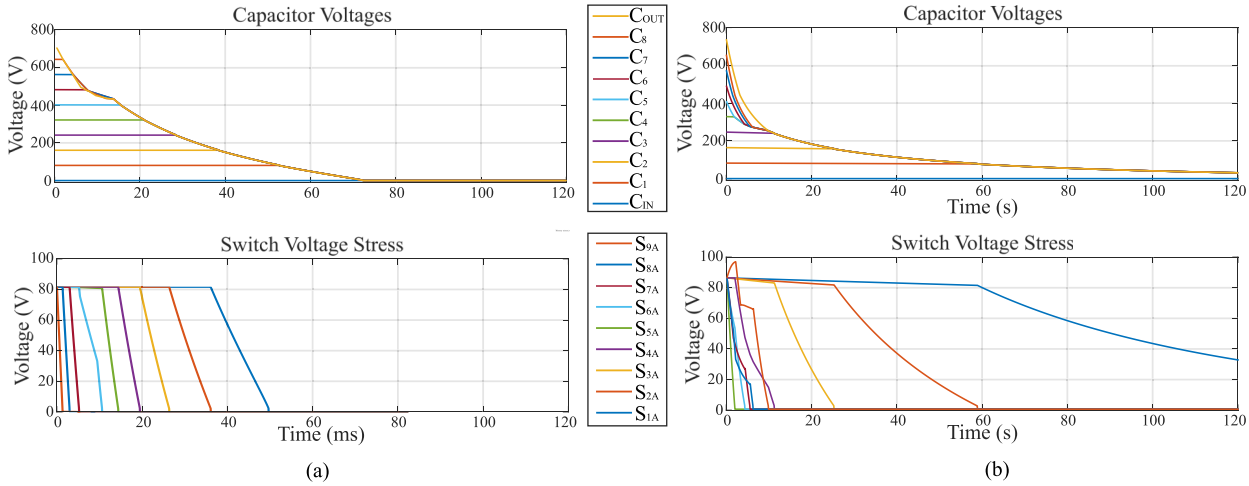

Fig. 12. (a) Modeled shutdown with auxiliary shutdown circuit. (b) Modeled shutdown with adjusted balancing resistor value to decrease voltage stress.

B. Auxiliary Shutdown Circuit

Fig. 10 shows a proposed auxiliary circuit which implements a switchable current regulator (I_C) [28]. This auxiliary circuit is similar to one proposed in [14] to aid in converter start-up. A normally high signal from the microcontroller, labeled Q_s keeps the current regulator OFF during nominal operation. Once shutdown occurs and Q_s transitions to 0 V, the current regulator turns ON and provides a discharge path for the output capacitance. The resistor, R_C sets the constant current, designed in this case to 100 mA.

The model was configured to account for this current regulating device, and the results are shown in Fig. 12(a). This method results in a shorter shutdown time than the previous method, and ensures no device overvoltage. This auxiliary shutdown circuit was built and tested with the hardware prototype. Fig. 11, shows the measured results, indicating no overshoot during shutdown. However, this auxiliary circuit does require added volume. For this prototype the auxiliary circuit was implemented in less than 0.4% of the total converter volume. It should also be noted that this auxiliary circuit does not consume any power during nominal operation and therefore, does not decrease the converter efficiency.

C. Adjustment of Balancing Resistors

As indicated by the proposed model, the selection of the balancing resistors has a significant impact on the discharge of the capacitors. To increase the discharge rate of the output capacitance the balancing resistor at the output can be decreased. For this example, the effective parallel resistance of the output capacitance was decreased to 1 MΩ. As shown in Fig. 12(b), this method results in a small amount of additional voltage stress on the switches, but is still well below their rated voltage. This technique of reducing the output capacitor balancing resistor was confirmed in hardware. As shown in Fig. 13, there is a small amount of overshoot observed, but well below the example shown in Fig. 8.

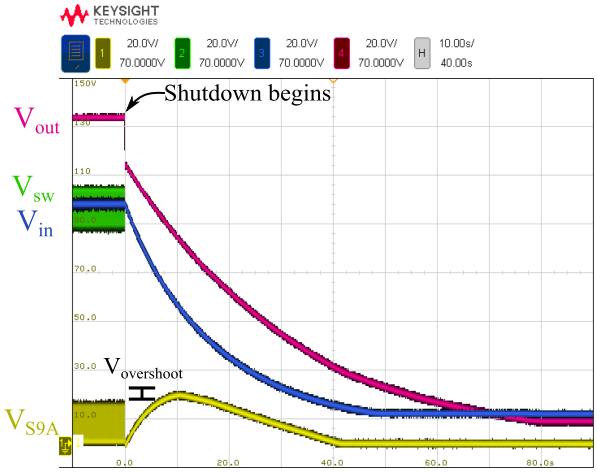

Fig. 13. Experimentally measured shutdown, with modified output capacitor balancing resistor. There is a small amount of overshoot measured with this method.

This method results in a negligible volume increase as the balancing resistors were already included in the design. However, this resistance does add to the overall converter losses. At 750 V output, these balancing resistors will dissipate 1.2 W. These additional losses are considered negligible at high power (2.5 kW for this prototype), but may be deemed significant at light load or idle operation. Fig. 14 shows this tradeoff between power dissipation and normalized switch stress in a plot where the output balancing resistance is adjusted. The power converter can thus select the appropriate tradeoff for a particular design, to meet the overall system objectives. With the chosen balancing resistor values, Fig. 13 demonstrates shutdown in approximately 80 s. This shutdown duration is significantly longer than shown with methods introduced in Sections IV-B and IV-C. Alternatively, the shutdown speed of this method could be shortened with the selection of a smaller balancing resistance. However, as highlighted in Fig. 14, selecting a smaller resistance also results in higher nominal power dissipation.

TABLE III
COMPARISON OF PROPOSED SHUTDOWN TECHNIQUES

Shutdown method	Section	Switch stress	Duration	Loss	Added volume
Resistive load	IV-A	$<$ nominal V_{DS}	120 ms	0 W	–
Auxiliary circuit	IV-B	$<$ nominal V_{DS}	80 ms	0 W	1 cm^3
Balancing resistors	IV-C	10% of nominal V_{DS}	80 s	1.2 W	–

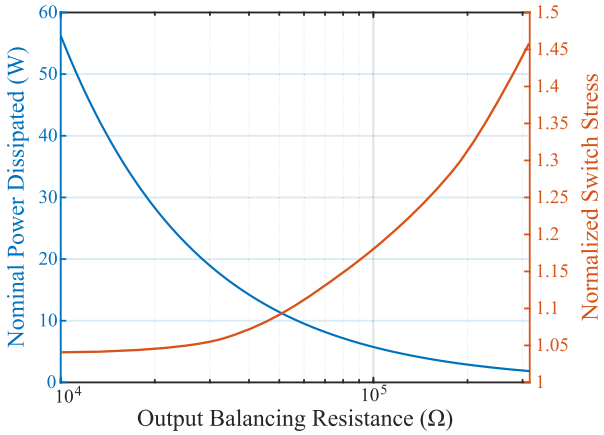

Fig. 14. Power dissipated in balancing resistors during nominal operation and normalized switch stress as a function of modified output resistance.

D. Comparison of Proposed Techniques

It should be noted that although the power converter itself was designed to achieve high power density, in this work startup and shutdown components were not weight or size optimized, but rather focused on demonstrating and exploring the various concepts. A summary of the proposed shutdown methods is shown in Table III, which highlights the added power loss and volume for the various shutdown techniques, as implemented. Note, this comparison is for the specific values tested with the presented experimental prototype and may vary for different converters. For this work, a nominally connected resistive load presents a safe, fast, and low loss shutdown method. However, this method may not be feasible in some applications, therefore motivating the use of the auxiliary circuit presented in Section IV-B. Finally, in a volume-limited application, adjustment of the balancing resistors ensures safe shutdown but with the consequence of additional losses.

VII. CONCLUSION

This work has demonstrated the need for safe shutdown techniques within the FCML converter. A framework for modeling the FCML converter during shutdown was introduced, which includes nonlinear component effects. Subsequently, this model may be used to design for safe shutdown dynamics with constrained device stresses. Experimental results verify safe shutdown with a resistive load. Furthermore, several additional techniques that also result in safe shutdown are modeled and evaluated, providing a framework by which optimal shutdown strategies can be selected for a given design.

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Samantha Coday (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering and mathematics from Southern Methodist University, TX, USA, in 2017, and the M.S. degree in electrical engineering and computer sciences, in 2019 from the University of California, Berkeley, CA, USA, where she is currently working toward the Ph.D. degree in electrical engineering.

Her research interests include hybrid switched-capacitor circuits focusing on the design and implementation of converters in harsh aerospace environments.

Ms. Coday is the recipient of the Outstanding Graduate Student Instructor Award at University of California, Berkeley, the Cadence Women in Technology Scholarship, and the ThinkSwiss Research Scholarship.

Nathan Miles Ellis (Member, IEEE) was born in Cork, Ireland. He received the B.S. degree in electrical and electronic engineering from the University College Cork, Ireland, in 2013, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Davis, CA, USA, in 2017 and 2020, respectively.

During this time he was funded in part by both Texas Instruments and the U.S. Department of Education in recognition of research excellence in areas of national need. He is currently a Postdoctoral Researcher with the Department of Electrical Engineering and Computer Sciences, the University of California, Berkeley. His research interests include mixed signal integrated circuit design, energy harvesting, renewable energy integration, biomedical devices, and spans several topics in high performance power converter design, including; hybridized switched-capacitor power converters, multilevel converters, and adiabatic gate-drives.

Dr. Ellis was the co-recipient of an IEEE Best Paper Award. He was named Best Graduate Researcher by UC Davis' Industrial Affiliates in 2017, before receiving the title of Analog Devices Outstanding Student Designer at the International Solid-State Circuits Conference (ISSCC) in 2020.

Robert Carl Nikolai Pilawa-Podgurski (Fellow, IEEE) was born in Hedemora, Sweden. He received the dual B.S. degrees in physics and electrical engineering and computer science, the M.Eng. degree in electrical engineering and computer science, and the Ph.D. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005, 2007, and 2012, respectively.

He is currently a Professor with Electrical Engineering and Computer Sciences Department, University of California, Berkeley, Berkeley, CA, USA. He was an Associate Professor of electrical and computer engineering with the University of Illinois Urbana-Champaign, Champaign, IL, USA. His research interests include power electronics, renewable energy applications, electric vehicles, CMOS power management, high density and high efficiency power converters, datacenter power delivery, and advanced control of power converters.

Dr. Pilawa-Podgurski was the Student Activities Chair for IEEE Energy Conversion Congress and Exposition 2016 and 2017 and the Technical Co-Chair for the 4th IEEE Workshop on Wide Bandgap Power Devices and Applications in 2016. From 2014 to 2022, he was the PELS Technical Committee 6—Emerging Power Electronics Technologies as Awards Chair, Secretary, Vice Chair, and Chair. From 2016 to 2019, he was the Chair of PELS Technical Committee 2 Power Conversion Systems and Components. From 2014 to 2019, he was an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. From 2018 to 2023, he was a Member of the IEEE ISSCC Power Management Committee. He was the recipient of the Chorafas Award for outstanding MIT EECS Master's thesis, the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35, the Air Force Office of Scientific Research Young Investigator Award in 2015, the UIUC Dean's Award for Excellence in Research in 2016, the UIUC Campus Distinguished Promotion Award in 2017, the UIUC ECE Ronald W. Pratt Faculty Outstanding Teaching Award in 2017, the IEEE Education Society Mac E. Van Valkenburg Award given for outstanding contributions to teaching unusually early in his career in 2018, and the UC Berkeley EECS Department Electrical Engineering Outstanding Teaching Award in 2023. He is the coauthor of 15 IEEE prize papers.