Letters

Minimizing Output Capacitance Loss in GaN Power HEMT

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***Abstract*—Output capacitance (C_{OSS}) loss (E_{DISS}) is produced when the C_{OSS} of a power device undergoes a cycle of charging and discharging, which ideally should be a lossless process. This nonideal phenomenon has been recently revealed to be a critical loss for wide-bandgap devices in high-frequency, soft-switching applications. Despite many studies on its characterizations and physical origins, the reduction of E_{DISS}, particularly through an approach applicable to circuit application instead of relying on physical device design, has seldom been reported. In this article, we found that the E_{DISS} of GaN-on-Si high electron mobility transistors (HEMTs) can be significantly reduced by tuning the bias of Si substrate (V_{Sub}) in dynamic switching. By connecting the substrate to the source or drain via the selected capacitance, V_{Sub} can be modulated to dynamically follow either the drain-to-source bias (V_{DS}) or a particular portion of V_{DS} in switching. Characterizations of a 650 V GaN HEMT with different substrate connections reveal that its E_{DISS} maximizes at $V_{Sub} = V_{DS}$ and minimizes at $V_{Sub} = 0.5V_{DS}$. Compared to the conventional substrate-to-source shorted connection, the E_{DISS} at $V_{Sub} = 0.5V_{DS}$ is reduced by up to 86%, and the ratio between E_{DISS} and the stored energy in C_{OSS} can be reduced from 14.6% to 2.2%. These results unveil a new, easy-to-implement approach to minimize the inherent C_{OSS} loss of GaN HEMTs in practical applications.**

***Index Terms*—Gallium nitride (GaN), high electron mobility transistor, high frequency, output capacitance loss, power semiconductor device, soft switching, substrate.**

I. Introduction

Wide bandgap gallium nitride (GaN) high electron mobility transistors (HEMTs) are gaining increased adoption in applications like mobile electronics and data centers. Benefitting from the high channel mobility and the high breakdown field of GaN, GaN power HEMTs enable low specific ON-resistance and small capacitance and thus become attractive for high-frequency applications [1]. In addition, most commercial GaN power HEMTs are fabricated on Si substrates up to 8 inches, allowing for a remarkable cost advantage [2]. However, a by-product of the low-cost GaN-on-Si wafer (and conductive Si substrate) is the high voltage drop and high electric field (E-field) in the GaN buffer layers and transition layers sandwiched between the GaN channel and Si substrate. To boost the vertical blocking capability and minimize the leakage current, the GaN buffer layer is usually doped with carbon or iron, which can introduce complex carrier traps [3]. This can further lead to the dynamic shifts of various parameters in GaN-on-Si HEMTs, such as the dynamic ON-resistance, breakdown voltage (BV), and threshold voltage [4], [5].

Another issue that originates from parametric instability is the dynamic output capacitance (C_{OSS}) loss (E_{DISS}). E_{DISS} is the loss generated when the device's C_{OSS} is charged and discharged, which ideally should be a lossless process [4]. After its first report in GaN HEMTs [6], it has been widely observed in a variety of GaN devices with different structures [7], [8], [9], [10], as well as in SiC devices [8], [11], [12]. From the application standpoint, E_{DISS} could become a significant loss in high-frequency, soft-switching applications [6], [8].

Prior studies on E_{DISS} center around its measurement and physical mechanisms. A few methods have been proven to be effective for E_{DISS} characterization, including Sawyer-Tower circuit [6], calorimetric method [7], nonlinear resonance [13], and unclamped-inductive-switching (UIS) circuit [9]. These methods unanimously reveal the fast increase of E_{DISS} with the peak drain-to-source voltage (V_{DS}), and E_{DISS} can reach over 15–20% of the stored energy in C_{OSS} (E_{OSS}) [4]. The other consensus has arrived that the E_{DISS} of GaN HEMTs is mainly due to the charge (de-)trapping [9], [14], although the specific location and origin of the relevant traps are still under debate.

Despite these studies, practical approaches to minimize E_{DISS} have seldom been reported. Guacci et al. [7] reported a reduction of E_{DISS} through optimizing the doping, thickness, and composition of the buffer layer, while the detailed designs are not disclosed. Zhuang et al. [15] reported a 30% lower E_{DISS} by applying a negative substrate bias (V_{Sub}), which reduces E_{OSS}, but the E_{DISS}/E_{OSS} ratio remains nearly the same or becomes even higher. This negative V_{Sub} was used in [15] primarily to probe the E_{DISS} origins; it could face difficulties being implemented in applications as it will increase the drain-to-substrate voltage drop and degrade the device BV.

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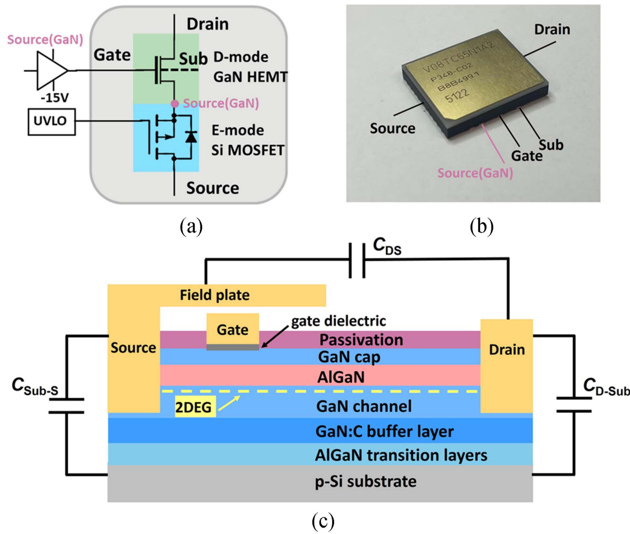

Fig. 1. (a) Schematic of D^3GaN. (b) A photo of D^3GaN in a surface mount package with controllable substrate bias. (c) Schematic of the D-mode GaN HEMT with the illustration of major components of C_{OSS}.

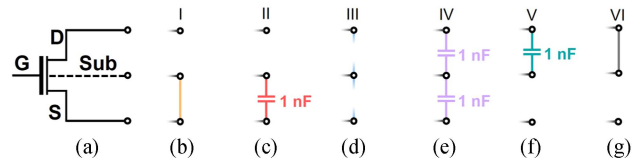

Fig. 2. Schematics of (a) device terminals, (b) Scheme I with source shorted to substrate. (c) Scheme II with 1-nF capacitor connected between source and substrate. (d) Scheme III with substrate floating. (e) Scheme IV with two 1-nF capacitors. (f) Scheme V with 1-nF connected between substrate and drain. (g) Scheme IV with substrate shorted to drain.

In this article, we report, for the first time, that E_{DISS} can be effectively suppressed by applying a dynamic, positive V_{Sub} that follows the switching V_{DS} with a certain ratio. Compared to the constant negative V_{Sub} used in [15], the V_{Sub} in this article is not only positive, which does not degrade BV, but also dynamically varying to follow V_{DS} in the entire switching process. Based on this finding, a new, effective, easy-to-implement method is proposed to modulate the dynamic V_{Sub} by connecting external capacitors between the substrate and source/drain. At $V_{Sub} = 0.5V_{DS}$, the E_{DISS} of a 650 V, 8mΩ GaN HEMT is trimmed by over six times, and the E_{DISS}/E_{OSS} ratio is reduced from 14.6% to 2.2%. The physical mechanism is unveiled through physics-based simulations. The impact of substrate connections on dynamic ON-resistance (R_{ON}) is also characterized.

II. DUT and Test Method

The device under test (DUT) is a 650V, 8mΩ depletion-mode (D-mode) GaN HEMT used in the direct-drive D-mode GaN device (D^3GaN) from VisIC Technologies [16]. The schematic and photo of the D^3GaN device are shown in Fig. 1(a) and (b), respectively. The working principle and characteristics of the D^3GaN device are elaborated in [17] and [18]. To measure the intrinsic E_{DISS} of GaN HEMT, in this article, we short the Si MOSFET in the D^3GaN device, and directly drive the gate of the D-mode GaN HEMT. Fig. 1(c) shows the DUT schematic. Major components of the DUT's C_{OSS} include the drain-to-source capacitance (C_{DS}), drain-to-substrate capacitance ($C_{D\text{-Sub}}$), and substrate-to-source capacitance ($C_{\text{Sub-}S}$). The gate-to-drain capacitance (C_{GD}) is minimal in GaN power HEMT and has a marginal contribution to C_{OSS}. If the Si substrate is floating, the V_{Sub} under dynamic switching is determined by the capacitor network, i.e., the relative magnitude of $C_{D\text{-Sub}}$ and $C_{\text{Sub-}S}$.

To tune the dynamic V_{Sub}, the effective $C_{D\text{-Sub}}$ or $C_{\text{Sub-}S}$ can be modulated by paralleling an external capacitor between the drain and substrate or the source and substrate, respectively, as shown in Fig. 2(a). Fig. 2(b)–(g) demonstrates six schemes of substrate termination investigated in this article. Scheme I shorts the substrate to the source, which is the conventional connection that many device vendors adopt. Scheme II alters the effective $C_{\text{Sub-}S}$ by adding a 1-nF capacitor between the substrate and source. Scheme III keeps the substrate floating. Scheme IV changes the effective $C_{D\text{-Sub}}$ and $C_{\text{Sub-}S}$ by adding two 1-nF capacitors, one connected between substrate and source and the other between substrate and drain. Scheme V alters the effective $C_{D\text{-Sub}}$ by adding a 1-nF capacitor between the substrate and drain. Scheme VI shorts the substrate to drain. All the 1-nF capacitors are implemented by the low serial resistance (ESR) C0G multilayer ceramic capacitors.

Here the external capacitors under scheme II and scheme V are selected to enable a V_{Sub}/V_{DS} ratio of 1/4 and 3/4, respectively, during the dynamic switching. When the substrate is floating in scheme III, the V_{Sub}/V_{DS} ratio depends on the physical device structure and could be device-specific. Such ratio is found to be 1/2 for the DUT characterized in this article. Scheme IV presents a general method to set a V_{Sub}/V_{DS} ratio of 1/2 by connecting two identical capacitors in parallel with $C_{D\text{-Sub}}$ and $C_{\text{Sub-}S}$, and selecting their capacitance to be considerably larger than $C_{D\text{-Sub}}$ and $C_{\text{Sub-}S}$. Here we use the same two capacitors in schemes II and V as they meet such requirement and can also eliminate the possible errors in E_{DISS} measurement due to the use of different capacitors in various schemes. The detailed measurements of V_{Sub}/V_{DS} ratio under different schemes will be presented in Section III.

Fig. 3 shows the I–V and C–V characteristics of the same DUT under six substrate connection schemes, measured on a curve tracer (Keysight B1505 Power Device Analyzer). The schemes I–III introduce very small differences in device characteristics, e.g., $<4\%$ shift in ON-resistance, 0.3 V shift in threshold voltage, and 11% shift in E_{OSS}. The scheme IV results in the same I–V characteristics as scheme III, suggesting the same V_{Sub} under two conditions. Despite such identical V_{Sub}, adding two 1-nF capacitors increases the C_{OSS} and E_{OSS}. Schemes V and VI result in shifts in both I–V and C–V characteristics; compared to scheme I, Scheme VI nearly doubles the E_{OSS} at 600 V.

In this article, we utilize an UIS test to characterize E_{DISS}. The test principle, setup, and calibration have been elaborated in [9] and [10]. As shown in Fig. 4(a), the UIS circuit consists of a power supply in series with a load inductor (L_{load}) and the DUT. Benefitted from the capability to produce fast, high-voltage resonance under a small bus voltage (V_{bus}), the

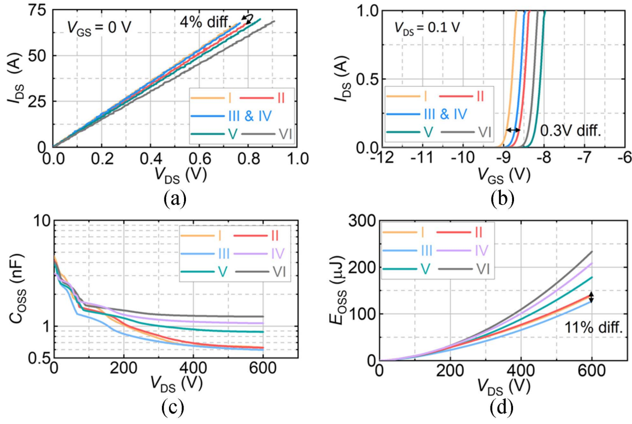

Fig. 3. (a) Output characteristics. (b) Transfer characteristics. (c) C_{OSS}-V_{DS}, and (d) E_{OSS}-V_{DS} of the DUT with substrate connection schemes I–VI.

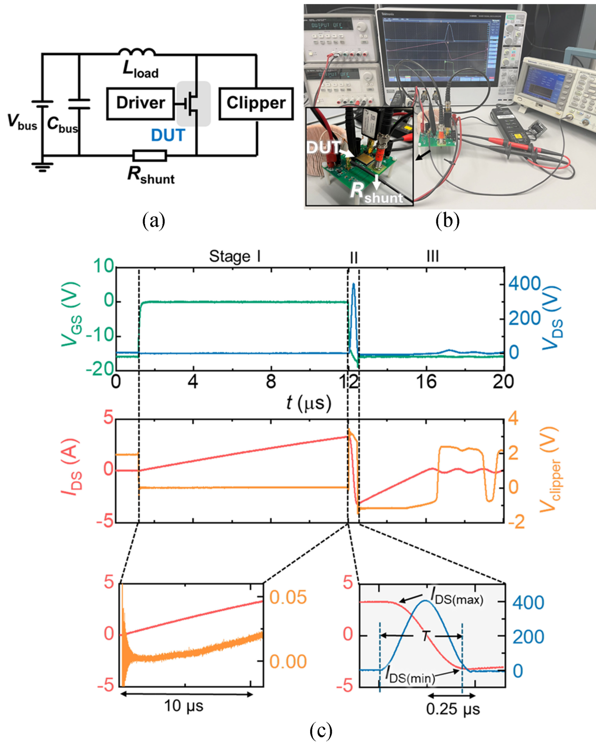

Fig. 4. (a) Schematic of a UIS circuit setup with a voltage clipper for the in-situ dynamic R_{ON} measurement. (b) Photograph of the prototyped test setup. (c) Typical UIS waveform and zoom-in waveforms in stages I and II. The dynamic R_{ON} and E_{DISS} are extracted in stages I and II, respectively.

UIS test could minimize the DUT's turn-OFF loss, facilitating the accurate extraction of E_{DISS}. Fig. 4(b) shows a test setup photo. A commercial screw-in co-axial shunt resistor with 0.1 Ω resistance (R_{shunt}) measures the DUT's drain-to-source current (I_{DS}) with a marginal insertion inductance. The DUT's V_{DS} and V_{Sub} are measured by two Tektronix THDP0200 high-voltage differential probes, and its gate-to-source voltage (V_{GS}) is measured by a Tektronix TDP1000 low-voltage differential probe. The UIS testing waveform was captured by a Tektronix MSO54 oscilloscope with up to 2 GHz analog bandwidth and 12-bit ADC for high horizontal and vertical resolutions. A very low V_{bus} of 5 V is used.

As previous reports revealed the impact of V_{Sub} on dynamic R_{ON} in GaN-on-Si HEMTs [19], [20], [21], we also measure the dynamic R_{ON} of the DUT under different substrate connection schemes. Similar to [22], a voltage clipper (CLP1500V15A1) is added to the UIS setup to characterize the dynamic R_{ON} during the in situ operation of the steady-state switching. This clipper can measure the DUT's ON-state voltage, $V_{clipper}$, for dynamic R_{ON} extraction. Such in situ measurement allows the extraction of E_{DISS} and dynamic R_{ON} from the same UIS cycle when the DUT is in the OFF-state and ON-state, respectively. This integrated measurements enables the in-situ evaluation of the substrate termination's impacts on the DUT's conduction and switching losses.

Fig. 4(c) shows a typical UIS waveform of the DUT, which involves three stages. In stage I, the DUT is turned ON, and V_{bus} charges L_{load}; in stage II, the DUT is turned OFF, and L_{load} resonates with the DUT's C_{OSS} for approximately a half cycle, which imitates the DUT's operation in resonant converters; in stage III, the DUT turns ON reversely, and L_{load} is discharged. The E_{DISS} extraction mainly relies on the UIS waveforms in stage II. A zoomed-in view of the stage I and II waveforms is also shown in Fig. 4(c), which is relevant to the dynamic R_{ON} and E_{DISS} measurements, respectively.

In the stage II waveform, the total loss (E_{total}) in this half resonance cycle can be calculated from the peak and valley values of the DUT's I_{DS}, denoted as $I_{DS(max)}$ and $I_{DS(min)}$, respectively. To obtain the DUT's E_{DISS}, the winding loss of L_{load} (E_{ind}) and the conduction loss of other parasitic components (E_{other}) are then subtracted from E_{total}. Here, E_{other} includes the losses incurred on R_{shunt} and the PCB board. The E_{DISS} is given by

$$E_{DISS} = E_{total} - E_{ind} - E_{other}$$
$$= \frac{1}{2} L \left(I^2_{DS(max)} - I^2_{DS(min)} \right) - \frac{1}{4} I^2_{DS(max)} (R_L + R_{other}) T \quad (1)$$

where L is L_{load}'s inductance, which is 15 μH in this article and R_L and R_{other} are the L_{load}'s ESR and the total ESR of the shunt and PCB parasitics, respectively. T is the period of a half-cycle resonance, which is modulated to be ∼0.5 μs in the tests for different substrate connection schemes, corresponding to a resonance frequency (f_R) of ∼1 MHz. L, $R_{L,}$ and R_{OTHER} are measured using an E4990A impendence analyzer at the f_R of the stage II resonance. By adopting the Litz-wire air core inductor and optimizing the PCB power loop, E_{ind} and E_{other} are trimmed to be marginal, i.e., as low as 6% of E_{total} [9]. Repeatable tests reveal an error as minimal as ±3% in the E_{DISS} extraction [9].

III. Measurement Results

In addition to E_{DISS} measurement, the UIS test provides a natural tool to measure the dynamic V_{Sub} in the same switching condition of E_{DISS} extraction. Fig. 5(a) shows the UIS waveforms for different substrate connection schemes under the peak resonance V_{DS} ($V_{DS(peak)}$) of 400 V. Under each scheme, V_{Sub} can dynamically follow V_{DS} with the same f_R of ∼1 MHz and a constant ratio of V_{DS}, validating the V_{Sub} modulation in

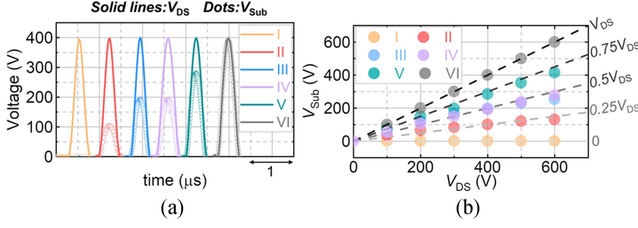

Fig. 5. UIS waveforms of the DUT with substrate schemes I–VI at $V_{\mathrm{DS(peak)}}$ of 400 V. (b) V_{Sub} as a function of $V_{\mathrm{DS(peak)}}$ for schemes I–VI.

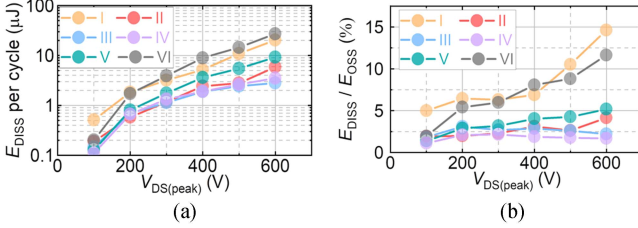

Fig. 6. Comparison of (a) E_{DISS} and (b) the $E_{\mathrm{DISS}}/E_{\mathrm{OSS}}$ ratio of the DUT substrate schemes I–VI as functions of $V_{\mathrm{DS(peak)}}$.

switching transients. By tuning the DUT ON-time in phase I, the $V_{\mathrm{DS(peak)}}$ can be changed under the same f_{R}. Fig. 5(b) shows the recorded peak V_{Sub} ($V_{\mathrm{Sub(peak)}}$) as a function of $V_{\mathrm{DS(peak)}}$ for all substrate connection schemes. Schemes II, III, IV, and V enable a $V_{\mathrm{Sub}}/V_{\mathrm{DS}}$ ratio of 1/4, 1/2, 1/2, and 3/4 under switching conditions, respectively.

After the dynamic V_{Sub} measurement, E_{DISS} is measured under the same UIS setup to ensure the identical V_{Sub} condition. To avoid the possible influence of the parasitics in voltage probes on the current measurement, all voltage probes are disconnected, only leaving the shunt resistor for current measurement.

Fig. 6(a) shows the measured E_{DISS} of the same DUT as a function of $V_{\mathrm{DS(peak)}}$ for different $V_{\mathrm{Sub}}/V_{\mathrm{DS}}$ ratios. Under all ratios, E_{DISS} increases with $V_{\mathrm{DS(peak)}}$ roughly following a power law, which is consistent with prior reports for devices under scheme I [6], [9]. Compared to scheme I ($V_{\mathrm{Sub}} = 0$ V), E_{DISS} of our DUT decreases at $V_{\mathrm{Sub}}/V_{\mathrm{DS}}$ ratios of 1/4 (scheme II), 1/2 (schemes III and IV) and 3/4 (scheme V), with the lowest E_{DISS} observed at $V_{\mathrm{Sub}} = 0.5V_{\mathrm{DS}}$, and E_{DISS} increases at $V_{\mathrm{Sub}} = V_{\mathrm{DS}}$. At $V_{\mathrm{DS(peak)}}$ of 600 V, E_{DISS} is reduced from 20.4 μJ under $V_{\mathrm{Sub}} = 0$ V to 2.8 μJ under $V_{\mathrm{Sub}} = 0.5V_{\mathrm{DS}}$.

To probe if the E_{DISS} reduction is due to the minimization of hysteresis loss or the E_{OSS} reduction, the $E_{\mathrm{DISS}}/E_{\mathrm{OSS}}$ ratio is plotted as a function of $V_{\mathrm{DS(peak)}}$ for different $V_{\mathrm{Sub}}/V_{\mathrm{DS}}$ ratios, as shown in Fig. 6(b). At $V_{\mathrm{DS(peak)}} = 600$ V, the $E_{\mathrm{DISS}}/E_{\mathrm{OSS}}$ ratio for the conventional scheme I is about 15%, similar to that reported in various GaN devices [4]. Such a ratio is significantly reduced to below 5% for the $V_{\mathrm{Sub}}/V_{\mathrm{DS}}$ ratios of 1/4, 1/2, and 3/4. In particular, at $V_{\mathrm{Sub}} = 0.5V_{\mathrm{DS}}$, the $E_{\mathrm{DISS}}/E_{\mathrm{OSS}}$ ratio is only ~2.2% and nearly independent of $V_{\mathrm{DS(peak)}}$. Note that schemes III and IV have nearly identical V_{Sub} and E_{DISS}, suggesting: the dynamic V_{Sub} is about $0.5V_{\mathrm{DS(peak)}}$ when the substrate is floating; and the DUT's E_{DISS} is primarily impacted by V_{Sub}. Scheme IV has a lower $E_{\mathrm{DISS}}/E_{\mathrm{OSS}}$ ratio due to its higher E_{OSS}.

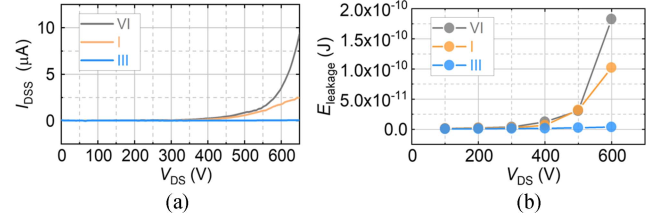

Fig. 7. (a) I_{DSS} as a function of V_{DS} of the DUT with the substrate connected to drain (scheme VI), connected to source (scheme I), and being floating (scheme III). (b) Calculated E_{leakage} as a function of V_{DS} for three substrate connection schemes.

Overall, these results suggest an up to 86% reduction in the intrinsic hysteresis loss at $V_{\mathrm{Sub}} = 0.5V_{\mathrm{DS}}$.

IV. Physical Mechanism

Previous research has revealed that the resistive loss in the device structure [7], [23], [24] and the trap-related loss in the GaN layers [14], [25] could both attribute to E_{DISS} of GaN HEMTs, and these mechanisms can both be impacted by V_{Sub}.

The resistive loss in device structure is first examined. Such loss can be induced by the capacitive (i.e., displacement) current flowing through the resistive device structure (e.g., Si substrate) or by the intrinsic leakage current. The former mechanism cannot explain the observed V_{Sub} impact on the measured E_{DISS}. For example, the C_{OSS} in scheme IV is higher than scheme I, suggesting a larger capacitive current under the similar volage slew rate. However, the E_{DISS} in scheme IV is much lower than scheme I.

To evaluate the impact of V_{Sub} on the DUT's intrinsic leakage current (I_{DSS}), the I_{DSS}-V_{DS} characterisitics are measured under schemes I, III, and VI on the curve tracer, as shown in Fig. 7(a). Note that, under scheme III, V_{Sub} in this dc test is between 0 and V_{DS} but may be different from the V_{Sub} in the ac switching test. The I_{DSS} in these three schemes starts to differ considerably when V_{DS} is higher than ~300 V. Scheme III shows the lowest I_{DSS} due to the reduced voltage drop and vertical E-field in the buffer layer. Buiding on such I_{DSS}-V_{DS} characterisitics, the resistive leakage loss (E_{leakage}) during the UIS test is then estimated by

$$E_{\mathrm{leakage}} = \int_0^T V_{\mathrm{DS}} I_{\mathrm{DSS}} \left(V_{\mathrm{DS}}\right) dt \quad (2)$$

where V_{DS} is extracted from the UIS waveform. Fig. 7(b) shows the calculated E_{leakage} under three substrate connection schemes. E_{leakage} in scheme III is lower than that in schemes I and II. However, E_{leakage} in all these schemes are orders of magnitude lower than the E_{DISS}, suggesting that the resistive loss is not a major cause of E_{DISS}.

Thus, the E_{DISS} reduction by modulating V_{Sub} is believed to be mainly related to the trapping behavior in the device structure. A physics-based TCAD simulation is performed to understand the underlying physical mechanism. The device models are based on those calibrated in [26] with a 1.5 × 10^{16} cm^{-3} deep-level acceptor trap added in the GaN buffer layer to account for the effect of carbon doping [5]. According to

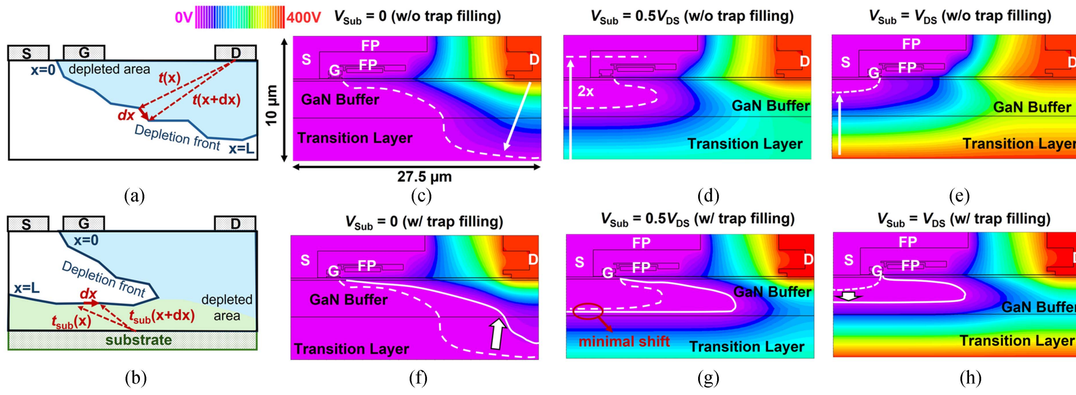

Fig. 8. Illustrations of calculating the depletion capacitance for an arbitrary depletion region when the substrate is connected to (a) source and (b) drain. The blue and green areas in (b) represent the depletion regions primarily induced by the drain bias and the substrate bias, respectively. The simulated potential contours at V_{Sub} of (c) 0 V, (d) $0.5V_{\mathrm{DS}}$, and (e) V_{DS}, all without the acceptor trap filling, as well as at V_{Sub} of (f) 0 V, (g) $0.5V_{\mathrm{DS}}$, and (h) V_{DS}, all with the filled acceptor trap. In (c)-(e), the dashed curves present the depletion front, and the line arrows point to the region with the shortest depletion depth. In (f)–(h), the dashed curves and solid curves show the depletion fronts before and after the acceptor trap filling, respectively. The white arrow shows the shifts of the depletion front closest to the drain or substrate. V_{DS} is 400 V in (c)–(h).

[9], [14], the E_{DISS} in GaN HEMTs can be explained by the distinct trapping states of the fast, shallow acceptor trap during the C_{OSS} charging and discharging, which results in the C_{OSS} shift. Thus, a 1.5×10^{16} cm^{-3} shallow acceptor trap is added to the GaN buffer layer, and we simulate the electrostatic potential contours when this trap is filled and un-filled to visualize the shift in depletion boundaries. As the C_{OSS} of GaN HEMTs is dominated by the depletion capacitance in the device structure, the shift in depletion boundaries corresponds to the C_{OSS} change [14].

To further scrutinize this correlation, Fig. 8(a) shows an arbitrary depletion region at a certain V_{DS} when the substrate is shorted to the source. As the local specific capacitance equals to the permittivity (ε) over the local depletion depth ($t(x)$), the total depletion capacitance can be derived by integrating the specific capacitance along the depletion front

$$C = \varepsilon W \int_0^L \frac{dx}{t\,(x)} \tag{3}$$

where W is the device width (normal to the cross section) and L is the length of the depletion front. This equation suggests that the major contribution of C_{OSS} comes from the region with the smallest $t(x)$, where the depletion front is closest to the drain.

When V_{Sub} dynamically follows a certain ratio of $V_{\mathrm{DS},}$ i.e., βV_{DS}, the substrate serves as an extension of the drain. Hence, the substrate-associated depletion capacitance also contributes to C_{OSS}. As shown in Fig. 8(b), The substrate-associated C_{OSS} ($C_{\mathrm{OSS}}^{\mathrm{Sub}}$) can be written as

$$C_{\mathrm{OSS}}^{\mathrm{Sub}} = \frac{dQ}{dV_{\mathrm{Sub}}}\frac{dV_{\mathrm{Sub}}}{dV_{\mathrm{DS}}} = \varepsilon W \int_0^{L_{\mathrm{Sub}}} \frac{dx}{t_{\mathrm{Sub}}\,(x)\,/\beta} \tag{4}$$

where Q is the substrate-associated depletion charge, $t_{\mathrm{Sub}}(x)$ is the local depletion depth with respect to the substrate, and L_{Sub} is the total length of the substrate-associated depletion front. Equation (4) suggests that, when converting the substrate-associated depletion capacitance into C_{OSS}, the physical depletion depth $t_{\mathrm{Sub}}(x)$ needs to be scaled by $1/\beta$.

Fig. 8(c)–(e) shows the simulated potential contours at $V_{\mathrm{DS}} =$ 400 V for V_{Sub} of 0 V, $0.5V_{\mathrm{DS}}$ and V_{DS}, respectively, all without the filling of acceptor traps. The depletion front is extracted from the zero potential contour and plotted in the dashed curves. The depletion front closet to the drain or the drain-connected substrate is marked in line arrows to highlight the region primarily contributing to C_{OSS}. Note that, in these plots, the lateral scale is large than the vertical scale. For V_{Sub} of 0 V and V_{DS}, the shortest depletion depth is located below the drain and above the substrate (and below the source), respectively. At $V_{\mathrm{Sub}} =$ $0.5V_{\mathrm{DS}}$, the depletion front is far away from the drain. The shortest depletion depth is located above the substrate, and its physical distance to the substrate needs to be scaled by a factor of 2. Comparing the depletion fronts at three V_{DS}, the magnitude of the shortest depletion depth is highest for $V_{\mathrm{Sub}} = 0.5V_{\mathrm{DS}}$. This explains the smaller C_{OSS} and E_{OSS} under $V_{\mathrm{Sub}} = 0.5V_{\mathrm{DS}}$ in Scheme III.

Fig. 8(f)–(h) shows the simulated potential contours with the filled acceptor trap for V_{Sub} of 0 V, $0.5V_{\mathrm{DS}}$ and V_{DS}, respectively, all at $V_{\mathrm{DS}} = 400$ V. The new depletion fronts are marked in solid curves, and the original depletion fronts before trap filling are also marked for comparison. At V_{Sub} of 0 V and V_{DS}, considerable shifts occur for the shortest depletion depth, which are illustrated in arrow symbols. These large shifts explain a considerable change in dynamic C_{OSS}. In contrast, at $V_{\mathrm{Sub}} =$ $0.5V_{\mathrm{DS}}$, the depletion boundary shift is mainly in the lateral direction, which is far from the drain. At the depletion front closest to the substrate, i.e., the location of the shortest depletion depth, a minimal shift is observed. This suggests, at $V_{\mathrm{Sub}} =$ $0.5V_{\mathrm{DS}}$, the depletion boundary shift occurs in the region with a marginal contribution to C_{OSS}, inducing a smaller change in C_{OSS} and E_{DISS}.

V. Impact on Dynamic R_{ON}

In high-freuqency, soft-switching applications, device loss is dominated by the conduction loss and C_{OSS} loss. To probe the

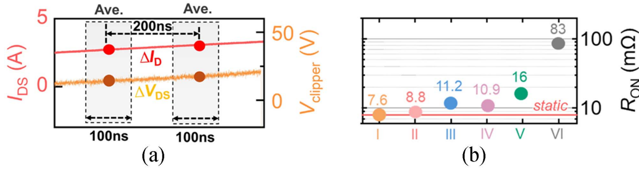

Fig. 9. (a) Illustration of the dynamic R_{ON} extraction using the incremental V_{DS} and I_{DS}, followed by averaging the measurement results in a 100 ns window. (e) Measured dynamic R_{ON} of the DUT under schemes I–VI at 400 V $V_{DS(peak)}$ in the steady-state switching.

impact of substrate termination on conduction loss, the dynamic R_{ON} is measured by the voltage clipper during the stage I of the UIS test [see Fig. 4(c)] under the steady-state switching. As shown in Fig. 9(a), the dynamic R_{ON} is extracted from the incremental ΔV_{DS} (measured by $V_{clipper}$) and ΔI_D across a 200 ns period to cancel the impacts of clipper noise and delay. To minimize the possible oscilloscope noise, R_{ON} at each moment is calculated by averaging the results of 250 adjacent measurements spanning a 100-ns window. The detailed data processing method has been elaborated in [22] and [27]. In the UIS test for dynamic R_{ON} extraction, a relative low $I_{DS(max)}$ of ∼3 A, switching frequency of 50 kHz, and V_{BUS} of 5 V are used to minimize the DUT's self-heating. Active fan cooling is also applied. Thermal camera images reveals a minimal temperature increase in the DUT under the steady-state swiching with different test schemes.

Fig. 9(b) shows the measured dynamic R_{ON} of the DUT under all substrate connection schemes at $V_{DS(peak)}$ of 400 V. The dynamic R_{ON} is found to increase with the V_{Sub}/V_{DS} ratio, being the lowest in scheme I and the highest in scheme VI. This in general can be illustrated by the back-gating effect and the trapping in the GaN buffer below the gate region [19]. The detailed physical analysis will be pursued in the future work. From the application standpoint, under the scheme III and IV, which is optimal for E_{DISS}, the DUT's dynamic R_{ON} is about ∼40% higher than that in scheme I. This suggests a tradeoff between the DUT's conduction loss and switching loss under various V_{Sub} modulations. Such trade-off needs to be taken into account in specific applications. It also suggests that, depending on the duty cycle in soft-switching applications, the DUT's substrate termination scheme can be further optimized to achieve the lowest total loss.

VI. Conclusion

In this article, we find that the inherent E_{DISS} of GaN-on-Si power HEMTs can be effectively suppressed by tuning V_{Sub} to follow V_{DS} dynamically with a V_{Sub}/V_{DS} magnitude ratio of 1/4 to 1/2. Accordingly, a new and easy-to-implement approach for E_{DISS} minimization is demonstrated by connecting external capacitor(s) between the substrate and the source and/or drain. At $V_{Sub} = 0.5V_{DS}$, E_{DISS} of a 650 V, 8 mΩ GaN HEMT is reduced by up to 86%, and the maximum E_{DISS}/E_{OSS} ratio is reduced from 14.6% to 2.2%. This result removes a critical roadblock for deploying GaN HEMTs in high-frequency, soft-switching applications.

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