# In-Chip Microfluidic Cooling Integrated on GaN Power IC Reaching High Power Density of 78 kW/l

Remco van Erp, Nirmana Perera, *Member, IEEE*, Luca Nela, Ibrahim Osama Elhagali, *Graduate Student Member, IEEE*, Hongkeng Zhu, *Graduate Student Member, IEEE*, and Elison Matioli, *Senior Member, IEEE*

***Abstract*—The lateral structure of gallium nitride (GaN) semiconductors enables monolithic integration of logic and power devices, which offers promise to miniaturize bulky converters into a compact package. However, the concentrated heat that arises from this dense integration can locally exceed 1 kW/cm$^2$, which surpasses the limit of current thermal management technologies. In this article, we demonstrate the potential of integrating in-chip microfluidic cooling directly on GaN power integrated circuits (ICs), together with additively manufactured packaging, to provide efficient thermal management, and achieve ultrahigh-power densities. A prototype power module and a 0.44 kW 48 V–24 V dc–dc converter were realized in a compact 32nd brick form factor to demonstrate its potential. Our results show a 14-fold reduction in thermal resistance and a four-fold increase in the total output power compared to heat-sink and fan cooling. An outstanding 78 kW/l was achieved, together with an increase in power conversion efficiency, surpassing 95%. By removing thermal limitations from power IC design, and enabling highly integrated topologies combined in a single liquid-cooled chip, this work paves the way for more efficient and highly compact power conversion in the future to support the electrification of our society.**

***Index Terms*—Gallium nitride (GaN) dc–dc converter, in-chip cooling, power density, power integrated circuit (IC), thermal management.**

## I. Introduction

THE electrification of our society is driving the increased adoption of power electronic systems for converting and delivering electric power. The stringent constraints on efficiency, weight, and volume in applications such as aerospace and ground-based transportation demand ever-increasing power densities [1], [2]. Gallium nitride (GaN) devices are a prime candidate to achieve these efficiency and power density targets due to their reduced specific on-resistance, smaller die sizes, and higher switching speeds compared to Si [3], [4]. The latter is essential for high power density converters, as it enables the miniaturization of energy storage components, i.e., inductors and capacitors [5]. Furthermore, the lateral device structure of GaN high-electron-mobility-transistors (HEMTs) enables integration of multiple power and logic devices [6], [7], [8], [9].

Various configurations of such GaN integrated circuits (ICs) are presently entering the market, including power switches in a half-bridge configuration with integrated gate drivers, level shifters, and bootstrap circuitry [10]. These ICs replace multiple discrete components with a single chip for voltage levels up to 650 V [11], [12], and enable more intricate converter topologies without increasing system-level complexity [13]. Such large-scale device integration trend is similar to that of Si-based logic [14].

However, with many heat-generating components densely integrated, GaN power ICs can face prohibitively high heat fluxes at full load [15]. The resulting self-heating causes significant degradation in device performance and efficiency, thus, the maximum power of such an IC is ultimately thermally limited. A significant reduction in the thermal resistance of GaN ICs is required to unlock their full potential for highly miniaturized power converters. However, unlike rapid developments in logic and power device integration, cooling integration is often overlooked.

In a conventional *indirect* cooling configuration, heat is transported from the junction to a remote heat sink, separated by layers of packaging and thermal interfaces, which prevent good heat transfer. *Direct* microfluidic cooling, in which these interfaces are eliminated and a coolant is in contact with the semiconductor device, has been actively investigated to overcome these thermal limitations [16]. Microscale convective cooling techniques, using microjets, microchannels, and manifold microchannels [17], [18], [19], [20], [21], [22] have demonstrated a 10-fold increase compared to indirect methods, with heat extraction up to 1.7 kW/cm$^2$ from discrete GaN-on-Si power devices [23], [24], [25], [26]. Practical issues that hinder adoption, such as manufacturing, packaging, and assembly using existing low-cost manufacturing methods have remained largely unaddressed.

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The authors are with the Power and Wide-Band-Gap Electronics Research Laboratory (POWERlab), Institute of Electrical and Micro Engineering, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: ibrahim.elhagali@epfl.ch; elison.matioli@epfl.ch).

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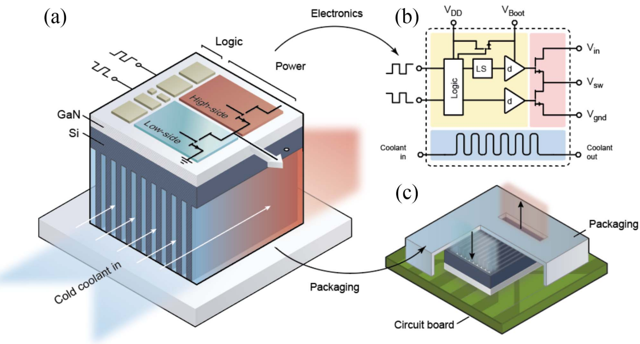


Fig. 1. (a) Illustration of the device unpackaged. (b) Schematic overview of the power-logic-microfluidic integrated circuit. (c) Illustration of the packaged device.

Here, we demonstrate a holistic approach to device, packaging, and system design, compatible with established manufacturing methods, to enable highly integrated power converters that fully exploit the benefits of microfluidically cooled GaN ICs. We show that, by considering cooling as a third layer of integration, in addition to logic and power, ultrahigh-power densities for switched-mode power supplies together with an increase in efficiency and reduction in temperature can be achieved. We first demonstrate the feasibility of integrating microfluidic cooling in GaN-on-Si HEMTs by studying the impact of in-chip coolant on electric device performance. Next, we demonstrate an integrated module that serves as a fundamental building block for power converters: a state-of-the-art half-bridge power module with integrated gate drivers, logic, and in-chip microfluidic cooling. New methods for packaging and assembly based on additive manufacturing were developed to distribute the coolant in the microfluidic channels. As a result, by turning the low-cost silicon substrate into a high-performance heat sink, over 350 W/cm$^2$ of heat flux can be extracted from the GaN IC.

We investigate, first, how the monolithic integration of power, logic, and cooling into a single IC improves the power density and efficiency of dc–dc converters in 48 V power switching applications. Second, we demonstrate the first-of-its-kind buck converter built around these ICs to obtain 0.44 kW dc–dc converters within a highly-miniaturized 1/32nd brick footprint, resulting in high power densities exceeding 78 kW/l, which demonstrates the promising capabilities of liquid-cooled power ICs as a modular building block for next-generation compact power conversion.

## II. Microfluid Cooling Integrated Power Module

In this section, a description of the device and a postprocessing micromanufacturing step are presented, along with device performance evaluation and comparison using different thermal management approaches.

### A. Proposed Integration Concept

Fig. 1(a) illustrates the concept of the proposed liquid-cooled power IC. The commercially-available IC consists of a 5 $\mu$m-thick AlGaN/GaN epilayer, epitaxially grown on a 500 $\mu$m-thick silicon substrate. The device contains two 80 V-rated power HEMTs with 8.5 m$\Omega$ on-resistance ($R_{\mathrm{ds,ON}}$), in a half-bridge configuration, as well as monolithically integrated gate driver circuitry, input logic interface, level shifter, and a bootstrap charging circuit. All electronics are integrated on the GaN layer, whereas the silicon substrate functions as a high-performance microfluidic heat sink. We refer to the resulting IC, illustrated in Fig. 1(b), as an integrated power module, as it contains power switches (marked in red), logic (marked in yellow), and cooling (marked in blue). After installation on a printed circuit board (PCB), the cooling channels in the backside are accessible from the top. The chip is then packaged to create a fluidic inlet and outlet to guide the coolant in and out of the die [see Fig. 1(c)].

### B. Design of Power Module

First, the design of the microchannels was optimized by focusing on the tradeoff between heat transfer and pressure drop. Decreasing the microchannel width, enhances the heat transfer surface area, but also the frictional losses, thus increasing the pressure drop. The optimal microchannel geometry was investigated by a one-dimensional theoretical analysis considering the temperature difference between the junction and the inlet fluid ($\Delta$T), and the coefficient of performance (COP) at a specific heat flux. The COP represents the ratio between the dissipated and the pumping powers [27]. The pressure drop is calculated from the microchannel geometry, fluid properties and flow rate (flow is assumed laminar and fully-developed). $\Delta$T is a function of thermal load and total thermal resistance between the junction and fluid. The total thermal resistance for a direct in-chip cooling includes three in-series resistances: conduction resistance through the remaining (unetched) Si substrate; convection resistance between the substrate and fluid; and flow thermal resistance due to the caloric heating of the fluid within the microchannel heat sink [27]. The total resistance is a function of the flow rate, fluid properties and geometry of the microchannels. Microchannel widths of 10, 50, and 100 $\mu$m were considered at three different heat fluxes of 250, 350, and 400 W/cm$^2$, and the results are shown in Fig. 2. The 100 $\mu$m-wide channels resulted in a large $\Delta$T. On the other hand, 10 $\mu$m-wide channels yielded a low temperature rise, however, at a very low COP due to the high pressure drop. In addition, these narrow channels are more prone to clogging. 50 $\mu$m-wide channels provided a good tradeoff between COP and $\Delta$T, in addition to the ease of fabrication and operation. The model has been validated with experimental results on test structures with 50 $\mu$m microchannels for heat fluxes measured at 250, 350, and 400 W/cm$^2$, showing an excellent agreement (see green stars in Fig. 2).

Subsequently, 50 $\mu$m microchannels were etched in an off-the-shelf die by applying a simple postprocessing method on the chips in a scalable wafer-based cleanroom process outlined in Fig. 3(a). The process started by placing unpackaged dies (EPC2152) with exposed silicon substrate on a carrier wafer. Direct laser writing lithography and deep-reactive-ion-etching were employed to fabricate 50 $\mu$m-wide and 400 $\mu$m-deep channels inside the silicon substrate. This approach enables rapid prototyping without requiring a change in the foundry

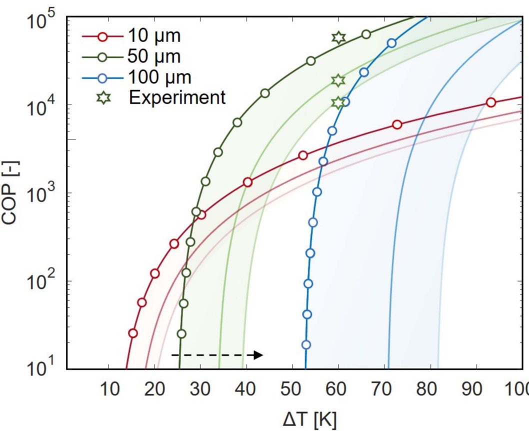


Fig. 2. COP versus ΔT for channel widths of 10, 50, and 100 $\mu$m, and heat fluxes of 250, 350, and 400 W/cm$^2$. The dashed arrow shows the direction of heat flux increase. Experimental results on test structures with 50 $\mu$m microchannels for heat fluxes experimentally measured at 250, 350, and 400 W/cm$^2$ are shown in green stars, agreeing with the model.

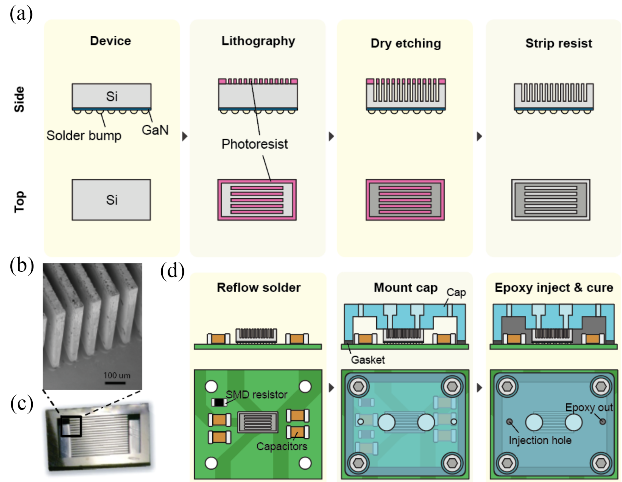


Fig. 3. (a) Die postprocessing method: Photoresist is spin-coated on the backside of the silicon substrate of the die, and cooling channels are lithographically patterned. Channels are subsequently etched in the substrate using dry etching, before the resist is stripped. (b) SEM image of channels etched in the backside of the die. (c) Picture of the die after postprocessing. (d) Packaging process, a plastic cap is mounted on the IC and an epoxy is injected to create a leak-tight seal. Cavities are present inside the cap to accommodate components that extend above the surface of the IC.

process, but also offers a clear route to low-cost and high-volume manufacturing by performing the channel etching over an entire wafer, before die singulation. Fig. 3(b) shows a close-up scanning electron microscope (SEM) image of the microchannels in the backside of the device, and a picture of the complete device backside is shown in Fig. 3(c).

A second challenge is supplying and distributing coolant to the IC within a compact form factor, without introducing complex manufacturing steps. A novel fluidic packaging method was developed to address these challenges: The postprocessed devices were soldered on a PCB before applying a custom packaging solution following the process outlined in Fig. 3(d): An additively manufactured cap that guides the fluid was mounted

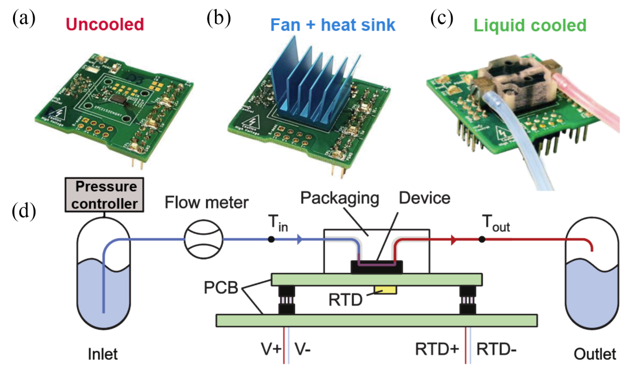


Fig. 4. Three different cooling approaches considered on the same power module for comparison. (a) Uncooled. (b) Heat sink and fan (c) In-chip microfluidically cooled.

on the IC, and a molding compound (EPO-TEK Glob Top) was injected in this cap to permanently seal all voids around the chip. Due to the height differences and tightly positioned components, additively manufacturing is an essential tool to adapt the packaging to the circuit layout. Pressure tests confirmed a reliable leak-tight operation of the final power module up to five bars with no leakage. The proposed method is a low-cost, practical solution to overcome the challenges of bridging the microscale and macroscale plumbing in microfluidic cooling.

## C. Experimental Evaluation

For comparison, two additional power modules were prepared using conventional cooling methods. In one case, an unprocessed die was soldered on a printed circuit board which relied purely on natural convection [see Fig. 4(a)] - referred to as *uncooled*. In a second reference device, a heat sink of comparable footprint to the 3D-printed cap was mounted on an unprocessed device, for which a fan was utilized to generate forced convection cooling, referred to as *Fan + heat sink (HS)* [see Fig. 4(b)]. Both of them were evaluated alongside the power IC with in-chip microfluidic cooling [see Fig. 4(c)], which was installed in an experimental setup shown in Fig. 4(d).

A reservoir of deionized (DI) water at 22 °C was pressurized with compressed air to control the flow rate of coolant passing through the above shown open-loop [see Fig. 4(d)] and supplying liquid to the cooled chip, which was monitored using a flow meter (Sensirion SLQ-QT500), and the coolant was disposed into a waste reservoir after use, in an open-loop setup.

No liquid leakage nor corrosion were observed under these operating conditions. DI water was used in this study since only low voltages were considered. For high voltage applications, dielectric coolants, such as Novec7200 should be used to avoid short-circuit since the silicon substrate is usually electrically connected to the source of the device. The use of such coolants for higher voltage single transistors (650 V) were demonstrated in previous works [28]. Further investigation on the effect of liquid cooling (either DI water or dielectric) embedded in the silicon substrate, presented in [28], revealed no negative impact on the device electrical characteristics, such as threshold voltage and dynamic on-resistance.

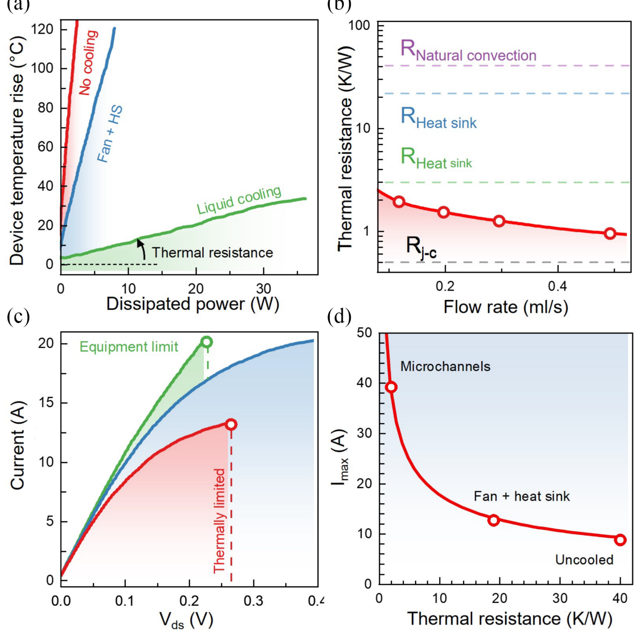


Fig. 5. (a) Device temperature rise versus dissipated power under reverse conduction for three different cooling approach. (b) Comparison of junction to coolant thermal resistance for three cooling approaches. (c) Device DC characteristics under forward conduction for different cooling approaches. (d) Theoretical maximum current for three cooling approaches based on the thermal resistance.

Coolant inlet and outlet temperature on the package were measured using a k-type thermocouple, and the device temperature was monitored using a resistance temperature detector (RTD) mounted right below the GaN device, thermally coupled using copper vias. This approach was previously described and validated in [29]. A control board provides the power module with an input voltage, complementary PWM signals, supply voltage, and connects the output terminals to a load.

Fig. 5(a) shows a steady-state temperature rise during power dissipation (measured under reverse conduction mode, in which the devices exhibit high forward voltage drops and dissipate larger power). The *uncooled* reference could dissipate 2.0 W of power before reaching a junction temperature rise of 100 °C, corresponding to a thermal resistance of 50 K/W. Adding a heat sink and fan resulted in a maximum dissipated power of 5.2 W, corresponding to a thermal resistance of 19.2 K/W. In comparison, embedded microchannel cooling at a flow rate of 0.5 ml/s showed a temperature rise of only 31 °C at a power dissipation of 35 W, corresponding to a thermal resistance of 0.88 K/W. This represents heat fluxes of up to 350 W/cm$^2$ (but not limited to), which justifies the range chosen in the model presented in Fig. 2. Thus, on a similar electrical device, a 22-fold reduction in temperature rise can be obtained by integrating microchannel cooling in the substrate. This corresponds to a thermal resistance of 0.89 K/W and heat transfer coefficient (HTC) of 112.4 kW/m$^2$ K for a flow rate of 0.5 ml/s and pressure drop below 0.4 bar. As a comparison, jet impingement demonstrated in top-side cooling of GaN IC in [30] showed an HTC of 100 kW/m$^2$ K at flow rate of 1 l/min and pressure drop of 1.8 bar. This shows the benefits of the proposed technology.

Lower device temperatures can be achieved by further increasing the flow rate [see Fig. 5(b)], which effectively reduces the temperature rise of the coolant. The thermal resistance obtained by integrating microchannel cooling is even lower than the junction-to-board thermal resistance ($R_{\text{j-b}}$) of the device, demonstrating that no bottom-side PCB cooling method can possibly extract as much heat as embedded microchannels.

The effect of the improved thermal management on the device dc characteristics (under forward conduction mode), can be seen in Fig. 5(c). While no noticeable variation in $R_{\text{ON}}$ was observed at a low forward voltage, as the forward voltage was increased, the effect of self-heating on output current became apparent. In the case of the *uncooled* device, a rapid decrease in the output current slope was observed above 7.5 A. The *Fan + HS* device showed a similar trend occurring above 10 A, while the liquid-cooled IC shows a nearly linear increase in output current up to 20 A (limited by the equipment) with minimal degradation. Thus, better cooling aids the increasing of the power IC's current capability in two ways: First, it raises the limit on how much power can be extracted, and second, it reduces conduction losses due to self-heating degradation. This combined effect [see Fig. 5(d)] leads to an exponential increase in current capability when reducing thermal resistance.

### D. Demonstration in Switching Mode

The integrated power modules were evaluated in a hard-switched synchronous buck-topology with 48 V input voltage and 24 V in the output (tested in open loop control) [see Fig. 6(a)]. In this work, no specific application was targeted for this step-down conversion, as the same cooling approach can be used for many different applications. The fast-switching capabilities of GaN HEMTs and the integrated gate driver circuitry enable their operation at switching frequencies exceeding 2 MHz [see Fig. 6(b)], which significantly reduces the requirements on inductor sizing, thus enabling an extremely compact 48 V to 24 V buck converter. The temperature rise of the device was measured using a RTD mounted underneath the PCB, located below the DUT. Conversion efficiencies measured at 0.5, 1, and 2 MHz for the three evaluated cases are shown in Fig. 6(f)–(h). In the case of natural convection, even at zero output current, the hard-switching losses due to charging and discharging the device output capacitance [31], as well as logic, and gate driver losses already caused a high temperature rise, which increased at higher switching frequencies. For example, at 1 MHz for the case without cooling, these losses caused a 55 °C temperature rise, without delivering any power to the load. At 2.2 A, which corresponds to an output power of 51 W, the device reached a temperature rise of 75 °C. For forced-air cooling, a larger maximum current of 6.8 A could be reached for the same device temperature rise, which corresponds to an output power of 142 W. In contrast, due to the much-improved cooling and reduced self-heating degradation, microfluidic cooling enabled a much higher output power. At an output current of 10 A, the device temperature rise remained below 30 °C (at 0.17 ml/s).

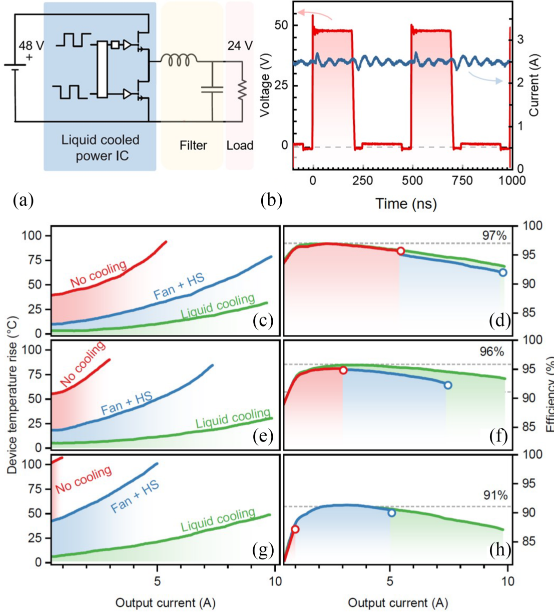


Fig. 6. (a) Circuit schematic of the evaluated buck-converter, wherein the components marked in blue are integrated within the liquid-cooled power IC. (b) Waveforms of the switching-node voltage and output current at 2 MHz operation. Chip temperature versus output current for an input voltage of 48 V and a 50% duty cycle at (c) 0.5 MHz, (e) 1 MHz, and (g) 2 MHz. Power conversion efficiency versus output current for an input voltage of 48 V and a 50% duty cycle at (d) 0.5 MHz, (f) 1 MHz, and (h) 2 MHz. The flow rate was 0.17 ml/s for the liquid cooled device.

At higher frequencies, where switching losses play an increasingly important role, the benefits of microfluidic cooling become even more apparent for maximizing output power. At 2 MHz, a 4.2-fold increase in output power could be achieved compared to forced air-cooling, while natural convection could no longer operate below 100 °C, even at zero output power (partially due to the stored energy at the output capacitance that is dissipated in the device channel).

The power conversion efficiency between the three cases shows an identical pattern up to 3 A of output current, peaking around 95%. This confirms that the postprocessing did not damage the performance of either the logic or the power HEMTs. Instead, above 3 A, the efficiency of microchannel cooled device is higher, over a larger range of currents. An increase of over 2 percentage points in efficiency (at 7.5 A) compared to forced air-cooling is observed, which corresponds to a reduction of around 25% in losses for the liquid-cooled device [see Fig. 6(f)–(h)]. Part of this can be accounted by the absence of self-heating degradation.

## III. Integrated Power Converter Design

To demonstrate the enormous impact of embedded microchannel cooling on power density, a highly-compact buck-converter was realized within an industry-standard 32nd brick form factor. The power IC, inductor, capacitors, cap, and fluidic connectors were fitted within a 19.1 mm × 23.4 mm footprint [see Fig. 7(a)] with a height of 12.6 mm, resulting in a volume of 5.63 ml, and was mounted on a readout PCB shown in Fig. 7(b).

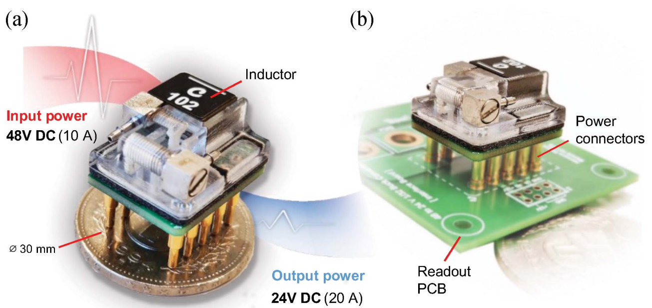


Fig. 7. (a) Thirty-second brick DC–DC converter, with embedded cooling, inductor, and fluidic connectors. The total volume of the PCB, electrical components, cap, and connectors is 5 ml. (b) Thirty-second brick converter installed on a readout PCB.

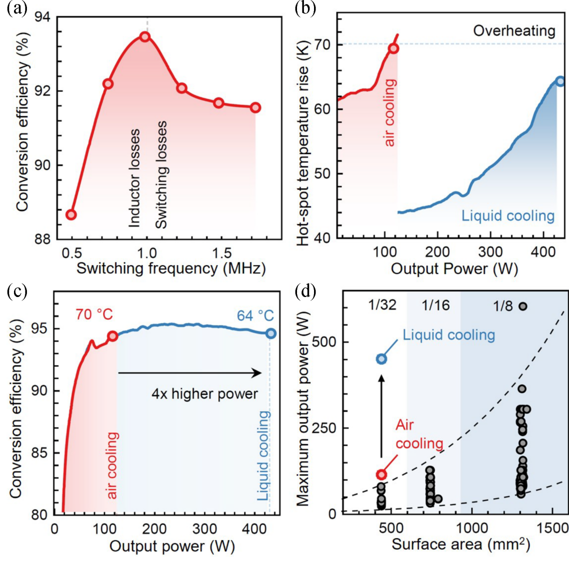


Fig. 8. (a) Efficiency versus switching frequency at output power of 100 W. (b) Temperature rise on the inductor for forced air-cooling and integrated liquid cooling. (c) Efficiency versus output power. (d) Maximum power versus converter surface area for commercially available standard DOSA brick power converters from online catalogs (in black) for 8th brick, 16th brick, and 32nd brick form factors, with input voltage of 48 V and different output voltages (although the power density of converters with different output voltages cannot be directly compared). Embedded microfluidic liquid cooling enables over a four-time increase in output power compared to forced air-cooling.

Inductor selection introduces a challenge since its inductance and dc resistance are inversely proportional to their volume. A higher inductance value reduces the output voltage ripple, and thus, the core and ac winding losses, but causes increased conduction losses. The tradeoff between conduction losses and core and winding losses was first investigated. Increasing the switching frequency from 600 kHz to 2 MHz can decrease the inductor losses by over two times. However, the increase in switching losses on the power IC can easily negate these effects. A sweep in switching frequency at a fixed inductance of 2 $\mu$H and output power of 100 W, revealed a peak efficiency at 1 MHz [see Fig. 8(a)]. Fig. 8(b) and (c) shows the temperature rise and efficiency versus output power for an input voltage of 48 V and a fixed 50% duty cycle at switching frequency of 1 MHz. This highly-compact buck converter reaches a high-power density of 78 kW/l with a maximum output power of 440 W before reaching

a temperature rise of 64 °C. In contrast, commercially-available 32nd brick 48 V-input dc–dc converters are currently limited to 60 W [see Fig. 8(d)]. This result shows that embedded liquid cooling enables over four-time increase in output power compared to air-cooling, while maintaining a low device temperature rise. This can have a major impact on space- and weight-sensitive applications, such as automotive and aerospace.

## IV. Conclusion

In this work, we have demonstrated a switch-mode power supply based on in-chip liquid-cooled power ICs with state-of-the-art electrical and thermal performance. A simple wafer-scale postprocessing method has the potential to be low cost and achieve high volume production. We have demonstrated that embedded microchannel cooling can reduce thermal resistance by over a factor of 20. Over 40 W of heat was extracted from a single IC, thus taking away existing design constraints that limit current applications.

With a hard-switched buck-converter topology, a fully integrated converter in a 32nd brick form factor, was demonstrated presenting over 4x-higher output power compared to forced air-cooling, at a very low flow rate of 0.5 ml/s. In applications where liquid cooling loops are readily available, such as automotive applications, this technology can be key for reducing weight and volume. It should be noted that there is significant room for improvement by optimizing the converter topology to further reduce switching losses, which was not within the scope of this work. Due to the heterogeneous power map of GaN ICs, a large opportunity arises for microfluidic topology optimization to ensure temperature uniformity. If this is correctly addressed, we foresee that high-frequency soft-switching topologies combined with embedded microchannel cooling will enable drastic increase in power density and efficiency.

The presented approach highlights the advantages of designing integrated semiconductor devices and cooling not as separate entities, but as one unified process. Altogether, the inclusion of microfluidic cooling and additive manufacturing in the toolbox of the power electronics engineers has the potential to break existing thermal limitations and enable an additional degree of integration. This extended toolbox can play a key role in the development of smaller and lighter power converters that are key for supporting the ongoing electrification of our society.

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**Remco van Erp** received the B.Sc. and M.Sc. degrees in mechanical engineering from Eindhoven University of Technology, Eindhoven, The Netherlands, in 2014 and 2017, respectively, and the Ph.D. degree in microsystems and microelectronics from Swiss Federal Institute of Technology Lausanne, Lausanne, Switzerland, in 2022.

He is currently co-founder and CEO of Corintis, Lausanne, Switzerland. His research interests include the design, validation, and manufacturing of micro-scale liquid cooling for high-power logic chips for datacenter applications.

**Nirmana Perera** (Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the University of Peradeniya, Peradeniya, Sri Lanka, in 2011, the M.Sc. degree in power electronics and energy systems from the University of Alberta, Edmonton, AB, Canada, in 2015, and the Ph.D. degree in electrical engineering from École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2022 (*with a focus on the design and analysis of high-frequency power converters, and characterization of wide-bandgap devices*).

He was a Lecturer with the Department of Electrical and Electronic Engineering, University of Peradeniya, Peradeniya, Sri Lanka, from 2015 to 2017. In 2022, he was an Application Engineer with Cambridge GaN Devices, Cambridge, U.K.

**Luca Nela** received the Ph.D. degree in GaN power devices from École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2022.

His research interests include the development of novel GaN power devices and converters.

Dr. Nela is the recipient of several awards in power electronics and devices including the Charitat Award for Best Young Researcher (2020, 2021), the Swiss Technology Award (2021), and the 2022 EPFL Doctoral Thesis Award.

**Ibrahim Osama Elhagali** (Graduate Student Member, IEEE) received the B.Sc. degree in mechanical engineering from Menofia University, Shibin Al Kawm, Egypt, in 2016, and the M.Sc. degree in mechanical engineering from Penn State University, State College, PA, USA, (*Fulbright Scholarship*), in 2021. He is currently working toward the Ph.D. degree in mechanical engineering from École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland.

His main research interest includes thermal management of high heat flux electronics.

**Hongkeng Zhu** (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2018 and 2021, respectively, and the engineering diploma from Ecole Centrale de Lyon, Lyon, France, in 2021. He is currently working toward the Ph.D. degree in electrical engineering with École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland.

His current research interests include wide bandgap semiconductor device design, characterization, and applications for high-frequency high-efficiency power conversion technologies.

Mr. Zhu is a Marie Skłodowska-Curie fellow.

**Elison Matioli** (Senior Member, IEEE) received the double B.Sc. degrees in 2005 in applied physics and mathematics from École Polytechnique, Palaiseau, France and in electrical engineering from Escola Politecnica, Universidade de Sao Paulo, São Paulo, Brazil, and the Ph.D. degree in 2010 in material science from the Materials Department, University of California at Santa Barbara, Santa Barbara, CA, USA.

He was a Postdoctoral Fellow with the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, until 2014. He is currently an Associate Professor with the Institute of Electrical and Micro-Engineering, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland. His research interests include wide-band-gap semiconductor devices for power electronics and ultrafast RF devices, thermal management of electronics, and high-efficiency high-power-density power converters.