Highly Efficient Three-Level AC–AC Converter With Identical In-Phase and Antiphase Buck–Boost Operations

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***Abstract*—In this article, a new coupled-inductors based three-level bipolar buck–boost ac–ac converter is proposed. The proposed converter can produce highly efficient and symmetric in-phase and antiphase buck and boost modes of operation with much lower component voltage and current stresses. This reduces the operation and design complexity, and helps to achieve a high-efficiency operation. The high-frequency modulating switches of the proposed converter are implemented with coupled-inductor-based dual-buck phase leg, producing three-level input and output voltages, and providing inherent protection from voltage-source short-circuit issue during switch transitions. The other salient features of the proposed converter are no-commutation issue, no need for *RC* snubbers or dedicated safe-commutation algorithms, provision of high-quality and continuous input/output currents, and support for nonresistive loads. An in-depth circuit analysis of the proposed converter is provided based on the proposed switch modulation strategies. The guidelines for component design/selection are discussed, followed by the comparisons with state-of-the-art three-level ac–ac converters. Finally, practical circuit verifications are performed on a laboratory-assembled prototype.**

***Index Terms*—AC–AC conversion, buck–boost voltage, coupled magnetics, in-phase/antiphase output, three-level voltages.**

I. Introduction

THE ac–ac power converters are crucial for industrial applications and addressing grid power quality issues. They fall into three main categories: indirect ac–dc–ac converters with a dc link [1], [2], matrix converters [3], [4], [5], and direct pulsewidth modulation (PWM) ac–ac converters [6], [7]. While indirect converters offer flexible control over all output voltage attributes (magnitude, phase, and frequency), they require a two-step conversion with large and costly dc-link capacitors [8]. Matrix and direct ac–ac converters provide single-stage conversion, eliminating the need for large dc-link capacitors.

Single-phase matrix converters [3], [4], [5] and direct ac–ac converters [6], [7] lack the ability to synthesize a finite output voltage at zero crossings of input voltage. As a result, they can only produce in-phase or antiphase output voltage (unipolar topologies [5], [9]), nonidentical in-phase and antiphase output voltages (bipolar topologies [7], [10]), or identical in-phase and antiphase output voltages (identical-bipolar topologies [3], [4], [5], [11]). Bipolar-type ac–ac converters are increasingly used for series voltage compensation applications, such as dynamic voltage restorers [10], to mitigate voltage dips and overvoltages. Identical-bipolar ac–ac converters [3], [4], [5], [11] can produce step-variable frequency output, useful in traction applications [4] and high-gain ac–dc rectifiers [5]. Emerging applications include using identical-bipolar ac–ac converters as flexible transformers [12], enabling series compensation voltage with controllable phase-shift ranging from 0 to 2π. However, conventional direct ac–ac converters [6] only provide in-phase or antiphase output voltage. Thus, research focus has shifted toward developing new ac–ac converters with bipolar output voltage.

Impedance-network-based *Z*-source ac–ac converters [7] are well-known nonidentical-bipolar ac–ac converters. Their various in-circuit improvements are proposed [13] to enhance their circuit performance and improve voltage/current profiles. Nevertheless, their practical use is hindered due to requiring a large passive element count, sharp variations in gain curve, and absence of in-phase buck operation. Current-source-type bipolar [14] and unified bipolar [10] buck–boost ac–ac converters are proposed with less passive elements. However, the former has large devices in power loop with only resistive load support. However, the latter has discontinuous input/output currents with the absence of in-phase boost operation. Dual-buck structured bipolar ac–ac converter [15] is proposed to eliminate the commutation issue of ac–ac converters. However, it requires a large number of circuit elements, the

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absence of in-phase boost operation, and an inefficient antiphase buck–boost operation. The identical-bipolar buck–boost ac–ac converters (or single-phase matrix converters) are developed in [3], [4], [5], and [11]. However, buck-type [3], [4] and boost-type [5] matrix converters have limited voltage transfer ratios. Z-source buck–boost matrix converter is developed [16]. However, it needs too many active switches and passive elements. Nondifferential ac choppers and dual-buck structured identical-bipolar buck [11] and buck–boost [17] type ac–ac converters are proposed. However, the former has a limited voltage transfer ratio, and the latter suffers from large component voltage/current stresses and ripples.

The above-described converters generate two-level voltages. The three-level ac–ac converters are gaining attention to reduce switching harmonics, offer more inductor voltage levels with smaller steps, and produce high-quality input/output voltages with reduced filtering demands. Traditional three-level ac–ac converters [18], [19] are typically constructed by cascading two-level converter units, offering modular structures, simple fabrication, and easy maintenance. However, they require twice the components of two-unit converters and can have discontinuous input currents. Flying-capacitor three-level ac–ac converters [20], [21] have been proposed but face challenges, such as capacitor voltage imbalance and complex voltage balancing techniques, resulting in some duty cycle loss. An innovative approach utilizing an auxiliary transformer for capacitor voltage balancing is presented in [22]; however, this converter still requires eight switches and allows only buck operation. Importantly, these three-level converters provide only in-phase or antiphase output voltage and encounter commutation issues [18], [19], [20], [21], [22].

Dual-buck phase leg and coupled-inductor [23] based ac–ac converters [24], [25], [26] offer three-level voltages and resolve commutation issues without requiring cascaded connections or capacitor voltage balancing. While basic topologies are provided in [24] and [25], limitations include restricted voltage transfer ranges for buck and boost topologies, higher stresses and poorer power quality for buck–boost topology, and unipolar operation with only in-phase or antiphase capability. A recent proposal introduces a dual-buck and coupled-inductor-based three-level bipolar ac–ac converter [26] capable of in-phase and antiphase buck–boost operations. However, it requires three high-frequency-modulated dual-buck phase legs with three-coupled inductors. The converter's in-phase and antiphase operations are nonidentical, posing challenges for circuit optimization. Antiphase operation results in higher voltage stress ($= v_{\text{in}} + v_o$, where v_{in} is the input supply voltage and v_o is the output voltage) and current stress [($> i_{\text{in}} + i_o$), where i_{in} is the input supply current and i_o is the output current] of switching devices, necessitating high-rating components and leading to increased implementation costs and reduced efficiency [26].

This article proposes a new highly efficient dual-buck and coupled-inductor-based three-level identical-bipolar buck–boost ac–ac converter. The proposed converter uses only two high-frequency-modulated dual-buck phase legs with coupled inductors, in combination with two line-frequency-modulated conventional phase legs. Its in-phase and antiphase buck and boost operations are identical with the same component voltage/current stresses and ripples. This simplifies the switch modulation, circuit operation, design, and optimization. Moreover, its bipolar buck–boost operations are highly efficient with low component voltage/current stresses and ripples. It can provide both three-level inputs and outputs. Additionally, a dedicated phase-shift control ensures that the input and output filter voltages and currents experience twice the switching frequency, thereby further reducing their values and requirements. The proposed converter has inherent protection from commutation issue without requiring extra circuitry or dedicated control. Moreover, it provides good quality and continuous input/output currents, and works normally with nonresistive loads.

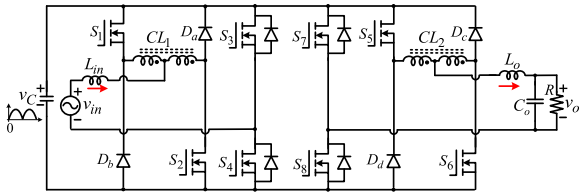


Fig. 1. Proposed identical-bipolar three-level buck–boost AC–AC converter.

II. Proposed AC–AC Converters

Fig. 1 illustrates the proposed converter. The positive (reference) input terminal $v_{\text{in}+}$ is connected through input inductor L_{in} to a coupled-inductor CL_1-based dual-buck phase leg (consisting of switches S_1 and S_2, and diodes D_a and D_b), and negative (reference) input terminal $v_{\text{in}-}$ is connected to midpoint of a conventional phase leg (consisting of switches S_3 and S_4). In an identical manner, the positive (reference) load terminal v_{o+} is attached to a coupled-inductor CL_2-based dual-buck phase leg (consisting of switches S_5 and S_6, and diodes D_c and D_d) through an output filter inductor L_o. The negative output terminal v_{o-} is connected to a conventional phase leg (of switches S_7 and S_8). A small filtering and lossless snubber capacitor C is added across the phase legs.

A. Identical In-Phase and Antiphase Buck Voltage Operations

Fig. 2 shows the phase-shifted PWM modulation of in-phase and antiphase buck operations when $v_{\text{in}} > 0$. For $v_{\text{in}} < 0$, gating signals of two switches of the same phase leg are interchanged. Fig. 2(a) and (b) are for in-phase operation. Fig. 2(c) and (d) are for antiphase operation. Switches S_1 and S_4 are completely on and S_2 and S_3 are completely off for both operations. Input inductor L_{in} and capacitor C create an input LC filter, providing a high-quality input current, and $v_C = v_{\text{in}}$.

A reference signal V_a is compared with two antiphase (180° phase-shifted) triangular waveforms v_{tri1} and v_{tri2} to generate high-frequency gating signals for switches S_5 and S_6. The duty ratio in buck mode is D_{bu}. Switches S_7 and S_8 are operated at line frequency. For in-phase and antiphase outputs, gating signals of switches S_5–S_8 are inverted.

1) Circuit Operation for $0 < \boldsymbol{D_{bu}} < 0.5$: Switching signals for in-phase and antiphase operations are shown in Fig. 2(a) and (c), respectively.

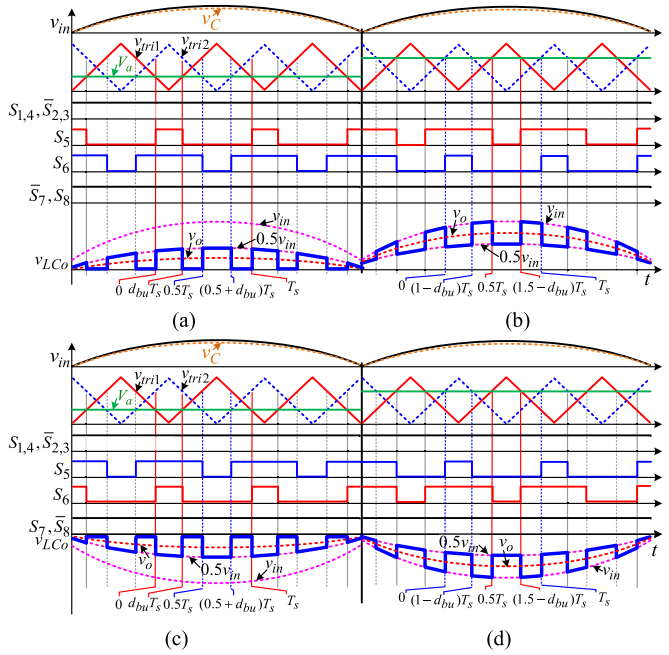


Fig. 2. Switching signals and significant waveforms for bipolar buck operation when $v_{\text{in}} > 0$. (a) and (b) are for in-phase operation. (a) $D_{bu} < 0.5$. (b) $D_{bu} > 0.5$. (c) and (d) are for antiphase operation. (c) $D_{bu} < 0.5$. (d) $D_{bu} > 0.5$.

I) *Interval-1 [0∼$D_{bu}T$]*: Fig. 3(a) shows the equivalent circuit for in-phase operation. Capacitor C provides energy to output inductor and load through switches S_5 and S_8. Common-mode current i_{cm2} of coupled inductor CL_2 flows through capacitor C and switches S_5 and S_6. For a unity turns ratio of coupled inductor, capacitor C voltage v_C $(= v_{\text{in}})$ is equally divided between two windings. The voltage level v_{LCo} of output LC filter is, therefore, equal to $v_{\text{in}}/2$

$$\begin{cases} v_{Lo} = 0.5v_{\text{in}} - v_o \\ \frac{di_{\text{cm2}}}{dt} = \frac{v_C(=v_{\text{in}})}{4L_m}\ ;\ \frac{di_{Lo}}{dt} = \frac{0.5v_{\text{in}} - v_o}{L_o} \end{cases} \quad \text{In}-\text{phase} \qquad (1)$$

Where L_m is the magnetizing inductance of a coupled inductor. For antiphase operation, as shown in Fig. 4(a), circuit operation is similar as explained for in-phase operation. However, switch S_7 is now turned on instead of S_8 and a negative capacitor voltage $-v_C$ is available across output LC filter. Therefore, we get

$$\{v_{Lo} = -0.5v_{\text{in}} - v_o \quad \text{Antiphase.} \qquad (2)$$

II) *Interval-2 [$D_{bu}T$∼0.5T]*: For in-phase operation [see Fig. 3(b)], capacitor C is disconnected from the output circuit and gets charged by v_{in}. Output inductor L_o provides energy to load through switch S_8 and diode D_d. Common-mode current i_{cm2} freewheels through switch S_6 and diode D_d. The voltage level v_{LCo} of output LC filter is equal to zero

$$\begin{cases} v_{Lo} = -v_o \\ \frac{di_{\text{cm2}}}{dt} = 0;\ \frac{di_{Lo}}{dt} = \frac{-v_o}{L_o} \end{cases} \quad \text{In}-\text{phase.} \qquad (3)$$

For antiphase operation [see Fig. 4(b)], inductor provides energy to load through switch S_7 and diode D_c. Common-mode current i_{cm2} freewheels through switch S_5 and diode D_c. Circuit equations remain the same as for in-phase operation.

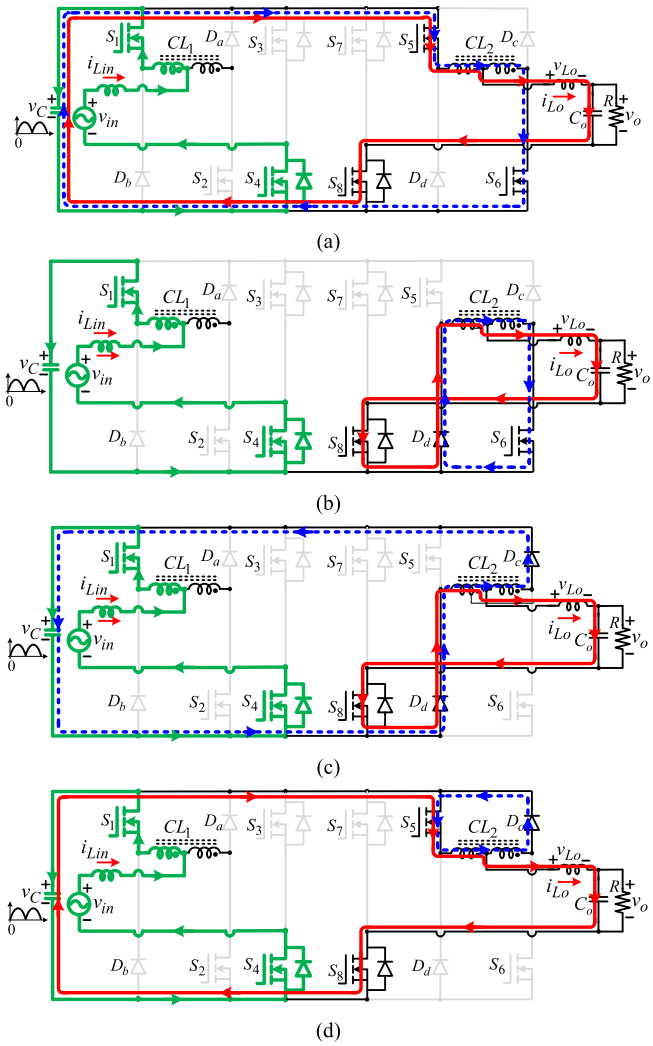


Fig. 3. Equivalent circuits for in-phase buck operation. (a) Interval-1. (b) Interval-2 and Interval-4. (c) Interval-3. (d) Interval-5.

III) *Interval-3 [0.5T∼$(0.5 + D_{bu})T$]*: For in-phase operation [see Fig. 3(c)], output inductor L_o keeps providing energy to load through switch S_8 and diode D_d. Common-mode current i_{cm2} flows from capacitor C through diodes D_c and D_d. Circuit equations remain same as in mode-1

$$\begin{cases} \frac{di_{\text{cm2}}}{dt} = -\frac{v_C\ (=v_{\text{in}}\ )}{4L_m} \end{cases} \quad \text{In}-\text{phase.} \qquad (4)$$

For antiphase operation [see Fig. 4(c)], the operation is same. The only difference is that the output inductor L_o current i_{Lo} flows through switch S_7 and diode D_c.

IV) *Interval-4 [$(0.5 + D_{bu})T$∼T]*: Operation in Interval-4 is exactly same as in Interval-2, corresponding to equivalent circuits of Figs. 3(b) and 4(b) for in-phase and antiphase operations, respectively.

The above discussion shows that for $0 < D_{bu} < 0.5$, the output LC filter voltage v_{LCo} varies between two levels: 0 and $v_{\text{in}}/2$.

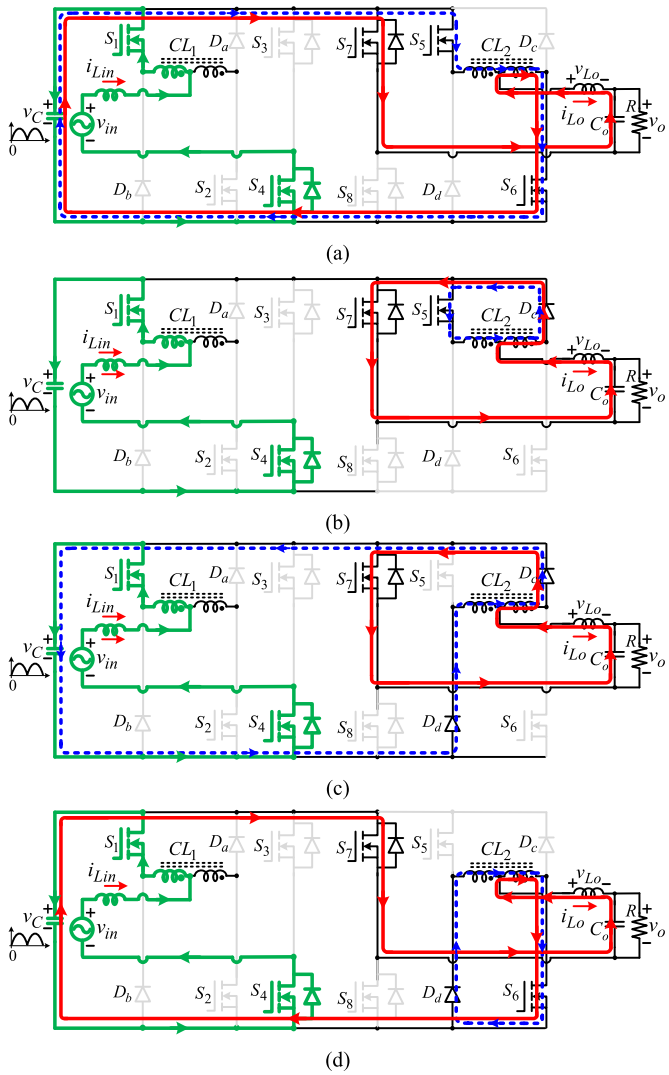


Fig. 4. Equivalent circuits for anti-phase buck operation. (a) Interval-1. (b) Interval-2 and Interval-4. (c) Interval-3. (d) Interval-5.

Moreover, the effective frequency of v_{LCo} is two times the actual operating frequency of switches S_5 and S_6.

2) *Circuit Operation for 0.5 < D_{bu} < 1*

Switching signals for in-phase and antiphase operations are shown in Fig. 2(b) and (d), respectively. For this duty ratio range, only one operation in Interval-5 occurs in conjunction with earlier explained operations in Interval-1 and Interval-3.

V) *Interval-5 [$(1-D_{bu})T \sim 0.5T$ and $(1.5-D_{bu})T \sim T$]*: For in-phase operation [see Fig. 3(d)], common-mode current i_{cm2} freewheels through switch S_5 and diode D_d. Voltage drop across coupled inductor is zero. This allows the complete capacitor *C* voltage v_C to apply across output *LC* filter, and $v_{LCo} = v_C = v_{\text{in}}$. Capacitor *C* provides energy to output inductor L_o and load

$$\begin{cases} v_{Lo} = v_{\text{in}} - v_o \\ \frac{di_{\text{cm2}}}{dt} = 0;\ \frac{di_{Lo}}{dt} = \frac{v_{\text{in}} - v_o}{L_o} \end{cases} \text{In-phase.} \quad (5)$$

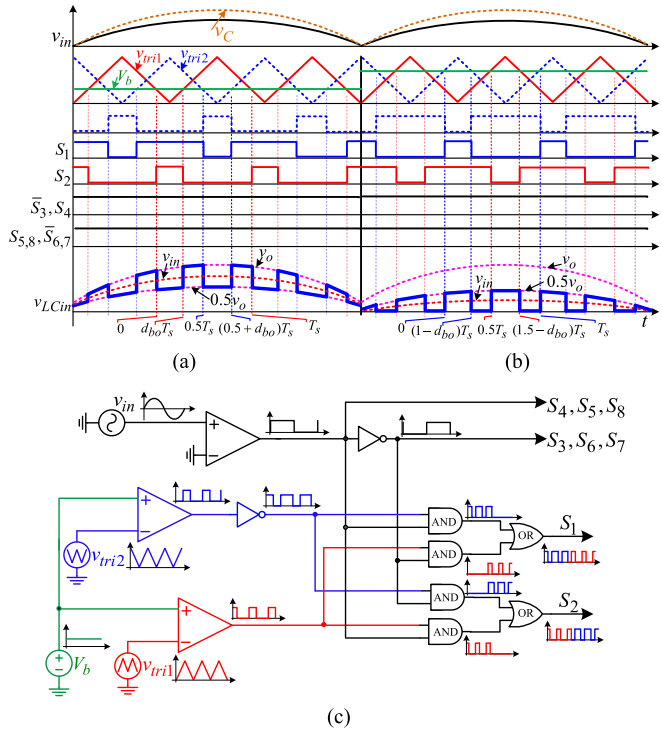


Fig. 5. Switching signals and significant waveforms for in-phase bipolar boost operation when $v_{\text{in}} > 0$. (a) $D_{bo} < 0.5$. (b) $D_{bo} > 0.5$. (c) Logic diagram for switching signals generation.

For antiphase operation, as shown in Fig. 4(d), circuit operation is similar as explained for in-phase operation. However, switches S_6 and S_7 are now turned on instead of switches S_5 and S_8, and reverse capacitor *C* voltage $-v_C$ is available across output *LC* filter. Therefore, the output inductor voltage becomes

$$\{v_{Lo} = -v_{\text{in}} - v_o \quad \text{Antiphase.} \quad (6)$$

The output *LC* filter voltage v_{LCo} varies between two levels: $v_{\text{in}}/2$ (Interval-1 and Interval-3) and v_{in}(Interval-5). Therefore, the output *LC* filter voltage has total three levels: 0, $v_{\text{in}}/2$, and v_{in}. The voltage across the output *LC* filter experiences double the switching frequency.

The voltage transfer ratio M_{bu} is given by

$$M_{bu} = \pm D_{bu} \quad (7)$$

where plus "+" sign is for in-phase operation and minus sign "−"is for antiphase operation.

B. *Identical In-Phase and Antiphase Boost Voltage Operations*

Fig. 5 shows the switching signals, key waveforms, and switch signal implementation for phase-shifted modulation for in-phase boost operation during the positive half-cycle of the input voltage $v_{\text{in}} > 0$. Fig. 5(a) and (b) shows the switching signals for boost duty ratios D_{bo} of $D_{bo} > 0.5$ and $D_{bo} < 0$, respectively. A reference signal V_b is compared with triangular carrier signal v_{tri1} to generate the PWM control signal of switch S_2. Same reference signal V_b is also compared with 180° phase-shifted triangular carrier signal v_{tri2} to generate the switching signal

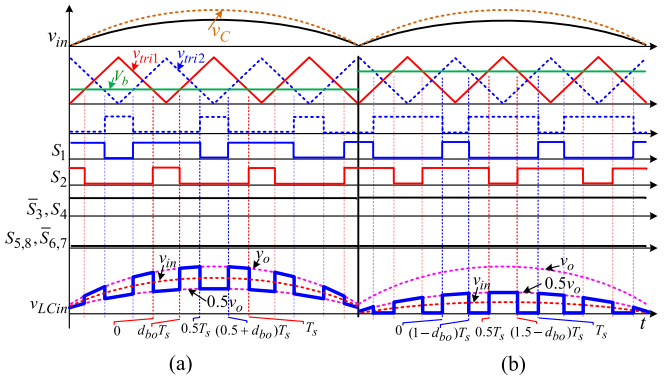


Fig. 6. Switching signals and significant waveforms for antiphase boost operation when $v_{\text{in}} > 0$. (a) $D_{bo} < 0.5$. (b) $D_{bo} > 0.5$.

for switch S_1. Switches S_4, S_5, and S_8 are completely turned on for $v_{\text{in}} > 0$, and switches S_3, S_6, and S_7 are fully turned off. For $v_{\text{in}} < 0$, the control signals of each switch are inverted. Fig. 5(c) shows the logic block diagram for the implementation of a phase-shifted PWM modulation strategy for in-phase boost operation. Fig. 6 shows the switching signals for antiphase boost operation.

For in-phase output, switches S_5 and S_8 are completely on and S_6 andS_7 are off. This creates an output LC filter (consisting of L_o and C_o) across capacitor C, and $v_C = v_o$. For antiphase operation, switches S_5 and S_8 are completely off and S_6 andS_7 are on. Thus, an output LC filter (L_oC_o) is again formed across capacitor C but with reversed voltage polarity $v_C = -v_o$. This produces high-quality output voltage with continuous output current.

1) Circuit Operation for $0 < \boldsymbol{D_{bo}} < 0.5$: Switching signals for in-phase and antiphase operations are shown in Figs. 5 and 6, respectively.

I) *Interval-1 [$0 \sim D_{bo}T$]*: Fig. 7(a) shows the equivalent circuit for in-phase operation. Input source v_{in} provides energy to input inductor L_{in} through switches S_2 andS_6. Common-mode current i_{cm1} flows through capacitor C and switches S_1 andS_6.

Positive capacitor C voltage is applied across output LC filter

$$\begin{cases} v_{L\text{in}} = \frac{v_{\text{in}} - 0.5v_o}{L_{\text{in}}} \\ \frac{di_{\text{cm1}}}{dt} = \frac{v_C(=v_o)}{4L_m}; \ \frac{di_{Lo}}{dt} = \frac{v_{\text{in}} - 0.5v_o}{L_{\text{in}}} \end{cases} \text{In} - \text{phase}. \quad (8)$$

For antiphase output, circuit operations are exactly the same. The only difference is that the reverse capacitor voltage is applied across the output LC filter, as shown in Fig. 8, and $v_C = -v_o$.

II) *Interval-2 [$D_{bo}T \sim 0.5T$]*: Input source v_{in} and inductor L_{in} provide energy to charging of capacitor C through switch S_6 and diode D_a, as shown in Fig. 7(b). Common-mode current i_{cm1} flows through switch S_1 and diode D_a

$$\begin{cases} v_{L\text{in}} = \frac{v_{\text{in}} - v_o}{L_{\text{in}}} \\ \frac{di_{\text{cm1}}}{dt} = 0; \ \frac{di_{Lo}}{dt} = \frac{v_{\text{in}} - v_o}{L_o} \end{cases} \text{In} - \text{phase}. \quad (9)$$

III) *Interval-3 [$0.5T \sim (0.5 + D_{bo})T$]*: Input source v_{in} and inductor L_{in} keep charging the capacitor C through switch S_6 and diode D_a[see Fig. 7(c)]. Common-mode current i_{cm1} flows through capacitor C and diodes D_a andD_b. Circuit equations

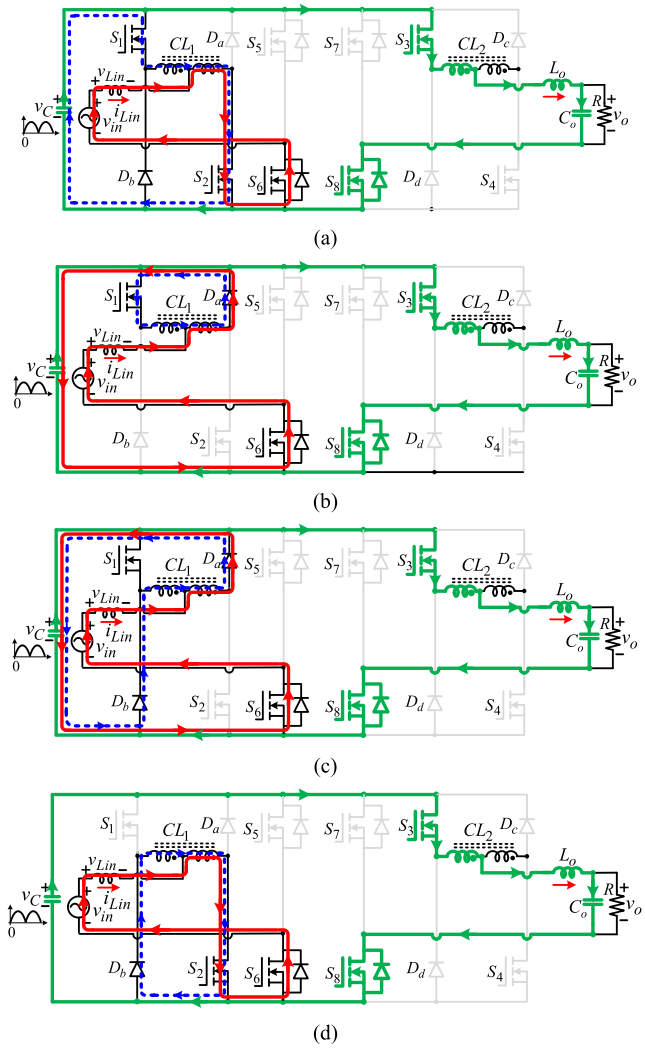


Fig. 7. Equivalent circuits for in-phase boost operation. (a) Interval-1. (b) Interval-2 and Interval-4. (c) Interval-3. (d) Interval-5.

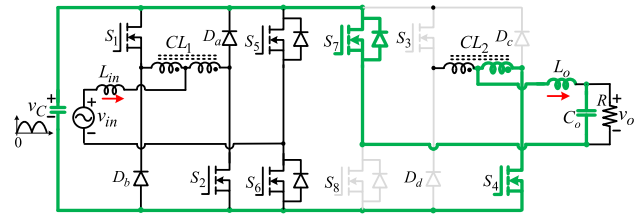


Fig. 8. Equivalent circuits for antiphase boost operation.

remain same as in Interval-2. Only this time, voltage of capacitor C is reversed across the coupled-inductor CL_1

$$\begin{cases} \frac{di_{\text{cm1}}}{dt} = -\frac{v_C\,(=v_o\,)}{4L_m} \end{cases} \text{In} - \text{phase}. \quad (10)$$

IV) *Interval-4 [$(0.5 + D_{bo})T \sim T$]*: The operation is exactly the same as in Interval-2. Input LC filter voltage $v_{LC\text{in}}$ has two levels: $v_o/2$ and v_o. Moreover, this filter voltage varies with twice the switching frequency.

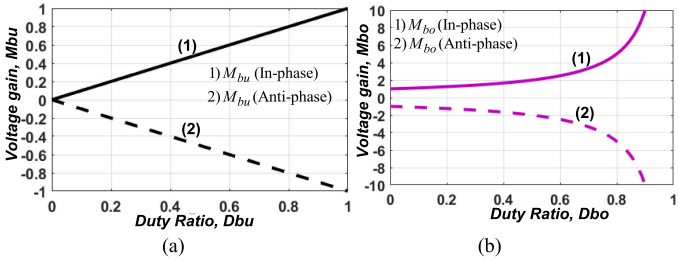


Fig. 9. Voltage gain versus switch duty ratios. (a) In-phase and antiphase buck operations. (b) In-phase and antiphase boost operations.

2) Circuit Operation for 0.5 < D_{bo} < 1: A new operation in Interval-5 exists in combination with operations in Interval-1 and Interval-3.

V) *Intervale-5 [$(1-D_{bo})T \sim 0.5T$ and $(1.5-D_{bo})T \sim T$]:* Input inductor L_{in} stores energy from input source v_{in} through switches S_2 and S_6[see Fig. 7(d)]. Common-mode current i_{cm1} freewheels through switch S_2 and diode D_b

$$\begin{cases} v_{L\text{in}} = \frac{v_{\text{in}}}{L_{\text{in}}} \\ \frac{di_{\text{cm1}}}{dt} = 0;\ \frac{di_{Lo}}{dt} = \frac{v_{\text{in}}}{L_{\text{in}}} \end{cases} \text{In}-\text{phase} \tag{11}$$

The input *LC* filter voltage $v_{LC\text{in}}$ has now two levels: 0 (Interval-5) and $v_o/2$ (Interval-1 and Interval-3). Therefore, the input *LC* filter voltage $v_{LC\text{in}}$ has a total of three levels: 0, $v_o/2$, and v_o. This voltage varies with twice the switching frequency.

The voltage transfer ratio M_{bo} for boost operation is given by

$$M_{bo} = \pm\frac{1}{1-D_{bo}} \tag{12}$$

where plus "+" sign is for in-phase operation and minus sign "−" is for antiphase operation. Fig. 9(a) and (b) shows the voltage gain plots for in-phase/antiphase buck and boost operations, respectively.

III. Flexible In-Phase and Antiphase Buck–Boost Voltage Operations

Fig. 10 shows the switch modulation for flexible in-phase [see Fig. 10(a) and (b)] and antiphase [see Fig. 10(c) and (d)] buck–boost voltage operations. Both dual-buck phase legs are modulated simultaneously and independently. There are eight operation scenarios based on the placement of buck and boost reference signals V_a and V_b. However, only two scenarios provide efficient buck–boost operation, i.e., when $\{(V_a > V_b) < 0.5)\}$ and $\{(V_a > V_b) > 0.5)\}$. This operation produces simultaneous three-level input and output voltages. The circuit operation is the combination of in-phase and antiphase buck and boost operations as explained earlier. Therefore, only in-phase operation is briefly described for $(V_a > V_b) < 0.5$.

A. Circuit Operation for $0 < D_{bu} < 0.5$ and $0 < D_{bo} < 0.5$

The equivalent circuits are shown in Fig. 11, corresponding to the switching signals of Fig. 10(a) and (b).

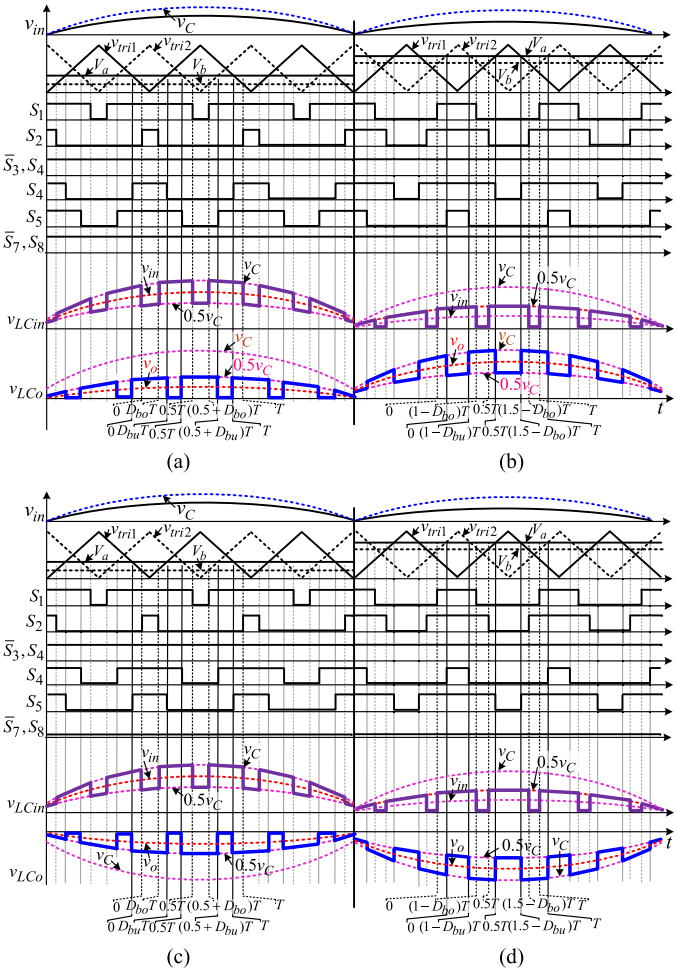


Fig. 10. Switching signals and significant waveforms for flexible bipolar buck–boost operation when $v_{\text{in}} > 0$. (a) and (b) are for in-phase operation. (a) $D_{bo} < 0.5$ and $D_{bu} < 0.5$. (b) $D_{bo} > 0.5$ and $D_{bu} < 0.5$. (c) and (d) are for antiphase operation. (c) $D_{bo} < 0.5$ and $D_{bu} < 0.5$. (d) $D_{bo} < 0.5$ and $D_{bu} < 0.5$.

1) *Interval-1 [$0 \sim D_{bu}T$ and $0 \sim D_{bo}T$]:* Input inductor L_{in} stores energy, and capacitor *C* provides energy to L_o and load [see Fig. 11(a)]. $v_{LC\text{in}} = v_C/2$ and $v_{LCo} = v_C/2$.
2) *Interval-2 [$0 \sim D_{bu}T$ and $D_{bo}T \sim 0.5T$]:* v_{in} and L_{in} provide energy to charge capacitor *C* [see Fig. 11(b)]. Capacitor *C* keeps providing energy to L_o and load. $v_{LC\text{in}} = v_C$, and $v_{LCo} = v_C/2$.
3) *Interval-3 [$D_{bu}T \sim 0.5T$ and $D_{bo}T \sim 0.5T$]:* Capacitor *C* keep charging from v_{in} and L_{in} [see Fig. 11(c)]. L_o starts providing energy to load. $v_{LC\text{in}} = v_C$, and $v_{LCo} = 0$.
4) *Interval-4 [$0.5D_{bu}T \sim (0.5+D_{bu})T$ and $D_{bo}T \sim 0.5T$]:* L_o gets charged from coupled-inductor CL_2 [see Fig. 11(d)]. Capacitor *C* keeps charging as previously. $v_{LC\text{in}} = v_C$, and $v_{LCo} = v_C/2$.
5) *Interval-5 [$0.5D_{bu}T \sim (0.5+D_{bu})T$ and $0.5D_{bo}T \sim (0.5+D_{bo})T$]:* L_{in} stores energy [see Fig. 11(e)]. L_o keeps charging. $v_{LC\text{in}} = v_C/2$, and $v_{LCo} = v_C/2$.
6) *Interval-6 [$0.5D_{bu}T \sim (0.5+D_{bu})T$ and $(0.5+D_{bo})T \sim T$]:* The operation is exactly the same as in Interval-4.

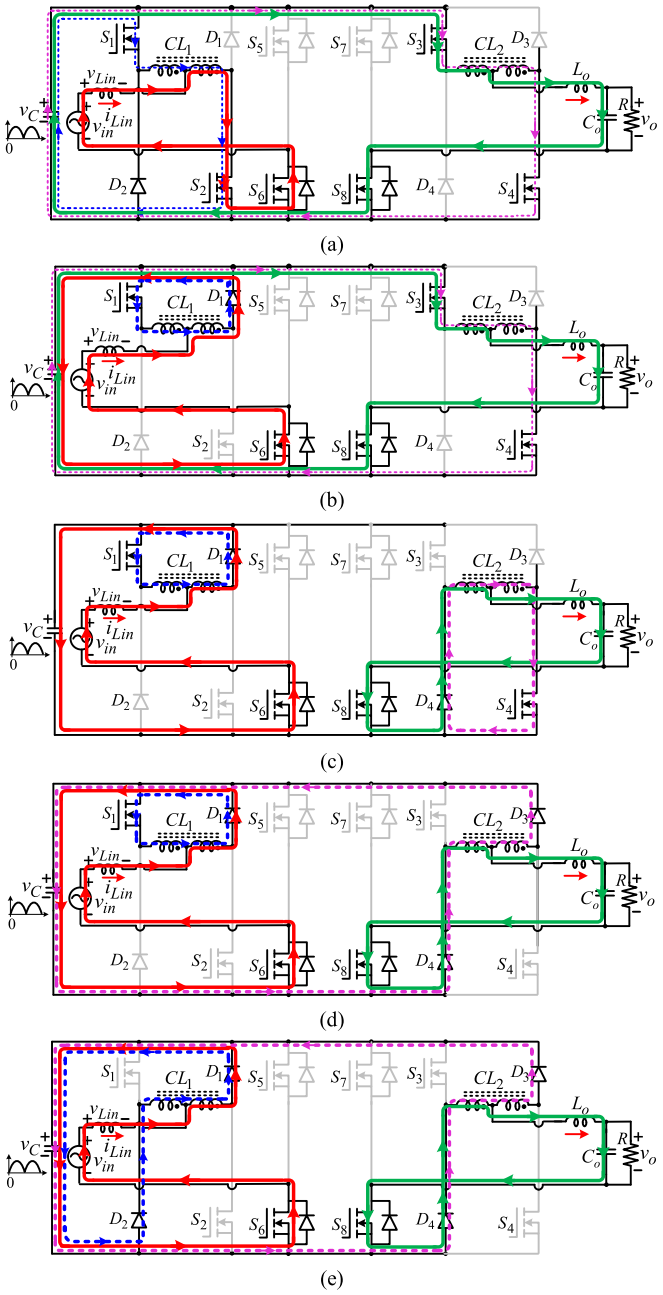


Fig. 11. Equivalent circuits for flexible in-phase operation. (a) Interval-1. (b) Interval-2 and Interval-8. (c) Interval-3 and Interval-7. (d) Interval-4 and Interval-6. (e) Interval-5.

7) *Interval-7 [$(0.5 + D_{bu})T \sim T$ and $(0.5 + D_{bo})T \sim T$]*: It is the same as Interval-3.
8) *Interval-8 [$T \sim 2D_{bu}T$ and $(0.5 + D_{bo})T \sim T$]*: It is the same as Interval-2.

The voltage transfer ratio M_{bb} for flexible buck–boost operation is given by

$$M_{bb} = \pm \frac{D_{bu}}{1 - D_{bo}}. \tag{13}$$

A 3-D plot of voltage gain M_{bb} variations with D_{bu} and D_{bo} is shown in Fig. 12 for in-phase operation. Various combinations

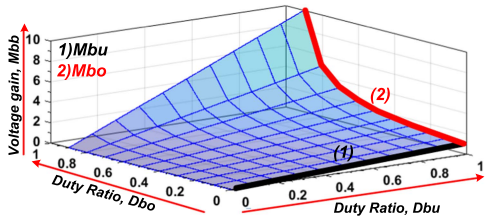


Fig. 12. Three-dimensional plot of voltage gain variations against converter duty ratios D_{bu} and D_{bo}.

TABLE I
CURRENT AND VOLTAGE RIPPLES/STRESSES OF COMPONENTS

Parameter		NIBu	NIBo
Switching devices	v_S	v_{in}	v_o
	i_S	i_o	i_{in}
Capacitor	v_C	v_{in}	v_o
	Δv_C	0	$\frac{i_o D_b T}{C}$
Coupled inductors	I_{cm}	$i_o/2$	$i_{in}/2$
	Δi_{cm}	$\frac{v_{in}}{4 f_s L_s} D$	$\frac{v_o}{4 f_s L_s} D$
Inductors	i_L	$i_{Lin} = i_{in}$, $i_{Lo} = i_o$	$i_{Lin} = i_{in}$, $i_{Lo} = i_o$
	Δi_L	$\Delta i_{Lo} = \frac{(0.5-D) v_o T}{L_o}$, $\frac{(1-D)(D-0.5) v_o T}{L_o}$	$\Delta i_{Lin} = \frac{(0.5-D) D v_o T}{L_{in}}$, $\frac{(1-D)(D-0.5) v_o T}{L_{in}}$

of buck and boost duty ratios (D_{bu} and D_{bo}) exist to achieve the same voltage gain. However, for optimal performance during buck operation, the boost duty ratio D_{bo} can be set to 0 (switches S_1 andS_2 are modulated at line frequency). The resultant buck gain curve M_{bu} is highlighted by the bold black line in Fig. 12. Similarly, for optimal boost operation, the buck duty ratio is set to 1 (switches S_5 andS_6 are modulated at line frequency), and the resultant boost gain curve M_{bo} is highlighted by the bold red line on the graph in Fig. 12.

IV. COMPONENT STRESSES/RIPPLES AND DESIGN DISCUSSION

Table I provides component voltage/current stresses and ripples of the proposed converter.

A. Switching Devices Voltage/Currents Stresses

Switch voltage/current stresses v_S /i_S are given by

$$\begin{cases} v_s^{\text{Buck}} = \frac{v_o}{M},\ v_s^{\text{Boost}} = v_o \\ i_s^{\text{Buck}} = i_o,\ i_s^{NIBo} = i_o\, M. \end{cases} \tag{14}$$

Maximum switch voltage stresses are experienced in buck operation when the input voltage is at its highest level. Switch current stresses are maximum when the input voltage is minimum.

B. Capacitor Design

Capacitor C voltage stress V_c is the same as switch voltage stress in (13). Capacitor voltage ripples are given by

$$\left\{ \Delta v_c^{\text{Buck}} \approx 0\ ,\ \Delta\, v_c^{\text{Boost}} = \frac{(M-1)}{M}\ \frac{i_o}{f_s C}. \right. \tag{15}$$

The maximum capacitor voltage ripple Δv_c occurs for minimum input voltage. By limiting this voltage ripple Δv_c to $x\%$ of V_c, the required capacitor value C can be determined.

C. Inductor Design

The common-mode dc-offset current $I_{\rm cm}$ and common-mode current ripples $\Delta i_{\rm cm}$ of coupled inductors are given by

$$\begin{cases} I_{\rm cm2} = \frac{i_o}{2}, \ I_{\rm cm1} = \frac{i_o G}{2} \\ \Delta\, i_{\rm cm2} = \frac{v_o}{4 f_s L_s}\, G, \ \Delta\, i_{\rm cm1} = \frac{v_o}{4 f_s L_s}\, \frac{(G-1)}{G^2}. \end{cases} \tag{16}$$

Coupled-inductor CL_1 has maximum offset current when the gain is maximum. The dc-offset current of CL_2 is independent of voltage gain. Self-inductances L_s of CL_1 and CL_2 can be selected to restrict their maximum current ripple to $y\%$ of offset currents $I_{\rm cm}$.

Input and output inductors $L_{\rm in}$ and L_o have current stresses I_L of $i_o G$ and i_o, respectively. Current ripples Δi_L of these inductors are given by

$$\begin{cases} \Delta i_{Lo} \ = (0.5 - G)\ \frac{v_o T}{f_s L_o}, \\ \Delta i_{L\rm in} \ = \frac{\left(1.5G - 0.5G^2 - 1\right)}{G^2}\ \frac{v_o T}{f_s L_o}. \end{cases} \tag{17}$$

By limiting the inductor current ripples to $y\%$ of their current stresses I_L, inductor values L can be selected.

D. Switch Device Selection and Passive Component Design

The operating conditions of the experimental prototype are given by $v_{\rm in} = 70 \sim 282\, V_{\rm rms}$, $v_o = 110\, V_{\rm rms}$, $P_o = 400$ W, and $f_s = 50$ kHz.

1) Maximum switch voltage stress $V_{S/D,\max}$ is equal to the peak value of the maximum input voltage $\sqrt{2} v_{\rm in,max} = 400$ V.
2) The maximum device current $I_{S/D,\max}$ (considering inductor current ripple) is given by

$$I_{S/D,\max} = \frac{3\sqrt{2}\, i_{\rm in,max}}{2} + \frac{v_o\, D_{bo}}{4 f_s L_s} = 13.54 \text{ A}. \tag{18}$$

In practice, MOSFETs model number 47N60CFD (600 V/46 A) and diodes RHRG3060 (600 V/30 A), as already available in the laboratory, were selected for the experiments.

3) Input inductor $L_{\rm in}$ directly affects the input current ripple and power quality. The value of the input inductor $L_{\rm in}$ is calculated to limit its current ripple $\Delta i_{L\rm in}$ to within 10% of the input current $i_{\rm in}$, as given by

$$L_{\rm in} = \frac{\sqrt{2} V_{o,\rm rms}\, (0.5 - D_{bo})\, D_{bo}}{\Delta i_{L\rm in}\, f_s} = 191\ \mu\text{H}. \tag{19}$$

In practice, an input inductor of 200 μH is used.

4) The capacitor C value can be calculated to maintain its voltage ripple Δv_C to 10% of its voltage stress v_C, as given by

$$C = \frac{\sqrt{2} I_{o,\rm rms} D_{bo}}{\Delta v_C\, f_s} = 2.4\ \mu\text{F}. \tag{20}$$

In practice, a 2.2 μF capacitor is used and the voltage ripple is allowed to be a little larger than 10% since this is again filtered by the output LC filter.

5) The value of output inductor $L_{\rm in}$ can be selected to maintain its current ripple Δi_{Lo} to 30% of output current i_o as

$$L_o = \frac{\sqrt{2} I_{o,\rm rms}\, (0.5 - D_{bo})}{\Delta i_{Lo}\, f_s} = 216\ \mu\text{H}. \tag{21}$$

In practice, an output inductor of 200 μH is used.

Output capacitor voltage ripple Δv_{Co} directly affects the load power quality. Its value is calculated to maintain its voltage ripple to 2% of the output voltage as

$$C_o = \frac{\Delta i_{Lo}}{8 \Delta v_o\, f_s} = 1.3\ \mu\text{H}. \tag{22}$$

A 2.2 μF film capacitor is used to implement the output filter capacitor.

V. Comparison With State-of-the-Art Coupled-Inductor-Based Three-Level AC–AC Converters

The cascaded-type [18], [19] and flying-capacitor [20], [21], [22] three-level ac–ac converters have commutation issues. Moreover, the former requires a greater number of components and the latter requires voltage balancing of flying capacitors. A comparison of the proposed and existing state-of-the-art dual-buck and coupled-inductor ac–ac converters [24], [26] is provided in Table II. The inverting buck–boost-type three-level converter [24] requires only two dual-buck phase legs with two coupled inductors. However, it provides only inverting buck–boost operation with higher component stresses/ripples and poor efficiency. The following research [26] proposed a bipolar three-level ac–ac converter. However, it requires three dual-buck phase legs with three coupled inductors. Also, it has nonidentical buck–boost voltage outputs and inefficient inverting buck–boost operation (with higher component stresses, ripples, and losses). The proposed converter requires only two dual-buck phase legs with two coupled inductors compared with [26]. Moreover, it can produce identical-bipolar buck and boost voltage processes, which are highly efficient with much lower voltage current stresses and ripples of components.

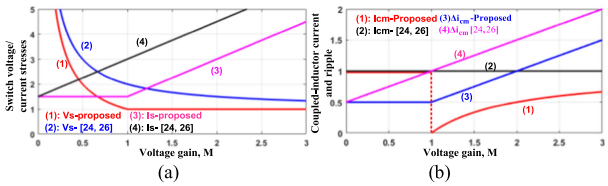
The switch voltage/current stresses v_s/i_s of the conventional converters [24], [26] are given by

$$\begin{cases} v_s = \frac{(M+1)\, v_o}{M}, \ i_s = \frac{3\,(M+1)}{2}\, i_o\,. \end{cases} \tag{23}$$

The normalized switch voltage and current stresses (v_s/v_o and i_s/i_o) of the proposed and conventional converters are plotted in Fig. 13(a) as a function of voltage gain. As observed, the proposed converter can significantly reduce switching devices' voltage/current stresses. Therefore, it would require less costly switching devices with better performance. The normalized common-mode dc-offset current $I_{\rm cm}$ and current ripple $\Delta i_{\rm cm}$ of coupled inductor of the proposed and counterpart converters are plotted in Fig. 13(b). As observed, the proposed converter has a smaller current handling requirement and inductance value, indicating that it can reduce magnetic requirements. Table II

TABLE II
COMPARISON OF THE PROPOSED AND EXISTING THREE-LEVEL AC–AC CONVERTERS

Parameters	Unipolar flying capacitor [21]	Unipolar dual buck [24]	Bipolar dual buck [26]	Proposed identical-bipolar dual-buck
Voltage gain, $M(=\frac{v_o}{v_{in}})$	$\frac{d}{1-d}$	$\frac{d}{1-d}$	$d_{bu}, \frac{1}{1-d_{bo}}$ $\frac{d_{bb}}{1-bb}$	$\pm d_{bu}, \pm\frac{1}{1-d_{bo}}$
Bipolar buck–boost operation	Unipolar buck–boost	Unipolar buck–boost	Bipolar buck–boost	Bipolar buck–boost
Identical-bipolar buck–boost process	N/A	N/A	No	Yes
No. of switches	$8(S_1-S_8)$	$4(S_1-S_4)$	$6\ (S_1-S_6)$	$8\ (S_1-S_8)$
No. of diodes	0	$4(D_1-D_4)$	$6\ (D_1-D_6)$	$4\ (D_1-D_4)$
No. of dual-buck phase legs	NA	2	3	2
No. of coupled inductors	0	$2(CL_1, CL_2)$	$3(CL_1-CL_3)$	$2(CL_1, CL_2)$
No of inductors	$1(L)$	$1(L)$	$2(L_{\text{in}}, L_o)$	$2(L_{\text{in}}, L_o)$
Switch voltage stress v_s	$v_{\text{in}}+v_o$	$v_{\text{in}}+v_o$	$v_{\text{in}}+v_o$	v_{in} or v_o
Switch current stress i_s	$i_{\text{in}}+i_o$	$\frac{3(i_{\text{in}}+i_o)}{2}$	$\frac{3(i_{\text{in}}+i_o)}{2}$	$\frac{3i_{\text{in}}}{2}$ or $\frac{3i_o}{2}$
DC-off set currents I_{cm} of coupled inductors	NA	$\frac{i_{\text{in}}+i_o}{2}$	$\frac{i_{\text{in}}+i_o}{2}$	$\frac{i_{\text{in}}}{2}$ or $\frac{i_o}{2}$
Current ripple of coupled inductor Δi_{cm}	N/A	$\frac{v_{\text{in}}+v_o}{4f_sL_s}D_{bb}$	$\frac{v_{\text{in}}+v_o}{4f_sL_s}D_{bb}$	$\frac{v_o}{4f_sL_s}D_{bu}$ or $\frac{v_{\text{in}}}{4f_sL_s}D_{bo}$
Commutation issue	Yes	No	No	No
Input current	Discont.	Discont.	Continuous	Continuous
Output current	Discont.	Discont.	Continuous.	Continuous
Measured efficiency (η)	v_{in}=242 V v_o=220 V η =85.4 % v_{in}=198 V v_o=220 V η =85 %	v_{in}=150 V v_o=110 V η =92.8 % v_{in}=70 V v_o=110 V η =90.6 %	v_{in}=150 V v_o=110 V η =93.3 % v_{in}=70 V v_o=110 V η =90.9 %	v_{in}=150 V v_o=110 V η =95.2% v_{in}=70 V v_o=110 V η =93.9 %



(a) (b)

Fig. 13. Comparison plots of the proposed and conventional converters. (a) Switch voltage and current stresses of the proposed and conventional converters. (b) Common-mode current and current ripples of coupled inductor.

also provides a comparison of the experimental reported efficiencies of the proposed converter and counterpart converters [21], [24], [26] alongside the respective operating conditions. As anticipated, the proposed converter demonstrates notably higher power conversion efficiency.

VI. LOSS ANALYSIS OF THE PROPOSED CONVERTER

Table III provides a detailed information of component voltage/current stresses and respective time intervals for the determination of their various losses.

TABLE III
CONDUCTION CURRENTS AND BLOCKING VOLTAGES OF COMPONENTS WITH RESPECTIVE TIME INTERVALS

In-phase Buck Operation				In-phase Boost Operation			
	Current/ voltage		Interval		Current/ voltage		Interval
S_1, S_4	i_s	i_oM_{bu}	T_s	S_1	i_s	i_oM_{bo}	$(1-D_{bo})T_s$
					v_s	v_o	$D_{bo}T_s$
S_5	i_s	$\frac{3i_o}{2}$	$D_{bu}T_s$	S_2	i_s	$\frac{3i_oM_{bo}}{2}$	$D_{bo}T_s$
	v_s	$\frac{v_o}{M_{bu}}$	$(1-D_{bu})T_s$		v_s	v_o	$(1-D_{bo})T_s$
S_6	i_s	$\frac{i_o}{2}$	$(1-D_{bu})T_s$	D_a	i_s	$\frac{3i_oM_{bo}}{2}$	$(1-D_{bo})T_s$
	v_s	$\frac{v_o}{M_{bu}}$	$D_{bu}T_s$		v_s	v_o	$D_{bo}T_s$
D_c	i_s	$\frac{i_o}{2}$	$D_{bu}T_s$	D_b	i_s	$\frac{i_oM_{bo}}{2}$	$D_{bo}T_s$
	v_s	$\frac{v_o}{M_{bu}}$	$(1-D_{bu})T_s$		v_s	V_o	$(1-D_{bo})T_s$
D_d	i_s	$\frac{3i_o}{2}$	$(1-D_{bu})T_s$	S_3, S_8	i_s	i_o	T_s
	v_s	$\frac{v_o}{M_{bu}}$	$D_{bu}T_s$				
S_8	i_s	i_o	T_s	S_6	i_s	i_oM_{bo}	T_s
L_{in}	i_L	i_oM_{bu}	T_s	L_{in}	i_L	i_oM_{bo}	T_s
	v_L	0	T_s		v_L	$(0.5-D_{bo})v_o$	$D_{bo}T_s$
C	i_c	0	T_s	C_i	i_c	I_o	$D_{bo}T_s$
						I_{in}	$(1-D_{bo})T_s$
L_o	i_L	i_o	T_s	L_o	i_L	I_o	T_s
	v_L	v_o	$(0.5-D_{bu})T_s$		v_L	0	T_s

A. Semiconductor Device Losses

The resistive conduction loss P_{sc} of MOSFETs can be determined as

$$P_{sc} = (I_{s,\text{rms}})^2\, r_{\text{DS,on}} \tag{24}$$

where $r_{\text{DS,on}}$ is the drain–source on-resistance of MOSFET and $I_{s,\text{rms}}$ is its rms current.

Switching loss of line-frequency MOSFETs is negligible. On the other hand, switching losses P_{sw} of high-frequency MOSFETs are mainly originated from the discharge of their junction capacitors C_{oss} during turn-on [27], as given by

$$P_{\text{sw}} = f_s\, .\, E_{oss}\,(V_s) \tag{25}$$

where f_s is the switching frequency and E_{oss} is the capacitive turn-on energy, which can be determined from MOSFET data sheet as a function of its blocking voltage V_s.

The conduction losses P_{Dc} of external diodes can be determined as

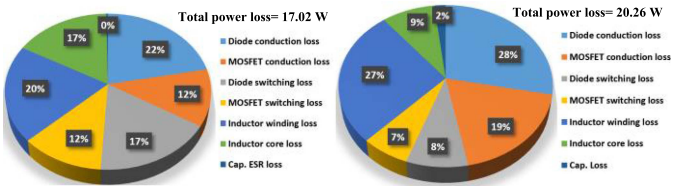
$$P_{Dc} = U_{Do}\, I_{D,\text{avg}} + (I_{D,\text{rms}})^2 r_D \tag{26}$$

where U_{Do} is the fixed voltage drop of diode and r_D is the forward resistance of the diode.

The diode switching loss P_{Drr} mainly comes from its reverse recovery as given by

$$P_{Drr} = \frac{1}{4}\, f_s.\, I_{rr}.\, V_D.\, t_b \tag{27}$$

where $V_D$is the diode blocking voltage, I_{rr} is the diode reverse recovery current, and t_b is the time duration of reverse recovery.



(a) (b)

Fig. 14. Loss breakdown of switching devices of the proposed converter. (a) NIBu operation. (b) NIBo operation.

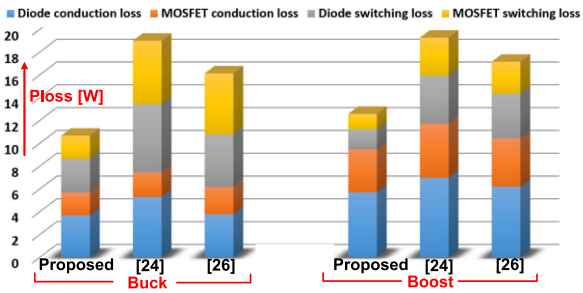


Fig. 15. Comparison of semiconductor device losses of the proposed and coupled-inductor-based three-level counterpart converters.

B. Passive Component Losses

Winding conduction losses P_{wc} of inductors can be found by

$$P_{\text{wc}} = (I_{w,\text{rms}})^2 \, r_L \tag{28}$$

where r_L is the inductor copper resistance and $I_{w,\text{rms}}$ is the rms current flowing through inductor winding.

The core loss P_{core} of inductor can be found through the following formula:

$$P_{\text{core}} \cong K_{fe} A_m l_m (\Delta B)^a. \tag{29}$$

In (28), the coefficient K_{fe} is associated with the frequency of operation. A_m and l_m represent the magnetic cross-sectional area and its mean magnetic path length, respectively. ΔB denotes the fluctuation in flux density, while "a" is a parameter obtained from the technical specifications provided by the core manufacturer.

The equivalent series resistance (ESR) conduction loss $P_{\text{ESR}c}$ of capacitor C is given by

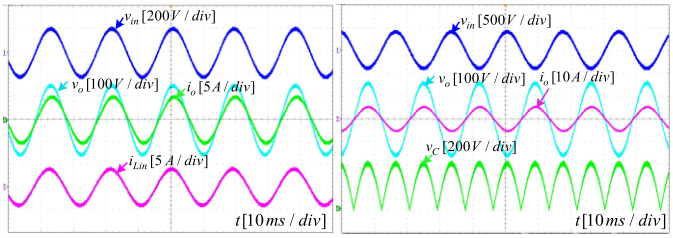
$$P_{\text{ESR}c} = (I_{c,\text{rms}})^2 \, r_C \tag{30}$$

where r_C is the ESR of the capacitor and $I_{c,\text{rms}}$ is the rms current flowing through the capacitor.

Fig. 14 provides a component loss breakdown of the proposed converter for the operating conditions of $v_o = 110$ V_{rms}, $P_o = 400$ W, and $f_s = 50$ kHz. Fig. 14(a) shows the loss breakdown for buck operation when $v_{\text{in}} = 150$ V_{rms}. Fig. 14(b) shows the loss breakdown for boost operation when $v_{\text{in}} = 70$ V_{rms}. As observed, total power loss is higher in boost operation due to significantly higher conduction loss of components with an increase in input current. Fig. 15 shows the comparison of MOSFET and diode conduction and switching losses of the proposed and counterpart converter for buck operation ($v_{\text{in}} = 150$ V_{rms}) and boost operation ($v_{\text{in}} = 70$ V_{rms}) when $P_o = 400$ W and $f_s = 50$ kHz. As observed, the proposed converter has much smaller conduction and switching losses and overall semiconductor device losses.

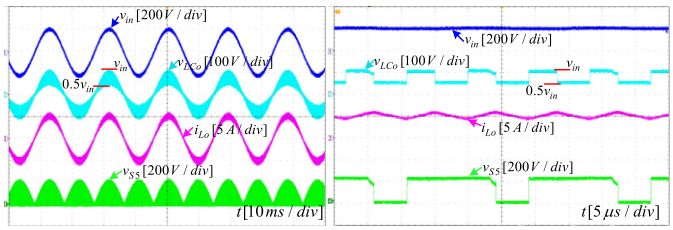
TABLE IV
COMPONENT VALUES AND ELECTRICAL CONDITIONS

Input ac supply voltage (v_{in})		(70~282) V_{rms}
Output voltage (v_o)		110 V_{rms}
Load power rating (P_o)		400 W
Switching frequency (f_s)		50 kHz
External diodes ($D_1 - D_4$)		RHRG3060
MOSFETs devices ($S_1 - S_8$)		47N60CFD
Capacitor C		2.2 μF
Coupled-inductors (CL_1, CL_2)		L_s =150 μH
Input–output filters	L_{in}, L_o	200 μH, 200 μH
	C_{in}, C_o	1 μF, 1 μF



(a) (b)

Fig. 16. Experimental waveforms for buck operation with RL load ($R = 31\ \Omega$ and $L = 5$ mH). (a) In-phase output when $v_{\text{in}} = 150$ V_{rms} and $D_{bu} < 0.5$. (b) Antiphase output when $v_{\text{in}} = 280$ V_{rms} and $D_{bu} > 0.5$.



(a) (b)

Fig. 17. In-phase buck operation when $v_{\text{in}} = 150$ V_{rms} and $D_{bu} < 0.5$ for RL load ($R = 31\ \Omega$ and $L = 5$ mH). (a) v_{LCo}, i_{Lo}, and v_{S5}. (b) Zoom-in waveforms of (a).

VII. EXPERIMENTAL RESULTS

A laboratory circuit of the proposed converter is assembled based on the operating conditions in Table IV. A DSP-kit number TMS320F28335 is used to generate eight switch control pulses for both buck and boost operations. Input voltage sensing and zero-crossing detection were performed using a voltage transducer LV-25P, enabling correct switching sequences for each half-cycle. The switches were then driven by eight switch control pulses from the DSP kit through gate drivers. Figs. 16–19 show the experimental tests for in-phase and antiphase buck operations. Fig. 16(a) shows the practical waveforms of the supply voltage v_{in}, input inductor current i_{Lin}, output voltage v_o, and output current i_o for in-phase buck operation to produce $v_o = 110$ V_{rms} from $v_{\text{in}} = 150$ V_{rms}. The switch duty ratio is $D_{bu} = 0.73$. Figs. 17 and 18 show the corresponding circuit waveforms for in-phase buck operation. Fig. 17(a) shows the waveforms of voltage across output LC filter v_{LCo}, output

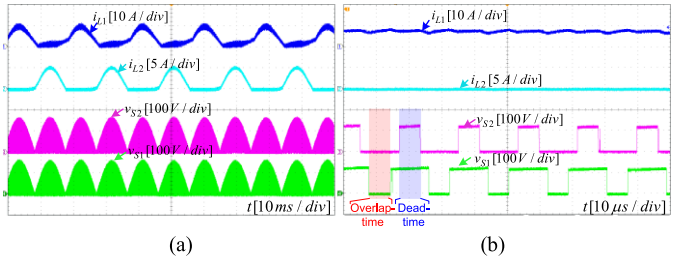


Fig. 18. In-phase buck operation when $v_{\text{in}} = 150\ \text{V}_{\text{rms}}$ and $D_{bu} < 0.5$. (a) v_{LCo}, i_{Lo}, and v_{S5}. (b) Zoom-in waveforms of (a).

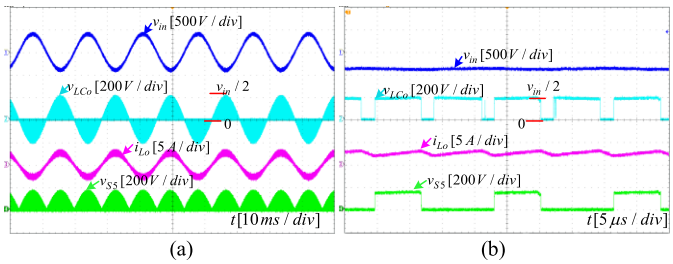


Fig. 19. Antiphase buck operation when $v_{\text{in}} = 282\ \text{V}_{\text{rms}}$ and $D_{bu} < 0.5$. (a) v_{LCo}, i_{Lo}, and v_{S5}. (b) Zoom-in waveforms of (a).

inductor current i_{Lo}, and switch S_5 voltage stress. Fig. 17(b) shows the enlarged waveforms of Fig. 17(a). As observed, the voltage v_{LCo} across output LC filter has two levels of $v_{\text{in}}/2$ and v_{in} (for $D_{bu} < 0.5$) with twice the switching frequency. Fig. 18(a) shows the winding currents i_{L1} and i_{L2} of coupled inductors C_{L1} and C_{L2}, and switch voltage stresses for in-phase buck operation. Fig. 18(b) shows the enlarged waveforms of Fig. 18(a). As observed, during PWM deadtime and overlap time in switching signals of S_5 and S_6, the winding currents i_{L1} and i_{L2} (which are the same as the current passing through switches S_1 and S_2) show no overshoot, proving that capacitor C has no shoot-through issue. Moreover, during the deadtime interval, switches S_1 and S_2 voltages show no overshoots, proving the inherent protection of the converter. Fig. 16(b) shows the practical waveforms of supply voltage v_{in}, output voltage v_o, output current i_o, and capacitor C voltage for antiphase buck operation to produce $v_o = 110\ \text{V}_{\text{rms}}$ from $v_{\text{in}} = 282\ \text{V}_{\text{rms}}$. Switch duty ratio is now reduced to $D_{bu} = 0.392$. Fig. 19(a) shows the waveforms of voltage across the output LC filter v_{LCo}, output inductor current i_{Lo}, and switch S_5 voltage stress for antiphase buck operation. Fig. 19(b) shows the enlarged waveforms of Fig. 19(a). As observed, the voltage v_{LCo} across output LC filter has two levels of 0 and $v_{\text{in}}/2$, for $D_{bu} > 0.5$. v_{LCo} and i_{Lo} again experience twice the ripple frequency than high-frequency switch S_6.

Figs. 20–22 show the experimental results for in-phase and antiphase boost operations. Fig. 20(a) shows the measured waveforms of the supply voltage v_{in}, output voltage v_o, output current i_o, and input inductor current i_{Lin} for in-phase boost operation to produce $v_o = 110\ \text{V}_{\text{rms}}$ from low input voltage of $v_{\text{in}} = 70\ \text{V}_{\text{rms}}$. The switch duty is adjusted to $D_{bo} = 0.36$. Fig. 20(b) shows the measured waveforms of input supply voltage v_{in}, output voltage v_o, output current i_o, and capacitor C voltage for antiphase boost

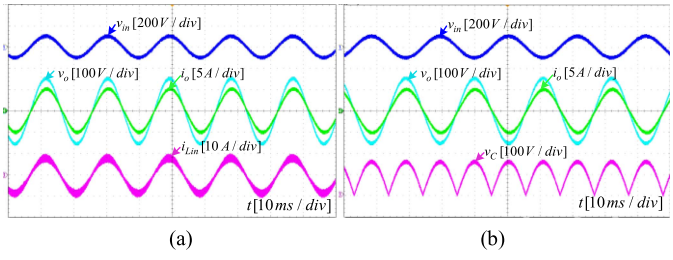


Fig. 20. Experimental waveforms for boost operation for resistive load when $v_{\text{in}} = 70\ \text{V}_{\text{rms}}$ and $D_{bo} < 0.5$. (a) In-phase output voltage. (b) Antiphase output voltage.

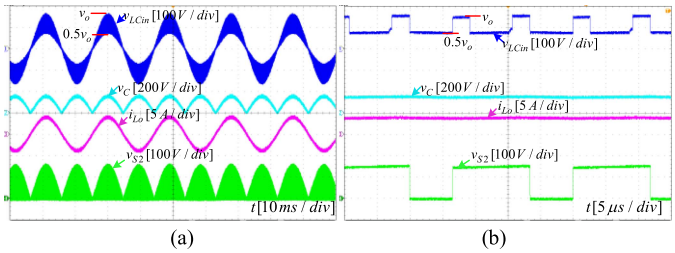


Fig. 21. In-phase boost operation for resistive load when $v_{\text{in}} = 70\ \text{V}_{\text{rms}}$ and $D_{bo} < 0.5$. (a) v_{LCin}, v_C, i_{Lo}, and v_{S2}. (b) Zoom-in waveforms of (a).

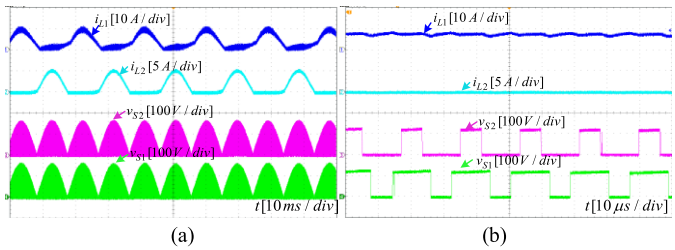
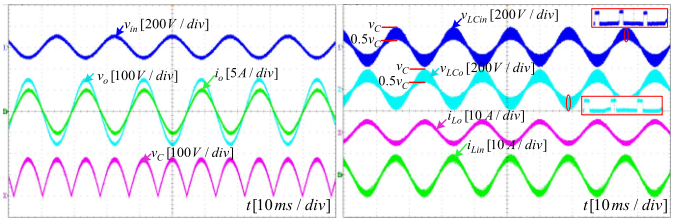


Fig. 22. In-phase boost operation for resistive load when $v_{\text{in}} = 70\ \text{V}_{\text{rms}}$ and $D_{bo} < 0.5$. (a) i_{L1}, i_{L2}, v_{S1}, and v_{S2}. (b) Zoom-in waveforms of (a).

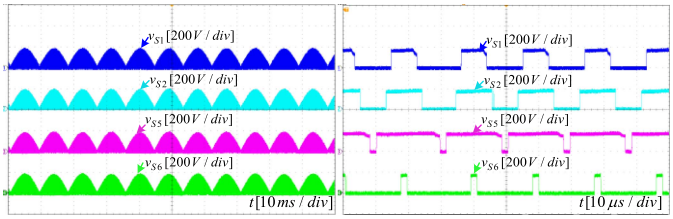
operation when $v_{\text{in}} = 70\ \text{V}_{\text{rms}}$ and $v_o = 110\ \text{V}_{\text{rms}}$. The same switch duty ratio of $D_{bo} = 0.36$ is required. Fig. 21(a) shows the waveforms of voltage v_{LCin} across input LC filter, capacitor C voltage, output inductor current i_{Lo}, and switch S_2 voltage. Fig. 21(b) shows the high-frequency waveforms of Fig. 21(a). The input LC filter voltage v_{LCin} has two voltage levels of $v_o/2$ and v_o for $D_{bo} < 0.5$. The effective frequency of these voltage levels of input LC filter is twice the switching frequency. Fig. 22(a) shows the waveforms of coupled-inductor currents i_{L1} and i_{L2} and switches S_1 and S_2 voltage stresses. Fig. 22(b) shows the enlarged waveforms of Fig. 22(a). Figs. 23 and 24 show the measured results for two duty ratio-controlled flexible antiphase boost operation to produce $v_o = 110\ \text{V}_{\text{rms}}$ from $v_{\text{in}} = 70\ \text{V}_{\text{rms}}$. The duty ratio combination selected as $D_{bo} = 0.42$ and $D_{bu} = 0.9$. Fig. 23(a) shows the input voltage v_{in}, output voltage/current v_o/i_o, and capacitor C voltage v_C. Fig. 23(b) shows the input/output LC filter voltages v_{LCin}/v_{LCo} and inductor currents i_{Lin}/i_{Lo}. As observed, both filter voltages v_{LCin}/v_{LCo} have two levels between $v_C/2$ and v_C. Fig. 24 shows the switches S_1, S_2, S_5, and S_6 voltage stresses.

Fig. 25 depicts the measured waveforms of the output voltage v_o, output current i_o, capacitor C voltage v_C, and voltage v_{LCo}



(a) (b)

Fig. 23. Experimental waveforms for two duty ratio-controlled boost operation with the resistive load when $D_{bo} = 0.4$ and $D_{bu} = 0.9$. (a) Input voltage, output voltage, output current, and capacitor voltage. (b) Voltages across input/output *LC* filters and input/output inductor currents.



(a) (b)

Fig. 24. Two duty ratio-controlled boost operation with the resistive load when $D_{bo} = 0.4$ and $D_{bu} = 0.9$. (a) Switch voltage stresses. (b) Enlarged waveforms of (a).

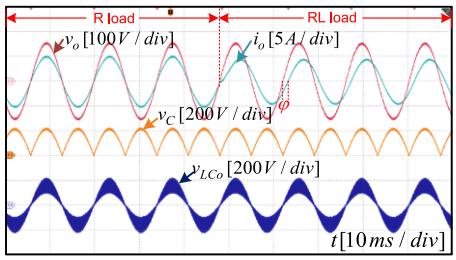


Fig. 25. Experimental waveforms for the change in load from resistive (*R*) to partial inductive (*RL*).

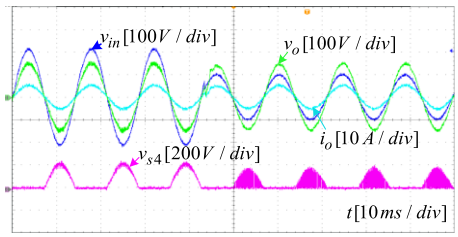


Fig. 26. Experimental results with closed-loop control for a step change in input voltage.

across the output *LC* filter for a change in load from a resistive load ($R = 32\ \Omega$) to a partial inductive load ($RL = 32\ \Omega + 30$ mH) for in-phase buck operation when $v_{\text{in}} = 150\ \text{V}_{\text{rms}}$ and $v_o = 110\ \text{V}_{\text{rms}}$. As observed, output current lags the output voltage with an angle φ when the load is changed to *RL*, and there is decrease in load current due to the increase in load impedance. However, the output voltage remains regulated. Fig. 26 depicts the experimental waveforms of the input voltage v_{in}, output voltage v_o, output current i_o, and voltage stress of switch S_4 in closed-loop voltage control for a step change in input voltage.

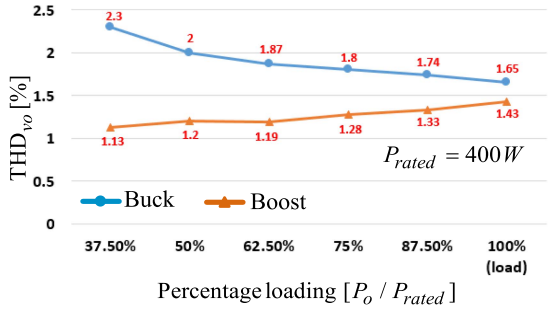


Fig. 27. Measured THD values of the output voltage.

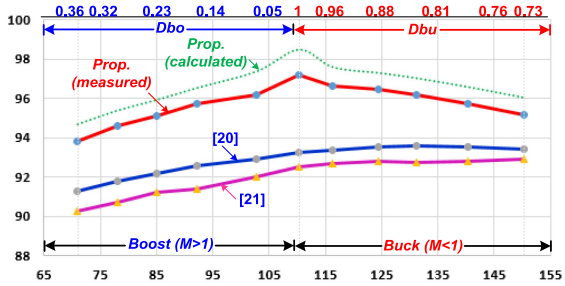


Fig. 28. Power conversion efficiency of the proposed and conventional converters with variations in input voltage and duty ratios.

Specifically, the input voltage has a step drop from 150 V_{rms} in buck operation to 70 V_{rms} in boost operation. As observed, the closed-loop control effectively regulates the output voltage to 110 V_{rms}. The measured THD of the output voltage THD_{vo} is plotted in Fig. 27 for variations in percentage loading (P_o/P_{rated}) conditions for a rated full-load power of P_{rated} =400 W. The THD_{vo} for buck operation is provided for $v_{\text{in}} = 150\ \text{V}_{\text{rms}}$, and for boost operation at $v_{\text{in}} = 150\ \text{V}_{\text{rms}}$. The output voltage is $v_o = 110\ \text{V}_{\text{rms}}$. Interestingly, THD of output voltage for boost operation is much lower. This can be explained by the capacitor *C* and output inductor L_o forming an additional *LC* filter across output capacitor C_o, significantly suppressing high-frequency ripple contents. Overall, THD remains below 2.5%.

Fig. 28 shows the measured efficiency of the proposed and coupled-inductor-based three-level ac–ac converters [24], [26] for variations in input voltage $v_{\text{in}} = (70 \sim 150)\text{V}_{\text{rms}}$ and duty ratio for buck and boost operations for a constant output voltage of $v_o = 110\ \text{V}_{\text{rms}}$ and output power of $P_o = 400$ W. As observed, the efficiency of the proposed converter is maximum for buck operation when $v_{\text{in}} = v_o = 110\ \text{V}_{\text{rms}}$. This is due to the absence of high-frequency switching of devices, resulting in negligible semiconductor switching losses and magnetic core loss. Moreover, the proposed converter reports the highest measured efficiency for the entire comparison range. In addition, Fig. 29 provides a comparison of the measured efficiency for the proposed buck operation ($v_{\text{in}} = 150\ \text{V}_{\text{rms}}$) and boost operation ($v_{\text{in}} = 70\ \text{V}_{\text{rms}}$) to generate a fixed output voltage ($v_o = 110\ \text{V}_{\text{rms}}$) for different load power levels. As observed, efficiency tends to be higher for buck operation at higher power levels, mainly attributed to its smaller conduction losses. However, at lower power levels, the efficiency of buck operation decreases more significantly, primarily due to the dominant switching losses of

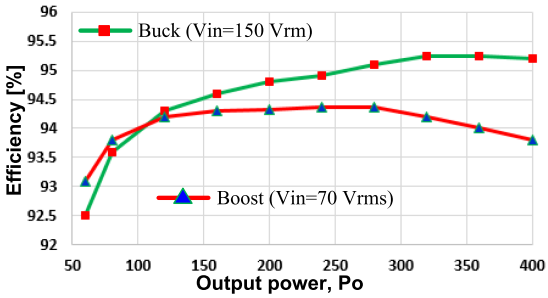


Fig. 29. Measured efficiency for buck and boost operations with variations in load power.

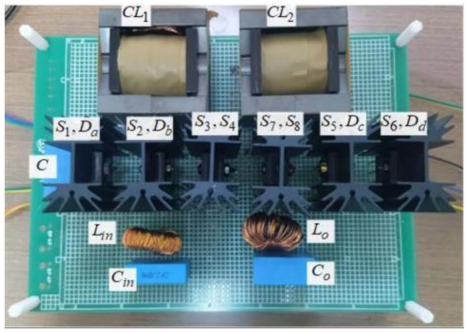


Fig. 30. Laboratory prototype of the proposed converter.

semiconductor devices and core losses of magnetic components. Fig. 30 shows the laboratory hardware prototype. The experimental results affirm the benefits of the proposed converter.

VIII. Conclusion

This article presented a novel three-level bipolar buck–boost ac–ac converter. By integrating second-order input and output *LC* filters with coupled-inductor-based dual-buck phase legs and conventional phase legs, along with a small film capacitor acting as an energy store and snubber, the proposed converter achieved identical in-phase and antiphase buck and boost operations with three-level input and output voltages. This design significantly reduced component stresses, ripples, and power loss, resulting in highly efficient operation. Moreover, the converter's bipolar operations simplified the PWM, circuit operation, control, design, and optimization. By modulating only two dual-buck phase legs at high frequency and providing inductor current flow paths during switch deadtimes, the converter eliminated the need for burdensome control or dedicated circuitry to address commutation issues. The detailed descriptions of circuit operation, voltage/current stress analysis, and design considerations were provided, along with comparisons with state-of-the-art converters. Finally, the experimental evaluations were performed which backed up the theoretical claims and benefits of the proposed converter.

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