Letters

Current-Cancellation-Based Heterogeneous Integration of *LLC*-DCX With Ultralow-Voltage High-Current Output for Data Centers

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***Abstract*—The efficiency and power density of ultralow-voltage (<1 V) high-current output dc transformers (DCXs) are limited by the losses and footprint area of the high-current windings. High-frequency current cancellation and power switches and high-current winding heterogeneous integration methods are proposed to reduce the length, area, and losses of high-current windings. With the proposed current-cancellation-based heterogeneous integration method, most of the high-current printed circuit board (PCB) windings of the transformer are replaced by power switches and capacitors, and almost zero PCB winding is achieved for the high-current secondary windings of the DCX. As a result, both power density and efficiency are improved significantly. A 36-V-to-0.75-V/150-A output DCX with a 48:1 turns-ratio transformer is designed and implemented with the four-layer PCB. A peak efficiency of 94.1% is achieved, while the power density of the high-frequency transformer in the DCX is 0.66 A/mm^2.**

***Index Terms*—Chip power, data center, dc transformer (DCX), heterogeneous integration, ultralow voltage high current.**

I. Introduction

THE explosive growth in data scale and computing power requirements has led to a continuous increase in energy consumption of data centers [1]. More efficient power solutions for data centers are needed urgently. A 48-V server data center architecture has been demonstrated more efficient than the conventional 12-V architecture due to much lower conduction loss [2]. However, due to the continuous decrease in xPU (CPU, GPU, etc.) voltage, which has now dropped to 0.6–0.8 V, how to achieve a high voltage conversion ratio while ensuring high efficiency and higher power density has become a significant challenge for a 48-V power system.

The two-stage architecture, which is composed of a voltage regulator and an unregulated dc transformer (DCX), has been proposed for the 48-V power systems [3], [4]. As shown in Fig. 1, if the DCX is employed as the second stage and fed by a high-voltage (e.g., 48 V, 36 V, etc.) dc bus, both the power delivery network losses and energy storage capacitance requirement can be reduced [5], while it is easy to implement the voltage regulator as well. However, it is a big challenge to implement a high-efficiency high-power-density DCX with high voltage conversion ratio, e.g., 48:1, sub-1-V output voltage, and hundreds of amperes high output current.

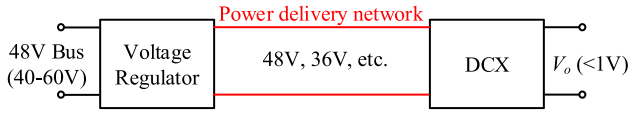

Fig. 1. Two-stage architecture with the voltage regulator cascaded DCX.

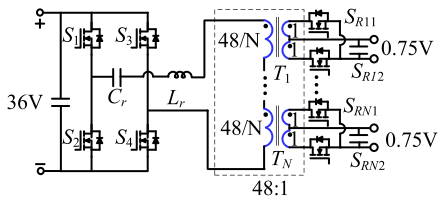

Fig. 2. *LLC*-DCX with matrix transformers.

Switched-capacitor-based and transformer-based solutions are two typical solutions for DCXs [6], [7]. Transformer-based DCX, especially *LLC*-resonant-converter-based DCX (*LLC*-DCX), is more suitable for high-conversion-ratio and high-current applications. Matrix transformers and magnetic integration methods have been proposed to reduce the volume and loss of high-frequency transformers and improve the efficiency and power density of *LLC*-DCX [8], [9], [10]. However, for the applications with sub-1-V ultralow output voltage, the volume and loss occupied by the magnetic core are small, and the area and loss occupied by the printed circuit board (PCB) winding are the root causes of limiting power density and efficiency of DCXs. The multilayer paralleled PCB can reduce the footprint of the high-current winding, but the winding losses are still high, while the cost will be increased. Until now, it has been a big challenge to reduce the footprint area and losses of high-current PCB windings.

The major contribution of this letter is to propose a method for heterogeneous integration of PCB windings, switches, and

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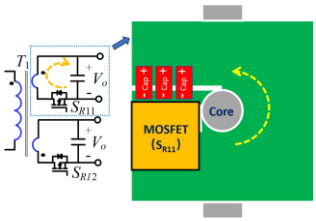

Fig. 3. Top view of secondary winding arrangement of a subtransformer.

capacitors based on the current cancellation principle. The integrated transformer structure with reduced winding loss and footprint is derived step by step by adopting the proposed method. A general winding–switch–capacitor hybrid integrated structure with switches inside the magnetic core is proposed for ultralow-voltage high-current applications. Feasibility and effectiveness of the proposed method are demonstrated with experimental results.

II. PCB Winding Integration With Current Cancellation

Fig. 2 shows an example of 36-V/0.75-V *LLC*-DCX. C_r is the resonant capacitor, and the resonant inductor L_r is the leakage inductance of the transformer. Matrix transformers are employed to provide high output current and totally 48:1 turns ratio. The number of matrix transformers N can be designed according to practical requirements. The size and losses of these transformers dominate the power density and efficiency of the whole DCX. Thus, the structure and implementation of the high-frequency transformer, which is the focus of this letter, are very critical.

Planar magnetic cores and PCB windings are considered to realize these transformers. The secondary winding arrangement of one of the subtransformers is shown in Fig. 3. The secondary windings are located at the top and bottom sides of the PCB board, and one of the secondary windings of the center-tapped rectifier is shown in Fig. 3. The synchronous rectification (SR) MOSFET and output capacitors are part of the secondary windings. As shown in Fig. 3, it is obvious that most of the area of the transformer is occupied by the high-current winding.

Winding integration is necessary to reduce the area and improve efficiency and power density of the transformer. Consider two subtransformers, T_1 and T_2, placed side by side, as shown in Fig. 4(a), where the two SRs, S_{R11} and S_{R21}, belong to different subtransformer. The primary winding of the two subtransformers, T_1 and T_2, is connected in series, and S_{R11} and S_{R21} will be ON or OFF simultaneously within the half switching cycle. According to the transformer structure and the winding current direction, the electric potential of the PCB winding within the dashed box in Fig. 4(a) is equal, and the current direction is opposite. Therefore, the high-frequency current in the windings within the dashed box can be canceled with each other, and the PCB winding in the dashed box can be removed. Then, the two cores of the two subtransformers can be merged into an integrated one. As a result, the integrated transformer with winding current cancellation and magnetic integration is derived and shown in Fig. 4(b). It is seen that, after integration, more

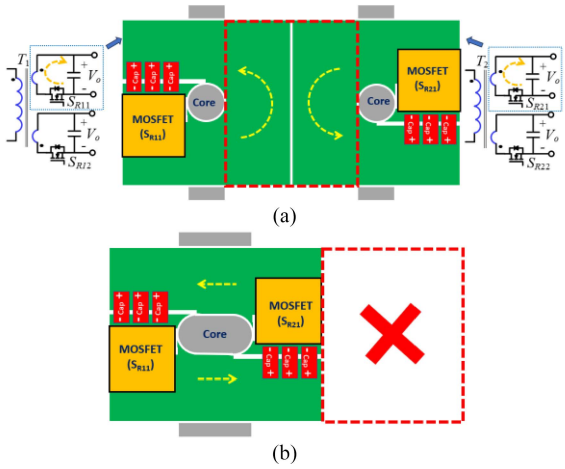

Fig. 4. Winding integration. (a) Before integration. (b) After integration.

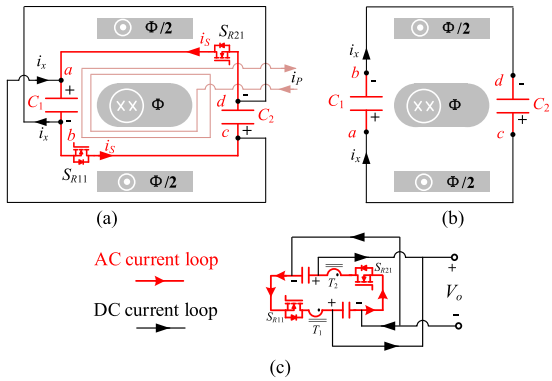

Fig. 5. Equivalent circuit of the integrated transformer shown in Fig. 4(b). (a) Output capacitors are paralleled by the PCB outside the core. (b) Only consider the loop outside the core. (c) Illustration of AC and DC current loops.

than one-third secondary windings, as well as the area and losses of the windings, have been reduced. In fact, the integrated transformer shown in Fig. 4(b) is a kind of fractional-turn transformer [11], [12]. Current-cancellation-based winding integration is an effective method to obtaining fractional-turn transformers.

In practice, the two sets of output capacitors are connected in parallel. Consider the parallel connection of capacitors; the equivalent circuit of the integrated transformer is shown in Fig. 5(a), where the two output capacitors C_1 and C_2 are paralleled by the wires outside the core. If the magnetic flux through the central core column is Φ, the flux through the two side core columns will be $\Phi/2$. According to Fig. 5(a), no matter how the secondary winding current is closed, the closure path of the secondary winding high-frequency current must include the SR MOSFET and the output capacitor. According to Kirchhoff's current law, the current flowing into node "a" must be equal to the current flowing out of node "b" in Fig. 5(a). Assume that a part of the high-frequency secondary winding current, i_x, is closed from the wire outside the core. The equivalent closed loop outside the magnetic core can be derived and shown in Fig. 5(b). According to the relationship between inductance and magnetic flux,

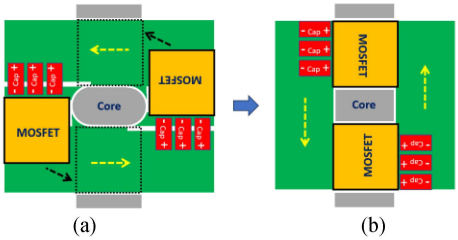

Fig. 6. Rearrangement position of MOSFETs. (a) Before. (b) After.

one has

$$L_x i_x = \Phi - \Phi/2 - \Phi/2 = 0 \tag{1}$$

where L_x is the equivalent inductance corresponding to the loop outside the core. It is seen that, since the total magnetic flux surrounded by the current loop outside the core is zero, the high-frequency current i_x passing through the wires outside the core would be zero too. Therefore, the high-frequency winding current will not flow through the wire outside the core. The high-frequency secondary winding current will close through the loop within the magnetic core, while the loops outside the core window act as the dc current loop. The equivalent ac and dc current loops of the integrated transformer are shown in Fig. 5(c).

III. Heterogeneous Integration for High-Current Output Applications

The winding integration process hints that when the windings outside the magnetic core have equal electrical potential and opposite current directions, these windings can be canceled to reduce the winding area and losses. Although a fractional-turn transformer is derived in Fig. 4, the windings still dominate the size of the transformer, and most of the windings are under the core. To expose more PCB windings on the outside of the core, it is proposed to swap the SR MOSFETs and the winding, i.e., placing the SR MOSFETs below the magnetic core to expose more PCB windings on the outside of the magnetic core, as illustrated in Fig. 6.

The transformer shown in Fig. 6(b) can be used as the basic cell. Multiple transformer cells can be further integrated following the process shown in Fig. 4. Take two sets of transformers as example. When the two transformer cells are placed side by side, as shown in Fig. 7(a), the windings within the dashed box can be canceled, and the transformer structure is derived, as shown in Fig. 7(b). It is seen that the area of the PCB windings is further reduced. Then, the two magnetic cores in the middle can be further integrated. The derived integrated magnetic transformer is shown in Fig. 7(c), where the integrated transformer is equal to four subtransformers shown in Fig. 3. As illustrated in Fig. 7(b) and (c), before the integration of the central columns of the two magnetic cores, the central region wound by the windings contains two magnetic columns and a blank area. After integrating the center column, the total area of the central magnetic column remains unchanged. Due to the elimination of the blank area, the length of the central magnetic column in the vertical direction, as well as the entire magnetic core, is

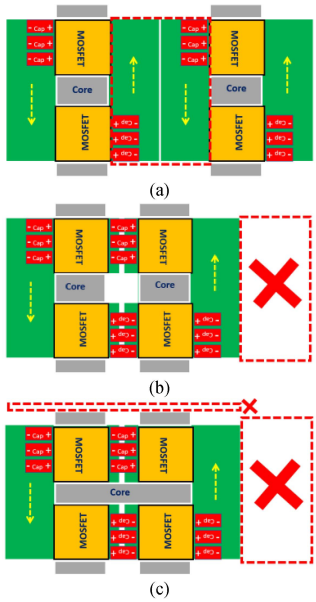

Fig. 7. Integration of two transformer cells. (a) Before integration. (b) Winding integration. (c) Magnetic core integration.

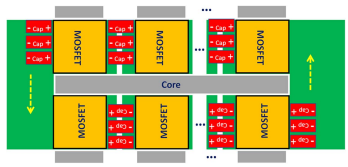

Fig. 8. General structure of the proposed integrated transformer for ultralow-voltage and high-current output applications.

reduced. Therefore, the overall footprint of the high-frequency transformer in Fig. 7(c) is slightly reduced. It is obvious that, by adopting the proposed integration method, the area and length of the high-current windings are reduced significantly. Most of the windings are realized through the SR MOSFETs and output filter capacitors directly. As a result, the power density of the high-frequency transformer can be improved dramatically.

The number of subtransformers in the proposed integrated transformer can be extended according to the output current and conduction loss requirements. The general structure of the proposed transformer for ultralow-voltage and high-current output applications is shown in Fig. 8, where the left- and right-side terminations are rearranged to achieve a symmetrical structure. It is seen that, with the increasing number of subtransformers in the integrated transformer, the proportion of PCB windings in the entire winding is further reduced. Almost zero PCB winding is achieved for the high-current output windings of the DCX.

IV. Design Example and Experimental Verifications

A. Design Example

A 36-V-to-0.75-V/150-A output *LLC*-DCX with the 48:1 turns-ratio transformer and 1-MHz switching frequency is designed based on the topology shown in Fig. 1. Six subtransformers with center-tapped rectifiers are used. Therefore, the structure of the integrated transformer is like the one shown

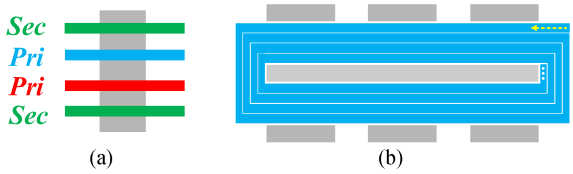

Fig. 9. Arrangement of the PCB windings. (a) Side view. (b) One of the primary winding layers.

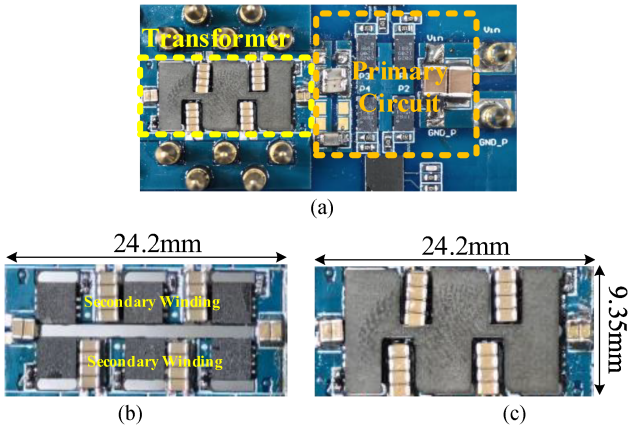

Fig. 10. Experimental prototype. (a) Whole prototype. (b) Transformer without core. (c) Transformer with core.

Fig. 8. The integrated magnetic core consists of a common central column and six side columns. Six SR MOSFETs are employed on the top and bottom layers of the PCB to implement the secondary windings of the transformer. Since the primary windings of these subtransformers are in series, the turns ratio of each subtransformer is 8:1, which means that only eight turns are needed for the primary windings.

The arrangement of the PCB windings of the high-frequency transformer in the DCX is illustrated in Fig. 9(a). The four-layer PCB is used to implement the high-frequency transformer. The top and bottom layers are secondary windings, while the middle two layers of the PCB are primary windings. Each primary winding layer has four turns, and the two layers of primary windings are connected in series through vias to achieve a total of eight turns. The structure of one of the primary winding layers is illustrated in Fig. 9(b). The top and bottom layers are used as the two secondary windings of the center-tapped transformer. The outputs of these subtransformers are connected in parallel on the terminals of the load only.

The experimental prototype is shown in Fig. 10, where Fig. 10(b) and (c) shows the high-frequency transformers without and with magnetic core, respectively. The layout of the secondary winding composed of SR MOSFETs and capacitors can be seen in Fig. 10(b). The copper thickness of the PCB windings is 3 oz. The specifications and part number of devices have been listed in Table I. The footprint of the high-frequency transformer in the DCX is 9.35 mm × 24.2 mm, and the thickness of the transformer is 5.2 mm. The compact prototype means that the current density of the high-frequency transformer can reach 0.66 A/mm^2.

TABLE I
SPECIFICATIONS OF THE PROTOTYPE

Parameters	Part number or values
Input/output	36 V/0.75 V to 150 A
Switching frequency	1MHz
Resonant inductor	70nH
Magnetizing inductance	4 μH
Output filter capacitor	GRM188R60J476ME15D
Primary switches	EPC2030
Primary driver	Si8273GB
Secondary switches	IQE006NE2LM5
Secondary driver	LMG1205YFXR

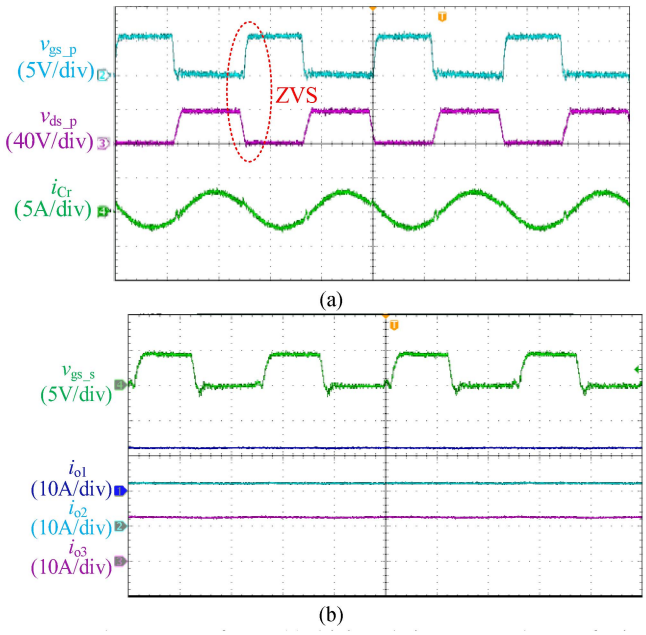

Fig. 11. Steady-state waveforms. (a) Driving and drain-source voltages of primary-side switch, and resonant current. (b) Driving voltage and output currents of three channels of the matrix transformer.

B. Experimental Results

The full-load operating waveforms of the designed prototype are shown in Fig. 11(a), where $v_{\mathrm{gs\_P}}$ and $v_{\mathrm{ds\_P}}$ are the gate–source and drain–source voltages of one of the primary-side switches, and i_{Cr} is the resonant current. It is shown that zero-voltage switching (ZVS) is achieved for the primary devices. The output current of each channel has been tested separately, with the waveforms of the output currents from three channels, i_{o1}, i_{o2}, and i_{o3}, as shown in Fig. 11(b), where it is seen that the output current of each channel is almost the same, and the ripple current of each channel is very small. It indicates that the high-frequency current passing through the wires outside

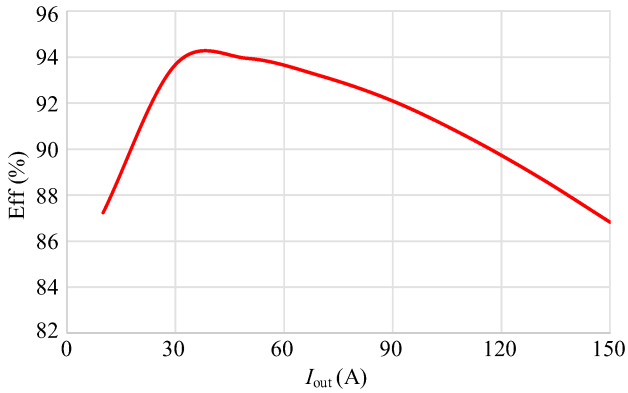

Fig. 12. Efficiency curves.

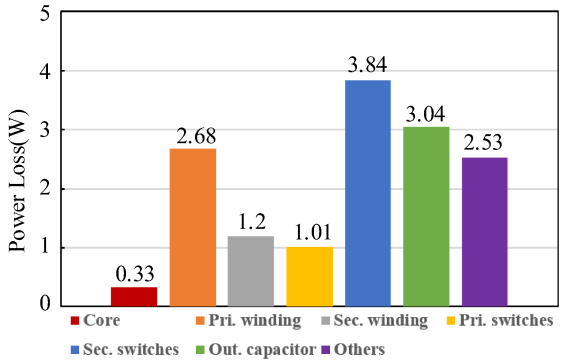

Fig. 13. Power loss distribution at 150-A output.

the core is very small, and the loops outside the core mainly act as a dc current loop.

The efficiency curve of the converter is shown in Fig. 12. One can see that, with only four-layer PCB, the designed converter maintained a peak efficiency of 94.1%, and the full-load efficiency with 150-A output current is 86.8%. The achievement of high efficiency and high power density is mainly due to the significant reduction in the footprint and losses of high-current windings by adopting the proposed current cancellation heterogeneous integration method. The loss breakdown of the *LLC*-DCX at 150-A output is shown in Fig. 13 based on experimental tests, simulation, and calculation. It can be seen that the loss of the primary-side switches is very small, while the high-frequency transformer, i.e., the core, windings, SR MOSFETs, and output capacitors, accounts for the majority of the losses. Especially, the losses of the SR MOSFETs and output capacitors are the main losses. The losses labeled "Others" included actual PCB losses in the primary circuit, losses caused by device interconnection on the primary and secondary sides, and other parts that are not easily calculated accurately. It should be noted that more focus should be paid on the thermal dissipation since MOSFETs are under the magnetic core. To avoid thermal issue, the power loss of each MOSFET must be considered. Although the total loss of secondary switches is 3.84 W, loss of each SR MOSFET is only 0.32 W. The thermal distribution of the

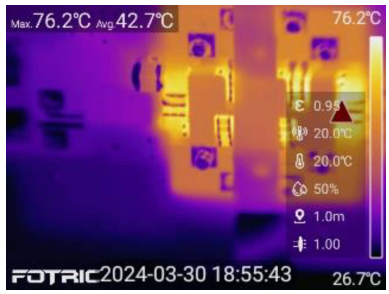

Fig. 14. Thermal distribution of the prototype with forced air cooling.

TABLE II
COMPARISON TO THE STATE OF THE ART

State of the art		[13]	[14]	This work
Year of publication		2024	2023	/
Turns ratio		48:1	48:1	48:1
Output voltage/current		1 V/350 A	1 V/300 A	0.75 V/150 A
Efficiency	Peak	94%	93.7%	94.1%
	Full load	85%	89%	86.8%
Number of layers of PCB		8	18	4
Current density of transformer		0.154 A/mm^2	0.44 A/mm^2	0.66 A/mm^2

prototype with forced air cooling is shown in Fig. 14; the thermal distribution coincides with the loss distribution.

The comparison to the state of the art has been summarized in Table II. The two papers, [13] and [14], focusing on the 48-V/1-V DCX published in 2023 and 2024, respectively, have been selected for comparison. It is seen that the proposed method achieves the highest current density by using the smallest number of PCB layers. Since the output voltage of this work is only 0.75 V, which is much lower than that in [13] and [14], the full-load efficiency of the proposed one is a bit lower than that in [14].

V. CONCLUSION

The current-cancellation-based heterogeneous integration method is proposed for the DCX, aiming to reduce the footprint and losses of high-current windings and achieve a high conversion ratio, sub-1-V ultralow voltage, and high-current output for data center applications. The footprint area, length, and losses of the high-current secondary windings of the high-frequency transformer are reduced because most of the PCB windings outside the magnetic core are eliminated. Almost all the secondary windings are implemented by synchronous MOSFETs and output filter capacitors directly. As a result, the power density and efficiency of the high-frequency transformer are improved significantly. The principle of the proposed heterogeneous integration is analyzed in detail. A 36-V/0.75-V-to-150-A *LLC*-DCX with the 48:1 turns-ratio transformer is designed to demonstrate the feasibility of the proposed method. A full-load efficiency of 86.8% is achieved with only four-layer PCB, and the power density of the 48:1 turns-ratio high-frequency transformer is up to 0.66 A/mm^2.

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