Capacitive Coupled Step-Down DC–DC Converter With Touch Current Limitation

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***Abstract*—This article proposes a high-efficiency step-down dc–dc converter with limited touch current and voltage gain equivalent to the conventional buck converter. By including a capacitive coupling cell, it is possible to reduce touch currents, presenting a higher safety degree against electric shocks. The main operating stages and equations describing the proposed converter are presented. The capacitive coupling cell operates through the resonant switched-capacitor principle and the impact of the parasitic elements is evaluated. Even though it has a resonant stage, the converter operates with a fixed switching frequency, simplifying the control scheme. A design guideline based on the converter specifications and safety criteria is presented. Simulation results are included to compare the touch current generated by the proposed converter and that of the conventional buck converter, demonstrating the effectiveness of the proposal. Experimental results for a 3 kW prototype operating at 180 kHz switching frequency are presented, including waveforms of main components, closed-loop control performance and efficiency curve, with a peak around 97.8%. An experimental evaluation comparing the proposed converter and the *LLC* half-bridge converter is also performed. Finally, the touch current tests demonstrated that the risk is automatically eliminated by the proposed converter in approximately 60 ms.**

***Index Terms*—Capacitive coupling, step-down converter, switched-capacitor, touch current.**

I. Introduction

In SEVERAL applications, galvanic isolation can be used as an additional safety resource, mainly for class I equipment [1], which use a grounded metallic enclosure to protect against single-fault conditions. Nevertheless, accidents and inappropriate installation and operation conditions can lead to electric chock hazards. For some applications, there are standards specifying practices and devices to monitor residual currents or conditions, such as earthing conductor faults. For instance, IEC 62109-2 defines safety requirements for photovoltaic (PV) systems [2]. For electric vehicles (EV), onboard and fast dc offboard chargers must satisfy the requirements imposed by IEC 61851 [3] or UL 2202 [4].

In this sense, magnetic elements are commonly used to provide high-frequency isolation, through coupled inductors or transformers [5], [6]. Coupled inductors are usually employed in low power systems, such as power supplies for portable devices, PV micro-inverters, etc [7]. However, due to the leakage inductance, topologies with coupled inductors normally require snubber circuits or overrated devices, reducing the converter efficiency [8]. For higher power systems, topologies with high-frequency transformers are largely used. One can highlight the phase-shift full-bridge (PSFB) converter, which employs the leakage inductance of the transformer to achieve turn-ON soft switching for a given power range [9]. Resonant topologies, such as *LLC* and *LCL*, present high efficiency and low electromagnetic interference (EMI), but operate with variable switching frequency [10], which increases the complexity to design passive elements and control system.

Despite the simplicity of magnetic devices, they increase the cost and volume of the converters. One can increase the switching frequency to reduce the volume of the magnetic elements, but core and copper losses also increase [6]. Nanocrystalline materials with higher flux density allow to reduce the volume [11], but they have limited performance for frequencies above 100 kHz when compared to ferrite cores [12].

On the other hand, galvanic isolation can also be obtained through capacitive coupling, which is largely used in integrated circuits for transmitting signals in digital isolators and gate drivers [13], [14]. Capacitive coupling has also been used in power converters. For instance, an *LLC* converter in which the resonant capacitor is replaced by two class-Y safety capacitors connected in series with the transformer is presented in [15], resulting in a transformer with smaller volume. Isolated versions of SEPIC and Ćuk converters were proposed, respectively, in [16] and [17], in which a third capacitor is added to the inferior branch, disconnecting the input and output references.

Following this approach, four topologies based on the canonical Ćuk, SEPIC, Zeta, and buck–boost converters were investigated in [18], evaluating the performance and tradeoffs of these capacitive isolated converters, using the concept of capacitive

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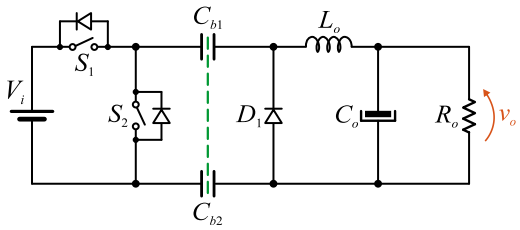

Fig. 1. Proposed capacitive coupled step-down DC–DC converter.

power transfer (CPT). In [19], a capacitive isolated resonant switched-capacitor dc–dc converter is presented, achieving high efficiency with reduced power level, however, requiring a high number of semiconductors. Other solutions with capacitive isolation for widespread topologies have also been published, such as the PSFB [20] and the dual active bridge (DAB) [21]. In addition, several low power topologies for LED drivers were also proposed [22], [23], which are based on a series resonant converter with multiple secondaries.

Capacitive isolation was also applied in power modules of a solid-state transformer (SST) [24]. In a similar way, a SST employing capacitively isolated series-stacked converter cells is presented in [25]. Recently, CPT has been spread as an alternative to conductive methods for wireless EV charging [26], [27], using resonant compensation networks [28]. However, in this case, the focus lies on the facilities that the CPT can offer for EV charging, rather than on a topology that provides galvanic isolation for safety purposes.

Therefore, this article proposes a high-efficiency step-down dc–dc converter with capacitive coupling and low component count, which is able to reduce touch currents. A switched-capacitor cell in resonant charge mode controls the power transfer and generates a high impedance path for dc or low-frequency currents. The proposed converter has the same static voltage gain of a buck-type converter, but with a higher safety degree. Consequently, the proposed topology preserves several features of the widespread buck converter, while also incorporates the capability to limit touch currents (for safety purposes). This feature was achieved with the addition of just one semiconductor and two capacitors, thereby maintaining simplicity, low cost, high efficiency, and control simplicity, if compared with isolated topologies using magnetic elements.

The rest of this article is organized as follows: the operation principles of the proposed converter are presented in Section II; analysis of the touch current levels is addressed in Section III with some design constraints; Section IV presents experimental results. Finally, Section V concludes this article.

II. Proposed Topology

The proposed dc–dc converter with capacitive coupling is shown in Fig. 1. This converter is derived from dc–dc buck converter, so that elements S_1, L_o, and C_o have the same functions, and voltage and current ratings. Elements C_{b1}, C_{b2}, S_2, and D_1 compose the capacitive coupling cell, which is able to transfer energy and to limit the touch current under direct contact of a human body at output of the converter. Switches S_1 and S_2 are pulsewidth modulated with a switching frequency f_s, and their command signals are complementary, so that S_1 operates with duty cycle D and S_2 ideally operates with $1-D$. However, a dead time is required to avoid shoot-through. The coupling capacitors (C_{b1} and C_{b2}) are class-Y safety capacitors and ideally have the same capacitance.

As will be addressed in Section II-A, during the stage that S_1 is turned ON, capacitors C_{b1} and C_{b2} are charged, and during the free-wheeling stage, the simultaneous conduction of S_2 and D_1 results in a series connection of C_{b1} and C_{b2} in a resonant path, so that the voltage across these capacitors are reset. The total inductance of this path (L_p), that takes into account the parasitic inductance of S_2, D_1, C_{b1}, C_{b2} and the traces of the printed circuit board (PCB), is illustrated in the simplified equivalent circuit shown in Fig. 2. For simplicity, the parasitic resistance of this path (R_p) was disregarded, since it does not significantly impact on the circuit operation stages.

A. Operation Stages

The operation stages of the proposed converter are presented in Fig. 2. For this analysis, the resonance period should be smaller than $(1-D)T_s$, where $T_s = 1/f_s$. Further, the following assumptions are made.

1) The output voltage presents small ripple, so that it can be approximated by its average value, i.e., $v_o(t) \approx V_o$, and the load current is given by $I_o = V_o/R_o$.
2) The same principle can be applied to the current through the filter inductor, i.e., $i_{Lo}(t) \approx I_{Lo}$, with $I_{Lo} = I_o$.
3) The capacitors C_{b1} and C_{b2} present the same capacitance C_b. In addition, as they are associated in series during normal operation, $C_{\text{eq}} = C_b/2$, $i_{C\text{eq}}(t) = i_{Cb1}(t) = i_{Cb2}(t)$ and $v_{C\text{eq}}(t) = v_{Cb1}(t) + v_{Cb2}(t)$.

The state plane diagram relating the voltage across the equivalent capacitor $v_{C\text{eq}}(t)$ and the current through the parasitic inductance $i_{Lp}(t)$ is presented in Fig. 3, while the main converter waveforms are presented in Fig. 4.

1) *Stage I [$t_0 - t_1$, Fig. 2(a)]:* during this stage, S_1 is turned ON, while S_2 and D_1 are turned OFF. The inductor current I_{Lo} linearly charges capacitors C_{b1} and C_{b2}, whose final voltage is $v_{Cb(pk)}$ (addressed in Section II-B). This stage ends when S_1 is turned OFF, after the time interval Δt_1, given by

$$\Delta t_1 = DT_s. \tag{1}$$

2) *Stage II [$t_1 - t_2$, Fig. 2(b)]:* during this period, D_1 assumes the current I_{Lo}, while S_1 and S_2 remain turned OFF. This stage lasts for a period t_d, which is the dead time of the switches S_1 and S_2, so that

$$\Delta t_2 = t_d. \tag{2}$$

3) *Stage III [$t_2 - t_3$, Fig. 2(c)]:* this stage begins when S_2 is turned ON. As can be seen in Fig. 2(c), C_{b1}, C_{b2}, and L_p form a resonant tank through S_2 and D_1. Meanwhile, D_1 still conducts I_{Lo}. It is important to note that S_2 is turned ON with a limited di/dt. The energy stored in C_{b1} and C_{b2}

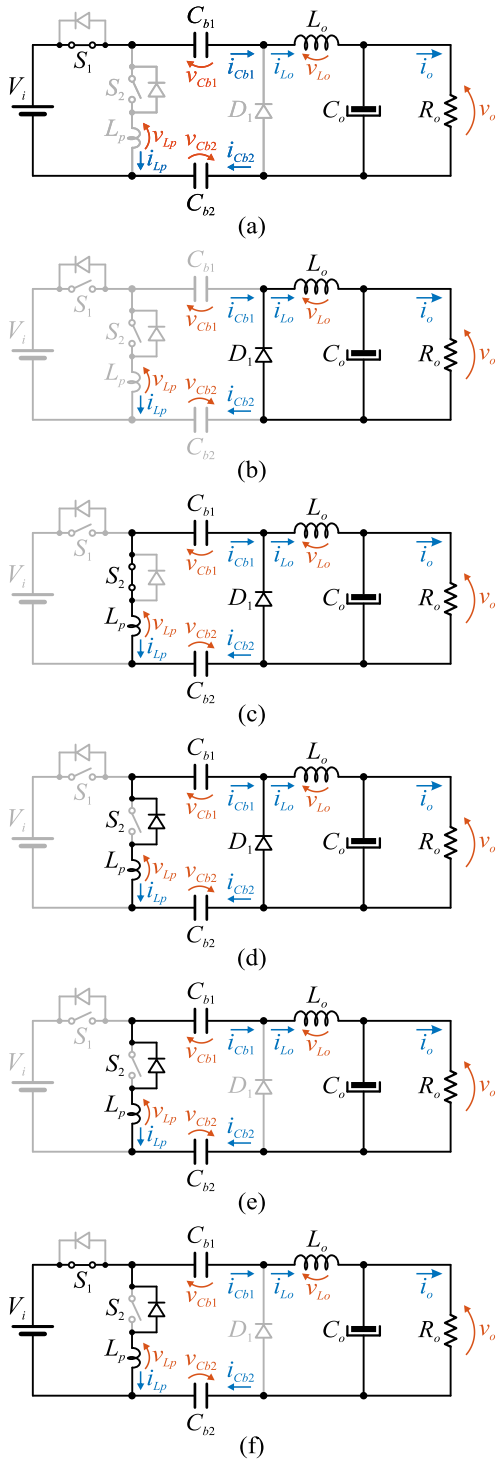

Fig. 2. Operation stages. (a) Stage I. (b) Stage II. (c) Stage III. (d) Stage IV. (e) Stage V. (f) Stage VI.

is transferred to L_p, as demonstrated in the state plane of Fig. 3, where

$$\omega \triangleq \sqrt{\frac{2}{L_p C_b}} \tag{3}$$

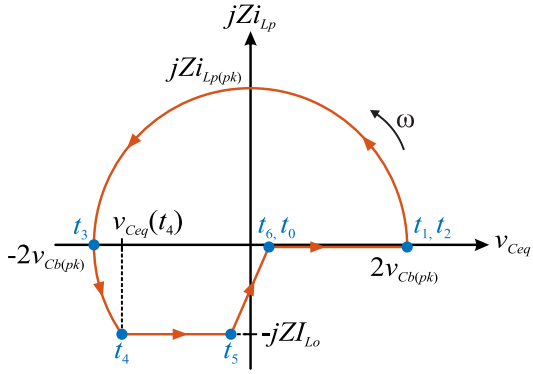

Fig. 3. State plane diagram.

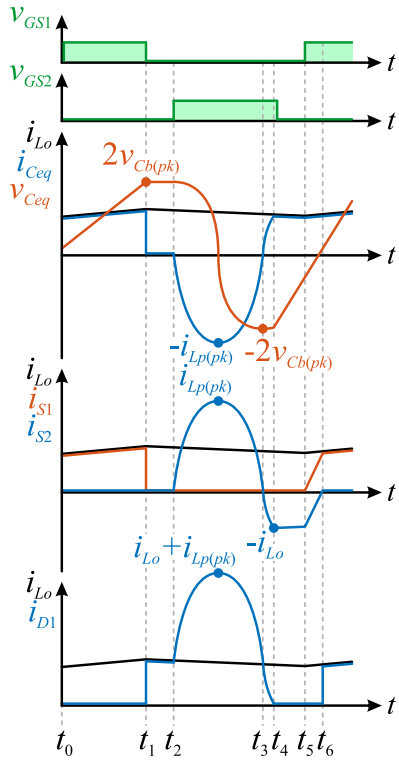

Fig. 4. Main converter waveforms.

is the resonance frequency (rad/s), and

$$Z \triangleq \sqrt{\frac{2L_p}{C_b}} \tag{4}$$

is the characteristic impedance (Ω) of resonant tank. Further, at the beginning of the resonance, both C_{b1} and C_{b2} are with their maximum voltage level. This way, $v_{Ceq}(t_2) = 2v_{Cb(pk)}$.

The current through the parasitic inductance achieves its highest level $i_{Lp(pk)}$, given by (5), before resonantly decreasing to zero. At this point, C_{b1} and C_{b2} are with their minimum voltage level, i.e., $v_{Ceq}(t_3) = -2v_{Cb(pk)}$.

$$i_{Lp(pk)} = \frac{2v_{Cb(pk)}}{Z}. \tag{5}$$

The duration of this resonant stage is given by

$$\Delta t_3 = \frac{\pi}{\omega}. \tag{6}$$

4) *Stage IV [$t_3 - t_4$, Fig. 2(d)]:* when i_{Lp} becomes negative, the antiparallel diode of S_2 is turned ON. D_1 is still conducting I_{Lo}. It is important to note that S_2 can be turned OFF under zero-current (ZCS). Gradually, i_{Lp} is increasing until reaching $-I_{Lo}$ at t_4 (see Fig. 3), when the current through D_1 reaches zero and it is turned OFF gunder ZCS.
This resonant stage lasts for

$$\Delta t_4 = \frac{1}{\omega} \arcsin\left(\frac{ZI_{Lo}}{2v_{cb(pk)}}\right). \tag{7}$$

5) *Stage V [$t_4 - t_5$, Fig. 2(e)]:* now, i_{Lp} remains constant and equals to $-I_{Lo}$. During this stage C_{b1} and C_{b2} are linearly charged by I_{Lo}.
The duration of this stage, Δt_5, is the period required to complete the free-wheeling stage, i.e., within $(1-D)T_s$. This stage ends when S_1 is turned ON again. It must be emphasized that a dead time must be observed from the S_2 turn-OFF (that may occur in Stages IV or V) to the S_1 turn-ON.

6) *Stage VI [$t_5 - t_6$, Fig. 2(f)]:* during this stage, with both S_1 and the antiparallel diode of S_2 turned ON, the input voltage is applied across the parasitic inductance, i.e., $v_{Lp} = V_i$. This way, L_p is linearly demagnetized. This stage ends when i_{Lp} reaches zero and the antiparallel diode of S_2 turns OFF, returning to Stage I. This period, given by (8), is very fast since L_p is usually very low. It must be observed that C_{b1} and C_{b2} are still being linearly charged by I_{Lo}

$$\Delta t_6 = \frac{L_p I_{\mathrm{Lo}}}{V_i}. \tag{8}$$

B. Voltage Across the Coupling Capacitors

In order to determine the maximum voltage across the coupling capacitors C_{b1} and C_{b2}, one can observe in Fig. 3 that $v_{C\mathrm{eq}}$ linearly varies from $v_{C\mathrm{eq}}(t_4)$ to $2v_{Cb(pk)}$ (at t_1), when $i_{Cb1} = i_{Cb2} = i_{C\mathrm{eq}} = I_{Lo}$. This comprises the time intervals Δt_1, Δt_5, and Δt_6. This way

$$\int_{v_{C\mathrm{eq}}(t_4)}^{2v_{Cb(pk)}} dv_{C\mathrm{eq}} = \frac{1}{C_{\mathrm{eq}}} \int_0^{\Delta t_1 + \Delta t_5 + \Delta t_6} i_{C\mathrm{eq}}\, dt. \tag{9}$$

But $\Delta t_5 + \Delta t_6 = (1-D)T_s - \Delta t_3 - \Delta t_4$. Considering that Δt_4 is small compared to Δt_3 and $v_{C\mathrm{eq}}(t_4) \approx -2v_{Cb(pk)}$, one can obtain

$$v_{Cb(pk)} \approx \frac{I_{Lo}}{2C_b}\left(T_s - \frac{\pi}{\omega}\right). \tag{10}$$

C. Determination of Static Gain

The voltage across L_o over the entire switching period is defined by

$$v_{Lo} = \begin{cases} V_i - V_o - 2v_{Cb}, & \text{for Stages I and VI.} \\ -V_o, & \text{for Stages II, III, and IV.} \\ -V_o - 2v_{Cb}, & \text{for Stage V.} \end{cases} \tag{11}$$

TABLE I
CONVERTER PARAMETERS

Parameter	Value
Input voltage	$V_i = 600$ V
Output voltage	$V_o = 400$ V
Output power	$P_o = 3$ kW
Switching frequency	$f_s = 180$ kHz
Output inductance	$L_o = 250$ μH
Output capacitance	$C_o = 25$ μF
Coupling capacitors	$C_{b1}, C_{b2} = 3$ μF
Loop inductance	$L_p = 40 - 180$ nH

The converter static gain (relation between V_o and V_i) can be determined through the inductor volt–second balance [29] by using (11). This way, it is possible to demonstrate that

$$V_o = DV_i - \frac{\Delta V}{2}\frac{\Delta t}{T_s} \tag{12}$$

where $\Delta V = 2v_{Cb(pk)} + v_{C\mathrm{eq}}(t_4)$ and $\Delta t = T_s - \Delta t_3 - \Delta t_4$.

For a proper design, $\Delta V \approx 0$, so that (12) can be simplified to

$$\frac{V_o}{V_i} = D \tag{13}$$

that is the static gain of an ideal step-down buck converter.

D. Impact of L_p on the Current Through the Semiconductors

The parameters given in Table I are used to evaluate the effect of the parasitic inductance L_p on the circuit operation. Fig. 5(a) shows the maximum switching frequency that the converter can operate according to the inductance L_p, in the range from 40 up to 180 nH for a given maximum duty cycle $D_{\max}$, so that all operation stages occur and S_2 is turned OFF under soft commutation. On the other hand, Fig. 5(b) shows the impact of the inductance L_p on the current peaks through the circuit. As can be seen, the variation of L_p significantly impacts the resonant current peak $i_{Lp(pk)}$. Therefore, this loop inductance can be used as degree of freedom to control the current of the switched-capacitor circuit, as long as the resonance period does not violate the required maximum duty cycle limit.

E. Voltage and Current Stress

The maximum voltage levels across S_1, S_2, and D_1 are equal to the input voltage V_i. Capacitors C_{b1}, C_{b2}, and C_o need to withstand the output voltage V_o.

The rms current through S_1 is given by (same as the buck converter)

$$I_{S1(\mathrm{rms})} = \sqrt{D} I_o. \tag{14}$$

The rms current through S_2 (in the positive direction) can be calculated by

$$I_{S2+(\mathrm{rms})} = \sqrt{\frac{T_r}{T_s}}\frac{i_{Lp(pk)}}{2} \tag{15}$$

where T_r is the resonance period, given by

$$T_r = 2\pi\sqrt{L_p C_{\mathrm{eq}}}. \tag{16}$$

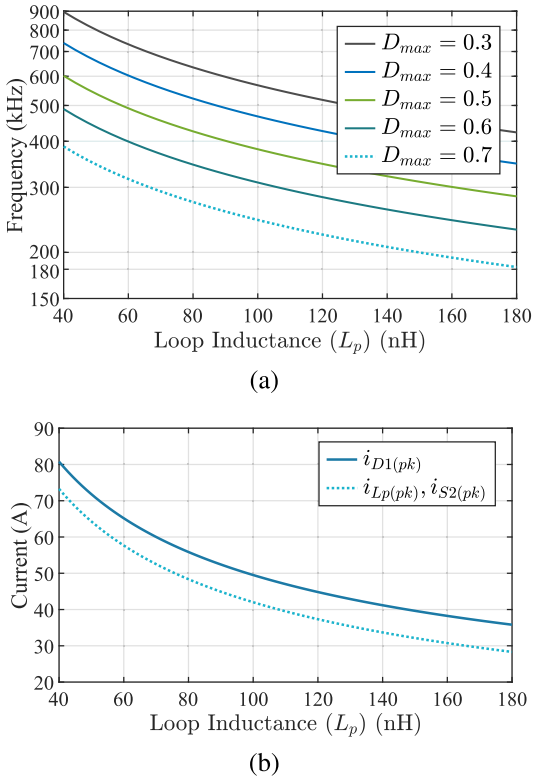

Fig. 5. Impact of loop inductance L_p on circuit operation. (a) Maximum switching frequency for different values of $D_{\max}$. (b) Current peaks through the circuit.

Diode D_1 conducts the sum of the currents through S_2 and L_o. This way, its rms current can be calculated by

$$I_{D1(\text{rms})} = \sqrt{\frac{T_r}{T_s}} \frac{i_{Lp(pk)} + I_o}{2}. \tag{17}$$

The rms current through the antiparallel diode of S_2 (in the negative direction) can be calculated by

$$I_{S2-(\text{rms})} = \sqrt{\left(1 - D - \frac{T_r}{2T_s}\right)} \left(I_o - \frac{\Delta i_{Lo}}{2}\right). \tag{18}$$

It is possible to demonstrate that the rms current through the coupling capacitors is given by

$$I_{Cb1,2(\text{rms})} = \sqrt{\frac{\left(4I_o^2 T_s - 2I_o^2 T_r + i_{Lp(pk)}^2 T_r\right)}{4T_s}}. \tag{19}$$

Finally, the rms current through the output capacitor is

$$I_{Co(\text{rms})} = \frac{\Delta i_{Lo}}{2\sqrt{3}}. \tag{20}$$

The behavior of the currents through the components is presented in Fig. 6. Fig. 6(a) presents the current levels as a function of output power, considering a constant output voltage. On the other hand, Fig. 6(b) presents the current behavior for different duty cycle values, considering a constant output current.

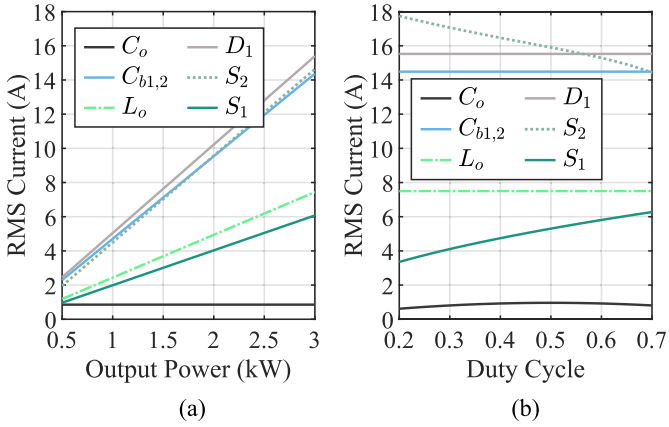

Fig. 6. Rms current levels through the components: (a) Fixed output voltage (400 V), and (b) Fixed output current (7.5 A).

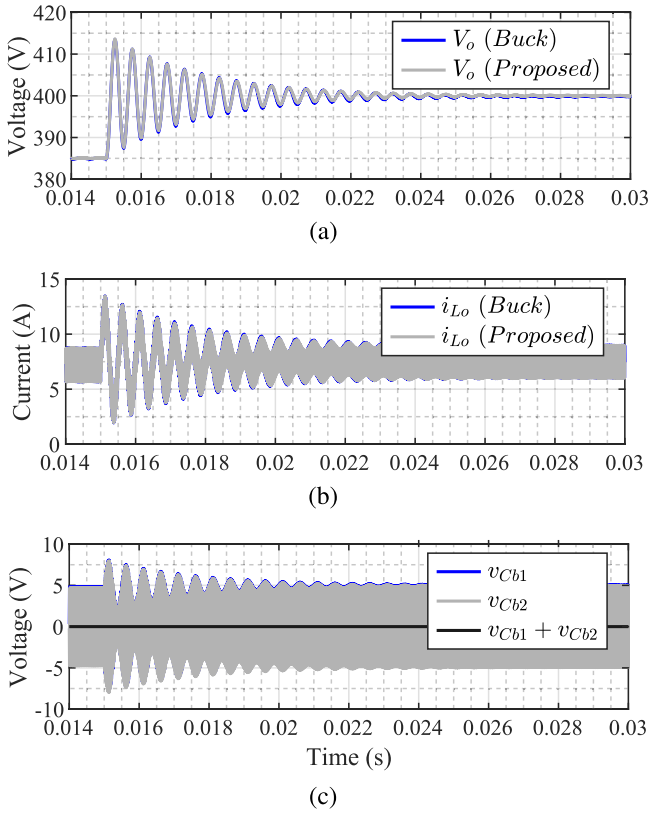

Fig. 7. Dynamic performance under duty cycle variation. (a) Output voltage. (b) Inductor current. (c) Coupling capacitor voltages.

F. Dynamic Behavior

The dynamic performance of the proposed converter under a duty cycle variation is shown in Fig. 7, and it is compared with the dynamic performance of the buck converter under same conditions. As can be seen in Fig. 7(a), both converters present a similar behavior on the output voltage. Similar feature can be observed in Fig. 7(b) for the current through the output inductor. It is important to note that voltages across C_{b1} and C_{b2} cancels each other on the proposed converter, as can be seen in Fig. 7(c),

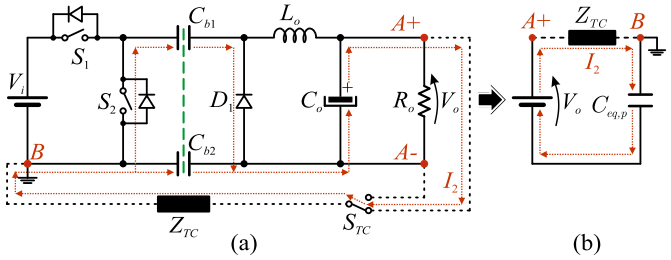

Fig. 8. Touch current analysis. (a) Converter circuit. (b) Equivalent circuit model.

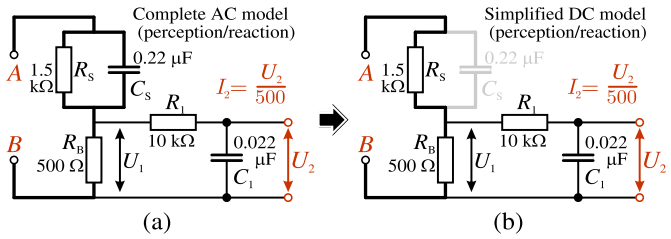

Fig. 9. IEC 60990 perception and reaction human body model. (a) Complete AC model. (b) Simplified DC model.

resulting in a null effect on the converter transient response. This way, the well-known buck converter dynamic model can be used to design the closed-loop control system.

III. Touch Current Analysis

Fig. 8(a) shows the touch current test circuit, where the capacitors C_{b1} and C_{b2} are connected in parallel, so that $C_{\text{eq},p} = 2C_b$, resulting in the equivalent model of Fig. 8(b). In Fig. 8, Z_{TC} represents the human body impedance model for touch current, defined by IEC 60990 [30] and the S_{TC} switch allows to select the pole to be touched ($A+$ or $A-$), simulating an electric shock condition.

The circuit of Fig. 9, obtained from IEC 60990 [30], illustrates the weighted touch current model Z_{TC}, that provides the touch voltage U_2 to calculate the touch current I_2, intended to represent the effect of residual current that can cause perception and reaction to electric shock. In this model R_S, R_B, and C_S are elements that represent the main path for the electric current through the human body. The capacitor C_S acts as a bypass for alternating current, representing the frequency impact, mainly in the range of 15–150 Hz. The elements R_1 and C_1 form a filter to reject high frequencies, characterizing the human skin capacitance. The model can be simplified for dc voltages with low ripple, using only the series association of R_S and R_B as the main path for the current through the body, since the C_S capacitor is charged in a few microseconds, losing its influence in the circuit.

For the case when the S_{TC} switch is in the $A-$ position, the Z_{TC} impedance will be virtually in parallel with the C_{b1} and C_{b2} capacitors, generating a high-frequency leakage current. However, the voltage ripple of these capacitors, when properly designed, should be much lower than the output voltage of the converter, not generating significant touch current.

It is considered now the situation in which the S_{TC} switch is in the position that connects the impedance at the $A+$ terminal, as in Fig. 8(a), and it is assumed that the average voltages of the coupling capacitors are initially zero. The resulting I_2 touch current charges the coupling capacitors with an average voltage and leads to $v_{Cb1(\text{avg})} = V_o$ and $v_{Cb2(\text{avg})} = -V_o$ (for the polarities defined in Fig. 2) after a certain amount of time, thus eliminating the shock condition. As pointed out earlier, for dc voltages the C_S capacitor in the Fig. 9 can be suppressed, so that R_S in series with R_B determine the main path for the current, whose association is defined as $R_{\text{TC}} = R_S + R_B$. Thus, the current I_2 can be evaluated by

$$I_2(t) = \frac{V_o}{R_{\text{TC}}} e^{-\frac{t}{R_{\text{TC}} C_{\text{eq},p}}}. \tag{21}$$

Therefore, the time T_{I2} required for the touch current elimination can be estimated by the time constant formed by $C_{\text{eq},p}$ and R_{TC}.

A. Coupling Capacitors Sizing

The sizing of the coupling capacitors must primarily meet the time criterion required to reduce the touch current to a low-risk level. IEC 60479-1 [31] defines risk zones relating time and current intensity to their effects on the human body, which can be used as a reference. In this case, the interval of 5 time constants is adopted and $C_{\text{eq},p}$ can be obtained by

$$C_{\text{eq},p} = \frac{T_{I2}}{5R_{\text{TC}}} \tag{22}$$

so that, $C_{b1} = C_{b2} = C_{\text{eq},p}/2$. The touch current level for the chosen time T_{I2} can then be estimated by (21).

Once the value of the capacitors is defined, the appropriate class-Y safety capacitors must be selected to transfer the desired power. These capacitors have an allowed rms current as a function of frequency. The switching frequency f_s is usually an arbitrary variable, however, high values allow reduction of passive elements and greater power transferred through the coupling capacitors.

B. Touch Current Simulation

A simulation was performed to compare the resulting touch current in a buck converter and in the proposed topology, for the case of touch at the positive pole ($A+$). Both converters were simulated with the parameters given in Table I. Fig. 10(a) shows the voltages of the coupling capacitors, which change from zero to 400 V in approximately 60 ms. Fig. 10(b) shows that the U_2 touch voltage of the buck converter remains indefinitely at 100 V while the touch voltage for the proposed converter is reduced to practically zero in this interval. The disturbance in the output voltage of both converters is identical, as shown in Fig. 10(c). On the other hand, the current through the output inductor in both converters presents the same transient, however, in the buck converter there is a dc level corresponding to the current I_2 after passing the transient, according to the Fig. 10(d).

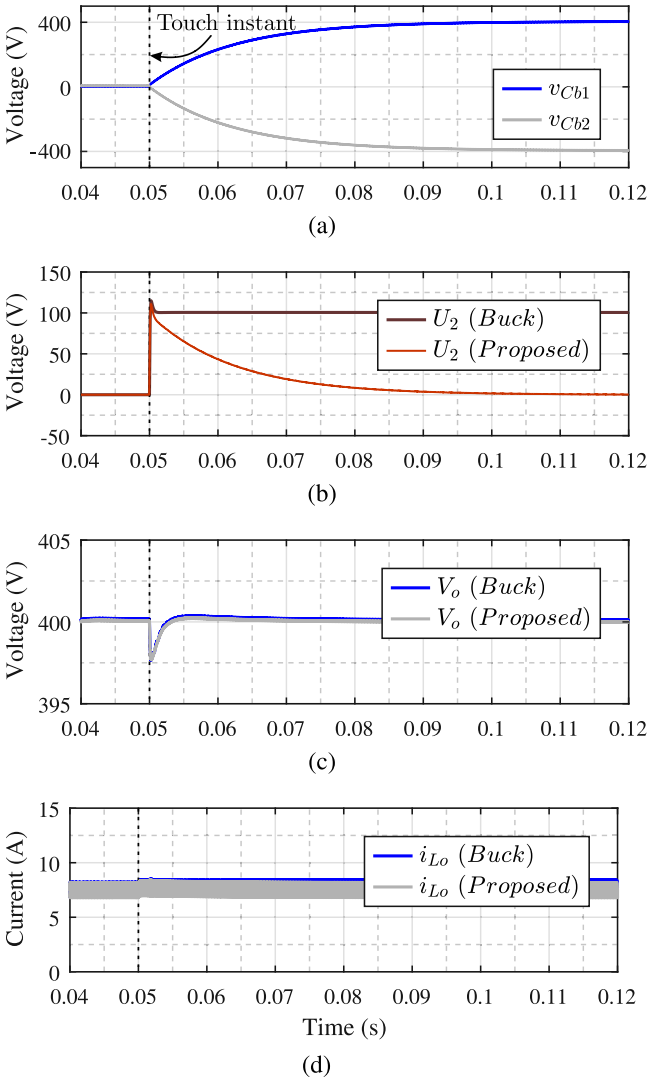

Fig. 10. Simulation of touch current in both buck and proposed converters. (a) Coupling capacitor voltages. (b) Touch voltages. (c) Output voltages. (d) Inductor currents.

As specified in IEC 60479-1 [31], Fig. 11 shows the risk zones. The DC-1 zone is considered imperceptible and the DC-2 is the zone of reaction and perception, that still is considered low risk. The DC-3 zone is called let-go, that is, impossibility of releasing due to involuntary muscle contraction. Finally, the zones DC-4.1, DC-4.2, and DC-4.3 present risks of ventricular fibrillation of 5%, 50%, and 95%, respectively. Above the DC-4.3 zone the risk of death is too high. Fig. 11 also shows the touch currents for both simulated converters, demonstrating their positions in the hazard zones. One can observe that for the proposed converter the touch current is always in low risk zones. These currents were obtained from the U_2 touch voltage of Fig. 10(b).

IV. Experimental Results

The proposed step-down dc–dc converter with capacitive coupling has been validated through a 3 kW prototype, with the main parameters defined in Table I. The main components

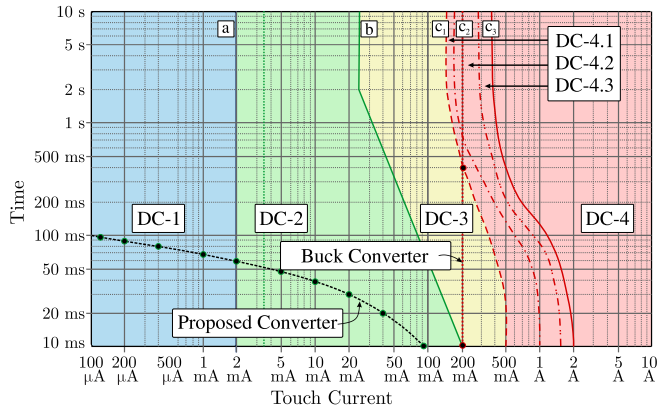

Fig. 11. Behavior of the touch current in the conventional buck converter and in the proposed converter.

TABLE II
Component Parameters

Component (Part number)	Main Parameters
S_1, S_2 (UJ4C075060K4S)	SiC, 750 V, $R_{DS(on)}$= 106 mΩ (T_j= 125 °C)
D_1 (C5D50065D)	SiC, 650 V, V_F= 1.0 V R_D= V_F/I_F = 18 mΩ (T_j= 125 °C, I_F= 25 A)
L_o	250 μH, EE 42/21/20 (THORNTON IP12R) R_{DC} = 17 mΩ, R_{AC}= 4.8 Ω
C_o (B32678G6256K000)	25 μF, 630 V, ESR= 3 mΩ, ESL= 15 nH
C_{b1}, C_{b2} (B32036A4105M)	3 x 1 μF, 1.5 kV_{DC}, ESR= 15 mΩ, ESL= 10 nH
G_{D1}, G_{D2} (STGAP2SICS)	R_{on}= 10 Ω, R_{off}= 47 Ω, V_{GS}= -5/15 V

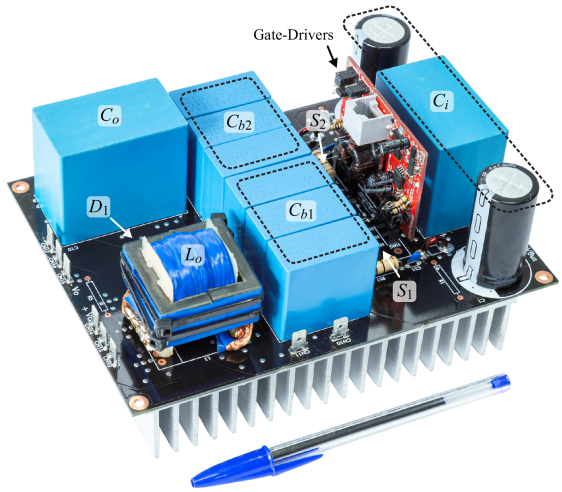

Fig. 12. Implemented converter.

of the experimental setup are given in Table II and a picture of the prototype is shown in Fig. 12.

A. Selection of $C_{b1,2}$ and L_p

The capacitances C_{b1} and C_{b2} were obtained from (22), defining a 99% reduction in the touch current I_2 within a time interval T_{I2} of 60 ms, thus reaching the DC-1 region of the Fig. 11. To

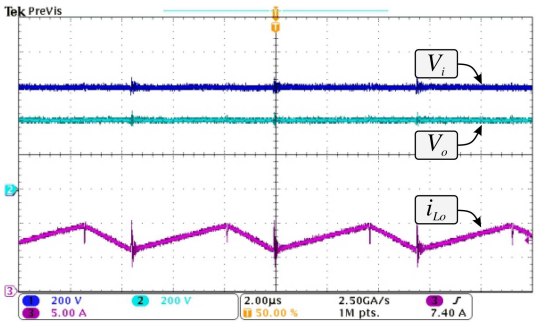

Fig. 13. Converter Gain: (Ch1) V_i, (Ch2) V_o and (Ch3) i_{Lo}.

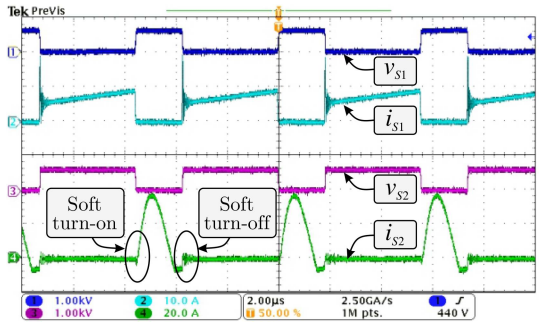

Fig. 14. Waveforms of the switches S_1 and S_2: (Ch1) v_{S1}, (Ch2) i_{S1}, (Ch3) v_{S2}, and (Ch4) i_{S2}.

achieve the required capacitance, three capacitors were used in parallel. According to the manufacturer's specification of the selected part number, each capacitor supports an rms current of 3.5 A at frequencies above 100 kHz. Thus, the rms current supported by the parallel association is up to 10.5 A. The switch S_1 always operates in hard commutation, so the frequency of 180 kHz was adopted, already considered high for this power range.

As the energy balancing of the coupling capacitors occurs during the OFF state of S_1, i.e., within Stage III, it must be observed that

$$\Delta t_3 < (1 - D_{\max})T_s \tag{23}$$

where $D_{\max}$ is the maximum duty cycle of the converter.

So, from (3), (6), and (23), one can obtain

$$L_p < \frac{2}{C_b}\left[\frac{(1 - D_{\max})T_s}{\pi}\right]^2. \tag{24}$$

This inductance is the result of different factors, such as PCB layout, connections, and jumpers for measurement. However, it can be adjusted by inserting an air core inductor into the S_2 switch path. For this design, a $D_{\max}$ of 0.7 was adopted, resulting in a maximum L_p inductance of 187 nH. It is important to note that for the designed PCB and the selected components, a total parasitic inductance around 120 nH was achieved, within the specified limit

It is important to note that the duty cycle can be larger than $D_{\max}$ during transients. However, the soft-switching of S_2 and D_1 will be lost. In this case, to maximize the soft-switching range, it is necessary to reduce f_s and/or minimize L_p.

B. Main Converter Waveforms

The waveforms presented hereinafter were obtained with the prototype of Fig. 12 operating at rated power. Fig. 13 shows the results for the static gain of the converter. As can be seen, the input voltage V_i is 600 V and the output voltage V_o is 400 V, corresponding to a duty cycle of 0.67. This result is in accordance with the static gain predicted by (13).

In addition, Fig. 14 shows the waveforms for switches S_1 and S_2, where it is possible to verify that S_2 features soft switching at turn-ON and turn-OFF. From Fig. 14 it is possible to observe that the resonant current peak is about 37 A, very close to the

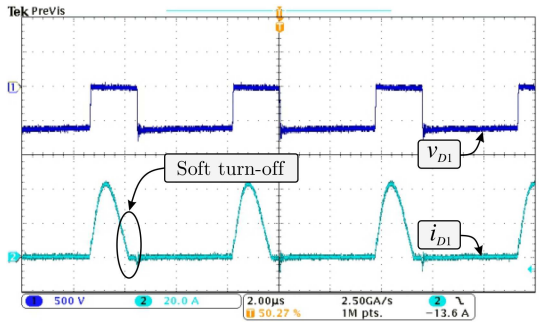

Fig. 15. Waveforms of the diode D_1: (Ch1) v_{D1}, (Ch2) i_{D1}.

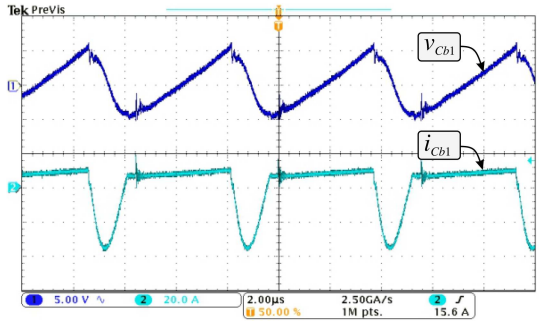

Fig. 16. Waveforms of the coupling capacitor C_{b1}: (Ch1) v_{Cb1} and (Ch2) i_{Cb1}.

value predicted from Fig. 5. Fig. 15 shows the waveforms for the diode D_1, demonstrating that it has the highest current amplitude among all elements. Despite that, D_1 turns OFF under a limited di/dt. Furthermore, Fig. 16 presents the voltage and current waveforms of capacitor C_{b1}. As can be seen in Fig. 16, the maximum voltage observed is about 5.1 V, as predicted by (10).

The touch current test result for touch at the positive pole is presented in Fig. 17. Due to the low amplitude of the current, the touch voltage U_2 was measured and then the touch current I_2 was obtained by the equation presented in Fig. 9. As expected, I_2 has an initial value of 200 mA. However, in less than 60 ms the current is near to zero.

Finally, Fig. 18 shows the behavior of the output voltage V_o under a sudden load change from 1.5 to 3 kW (rated power),

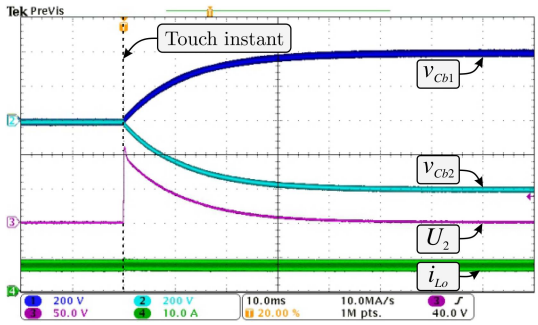

Fig. 17. Touch current test result for touch at the positive pole: (Ch1) v_{Cb1}, (Ch2) v_{Cb2}, (Ch3) U_2 and (Ch4) i_{Lo}.

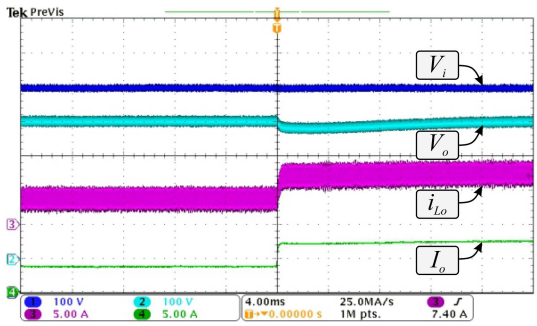

Fig. 18. Sudden load change from 1.5 kW to 3 kW: (Ch1) V_i, (Ch2) V_o, (Ch3) i_{Lo} and (Ch4) I_o.

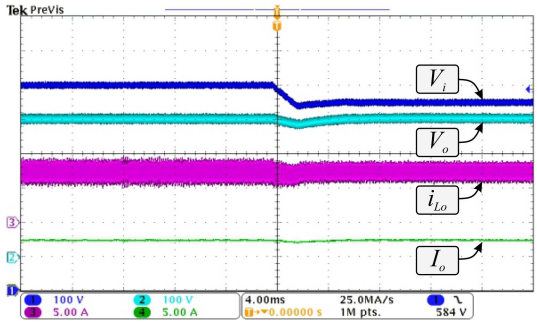

Fig. 19. Input voltage variation from 600 to 550 V: (Ch1) V_i, (Ch2) V_o, (Ch3) i_{Lo} and (Ch4) I_o.

with a settling time around 12 ms. The converter is operating in closed-loop with a dual-loop control structure. Both the inner current loop and the outer voltage loop were implemented with a proportional–integral (PI) controller, digitally programmed into the TMS320F28335 real-time microcontroller. For designing the controllers, the frequency response approach was used. The adopted cutoff frequencies for the compensated current and voltage open-loops were around 10 and 1 kHz, respectively. In addition, Fig. 19 demonstrate the performance of the closed-loop proposed converter under an input voltage variation from 600 to 550 V.

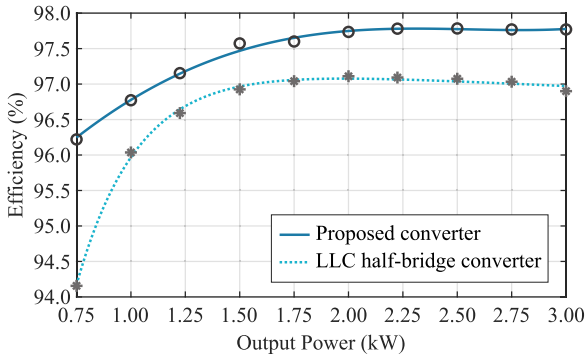

Fig. 20. Experimental efficiency curves as a function of the output power with output voltage of 400 V.

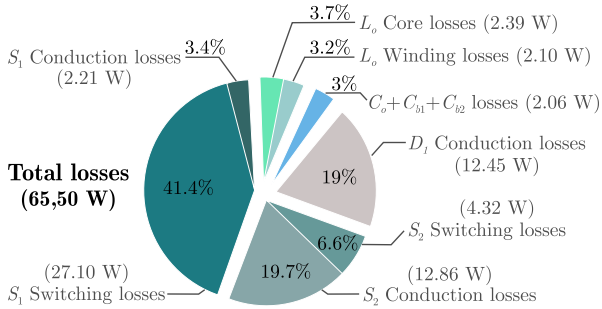

Fig. 21. Loss breakdown analysis of the proposed converter at rated power.

C. Global Efficiency and Loss Breakdown Analysis

The efficiency curve as a function of the output power is presented in Fig. 20. The proposed converter reached a maximum efficiency of 97.8% (close to the rated power) and even a high efficiency at low power (above 95.5% for 1/6 of rated power). These values have been measured using the Yokogawa WT3000E power analyzer.

In addition, Fig. 21 shows the loss breakdown analysis of the proposed converter at rated power. A simulation was carried out in PLECS software to evaluate the losses in semiconductors, meanwhile the losses in passive elements were estimated from current efforts and the data provided by the manufacturers. The total power losses for nominal output power is 65.5 W, resulting in a theoretical efficiency of 97.9%, very close to the experimental result of Fig. 20.

As can be seen in Fig. 21, losses are mainly concentrated in semiconductors. It is important to note that S_1 operates with hard commutation, resulting in high switching losses (approximately 45% of total losses). On the other hand, S_2 presents mainly conduction losses due to its high rms current. Although S_2 turns ON and turns OFF under soft-switching, its body diode presents an important reverse recovery loss when S_1 is turned ON. Even though a SiC device was used in S_2, with only 58 nC of reverse recovery charge, the switching frequency of 180 kHz resulted in a loss of approximately 4.3 W. In addition, D_1 also presents significant losses. Since a SiC device was used, it presents negligible turn-ON switching losses, and the turn-OFF transition occurs under ZCS. Since this device presents the highest current level, conduction losses are significant (about

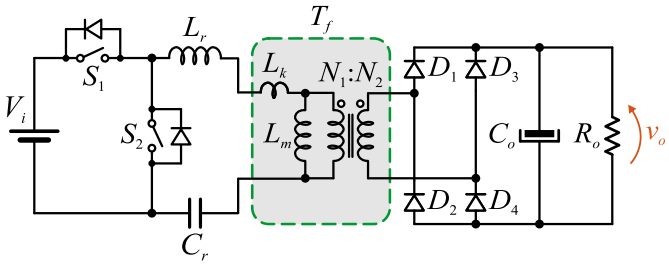

Fig. 22. *LLC* half-bridge converter [32].

TABLE III
COMPONENT PARAMETERS OF THE *LLC* HALF-BRIDGE CONVERTER

Component (Part number)	Main Parameters
S_1, S_2 (UJ4C075060K4S)	SiC, 750 V, $R_{DS(on)}$ = 106 mΩ (T_j = 125 °C)
D_1–D_4 (C5D50065D)	SiC, 650 V, V_F = 1.0 V $R_D = V_F/I_F$ = 18 mΩ (T_j = 125 °C, I_F = 25 A)
T_f	$n = 0.75$ ($N_1 = 6, N_2 = 8$) $L_m = 375$ μH, $L_k = 0.96$ μH EE 65/26/39 (THORNTON IP12R) $R_{DC\,(N1)} = 6.4m\Omega$, $R_{DC\,(N2)} = 8.1m\Omega$
L_r	16 μH, EE 42/21/20 (THORNTON IP12R) $R_{DC} = 3.5m\Omega$
C_r (B32612A2472K289)	8 x 4.7 nF, 2000 V_{DC}, ESR = 5.5 mΩ, ESL = 25 nH
C_o (B32678G6256K000)	25 μF, 630 V, ESR = 3 mΩ, ESL = 15 nH
G_{D1}, G_{D2} (STGAP2SICS)	R_{on} = 1.5 Ω, R_{off} = 10 Ω, V_{GS} = -5/15 V

19% of total losses). Finally, passive elements account for only 10% of total losses. The losses on the filter inductor comprises 7% and all capacitors together comprise only 3% of total losses. This highlights the advantage of this topology, especially in thermal handling, since it is notably simpler to dissipate heat from semiconductor devices than from reactive elements.

D. Experimental Comparative Evaluation

A comparative evaluation of the proposed converter was carried out with an isolated *LLC* half-bridge converter, shown in Fig. 22. This state-of-the-art transformer based isolated converter has important advantages, such as soft-switching for all semiconductor devices in practically the entire load range as well as the galvanic insulation provided by the transformer, which enables to limit the touch current. Therefore, to carry out a fair comparison, the same specifications and semiconductor devices were used for both proposed and *LLC* half-bridge converters. The design of the *LLC* converter was performed to achieve a resonance frequency f_0 around 180 kHz, with a switching frequency range f_s from 168 to 187 kHz in a respective load range from 0.75 to 3 kW. The transformer turns ratio was chosen so that the converter operates in the unity normalized gain region ($f_s \approx f_0$), where the voltage gain is less affected by the load. Table III presents the main parameters of the *LLC* half-bridge converter.

Since the resonant inductor L_r of the *LLC* converter is subjected to a high current ripple and needs to operate under a variable frequency range, it has the same volume of the inductor L_o of the proposed converter. In addition, both converters share

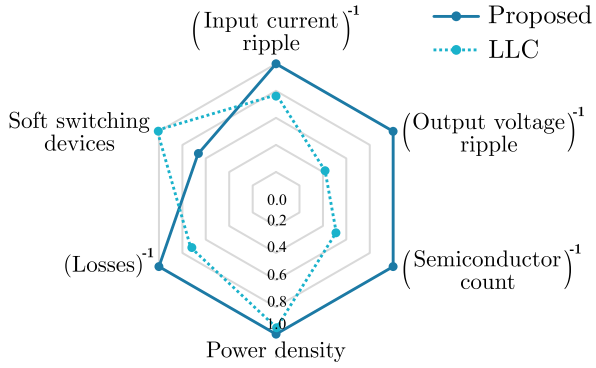

Fig. 23. Comparative evaluation between the proposed converter and the *LLC* converter.

the same input and output capacitors, heat sink and PCB area. Consequently, only the volumes of the elements used for energy transfer were compared. The total volume occupied by the coupling capacitors C_{b1} and C_{b2} is approximately 200 cm^3. On the other hand, for the *LLC* converter, the transformer T_f has a volume around 275 cm^3 and the resonant capacitor C_r has a volume around 10 cm^3. Consequently, for these devices, the *LLC* converter presents a volume approximately 42.5% greater that the proposed converter. Despite that, the power densities of both proposed and *LLC* converters are similar, being 1.67 and 1.59 kW/dm^3, respectively.

In addition, the proposed converter has the same input and output characteristics of the buck converter. Consequently, the input current is discontinuous, and the ripple amplitude depends on the inductor design and converter operating point. In general, the input current peak is $I_{i(pk)} = I_o + 0.5\Delta i_{Lo}$ and the rms current is equal to $I_{i(\text{rms})} = I_o\sqrt{D}$. On the other hand, when *LLC* converter operates with $f_s \approx f_0$, S_1 and S_2 alternately conduct a half cycle of the transformer current, also resulting in a discontinuity at the input. In general, the input current peak for this converter is $I_{i(pk)} = \pi I_i$ and $I_{i(\text{rms})} = I_{i(pk)}/2$, where $I_i = P_i/V_i$ and P_i is the input power [32].

The efficiency curve of the *LLC* half-bridge converter, as a function of the output power, is also shown in Fig. 20. As can be seen, the proposed converter presents better performance for the entire load range. For instance, the peak efficiency for the proposed converter was 97.8% (for a load of 2.2 kW), while for the *LLC* converter was 97.1% (for a load of 2.0 kW). At rated power, the efficiency of the proposed converter was 97.8%, with 66.9 W of losses. On the other hand, the *LLC* converter presented an efficiency of 96.9% in the same condition, with 93 W of losses.

Finally, it must be emphasized that the *LLC* half-bridge converter has the disadvantage of operating with a variable switching frequency, making its control more complex [32] when compared with the proposed converter, that uses conventional control loops with constant switching frequency.

Fig. 23 shows the main parameters that were compared, also including output voltage ripple at nominal power for same capacitor value and the percentage of semiconductors that have soft switching, which can be a good index for EMI analysis. In

this radar chart, the parameters were always normalized based on the converter that qualitatively exhibits the best performance. In addition, for most parameters, the inverse normalized value was utilized, such that outward represents better performance across all axes, and the converter with a larger area indicates better overall performance.

V. Conclusion

A topology with capacitive coupling capable of limiting and extinguishing the touch current was proposed in this article, which was validated through simulation and experimental analysis. From the analysis of the impact of the parasitic elements, it was demonstrated that the operation of the switched capacitor presents a resonant behavior, whose period can be controlled by the inductance of the loop. The efficiency curve as a function of the output power demonstrated that the converter can operate with high power levels and high efficiency.

Finally, it is noteworthy that this topology can be a simple and efficient alternative to other applications, not necessarily focused on safety isolation, but also on functional isolation, being a candidate for EV onboard and/or fast dc offboard chargers.

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