Analysis and Improvement of Synchronous PWM-Based Closed-Loop Current Control for Machine Drive

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***Abstract*—Synchronous pulsewidth modulation (PWM) scheme is more attractive than asynchronous one in low switching to fundamental frequency ratios, for its better harmonic spectrum. But, when a customized synchronous PWM scheme is incorporated into the field-oriented control, the dynamic response speed usually needs to be limited strictly, otherwise some violent current oscillations would appear. As a negative result, the tracking speed to the command is degraded too low to be used in most applications. To address this problem, existing methods mainly introduced a phase regulation loop inside the current control loop, trying to eliminate the phase error between the sampling phases of desired and actual voltages (i.e., maintaining synchronization), which does bring benefits to the current dynamic response. However, this phase regulation loop is always designed empirically due to the lack of a mathematical model and its interaction with the current loop has not been revealed up to date. As a result, the final performance is still not satisfactory. However, the dynamic response is crucial, especially in new energy vehicle applications. To explore this problem, the phase regulation loop is mathematically modeled first in the discrete-time domain, based on which the whole system including both the current loop and the phase loop is analyzed. Consequently, the reason is discovered and the relationship between the phase loop and the current loop is clarified. Furthermore, a novel phase-error regulator is proposed allowing the phase loop to work in the deadbeat mode and the current loop. Compared with the traditional one, with the proposed phase loop the whole closed-loop system achieves a faster dynamic response and produces much smaller current oscillations. All of the design and analysis are experimentally verified on an 18-kW interior permanent magnet synchronous machines drive test rig.**

***Index Terms*—Discrete-time design, low pulse ratio, phase regulation loop, synchronous pulsewidth modulation (PWM), time delay.**

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Nomenclature

P	Pulse ratio.
f_e, θ_e	Electrical frequency and angle.
f_s, T_s	Actual sampling frequency and period.
$\theta_{\rm ref}$, θ_u	Desired and actual voltage sampling phases.
$T_{\rm s0}$, $\theta_{\rm fix}$	Initial sampling period and fixed electrical angle increment of $\theta_{\rm ref}$ and θ_u in each sample.
$\boldsymbol{u}$, $\boldsymbol{i}$	Voltage and current vectors.
M	Modulation index (normalized by $2U_{\rm dc}/\pi$).

I. Introduction

UNDER the trend of increasing the speed for reducing the motor size in electric vehicle applications, the interior permanent magnet synchronous machines (IPMSMs) become more and more popular due to their wide speed range operations in addition to high efficiency and power density [1]. However, in high-speed electric drives, the pulse ratio P (i.e., the pulse number during one fundamental period) is low due to the limited switching frequencies of the inverter allowed. Oscillatory response and even instability may occur if the digital control delay and the discretizing errors of current regulators are not properly dealt with [2]. As reported in [2], [3], [4], and [5], designing the current regulator directly in the discrete-time domain allows the control performance to improve. However, in addition to the regulator design problem, the harmonics due to asynchronous pulsewidth modulation (PWM) in such low pulse ratios are obvious and may result in torque ripples and noises, which cannot be restrained effectively just by regulator design [6].

Synchronizing PWM is considered an effective method to remove these harmonics. Typically, they include synchronous space vector PWM (SSVPWM) and synchronous optimal PWM (SOPWM) aiming to minimize current total harmonic distortion or eliminate selective harmonics [7], [8], [9], [10]. The voltage pulses of these schemes are customized to half-wave symmetry, quarter-wave symmetry, and three-phase symmetry, thus suppressing even-harmonics and subharmonics theoretically. For example, as shown in Fig. 1, the vector sequence generated at 30° is 0127, at 90° is 7210, and so on. On this basis, the above symmetries can be realized with $P = 3$ [7]. Of course, there is not only one SSVPWM strategy conforming to the above symmetries, but various SSVPWM strategies have a common feature with

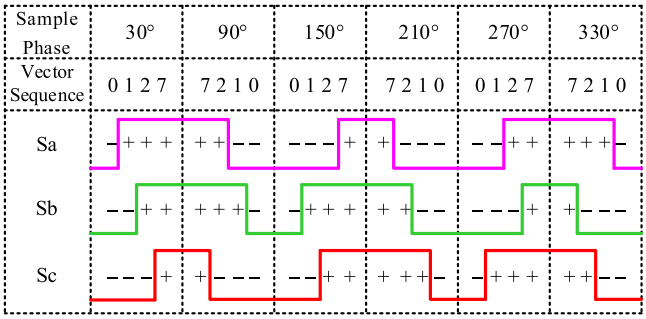

Fig. 1. Sample phase, vector sequence, and pulse of SSVPWM with $P = 3$. (0 and 7 represent zero vectors, 1 and 2 represent active vectors, and + and − represent high and low levels.)

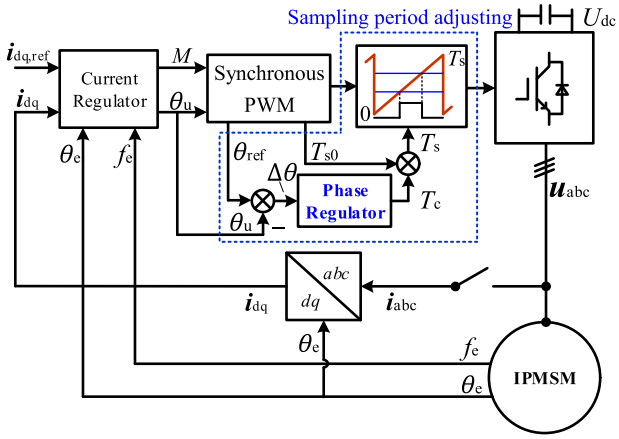

Fig. 2. Diagram of the drive system with a synchronous PWM.

Fig. 1, that is, specific vector sequences are generated at specific sampling phases, typically including conventional space vector strategy, basic bus clamping strategy, and boundary sampling strategy, which are summarized well in [7] and [8].

In [11], a similar sampling premise is also imposed on SOPWM to facilitate the acquisition of the fundamental current.

It has been proved in [12] and [13] that the sampled current with SOPWM contains significant harmonic contents. Using fundamental component observers is widely recognized as a resource-intensive method [13]. Therefore, to eliminate the 6th harmonic conveniently, the desired sampling phases in [11] are artificially fixed at $(\pi/6) \times n$, $n = 0, 1, \ldots, 11$, since the 6th harmonic has opposite values at each multiple of $\pi/6$, meaning that it can be eliminated by averaging two sampling values with $\pi/6$ intervals. Nonetheless, the sampling phase of the command voltage in a field-oriented control (FOC) system is calculated from its current regulator and is generally random [14]. If the voltage phases out of the current regulator are artificially fixed at those specific phases, the current reference cannot be tracked and even oscillations appear. On the contrary, if the voltage command is faithfully used to produce PWM, the obtained pulse pattern would lose symmetry characteristics, degrading the harmonic property.

To release this conflict, the scholars in [11], [15], [16], [17], and [18] incorporated SSVPWM or SOPWM into the FOC with a sampling period adjustment mechanism, as seen in Fig. 2, to forwardly control the phase error between these two voltages in real time. P or PI regulators are often selected as phase regulators. As a result, the voltage sampling phase can indeed be locked to the desired phase in the steady state. However, during the transient state, the convergence rate is closely related to the regulator parameters. Yang et al. [15] reported that their phase regulation method can work in a deadbeat fashion, but it was pointed out in [16] that the method in [15] may cause oscillations due to the time delay. As a solution, they gave an optimal parameter design of the P regulator by trial-and-error, but could not achieve the deadbeat response. In [17], a PI regulator is used, but the integral action would further reduce the response speed. In [18], the reported regulator parameter follows that given in [16]. Besides, to improve the response speed, a feedforward (FF) mechanism is introduced to compensate for a possible sudden phase error in the dynamic process [11]. However, the simultaneous action of the FF mechanism and the phase regulator inevitably produces an overshoot, causing prolongation of the transient process. Since the theory about the phase regulator design in this synchronous PWM-based closed-loop current control application has not been built up to date, the above empirical method cannot give the optimal design in any way.

Although there are some research works around the phase regulation loops themselves [19], [20], [21], [22], the model and the control focus are usually different due to the different research objects. Common phase regulation loops which mainly focus on antinoise or filtering ability are not suitable for the study in this article. In the synchronous PWM-based FOC system, the current loop is coupled with the phase regulation loop, whose output voltage phase is affected by the behavior of the current regulator. In other words, the current control itself will bring disturbance to the phase regulation loop, which is unique in this study. If the principle of the interaction between the phase regulation loop and the current loop is not clear, the system may be not stable or some oscillations appear due to inappropriate design. In [11], [15], [16], [17], and [18], the entire current loop conventionally operated in a slow dynamic manner. The authors think that this may be a compromise to suppress the dynamic oscillations, which will be explained by the analysis and overcome by the optimization design proposed in this article.

The main contribution of this article is that the principle behind the phase regulation loop in a synchronous PWM-based closed-loop current control scheme and its connection with the current control is revealed through discrete-time modeling analysis, by which a deadbeat phase regulation method is proposed and the guidance for the design of the current regulator is presented. The results show that the dynamic response of the redesigned closed-loop system is enhanced significantly compared with the state-of-the-art designs.

II. Analysis of Existing Problem

To facilitate understanding, the sampling period adjustment mechanism in Fig. 2 is reviewed in this section. This mechanism is an addition to the typical FOC structure. Its function is to adjust

the carrier period (i.e., sampling period) in real time according to desired and actual voltage sampling phases, in which the desired voltage sampling phases θ_{ref} are some fixed values while the actual voltage sampling phase θ_u is calculated by the current regulator time-by-time, i.e.,

$$\theta_u = \theta_e + a\tan(u_q/u_d) \tag{1}$$

where θ_e is the sampled electrical angle, and u_d and u_q are the d- and q-axis output voltages of the current regulator. Generally, the current regulator designed directly in the discrete-time domain is beneficial to overcome the adverse effects of control delay and discretization errors. Therefore, the authors employ the digital current regulator in [5], which is not the focus of this article and will not be detailed.

Since u_d and u_q cannot be adjusted artificially, to keep θ_u synchronizing with θ_{ref}, the sampled electrical angle θ_e should be controlled according to (1), which is achieved by adjusting the sampling period T_s, usually through two steps:

Step 1 (S1) is that the initial sampling period T_{s0} is adapted to the electrical frequency f_e. As for a specific synchronous PWM scheme, the desired sampling phases θ_{ref} are usually fixed and evenly distributed over one fundamental period [7], [8]. The increment of θ_{ref} in each sample should be exactly equal to the electrical angle increment within T_{s0}, denoted as θ_{fix} (i.e., $\theta_{\text{fix}} = 2\pi f_e \cdot T_{s0}$). Based on this, the initial sampling period T_{s0} can be determined, i.e., $T_{s0} = \theta_{\text{fix}}/(2\pi f_e)$. For example, T_{s0} is set as $1/(12f_e)$, when θ_{ref} are fixed at $(\pi/6)\times n, n = 0, 1, \ldots, 11$, i.e., $\theta_{\text{fix}} = \pi/6$, as presented in [11]. As a result, the increment of θ_e in (1) in each sample is exactly equal to θ_{fix}. In other words, θ_u can maintain the same increment with θ_{ref} during the steady state, which makes it possible to synchronize two voltage phases.

Step 2 (S2) is to compensate for the phase error $\Delta\theta$ by calculating the compensation value T_c of the sampling period. A sampling at the frequency obtained from S1, the phase error, $\Delta\theta = \theta_{\text{ref}} - \theta_u$, may still appear, adversely interfering with current responses. Mitigating $\Delta\theta$ as quickly as possible, especially during transients is crucial to improve dynamic response. The phase regulator calculates the compensation value T_c, added to T_{s0}, so that the next sampled electrical angle θ_e can be adjusted, i.e., $\theta_{e,k+1} = \theta_{e,k} + \theta_{\text{fix},k} + \theta_{c,k}$, where $\theta_{c,k} = 2\pi f_e \cdot T_c$ represents the compensation angle (the delay is not considered temporarily). As a result, θ_u is expected to be adjusted to θ_{ref}.

How to lock θ_u to θ_{ref} as quickly as possible in addition to stabilizing the current control is an interesting research topic. Although the designs of the phase regulator have been given in [11], [15], [16], [17], and [18], these designs may not be optimal because they are usually given based on experience rather than rigorous mathematical analysis. Besides, at first sight, the above work is done only through the phase regulator in Fig. 2. However, it is worth noting that θ_u is also affected by u_d and u_q in (1), especially during the transient state. In other words, the behavior of the current regulator will also have an effect on the dynamic response, which unfortunately has not been a concern in the previous research work. To illustrate this conclusion intuitively, it will be explained from two aspects, i.e., the phase regulation loop itself and its connection with the current control.

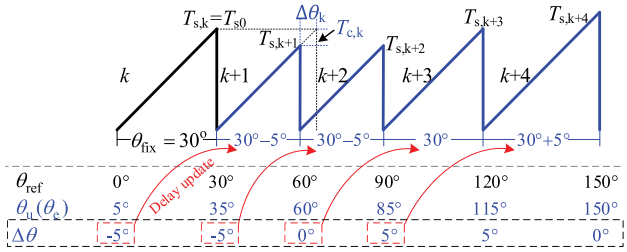

Fig. 3. Failed phase-locked implementation process.

A. Phase Regulation Loop

In the analysis of the phase regulation loop itself, the influence of current control is not considered temporarily, meaning that $a\tan(u_q/u_d)$ in (1) is assumed to be constant and might as well be 0, i.e., $\theta_u = \theta_e$. Assume that a phase error, $\Delta\theta_k = \theta_{\text{ref},k} - \theta_{u,k} = \theta_{\text{ref},k} - \theta_{e,k} \neq 0$, is produced at the kth sampling instant, as shown in Fig. 3. To eliminate $\Delta\theta_k$, the sampled electrical angle will be corrected by adjusting the sampling period, i.e., the electrical angle increment θ_{fix} will be adjusted. Intuitively, compensating $\Delta\theta_k$ completely in one sampling period is best for fast dynamic response, as attempted in [15]. The desired compensation value for the kth period, i.e., $T_{c,k}$, is calculated as

$$\begin{aligned} \Delta\theta_k &= \theta_{\text{ref},k} - \theta_{u,k} \\ T_{c,k} &= \Delta\theta_k/(2\pi f_e). \end{aligned} \tag{2}$$

In theory, $T_{c,k}$ should be added to T_{s0}, producing a new sampling period $T_{s,k}$ in the kth interval. However, the period register in a DSP is usually uploaded in a shadow mode to avoid uncertain interferences (i.e., existing time delay). In other words, the new sampling period T_s does not change until the $(k+1)$th interval (see Fig. 3). As a result, the angle compensation actually takes effect in the $(k+2)$th interval, i.e.,

$$T_{s,k+1} = T_{s0} + T_{c,k} \tag{3a}$$

$$\theta_{e,k+2} = \theta_{e,k+1} + \theta_{\text{fix},k+1} + \Delta\theta_k. \tag{3b}$$

Based on (3b), the mathematical expression of the phase error at the $(k+2)$th instant can be derived as

$$\begin{aligned} \Delta\theta_{k+2} &= \theta_{\text{ref},k+2} - \theta_{e,k+2} \\ &= \theta_{\text{ref},k+1} + \theta_{\text{fix},k+1} - (\theta_{e,k+1} + \theta_{\text{fix},k+1} + \Delta\theta_k) \\ &= \Delta\theta_{k+1} - \Delta\theta_k. \end{aligned} \tag{4}$$

Iterating (3b) and (4) repeatedly, the phase error $\Delta\theta$ in the subsequent intervals can be calculated, as highlighted with an example within the dotted box in Fig. 3. As seen, $\Delta\theta$ would pulsate at a constant amplitude. This phenomenon is also seen in [16]. In other words, this complete compensation will fail due to the time delay. To address this problem, Kim et al. [16] used a proportional regulator to control $\Delta\theta$, by which (3) and (4) can be rewritten as

$$T_{s,k+1} = T_{s0} + \alpha \cdot \Delta\theta_k/(2\pi f_e) \tag{5a}$$

$$\theta_{e,k+2} = \theta_{e,k+1} + \theta_{\text{fix},k+1} + \theta_{c,k} \tag{5b}$$

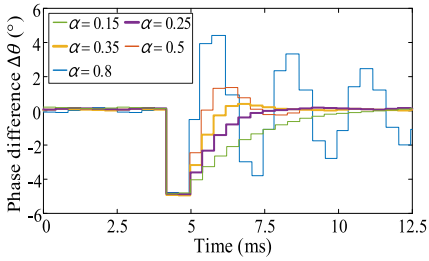

Fig. 4. Simulation result of phase error response with different α. (At some time, a step phase error of 5° is added in $\Delta\theta$, which is adjusted by the phase regulation loop subsequently).

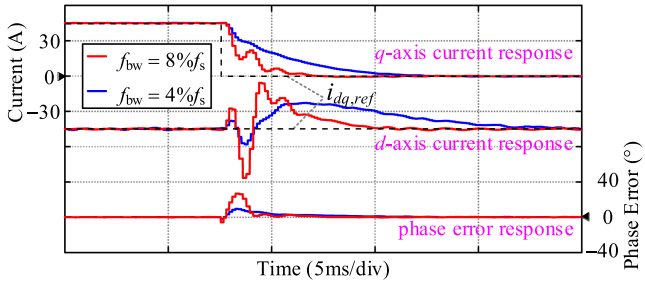

Fig. 5. Simulation results of current step response under different current loop bandwidths and $\alpha = 0.3$.

and

$$\Delta\theta_{k+2} = \Delta\theta_{k+1} - \theta_{c,k} \tag{6}$$

where α is the proportional parameter used to adjust the size of the compensation and $\theta_{c,k} = \alpha{\cdot}\Delta\theta_k$ represents the adjusted compensation angle.

By a simulation-based trial-and-error method in [16], it is found that choosing α in the range of 0.25–0.35 can realize the tradeoff between response speed and damping, as shown in Fig. 4. Therefore, it is recommended to choose $\alpha = 0.3$ in [16]. Similar empirical parameter choices can be found in [11] and [18]. Besides, it is easy to find that $\Delta\theta$ in Fig. 4 can converge to 0 after a transient, so there is no need for integration action in the phase regulator.

However, due to the absence of theoretical guidance, empirical designs can be problematic or at least usually suboptimal. As seen in Fig. 4, based on this proportional regulation, $\Delta\theta$ requires more than six samples to reach the steady state, meaning that the response time of the current loop will be longer theoretically since the current loop is the outer loop from Fig. 2. It is well known that the dynamic response of the current loop is crucial for machine drive and the subject of dynamic improvement for current control has received a lot of attention over several decades [2], [3], [4], [5]. Nonetheless, the above-phase control method will severely limit this dynamic performance.

B. Effect of Current Control on Phase Control

Another problem that needs to be clarified is the effect of current control on the phase control. As indicated by (1), output voltages of the current regulator will affect the actual voltage sampling phase θ_u, i.e., the input of the phase regulation loop, which in turn affects the output PWM voltage and the resulting currents. In other words, the current control and the phase control are coupled with each other. If this coupling is not well handled, the dynamic response of the whole control loop will be significantly decreased.

For example, Fig. 5 shows the current step responses under two different current loop bandwidths and the same phase regulator parameter $\alpha = 0.3$. As seen, the current loop bandwidth has a significant effect on the whole closed-loop system dynamics. At low bandwidth $f_{\rm bw} = 4\%f_s$, the response speed is slow and the oscillation is small. By contrast, increasing the bandwidth to $f_{\rm bw} = 8\%f_s$ increases the response speed but intensifies the oscillation. It is important to emphasize that this phenomenon is not caused by the current control itself. Because even at higher bandwidths there is no such oscillation based on an asynchronous SVPWM scheme without the above phase regulation loop in [5]. To avoid this phenomenon, previous designs usually set a low current loop bandwidth, or used ramp current responses instead of step current responses, which limited the dynamic response speed severely [11], [15], [16], [17], [18].

Through the above analysis, it can be seen that the traditional synchronous PWM closed-loop design still has the problems of poor phase regulators and overall system control designs. To explain and address these problems, an analytical discrete-time design method for the synchronous PWM closed-loop system is proposed in the next section.

III. Discrete-Time Analysis and Control Design

A. Phase Regulation Loop Modeling

To analyze the above problems, an analytical discrete phase regulation loop model is needed first. From the review of the sampling period adjustment mechanism in Section II, the block diagram of the phase regulation loop can be established, as shown in Fig. 6, whose five main parts are given as follows:

1) reference phase generator;
2) error regulator;
3) angle-time converter;
4) angle adjustment plant;
5) disturbance generator.

1) Reference Phase Generator: The reference phase generator provides the reference phase, which equals the sum of the value of the previous instant and a fixed increment. It should be noted that for a specific synchronous PWM scheme, the angle increment $\theta_{\rm fix}$ and the angle initialization value are certain. For example, as shown in Fig. 1, the angle increment $\theta_{\rm fix}$ for this synchronous PWM scheme is 60°, and the angle initialization value is any one of the six sample phases (30°, 90°, 150°, 210°, 270°, or 330°), depending on the initial stator space voltage vector angle of the machine when this scheme is put into operation. Therefore, the reference phase $\theta_{\rm ref}$ produced by this part is a completely undisturbed angle variable.

2) Error Regulator: The error regulator calculates the expected compensation value to make up for the phase error. The P regulator is the common selection previously, but may not be the most appropriate in this study. Later, the appropriate form

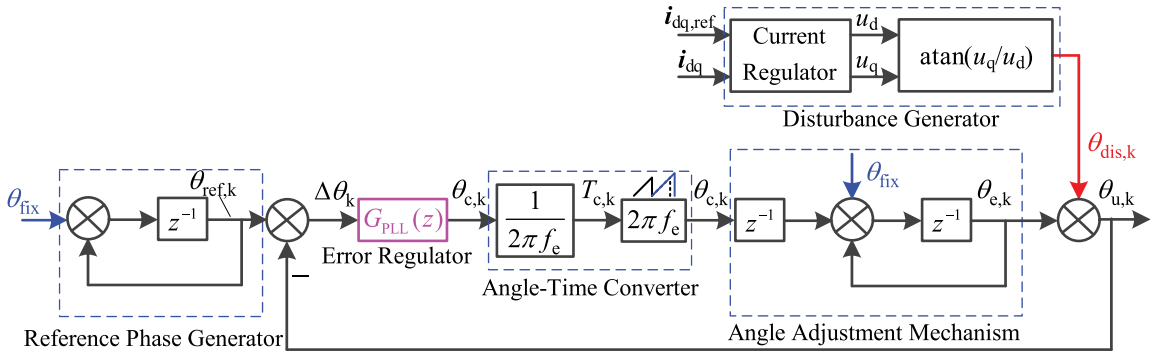

Fig. 6. Block diagram of the phase regulation loop.

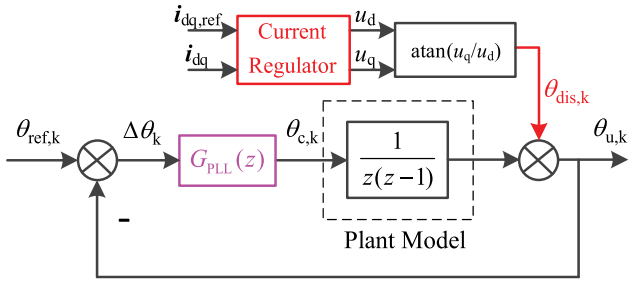

Fig. 7. Simplified block diagram of the phase regulation loop.

of the regulator will be discussed after all parts are introduced completely.

3) Angle-Time Converter: The angle-time converter translates the compensation value of the angle into the adjustment value of the sampling period. It should be noted that changing the sampling period is a physical implementation. However, for the phase regulation loop analysis, this process needs to be viewed in terms of the angle increment, which is the reason for first dividing by $2\pi f_e$ and then multiplying by $2\pi f_e$ in Fig. 6. In other words, this execution process is redundant to the control schematic analysis.

4) Angle Adjustment Plant: The angle adjustment plant is derived from (5b), which has been explained in detail in Section II-A. It is important to emphasize that there is a time-delay factor z^{-1}, which is different from the reference phase generator.

5) Disturbance Generator: Although u_d and u_q derived from the current regulator output cannot be adjusted artificially, they always vary with behaviors of the current regulator. Therefore, at the end of the phase regulation loop, the effect of the current regulator output must be taken into account, as indicated by (1). From the control schematic view, the output of the current regulator should be regarded as a disturbance to the phase regulation loop. It is especially important to emphasize that this disturbance is the only excitation input to this loop. The other two inputs $\theta_{\rm fix}$, marked with blue arrows, do not affect the response of this loop because they are fixed values.

Therefore, this phase regulation loop should be designed primarily around restraining the disturbance caused by the output variation of the current regulator. To facilitate subsequent analysis, the control schematic is simplified as Fig. 7 by ignoring the effect of two constant inputs $\theta_{\rm fix}$.

B. Discrete-Time Analysis of Previous Design

A synchronous PWM scheme must strictly produce the PWM pulses based on the reference phase $\theta_{\rm ref}$ applied in sequence rather than the actual voltage output phase θ_u, to avoid excessive switching actions, which may damage power devices [23]. In other words, only by locking θ_u to $\theta_{\rm ref}$ as quickly as possible can the current loop be stabilized as quickly as possible, otherwise the error between the actual output voltage (faithful to $\theta_{\rm ref}$) and desired control voltage (faithful to θ_u) will produce continuous disturbance to the current control, intensifying the dynamic oscillations. Based on this reason, previous researchers usually focused on the reference tracking performance of the phase regulation loop [11], [15], [16], [17], [18]. However, in authors' opinion, the disturbance rejection performance in addition to the reference tracking performance is also quite important for the design of the phase regulation loop, since the sole source of excitation on the phase regulation loop is actually the disturbance brought by the current control. To analyze this effect, the phase regulation loop in Fig. 7 can be mathematically modeled as

$$\theta_{u,k}=\frac{G_{\rm PLL}(z)}{z^2-z+G_{\rm PLL}(z)}\theta_{{\rm ref},k}+\frac{z^2-z}{z^2-z+G_{\rm PLL}(z)}\theta_{{\rm dis},k}. \tag{7}$$

When the proportional regulator is applied, it can be further simplified as

$$\theta_{u,k}=\frac{\alpha}{z^2-z+\alpha}\theta_{{\rm ref},k}+\frac{z^2-z}{z^2-z+\alpha}\theta_{{\rm dis},k}. \tag{8}$$

In Fig. 8, the root locus map of (8) is drawn. The two roots overlap on the real axis at $\alpha=0.25$, which corresponds to the fastest dynamic response under the damping ratio equal to 1. Further increasing α to 0.35, the response speed would be faster, but the damping ratio decreases to 0.707. From the control textbook [24], to achieve a compromise between the response speed and the damping ratio, the parameters are generally designed in the damping ratio from 0.707 to 1. Therefore, the appropriate range for the proportional parameter α is $\alpha\in[0.25, 0.35]$, which corresponds well to the simulation-based results in Fig. 4. By the way, if the FF mechanism in [11] is adopted, based on the proposed modeling method, it is not difficult to

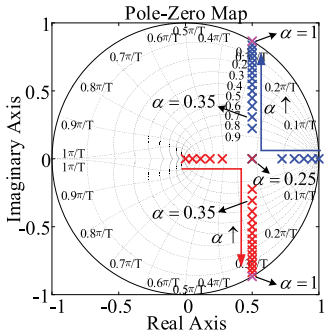

Fig. 8. Root locus of (8) with different α.

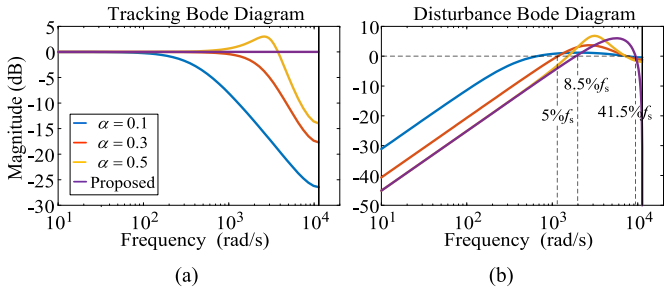

Fig. 9. Bode plots of the tracking and disturbance transfer functions in (8) and (10) (conditions: $f_s = 3.6$ kHz.). (a) Tracking response. (b) Disturbance response.

find that the phase regulation loop cannot realize the deadbeat response since the FF mechanism cannot change the closed-loop poles of the plant. Besides, an overshoot will occur due to the simultaneous action with the phase regulator.

To further explain the effect of the current control on the phase regulation loop, the magnitude–frequency responses of the tracking and disturbance transfer functions in (8) are plotted in Fig. 9. On the one hand, for the tracking response, the larger α is, the higher the bandwidth is, but too large α will cause a bulge in the amplitude–frequency response, resulting in a large overshoot. Therefore, $\alpha = 0.3$ seems like a good choice. On the other hand, as for the disturbance response, the low-frequency disturbance can be well suppressed in general. With the increase in the frequency of the disturbance signal, the attenuation effect becomes weak. Even when the frequency is higher than a certain value, there will be an amplification effect. The critical frequency for the parameter selection of $\alpha = 0.3$ is about $5\% f_s$ Hz. In other words, if the output signal of the current regulator contains a signal with a frequency higher than this critical frequency, this signal will be amplified into the output phase, intensifying the oscillation of the phase regulation loop, which in turn intensifies the oscillation of the current loop. This explains why the oscillations in Fig. 5 with a bandwidth of 8% f_s Hz are significantly higher than those with $4\% f_s$ Hz. At low bandwidth, the high-frequency component of the output signal of the current regulator can be effectively attenuated, so that the disturbances entering the phase regulation loop are mainly low-frequency signals, which can be effectively attenuated by the phase regulation loop itself.

However, reducing the bandwidth of the current regulator to suppress the oscillation is obviously not an optimal solution since the response time will be longer, as seen in Fig. 5.

C. Proposed Discrete-Time Phase Regulator

From the above analysis, it is easy to find that the focus of improvement at hand is how to effectively suppress oscillations without reducing the bandwidth of the current loop excessively. Adding a low-pass filter to the output phase of the current regulator appears to suppress oscillations but reduces the response speed inevitably. Actually, the upper limit of the frequency of the suppressed disturbance signal in the phase regulation loop determines the upper limit of the bandwidth of the current loop. Therefore, the efficient solution is to improve the performance of the phase regulation loop, which can be achieved by improving the phase regulator. More specifically, through the improvement of $G_{\mathrm{PLL}}(z)$ in (7), the critical frequency of the disturbance response amplitude–frequency curve can shift to the right, while at the same time not making the tracking response amplitude–frequency curve bulge to avoid an overshoot.

From the control theory [24], if all the closed-loop poles are placed at the origin, the disturbance is expected to be suppressed in the shortest possible time. To this aim, the desired characteristic polynomial can be expressed as z or z^2. After derivation, it is found that $G_{\mathrm{PLL}}(z)$ corresponding to the former is physically unrealizable. Therefore, only based on the latter case, the proposed control law is uniquely derived as

$$G_{\mathrm{PLL}}(z) = \frac{z}{z+1}. \tag{9}$$

Substituting (9) into (7), one has

$$\theta_{u,k} = \frac{1}{z^2}\theta_{\mathrm{ref},k} + \left(1 - \frac{1}{z^2}\right)\theta_{\mathrm{dis},k}. \tag{10}$$

As seen, both poles are placed at the origin, thus the fastest dynamic response is achieved.

For digital implementation, the proposed phase regulator (9) can be expressed as

$$\theta_{c,k} = \Delta\theta_k - \theta_{c,k-1} \tag{11a}$$

$$T_{s,k+1} = T_{s0} + T_{c,k} = T_{s0} + \theta_{c,k}/(2\pi f_e) \tag{11b}$$

where $\theta_{c,k}$ in (11a) is the compensation angle determined by the phase error in the kth interval and the previous compensation angle in the $(k-1)$th interval. As seen, there are no tuning parameters for the proposed phase regulator, which is easy to use directly.

To intuitively compare the reference tracking and disturbance rejection performance of the proposed design with those of the traditional design, amplitude–frequency responses of the proposed design are also plotted in Fig. 9. As seen, the proposed phase regulator can track the reference signal without attenuation, whereas the traditional phase regulator cannot reach the bandwidth of the proposed phase regulator no matter how the parameter is adjusted. It should be noted that the desired references θ_{ref} in a synchronous PWM are constants. Therefore, there is no noise that needs to be suppressed for the reference

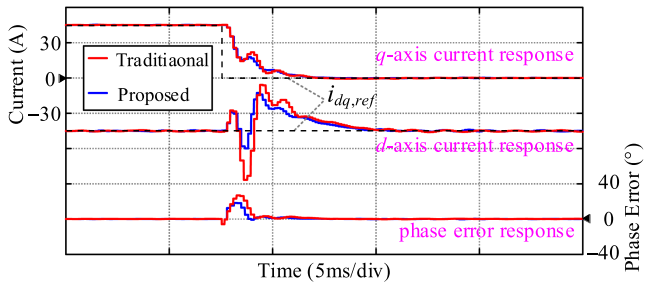

Fig. 10. Simulation results of current step response with different phase regulators and $f_{\rm bw} = 8\%f_s$.

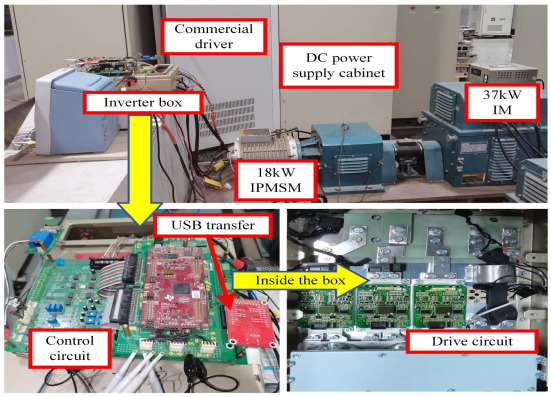

Fig. 11. IPMSM drive test rig.

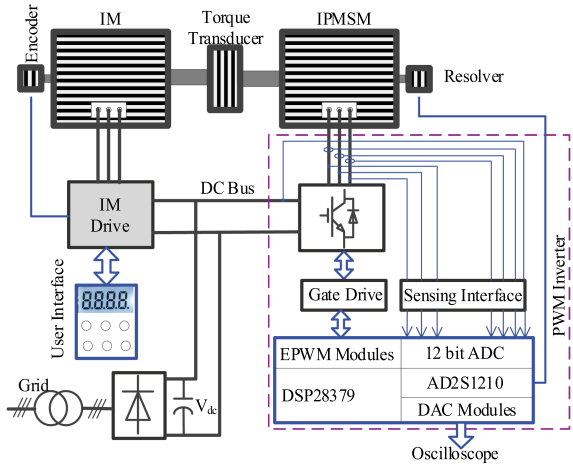

Fig. 12. Block diagram of the test bench.

TABLE I
PARAMETERS OF THE 18-KW IPMSM DRIVE SYSTEM

Parameter	Magnitude
Stator resistance R_s	0.06 Ω
d-axis inductance L_d	0.31 mH
q-axis inductance L_q	1.04 mH
PM flux linkage φ_f	0.078 Wb
Maximum speed f_{max}	300 Hz

tracking. Its rapidity can be fully utilized under no overshoot. As for the disturbance response, the critical frequency is about 8.5% f_s Hz for the proposed design, which is 1.7 times the traditional design of 5% f_s Hz.

To verify the improvement in the dynamic performance, the current step responses with the proposed phase regulator are performed again and shown in Fig. 10. All settings are the same as those in Fig. 5 except for the phase regulators. The current loop bandwidth is set as $f_{\rm bw} = 8\% f_s$ (slightly less than the upper limit as suggested in Fig. 9). As seen, the phase error and current oscillations with the proposed phase regulator are obviously suppressed under this high bandwidth. Besides, compared with the low-bandwidth case in Fig. 5, the response speed is obviously improved.

By the way, only from the result, the proposed design in this article seems a little simple, but the theoretical analysis, new insights on the focus of the phase regulation loop, and improvement ideas provide important guidance for the synchronous PWM-based closed-loop current control design, based on which better control performance can be obtained.

IV. Experimental Results

The DSP TMS320F28379 based experimental platform is shown in Fig. 11, and its block diagram of circuit topology is shown in Fig. 12. The effectiveness of the proposed scheme is validated on an 18-kW IPMSM drive system with parameters in Table I, and a 37-kW IM is used as the load machine, operating in the speed-regulation mode and changing the load with the load variation of the tested IPMSM. The current regulator is designed for an IPMSM as presented in [5]. Other types of machines differ only in the design of the current regulator. The proposed improvement for the phase regulation loop is universal to any type of machine. An SOPWM with $P = 7$, aiming to eliminate 5th and 7th harmonics is adopted. The desired sampling instants $\theta_{\rm ref}$ are set at $(\pi/6)\times n$, $n = 0, 1, \ldots, 11$, to facilitate adopting the fundamental current sampling method in [11]. The initial sampling period T_{s0} is set as $1/(12f_e)$ and constantly regulated by the output T_c of the phase regulator. Detailed principles of the SOPWM and the current sampling method can be found in [10] and [11], which are not the focus of this article. In the following test, the proposed phase regulator will be compared with the commonly used proportional regulator [11], [16], [17], [18]. As suggested in [18], the proportional parameter α is set as 0.3, though no parameter is required for the proposed phase regulator.

Two data acquisition methods are adopted in experiments. One is to capture the actual voltage pulse and currents through the oscilloscope (the right sides of Figs. 14 and 15), and the other is to transfer the variable data in the DSP program (d- and q-axis currents on the left sides of Figs. 14 and 15, and various angle variables in Figs. 13–15) to the PC through a high-speed USB communication in real time. The former method is necessary to capture the actual voltage and current signal, and the latter method really reflects the actual values faced by the designed control algorithm, which is beneficial to the evaluation of the control performance. Besides, when using high-speed USB communication, the upload frequency is the same as the sampling frequency of the control system.

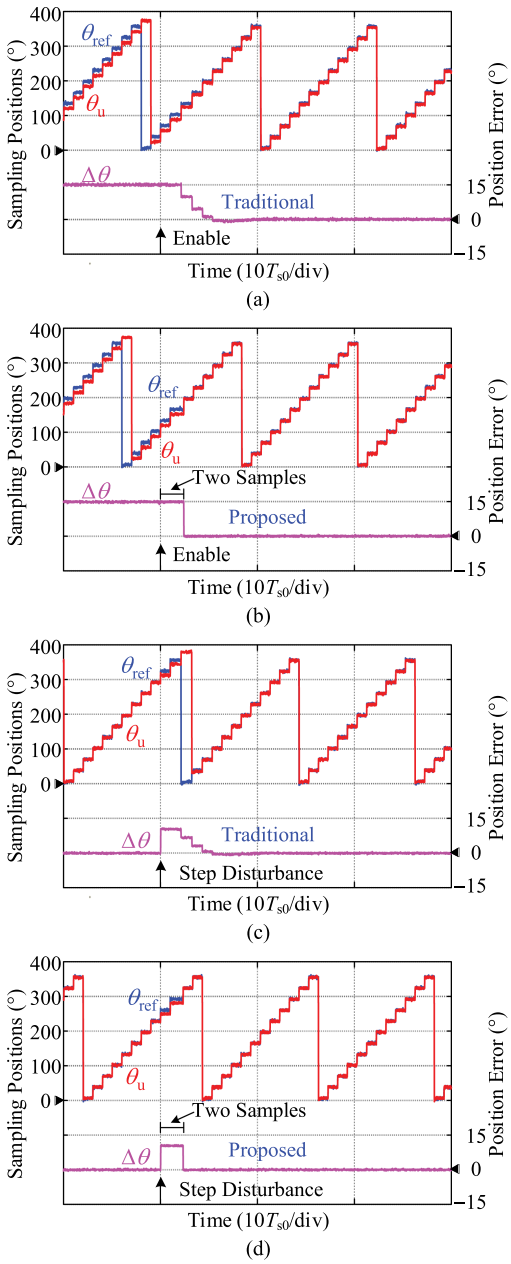

Fig. 13. Open-loop test for the phase regulation loop. (a) Tracking response for the traditional scheme. (b) Tracking response for the proposed scheme. (c) Disturbance response for the traditional scheme. (d) Disturbance response for the proposed scheme.

To avoid the interference of the current regulation on the phase regulation loop, the open-loop tests for the phase regulation loops themselves, without connecting IPMSM, are performed first and shown in Fig. 13. In the DSP program, an angle variable with an integral step of $T_s = T_{s0} + T_c$ and a frequency of 300 Hz is used as the voltage phase θ_u, instead of the output of the current regulator. First, the phase regulators are not enabled, i.e., $T_c = 0$. At some time, the phase regulators are enabled, which can verify the reference tracking performance, as shown in Fig. 13(a) and (b). Then, after θ_u converges to $\theta_{\rm ref}$, a step disturbance of $-10°$ is added to θ_u to verify the disturbance rejection performance, as shown in Fig. 13(c) and (d). As seen, for both the reference tracking and the disturbance rejection, the phase error $\Delta\theta$ of the proposed scheme converges to 0 in two samples without any oscillations, whereas the previous scheme requires more than six samples, which verifies the significant improvement of the proposed phase regulation loop itself in the dynamic response.

To further verify the dynamic improvement in the current response brought by this proposed scheme, the closed-loop current step and disturbance responses using two different phase regulators are compared in Figs. 14 and 15, respectively. The desired bandwidth of the current regulator is tuned to about 8% f_s Hz according to the above theoretical analysis. The IPMSM is driven to its maximum speed of 300 Hz by the load machine. Besides, for protection, the output T_c of the phase regulator is limited to $T_c \in [-0.3T_{s0}, 0.3T_{s0}]$.

Fig. 14 shows the unloading test using two different phase regulators. At some time, the load reference current steps back to 0, after which disturbances due to the regulation of the current regulator are constantly input into the phase regulation loops, causing longer settling time in this closed-loop test than the open-loop result in Fig. 13, but this does not affect the performance comparison. Obviously, the phase error $\Delta\theta$ and the responses of both the d- and q-axis currents using the proposed scheme have much smaller oscillations than those using the previous scheme, which verifies the enhancement in reference tracking performance with the proposed scheme. Besides, from the point of view of the shift degree of the phase current in the dynamic process, the phase current in Fig. 14(a) shifts significantly, while the phase current in Fig. 14(b) does not. By the way, the symmetries of gate pulses are well maintained even during the dynamic since the synchronous PWM scheme strictly produces the PWM pulses based on the reference phase $\theta_{\rm ref}$ applied in sequence rather than the current regulator output θ_u.

For the electric drive system, the most important disturbance comes from the back electromotive force (EMF) disturbance under the sudden change of the machine speed. However, it is usually difficult to simulate extreme accelerations in the laboratory due to mechanical limitations. As known by the mechanical voltage equation, a sudden change in the back EMF causes a sudden change in the q-axis voltage [3], thus applying a step voltage (20 V in this experiment) to the q-axis voltage command is a simple and widely used method for testing disturbance rejection performance of a closed-loop current control system [5]. Fig. 15 shows the current response to step disturbances using two different phase regulators. During the dynamic process, the current regulator output is saturated and the generated PWM pulses are almost constant over every fundamental period, creating an extreme situation for testing the behavior of the current regulator with the phase regulation loop. Since the phase regulation loop is the inner loop, it will not fail even in the presence of the dynamic saturation of the current loop. Obviously, a better dynamic, with a smaller oscillation amplitude and settling time, is achieved by the proposed scheme in Fig. 15.

In conclusion, compared to the previous scheme, in addition to the enhancement of the phase regulation loop itself, the two key

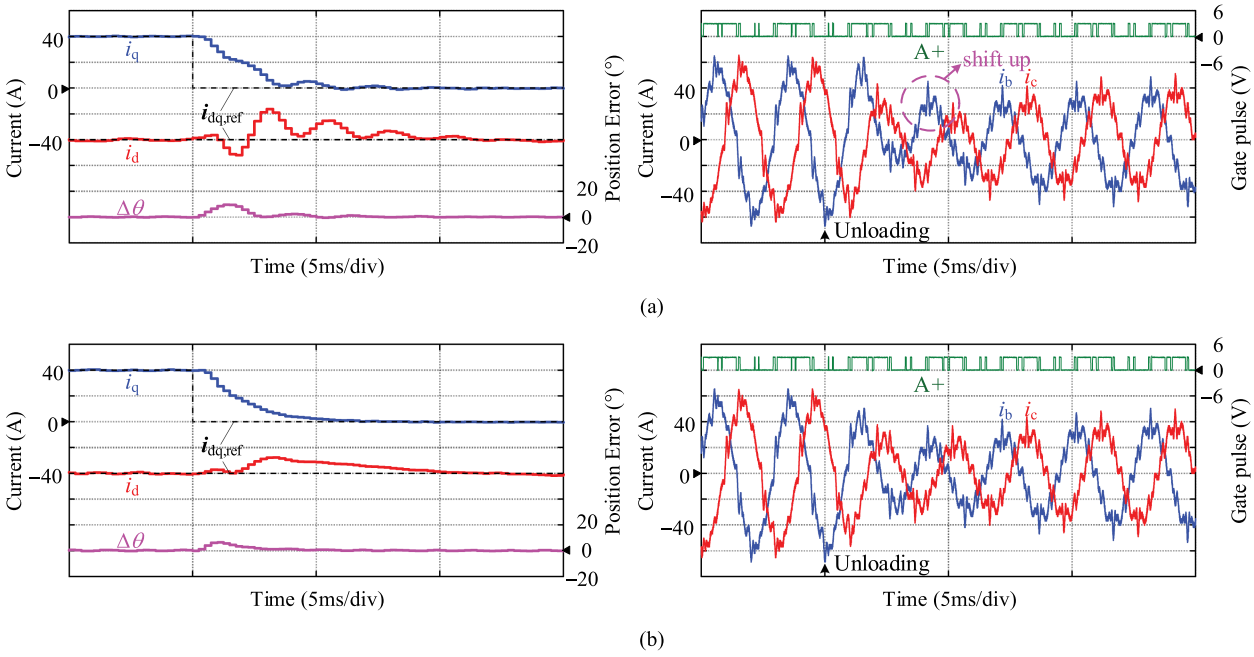

Fig. 14. Results of the unloading experiments. (a) Using the traditional scheme. (b) Using the proposed scheme.

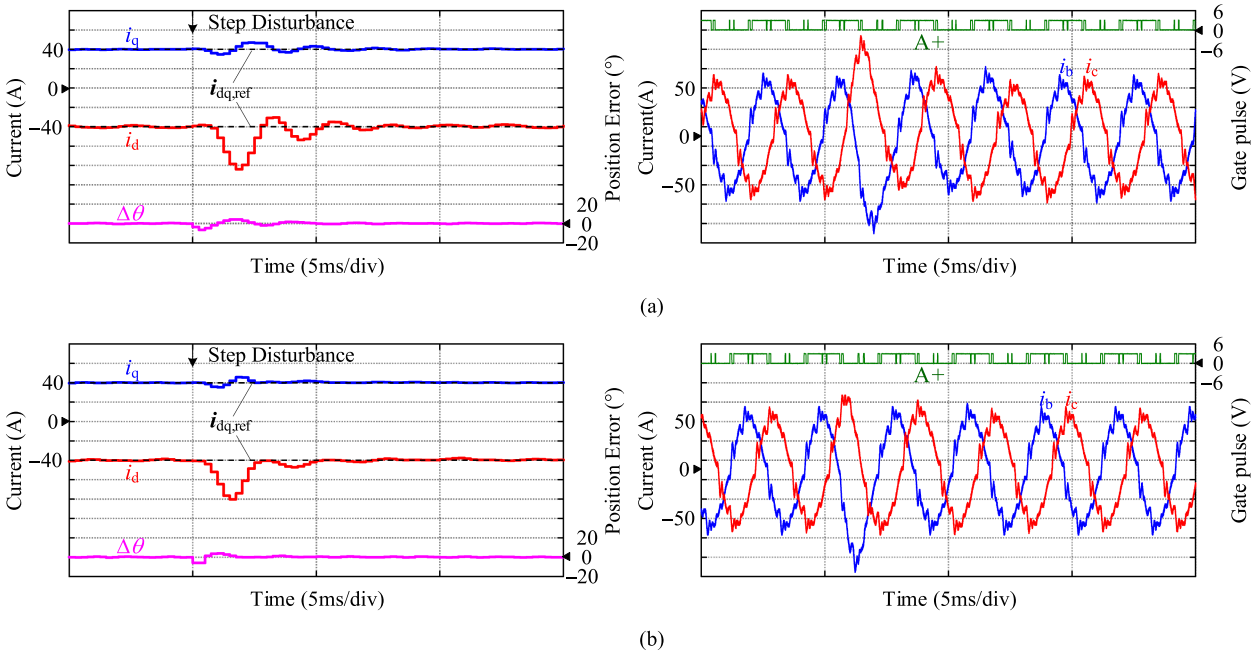

Fig. 15. Current responses to step disturbances. (a) Using the traditional scheme. (b) Using the proposed scheme.

performance indicators (both reference tracking and disturbance rejection) for the current control are improved based on the proposed scheme.

Besides, the harmonic analysis result of the phase current by using the SOPWM in the steady state is shown in Fig. 16. Somewhat unexpectedly, although the SOPWM aiming to eliminate the 5th and 7th PWM harmonics is used, there are still slightly 5th and 7th harmonics presented in the stator currents, which are mainly caused by 5th and 7th back-EMF harmonics of IPMSM. By the way, although the current harmonic characteristics obtained with synchronous PWM at such a low pulse ratio are undoubtedly better than those obtained with traditional asynchronous SVPWM [6], this does not mean that using synchronous PWM will maintain fairly good sinusoidal output currents. After all, the fact that a fundamental period has only a few pulses makes it difficult to approximate a standard sine waveform anyway.

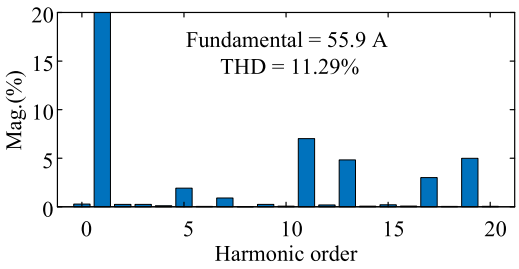

Fig. 16. Harmonic spectrum of the phase current of the SOPWM in Figs. 14 and 15 in steady state.

V. Conclusion

The problem of poor dynamic response of the current control with the traditional synchronizing technique for PWM is studied in this article. Through the discrete-time modeling analysis, the theory of the phase regulation loop implementing the synchronous PWM-based closed-loop current control and its interaction with the current control loop is revealed, based on which the reason for the poor dynamic response is explained. Furthermore, an improved discrete-time phase regulator with a deadbeat response is proposed, and the guidance for the design of the current regulator is presented, which yields a great dynamic response, as demonstrated by the experimental results. The contribution of this article lays a solid foundation for designing a synchronous PWM-based closed-loop current control.

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