Adaptive Synchronous Rectifier On-Time Control Within Dead-Time for Improving Light-Load Performance of *LLC* Resonant Converters

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***Abstract*—*LLC* resonant converter exhibits nonmonotonic voltage gain at light-load, which could lead to the malfunction of traditional pulse frequency modulation strategy and degraded efficiency due to excessive increase in switching frequency. To address this issue, an adaptive synchronous rectifier (SR) on-time control within dead-time is proposed for *LLC* resonant converters to normalize the voltage gain and enhance the light-load efficiency. First, the root cause of nonmonotonic voltage gain is analyzed and revealed as the energy accumulated in resonant inductor due to mismatched output capacitor discharge between primary and secondary side switches within dead-time. To suppress the energy accumulation, an adaptive SR on-time control within dead-time is developed to synchronize the output capacitor discharge processes of primary and secondary side switches, which is characterized as: 1) SR is turned ON within dead-time to accelerate its output capacitor discharge; 2) the turn-ON rate of SR is controlled by designing its gate resistor to match the output capacitor discharge rate of primary side switches; 3) the turn-ON instant of SR is adaptively tuned according to the switching frequency. With the proposed SR control, the energy accumulation of resonant inductor during output capacitor discharge of switches is fully suppressed, resulting in a monotonic voltage gain at light-load, which facilitates voltage regulation and improves light-load efficiency. A 360–440-V input, 50-V/1-kW output *LLC* prototype is built to verify the effectiveness of proposed SR control.**

***Index Terms*—Dead-time, *LLC*, light-load, nonmonotonicity, synchronous rectifier (SR), voltage regulation.**

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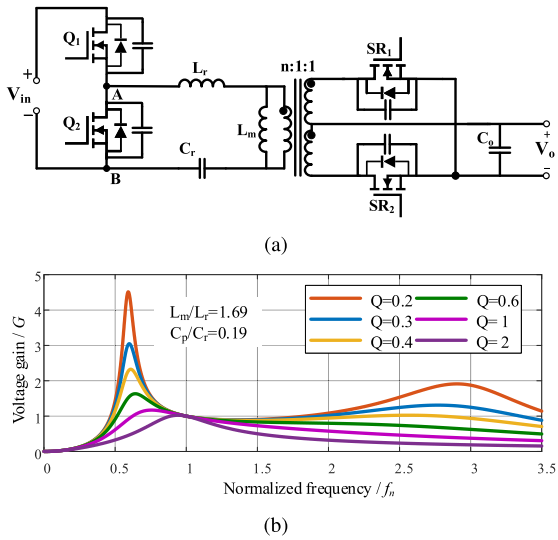

Fig. 1. *LLC* resonant converter: (a) Typical topology. (b) Voltage gain curves.

I. Introduction

LLC resonant converter shown in Fig. 1(a) has excellent soft-switching performance to realize zero-voltage switching (ZVS) of primary-side switches and zero-current switching (ZCS) of secondary-side rectifiers [1]. Consequently, it becomes one of the most popular topologies for high-efficiency and high-power-density applications, such as on board charger, data center, and aerospace [2], [3], [4].

Traditionally, *LLC* resonant converter adopts pulse frequency modulation (PFM) strategy to regulate output voltage because its voltage gain decreases monotonically with increasing switching frequency at heavy load [5]. However, the monotonicity of voltage gain weakens as load decreases. In particular, the voltage gain is nonmonotonic at light-load, as shown in Fig. 1(b), which could lead to the malfunction of PFM strategy [6]. To this end, the common approach is to optimize converter parameters to normalize voltage gain within a specified load range [7]. Nevertheless, the parameter optimization must be a tradeoff between small magnetizing inductance and wide switching frequency range. Small magnetizing inductance leads to large magnetizing current, which increases turn-OFF loss and conduction loss, while

wide switching frequency range results in high electromagnetic interference (EMI) and an excessive increase in switching frequency at light-load. To sum up, although this approach can achieve voltage regulation at light-load, it leads to difficult EMI design and degraded efficiency.

To improve light-load voltage regulation capability and efficiency, some methods have been proposed in [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22]. From the perspective of operating mechanism, they can be divided into four types, i.e., 1) reducing equivalent input voltage; 2) increasing equivalent load; 3) controlling energy backflow; and 4) optimizing converter topology.

For the first type, the phase-shift modulation (PSM) of primary-side switches is applied to full-bridge resonant converter to reduce equivalent input voltage [8], [9]. In literature [8], PSM strategy is used at light-load to replace PFM strategy to regulate the output voltage. Although light-load voltage regulation is achieved, it has low efficiency because the load-independent losses that account for a large proportion of total loss are ignored. Kim et al. [9] proposed a load-adaptive PSM strategy considering magnetic core loss and driving loss to obtain optimal efficiency at light-load. However, its power loss model is established in the rated condition, resulting in reduced accuracy in other conditions. In addition, the small magnetizing inductance is required in these strategies to ensure ZVS operation, which increases the turn-OFF loss and conduction loss. To this end, a hybrid variable-frequency-duty-cycle modulation strategy is proposed in [10] to achieve voltage regulation with large magnetizing inductance, which operates the precalculated frequency and duty cycle according to load conditions. Nevertheless, its duty cycle of control signal is asymmetrical, resulting in a dc bias that increases conduction loss and difficulty of magnetic design.

For the second type, burst control is widely used in *LLC* resonant converter, which increases equivalent load by reducing converter operating time [11], [12], [13]. But the low burst frequency causes poor dynamic performance [11]. To improve dynamic performance and reduce computational burden of burst control, optimal trajectory control (OTC) and simplified OTC are proposed [12], [13]. Nevertheless, the large low-frequency voltage ripple remains unresolved. A valley switching control based on additional sensed voltage signal is proposed in [14] to solve this problem. Moreover, Shu and Wang [15] improved the light-load performance through circuit reconfiguration. It changes the voltage ratio of primary-side and secondary-side at light-load to increase equivalent load. However, additional components are required, thereby increasing the cost and complexity.

Some methods are proposed based on the idea of controlling energy backflow [16], [17], [18]. [16] extends the on-time of synchronous rectifier (SR) to generate reverse current, which loses the ZCS of SR and increases conduction loss. A phase-shift control method between primary and secondary sides is proposed in [17] to control energy backflow. Its phase-shift angle is fixed, and the output voltage is adjusted by controlling the ratio of phase-shift mode to total cycle. If the phase shift angle is zero, it is the same as burst control. Hence, it also causes low-frequency voltage ripple. To that end, an improved phase-shift control method based on time domain analytical model is proposed [18]. It no longer operates like burst control, thus eliminating low-frequency voltage ripple. However, phase-shift-based methods are only valid for full-bridge converter. Moreover, the increased conduction loss due to energy backflow cannot be avoided, which reduces light-load efficiency.

The first three types mainly realize light-load voltage regulation through control strategies, which are limited by poor dynamic performance, topology limitation, and increased conduction loss at light-load, respectively. Moreover, the voltage gain at light-load is still nonmonotonic.

To that end, the fourth type of methods attempts to change the nonmonotonicity of voltage gain by optimizing converter topology. Yeon et al. [19] and Jing et al. [20] utilized Bode plot and conclude that a double pole at high-frequency causes the nonmonotonicity of voltage gain at light-load. Accordingly, auxiliary capacitor and resistor are added, respectively, in parallel with resonant inductor to eliminate the double pole. Kim [21] analyzed the abnormal rise of output voltage at no-load, and proposes a method of paralleling auxiliary capacitor with primary-side switch to realize no-load voltage regulation. Kim et al. [22] proposed a parameter optimization method from the perspective of converter design. Since the parasitic parameter of components is uncontrollable, it is unavoidable to add auxiliary capacitor in topology. However, adding additional component to topology increases the output capacitor discharge time of primary-side switches, which reduces the effective on-time and therefore increases conduction loss. In short, although the nonmonotonicity of voltage gain is changed, the efficiency is reduced due to the increased conduction loss, especially at heavy-load.

To normalize the voltage gain at light-load while preserving the excellent heavy-load performance, an adaptive SR on-time control within dead-time is proposed for *LLC* resonant converters to synchronize output capacitor discharge processes of primary and secondary side switches and therefore normalize the voltage gain and enhance the light-load efficiency. The contribution of this article can be listed as follows.

1) The root cause of nonmonotonic voltage gain at light-load is analyzed from the perspective of energy transmission. It is revealed that the energy accumulated in resonant inductor during the mismatched output capacitor discharge processes of primary and secondary side switches, which is transmitted to output and increases with switching frequency, leads to the nonmonotonic voltage gain at light-load.
2) An adaptive SR on-time control within dead-time is developed to synchronize the output capacitor discharge processes of primary and secondary side switches and therefore suppress the energy accumulation of resonant inductor. Different from the foresaid fourth type of methods, the proposed SR control reduces output capacitor discharge time of SRs instead of increasing output capacitor discharge time of primary side switches. With this effect, the effective on-time of switches is preserved, so as not to increase the conduction loss.
3) The proposed SR on-time control is characterized as: 1) It synchronizes the output capacitor discharge processes

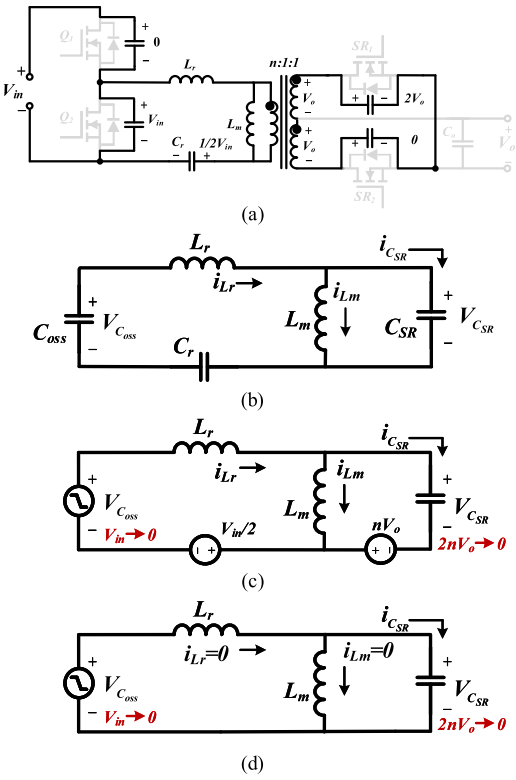

Fig. 2. Operating mode during output capacitor discharge of switches: (a) Initial condition. (b) Equivalent circuit of initial condition. (c) Equivalent circuit with independent voltage sources. (d) Simplified equivalent circuit.

by accelerating and controlling the SR output capacitor discharge rate, which normalizes the light-load voltage gain and therefore reduces excessive switching frequency and improves light-load efficiency. 2) It only introduces additional SR turn-ON loss at light load, thus guaranteeing the heavy-load efficiency of converter. 3) No additional components are required, thus not increasing the original volume and cost of converter. 4) It is not limited by topology and has wide ZVS operating range and low output voltage ripple.

II. Analysis of Non-Monotonicity of Light-Load Voltage Gain

The abnormal rise of output voltage at no-load was investigated in [21]. It is caused by the peaking current of resonant inductor during output capacitor discharge of switches. However, as the key to voltage regulation problem, the nonmonotonic light-load voltage gain is still not well-explained. To essentially solve voltage regulation problem, the nonmonotonicity of light-load voltage gain is analyzed.

First, the operating mode of *LLC* resonant converter during output capacitor discharge of switches is illustrated in detail. The initial condition of output capacitor discharge of switches and its equivalent circuit are shown in Fig. 2(a) and (b). C_{oss} and C_{SR} are, respectively, the equivalent output capacitor of primary-side switches and the equivalent output capacitor of SRs reflected on the primary-side. By assuming that resonant capacitor C_r is

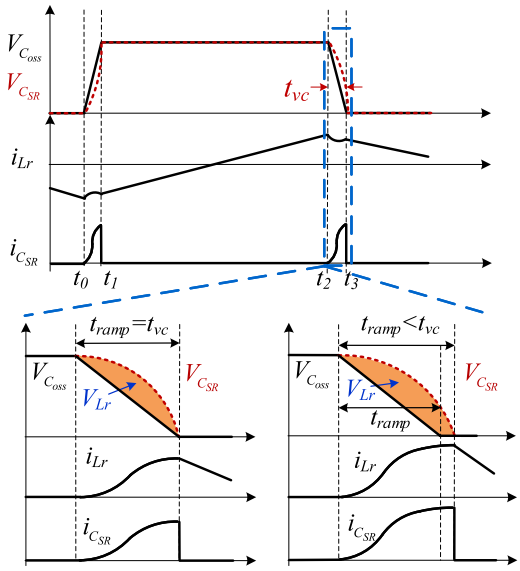

Fig. 3. Key waveforms during output capacitor discharge of switches.

much larger than C_{oss} and C_{SR}, the voltage across C_r can be regarded as a constant voltage source of $V_{\text{in}}/2$ during the output capacitor discharge of switches. Also, since the variation of magnetizing current during output capacitor discharge is much smaller than its peak value $i_{\text{Lm\_pk}}$, the magnetizing current i_{Lm} is considered constant during this period, which is equal to $i_{\text{Lm\_pk}}$. In addition, i_{Lm} mainly flows to the primary-side switches, so C_{oss} can be regarded as a ramp voltage source. It decreases from V_{in} to zero during output capacitor discharge. As a result, the equivalent circuit can be expressed as Fig. 2(c) with independent voltage sources. Further, when C_r is infinite, output voltage V_o can be expressed as follows:

$$V_o = \frac{V_{\text{in}} L_m}{2n(L_m + L_r)}. \tag{1}$$

On this basis, when magnetizing inductor L_m is much larger than resonant inductor L_r, output voltage V_o can be approximated as $V_{\text{in}}/2n$. To that end, the voltage sources $V_{\text{in}}/2$ and nV_o in Fig. 2(c) can be canceled out to obtain a simplified equivalent circuit, as shown in Fig. 2(d). Affected by the ramp voltage source, the voltage across C_{SR} gradually decreases from the initial value of $2nV_o$ to zero. Its voltage change rate is determined by the resonant circuit composed of L_r, L_m, and C_{SR}, as shown in Fig. 2(d).

Fig. 3 shows the zoomed-in waveforms during output capacitor discharge of switches, where $V_{C_{\text{oss}}}$, $V_{C_{\text{SR}}}$, and $i_{C_{\text{SR}}}$ correspond to Fig. 2(d). Both t_0 to t_1 and t_2 to t_3 represent output capacitor discharge period of switches. In this period, $V_{C_{\text{oss}}}$, namely the equivalent ramp voltage source in Fig. 2(d), decreases from V_{in} to zero. The output capacitor discharge rate of primary-side switches is determined by magnetizing current, which can be considered as its peak value $i_{\text{Lm\_pk}}$ during the output capacitor discharge process. Consequently, the output capacitor discharge

process of primary-side switches can be expressed as follows:

$$V_{C_{\text{oss}}}(t) = V_{\text{in}} - \frac{i_{\text{Lm\_pk}}}{C_{\text{oss}}} t. \tag{2}$$

Accordingly, the output capacitor discharge time of primary-side switches t_{ramp} satisfying $V_{C_{\text{oss}}}(t_{\text{ramp}}) = 0$ can be expressed as follows:

$$t_{\text{ramp}} = \frac{V_{\text{in}} C_{\text{oss}}}{i_{\text{Lm\_pk}}} \tag{3}$$

where $i_{\text{Lm\_pk}} = V_{\text{in}}/8 f_s (L_m + L_r)$. Different from $V_{C_{\text{oss}}}$, the change rate of $V_{C_{\text{SR}}}$ during output capacitor discharge of switches is determined by the resonance of the equivalent circuit in Fig. 2(d). Usually, the equivalent frequency of output capacitor discharge of primary-side switches f_{ramp} is larger than the resonant frequency determined by L_r, L_m, and C_{SR} [21]. Therefore, the output capacitor discharge time of SR is no less than t_{ramp}.

$V_{C_{\text{SR}}}$ and $i_{C_{\text{SR}}}$ can be derived from (2) and the equivalent circuit of Fig. 2(d) as follows:

$$V_{C_{\text{SR}}}(t) = V_{\text{in}} - \frac{L_m i_{\text{Lm\_pk}}}{(L_m + L_r) C_{\text{oss}}} \left[t - \frac{1}{w} \sin(wt) \right] \tag{4}$$

$$i_{C_{\text{SR}}}(t) = \frac{L_m i_{\text{Lm\_pk}} C_{\text{SR}}}{(L_m + L_r) C_{\text{oss}}} [\cos(wt) - 1] \tag{5}$$

where $w = 1/\sqrt{(L_m // L_r) C_{\text{SR}}}$. When $V_{C_{\text{SR}}} = 0$, the SR is conducted. At this time, $i_{C_{\text{SR}}}$, namely peaking current of L_r in [21], flows to the output regardless of the load condition. Based on this analysis, the abnormal rise of output voltage at no-load can be explained. However, the peaking current cannot directly characterize the effect on the voltage gain and the relationship between the effect and the switching frequency. Therefore, this is not enough to illustrate the nonmonotonicity of light-load voltage gain, which is the essence of light-load voltage regulation problem. To this end, the nonmonotonicity of light-load voltage gain is analyzed.

The difference in output capacitor discharge rate of primary and secondary side switches leads to an increase in flux linkage of resonant inductor during output capacitor discharge, as shown in Fig. 3. The flux linkage of resonant inductor ψ_{Lr} during output capacitor discharge can be expressed as follows:

$$\psi_{Lr} = \int_0^{t_{\text{vc}}} V_{Lr} dt. \tag{6}$$

The increment of ψ_{Lr} during output capacitor discharge leads to the energy accumulated in resonant inductor, which is transmitted to output after the output capacitor discharge. The energy accumulated in resonant inductor E_{Lr} during output capacitor discharge can be expressed as follows:

$$E_{Lr} = {\psi_{Lr}}^2 / 2 L_r. \tag{7}$$

The aforementioned energy transmitted to the output weakens the monotonicity of the voltage gain originally regulated by the impedance network, especially at light-load. Therefore, the nonmonotonicity of light-load voltage gain is analyzed from the perspective of energy transmission.

TABLE I
KEY PARAMETERS OF LLC PROTOTYPE CONVERTER

Parameter	Values
Input voltage	360−440 V
Output voltage	50 V
Nominal power	1 kW
Resonant inductor	36 uH
Magnetizing inductor	216 uH
Resonant capacitor	27.43 nF
Resonant frequency	160 kHz
Switching frequency range	135−205 kHz
Transformer turns ratio	8:1:1
Dead-time	320 ns
Primary-side switch	STW11NM80
Synchronous rectifier	RX3R10BBH

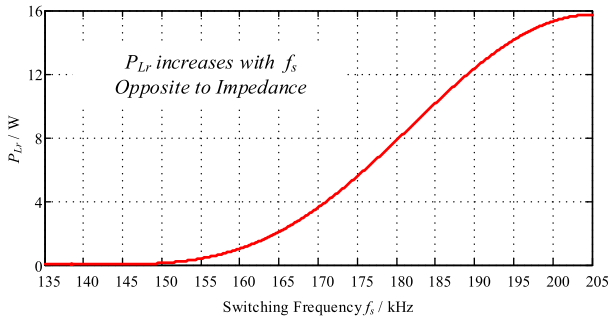

Fig. 4. Curve of P_{Lr} versus switching frequency f_s.

As shown in the zoomed-in waveforms in Fig. 3, the total output capacitor discharge process includes two cases of $t_{\text{vc}} = t_{\text{ramp}}$ and $t_{\text{vc}} > t_{\text{ramp}}$, where t_{vc} is the total time of output capacitor discharge. They differ only in that ψ_{Lr} continues to increase after $V_{C_{\text{oss}}} = 0$ when $t_{\text{vc}} > t_{\text{ramp}}$. As a result, their tendencies of energy accumulated in L_r with switching frequency are similar. To avoid complexity, the following analysis is performed in the case of $t_{\text{vc}} = t_{\text{ramp}}$.

Substituting (2) and (4) into (6), ψ_{Lr} during output capacitor discharge of switches can be further expressed as follows:

$$\begin{aligned} \psi_{Lr} &= \int_0^{t_{\text{vc}}} [V_{C_{\text{SR}}}(t) - V_{C_{\text{oss}}}(t)] dt \\ &= \int_0^{t_{\text{ramp}}} \left[\frac{L_r i_{\text{Lm\_pk}}}{(L_m + L_r) C_{\text{oss}}} t + \frac{L_m i_{\text{Lm\_pk}}}{(L_m + L_r) C_{\text{oss}} w} \sin(wt) \right] dt \end{aligned} \tag{8}$$

when $L_m >> L_r$, it can be simplified as follows:

$$\psi_{Lr} \approx \frac{V_{\text{in}}}{8 w^2 C_{\text{oss}} f_s (L_m + L_r)} [1 - \cos(w t_{\text{ramp}})]. \tag{9}$$

Substituting (9) into (7), E_{Lr} can be obtained. It is noted that E_{Lr} is load-independent. The power caused by E_{Lr} can be expressed as follows:

$$P_{Lr} = 2 f_s E_{Lr} \tag{10}$$

Using the above formulas, the curve of P_{Lr} versus switching frequency f_s based on the parameters in Table I can be plotted, as shown in Fig. 4. It can be seen that P_{Lr} increases with f_s.

It is noted that the output capacitance of switches is not a fixed value, and it changes nonlinearly as the drain-source voltage changes. In order to obtain a fixed equivalent output capacitance as accurately as possible for analysis and driver circuit design, the C_{oss} and $C_{\text{SR\_oss}}$ can be derived based on the nonlinear curves of output capacitance in the datasheets of switching components. In this example, STW11NM80 and RX3R10BBH are selected as the primary side switches and SRs, respectively. The equivalent value of C_{oss} and $C_{\text{SR\_oss}}$ can be obtained as follows:

$$C_{\text{oss}} = \frac{1}{400}\int_0^{400} C_{\text{oss\_STW11NM80}}(V_{ds})dV_{ds} \tag{11}$$

$$C_{\text{SR\_oss}} = \frac{1}{100}\int_0^{100} C_{\text{SR\_oss\_RX3R10BBH}}(V_{ds})dV_{ds} \tag{12}$$

where $C_{\text{oss\_STW11NM80}}(V_{ds})$ represents the output capacitance of STW11NM80, and $C_{\text{SR\_oss\_RX3R10BBH}}(V_{ds})$ represents RX3R10BBH according to the drain-source voltage.

To intuitively demonstrate the impact of P_{Lr} on voltage gain, the output voltage equation of the *LLC* resonant converter is derived. First, the output voltage equation without considering the effect of output capacitor of switches is derived. It can be assumed that the resonant current is equal to the magnetizing current when the primary-side switches are turned OFF in above resonance, because the difference between the resonant current and the magnetizing current is small at light load. On this basis, the time domain equations of *LLC* resonant converter in above resonance can be expressed as follows:

$$V_{Cr}(t) = V_{\text{in}} - L_r\frac{di_{Lr}}{dt} - nV_o \tag{13}$$

$$i_{Lr}(t) = C_r\frac{dV_{Cr}(t)}{dt} \tag{14}$$

$$nV_o = L_m\frac{di_{Lm}(t)}{dt}. \tag{15}$$

If the initial conditions at $t = 0$ are defined to be $V_{Cr}(0) = V_{Cr0}$, $i_{Lr}(0) = I_{Lr0}$ and $i_{Lm}(0) = I_{Lm0}$, (13)–(15) can be solved and shown in (16)–(18).

$$V_{Cr}(t) = V_{\text{in}} - I_{Lr0}\sqrt{\frac{L_r}{C_r}}\sin\left(\frac{1}{\sqrt{L_rC_r}}t\right) - nV_o - (V_{Cr0} + V_{\text{in}} - nV_o)\cos\left(\frac{1}{\sqrt{L_rC_r}}t\right) \tag{16}$$

$$i_{Lr}(t) = (V_{Cr0} + V_{\text{in}} - nV_o)\sqrt{\frac{C_r}{L_r}}\sin\left(\frac{1}{\sqrt{L_rC_r}}t\right) - I_{Lr0}\cos\left(\frac{1}{\sqrt{L_rC_r}}t\right) \tag{17}$$

$$i_{Lm}(t) = \frac{nV_ot}{L_m} + I_{Lm0}. \tag{18}$$

With the boundary conditions for i_{Lm}, V_{Cr} and i_{Lr}, V_o can be solved and shown in (19), where $A = 1/(4f_s\sqrt{L_rC_r})$, and $K = L_m/L_r$.

$$V_o = \frac{V_{\text{in}}\sin(A)}{2n(\frac{A}{K}\cos(A) + \sin(A))}. \tag{19}$$

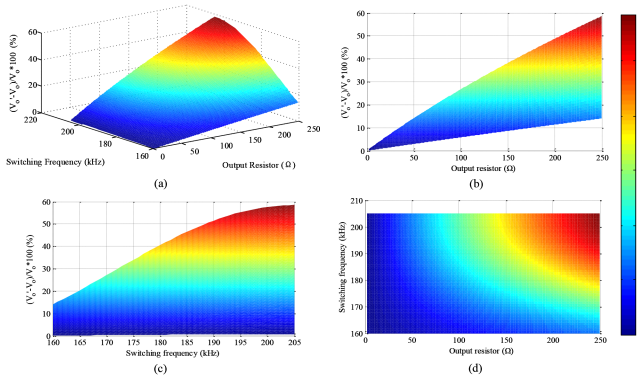

Fig. 5. Relationship among P_{Lr} impact on output voltage, switching frequency, output load resistor: (a) 3-D figure. (b) Top view. (c) Main view. (d) Left view.

To evaluate the impact of the energy accumulated by the resonant inductor during the output capacitor discharge on output voltage, P_{Lr} is injected into (19) to obtain the output voltage expression shown in (20), where R is the output resistor.

$$V_o{}' = \sqrt{\left(\frac{V_{in}\sin(A)}{2n(\frac{A}{K}\cos(A) + \sin(A))}\right)^2 + P_{Lr}R}. \tag{20}$$

Based on the above equations, the relationship among P_{Lr} impact on output voltage, switching frequency, and output load resistor is demonstrated in Fig. 5.

Fig. 5(a) shows the effect of P_{Lr} on the output voltage of *LLC* resonant converter. The different proportions are represented by the heatmap with different colors. Fig. 5(b)–(d) is the top view, main view and right view of (a), respectively. According to Fig. 5(b), as the load decreases, the effect of P_{Lr} on the output voltage gradually increases, where the redder the color, the more the P_{Lr} affects the output voltage. Fig. 5(c) shows that the effect of P_{Lr} on the output voltage increases with the switching frequency, which is stronger than the effect of PFM-based voltage regulation mechanism at light load, resulting in nonmonotonic voltage gain. The influence of P_{Lr} on output voltage is related to switching frequency and load condition, as shown in Fig. 5(d).

To summarize, the nonmonotonicity of light-load voltage gain can be illustrated as: PFM-based voltage regulation mechanism of *LLC* resonant converter is on the basis of impedance regulation of resonant circuit by changing switching frequency. Since the converter always operates in inductive region, the impedance of resonant components increases with switching frequency, so the output voltage decreases monotonously with the increase of switching frequency. However, the P_{Lr} transmitted to output may increase with switching frequency in case of mismatched output capacitor of primary and secondary side switches, resulting in an increase in output voltage. It has the opposite effect of PFM-based voltage regulation mechanism, thus weakening the monotonicity of voltage gain. Especially at light-load, it causes the nonmonotonic voltage gain due to high proportion of P_{Lr} to output power.

It can be concluded that the energy accumulated in resonant inductor during the output capacitor discharge of switches may increase with switching frequency in case of mismatched output capacitor discharge processes of primary and secondary side switches, which is contrary to traditional PFM-based voltage regulation mechanism, thus weakening the monotonicity of voltage gain. At light-load, it makes the voltage gain nonmonotonic, thereby causing the malfunction of PFM strategy and degraded efficiency due to excessive increase in switching frequency. It is noted that this energy accumulation is caused by the increase of flux linkage of resonant inductor due to the mismatched output capacitor discharge between primary and secondary sides. Therefore, it can be suppressed by synchronizing the output capacitor discharge processes of primary and secondary sides.

III. Proposed Adaptive SR On-Time Control Within Dead-Time

A. Concept of Proposed SR On-Time Control

To normalize the light-load voltage gain, an SR on-time control within dead-time is proposed to suppress the energy accumulation of resonant inductor. Its idea is to accelerate the output capacitor discharge of secondary side switches by actively turning ON SR during output capacitor discharge, so as to match the output capacitor discharge process of primary side switches and therefore suppress the energy accumulation of resonant inductor. Since the output capacitor discharge of switches begins after the turn-OFF instant of primary side switch and ends within dead-time, SR should be turned ON within dead-time to match the discharge process of primary side.

Fig. 6 shows the key waveforms using proposed SR on-time control at light-load. In the proposed control, both the rising and falling edge of gate-source voltage of SRs appear during the dead-time of primary-side control signal, as shown in Fig. 6(a). Due to this effect, the decrease process of the drain-source voltage of SR_1 during dead-time is synchronized with the drain-source voltage of Q_2, thereby reducing the change of the resonant current during dead-time. V_{SR_g} and V_{SR_gs} in Fig. 6(b) represent the output signal of driver and the gate-source signal of SR, respectively. It can be seen that the $V_{C_{SR}}$ decreases at an approximately constant rate by turning ON SR within dead-time, which is similar to the discharge rate of primary side. At this time, the gate-source voltage of SR is equal to Miller voltage V_{Miller}. Thus, the output capacitor discharge of SR is accelerated by actively turning ON SR, no longer relying on the resonance of equivalent circuit in Fig. 2(d). Therefore, $V_{C_{SR}}$ can be adjusted to approximately synchronize $V_{C_{\text{oss}}}$ during output capacitor discharge of switches, so as to suppress the energy accumulation of resonant inductor and therefore normalize the voltage gain at light-load. Instead of relying on circuit resonance, the output capacitor discharge of SRs in the proposed SR control is realized by controlling SR to actively turn-ON within dead-time, so as to achieve the purpose of matching the output capacitor discharge process of SRs with that of the primary side switches. Although the SR turn-ON rate is changed in the proposed method, it is not to make the SR turn-ON rate as fast as possible as common sense, but to control the SR turn-ON rate so that the SRs can match the output capacitor discharge process of the primary side switches. It is worth mentioning that the proposed SR on-time control is compatible with the conventional synchronous rectification control since it mainly operates during the dead-time. To achieve the proposed SR control and synchronous rectification control simultaneously, it is only necessary to add an interlocking mechanism of SR control signals to avoid the shoot-through of SRs.

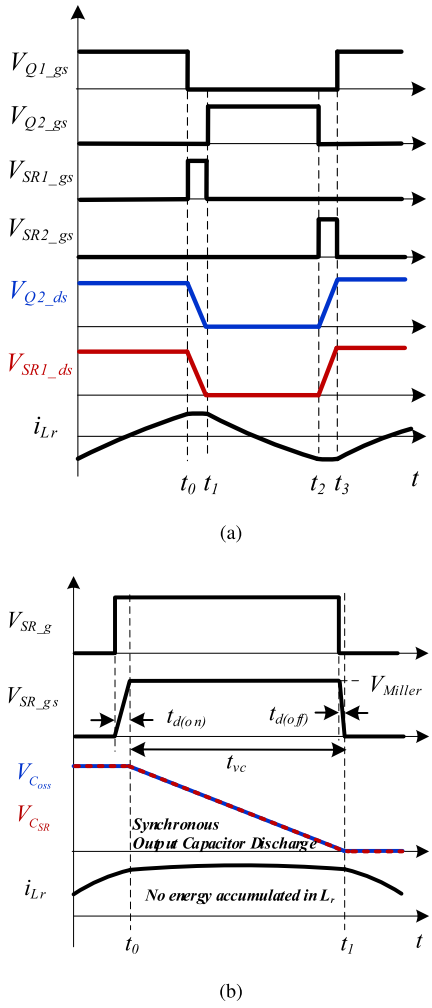

Fig. 6. Key waveforms using the proposed SR on-time control: (a) Macroscopic switching period. (b) Zoomed output capacitor discharge period.

The proposed SR control can reduce the resonant current variation during output capacitor discharge of switches, which is similar to the effect of auxiliary circuit methods proposed in [19], [20], [21], [22]. Compared with these methods, the proposed SR control has some significant advantages. First, no additional auxiliary component is required, thus not increasing the original volume and cost of converter. Second, the output capacitor discharge rate of SR is increased instead of reducing the discharge rate of primary side switches, which avoids the decrease in effective on-time of switches. As a result, the proposed SR control does not cause an increase in conduction loss, so that it can improve the light-load performance without reducing the heavy-load performance. It is worth noting that the light

load voltage gain can theoretically be normalized by selecting MOSFET device to match its output capacitance. However, in the converter design process, the switching device selection has many limitations. Compared with the output capacitance, the V_{ds_max}, I_{d_max}, R_{ds_on} and price should be given priority in the selection. As a result, it is difficult to select the MOSFET device that can meet all the above design requirements in practical applications.

Two issues should be addressed to implement the proposed SR control, which are as follows:

1) *Discharge Rate Matching:* The output capacitor discharge rate of SR should match the primary side so that the output capacitor discharge processes of primary and secondary sides could be synchronized.

2) *SR Control Signal Generation:* Since the output capacitor discharge time of primary side switches varies with switching frequency, fixed on-time of SR cannot accurately synchronize the output capacitor discharge process. An adaptive SR on-time control according to the switching frequency is required.

Next, the abovementioned issues will be handled in detail.

B. SR Gate Resistor Design Guideline

To make it possible to synchronize output capacitor discharge processes of primary and secondary side switches, the output capacitor discharge rate of SR should be controlled to match the discharge rate of primary side. It is noted that SRs are usually able to achieve ZVS operation with very little turn-ON loss at heavy-load. Therefore, the change of SR turn-ON rate does not increase the turn-ON loss at heavy-load, so it does not affect the heavy-load efficiency.

The turn-ON rate of SR is not only related to its component characteristics, but also determined by the driver and gate resistor. From the perspective of converter design, the selection of driver and component needs to take into account system performance requirement and cost. In contrast, the gate resistor only affects the switching characteristics of SR. Consequently, the matching of output capacitor discharge rate in proposed SR on-time control is realized by the SR gate resistor design. It is noted that the turn-ON rate of SR determines its output capacitor discharge rate, so the main design consideration is for the on-resistor. The off-resistor of gate resistor should be as small as possible to achieve fast turn-OFF.

Fig. 7(a) shows the turn-ON transition process of SR, which can be divided into three stages.

Stage 1 $[t_0 - t_1]$ is the turn-ON delay time. At t_0, the control signal of SR is changed from low to high. The gate-source capacitor C_{gs} begins to be charged and the gate-source voltage V_{gs} starts to rise. This stage ends until V_{gs} rises to V_{th} at t_1. During this stage, SR is in OFF-state and no current flows.

Stage 2 $[t_1 - t_2]$ is the current rise stage. In this stage, V_{gs} continues to rise. And the current starts to flow through SR, which can be expressed as follows:

$$i_d(t) = g_{fs}[V_{gs}(t) - V_{\text{th}}] \tag{21}$$

where g_{fs} is the forward transconductance of SR, and V_{th} is the threshold voltage of SR. Due to the presence of parasitic

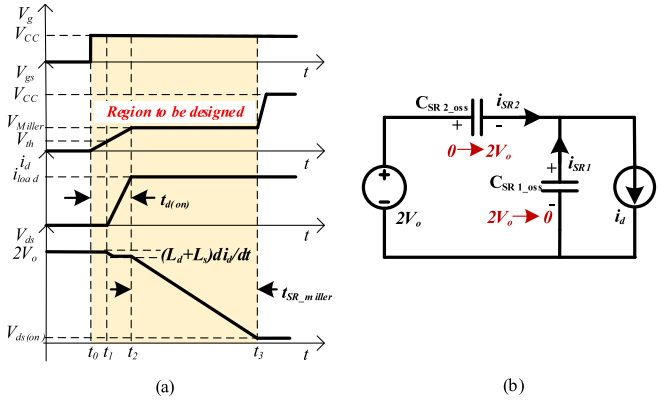

Fig. 7. (a) Typical turn-ON transition process of SRs. (b) Secondary-side equivalent circuit during voltage falling stage.

inductance L_d and L_s, the drain-source voltage V_{ds} drops by $(L_d + L_s)di_d/dt$. This stage ends when i_d is equal to load current i_{load}. At this time, V_{gs} reaches the Miller voltage V_{Miller}, which can be derived from (11) as foolows:

$$V_{\text{Miller}} = \frac{i_{\text{load}}}{g_{fs}} + V_{\text{th}}. \tag{22}$$

Stage 3 $[t_2 - t_3]$ is the voltage falling stage, which is the most important stage for the gate resistor design. During this stage, V_{gs} stops rising and the driving current i_g flows to the Miller capacitance C_{gd}, causing V_{ds} to drop rapidly. The change rate of V_{ds} in this stage can be expressed as follows:

$$\left|\frac{dV_{ds}}{dt}\right| = \frac{i_g}{C_{gd}} \tag{23}$$

where $i_g = (V_{CC} - V_{\text{Miller}})/R_g$. When V_{ds} drops to conduction voltage V_{ds_on}, the voltage falling stage ends.

Consequently, for the selected driver and SR, the turn-ON rate of SR is jointly determined by V_{Miller} and ON-resistor of SR R_g. To obtain the relationship between V_{Miller} and R_g, the secondary-side equivalent circuit during voltage falling stage is derived. As shown in Fig. 7(b), SR_1 can be equivalent to capacitor C_{SR1} connected in parallel with current source i_d, which is controlled to turn ON. And SR_2 can be equivalent to capacitor C_{SR2}. The two capacitors represent their output capacitance $C_{\text{SR\_oss}}$, and the current flowing through i_d is equal to i_{load}. During this period, the voltage across SR_1 decreases from $2V_o$ to zero, while the voltage across SR_2 rises from zero to $2V_o$. Based on Kirchhoff's law, the absolute values of their drain-source voltage change rates are equal. Accordingly, the following equation can be obtained:

$$i_{\text{load}} = 2C_{\text{SR\_oss}}\left|\frac{dV_{ds}}{dt}\right|. \tag{24}$$

Combining (22), (23), and (24), the relationship between R_g and $|dV_{ds}/dt|$ can be expressed as follows:

$$\left|\frac{dV_{ds}}{dt}\right| = \frac{(V_{CC} - V_{tah})g_{fs}}{2C_{\text{SR\_oss}} + g_{fs}C_{gd}R_g}. \tag{25}$$

Except for R_g, other parameters in the right hand of (25) are available in the datasheet.

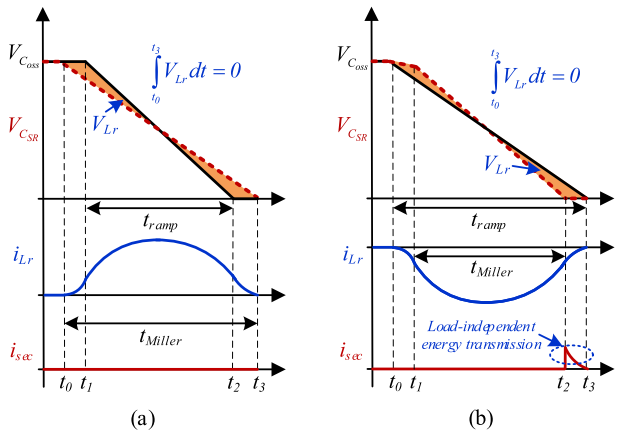

Fig. 8. Typical waveforms during output capacitor discharge using R_g designed based on different t_{ramp}: (a) $t_{\text{ramp\_max}}$. (b) $t_{\text{ramp\_min}}$.

In the turn-ON process of SRs, the change of V_{ds} in stage 1 and stage 2 is much less than that in stage 3. To simplify the parameter design, consider the duration of stage 3 t_{Miller} as the time for V_{ds} to decrease from $2V_o$ to zero. R_g could be designed to satisfy $|dV_{ds}/dt| = 2V_o/t_{\text{ramp}}$.

Since the output capacitor discharge time of primary side switches t_{ramp} varies with switching frequency, the selection of t_{ramp} needs to be considered. Different selections of t_{ramp} lead to the following conditions during output capacitor discharge of switches.

Fig. 8(a) shows the typical waveforms during output capacitor discharge using R_g designed based on the maximum output capacitor discharge time of primary side switches $t_{\text{ramp\_max}}$. In this case, the discharge rate of secondary side is less than that of primary side in most operating conditions. Accordingly, the energy suppression of resonant inductor could be realized by turning ON SR before output capacitor discharge of primary side starts and making its drain-source voltage decrease to zero after the discharge of primary side ends.

When R_g is designed based on the minimum discharge time of primary side switches $t_{\text{ramp\_min}}$, the discharge rate of secondary side is larger than that of primary side. Although energy suppression of resonant inductor during output capacitor discharge can also be achieved by delaying the turn-ON instant of SR, the drain-source voltage of SR will decrease to zero before the discharge of primary side ends, that is, the SR conducts. Thus, there is load-independent energy transmitted to output, as shown in Fig. 8(b), which weakens the monotonicity of voltage gain. As a result, $t_{\text{ramp\_max}}$ should be selected to design R_g.

C. Adaptive SR On-Time Control Within Dead-Time

Since t_{ramp} varies with switching frequency, the turn-ON and turn-OFF instants of SRs should be adaptively tuned according to switching frequency to match the primary side.

According to the proposed SR gate resistor design guideline, the turn-ON rate of SR is controlled so that the output capacitor discharge time of secondary side switches is equal to $t_{\text{ramp\_max}}$, as shown in Fig. 8(a). Therefore, the discharge rate of secondary side is slower than that of primary side in most working conditions. To suppress energy accumulation of resonant inductor during output capacitor discharge, the start moment of discharge of secondary side should be ahead of that of primary side. And its leading time t_{lead} could be expressed as follows:

$$t_{\text{lead}} = \frac{t_{\text{ramp\_max}} - t_{\text{ramp}}}{2}. \tag{26}$$

Considering the turn-OFF delay time of primary side switch $t_{p\_d(\text{off})}$ and the turn-ON delay time of SR $t_{SR\_d(\text{on})}$, the turn-ON instant of SR_1 can be described as follows:

$$t_{\text{SR1\_on}} = t_{\text{Q1\_on}} + \frac{1}{2f_s} - t_{dt} + t_{Q1\_d(\text{off})} - t_{\text{SR1\_d(on)}} - t_{\text{lead}} \tag{27}$$

where $t_{\text{SR1\_on}}$ is the turn-ON instant of SR_1, $t_{\text{Q1\_on}}$ is the turn-ON instant of Q_1, and t_{dt} is the dead-time. SR_1 and Q_1 correspond to Fig. 1(a). Similarly, the turn-ON instant of SR_2 can be obtained.

At the end of output capacitor discharge of SR, the turn-OFF instant of SR is short because its drain current is small and the Miller voltage is close to threshold voltage. As a result, the on-time of SR Δt_{SR} can be simplified as follows:

$$\Delta t_{\text{SR}} = t_{\text{SR\_d(on)}} + t_{\text{ramp\_max}}. \tag{28}$$

And the turn-OFF instant of SR $t_{\text{SR\_off}}$ can be obtained by $t_{\text{SR\_off}} = t_{\text{SR\_on}} + \Delta t_{\text{SR}}$.

In addition, the boundary condition for using the proposed SR control should be determined. To guarantee efficient voltage regulation, the boundary load condition of proposed SR on-time control should correspond to the load condition of the critical monotonic voltage gain of *LLC* resonant converter. However, the traditional voltage gain model of *LLC* resonant converter is derived based on fundamental harmonic approximation (FHA) method, which has low accuracy when the switching frequency is far from resonant frequency or at light-load. On the other hand, the accurate time-domain model of *LLC* resonant converter is too complex and difficult to solve. Moreover, the key parameters required for modeling and obtained in practical applications are not accurate. To sum up, it is difficult to directly obtain accurate critical load condition of proposed SR on-time control through mathematical model.

Another feasible idea of boundary load condition selection is to use the critical load condition that can satisfy the minimum voltage gain required by converter as the boundary load condition, so that the output voltage regulation can also be achieved in the widest possible load range by using the proposed SR on-time control. It should be noted that, in addition to the load condition being less than the critical load condition, the operating conditions of the proposed SR on-time control also include that the switching frequency is not less than resonant frequency. This is because the effect of the proposed SR on-time control is to make the voltage gain of *LLC* resonant converter monotonic at light-load, while the light-load voltage gain in below resonance is inherently monotonic. To intuitively show the foresaid boundary condition of proposed SR on-time control, the flowchart of overall control method of *LLC* resonant converter using the proposed SR on-time control is shown in Fig. 9.

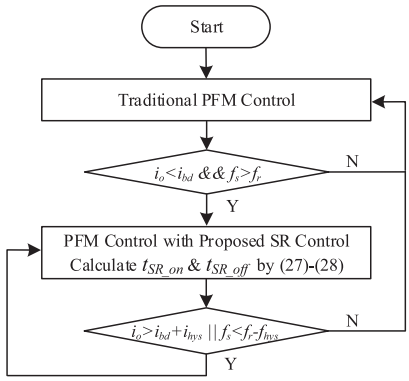

Fig. 9. Flowchart of overall control method using proposed SR control.

In the beginning, the traditional PFM control is used to regulate voltage. When the load is large enough, the traditional impedance-based voltage regulation mechanism dominates, and the output voltage decreases as switching frequency increases. As the proportion of accumulated energy of resonant inductor to load increases, the output voltage becomes difficult to regulate by adjusting switching frequency because this energy instead increases with switching frequency. When the load current i_o is less than the boundary load condition current i_{bd} and the switching frequency f_s is greater than the resonant frequency f_r, the proposed SR control starts to work with PFM control. It suppresses the energy accumulation by synchronizing the output capacitor discharge processes of primary side switches and SRs. When i_o is larger than i_{bd} or f_s is less than f_r, the proposed SR control stops to work and PFM control is only used to regulate output voltage. Moreover, a hysteresis current i_{hys} and hysteresis frequency f_{hys} can be added to the boundary condition judgment to ensure the continuity of voltage gain.

D. Sensitivity Analysis

For the proposed SR control, the monotonic light-load voltage gain is achieved by suppressing the energy accumulation of the resonant inductor during the output capacitor discharge of the primary and secondary side switches. Under ideal conditions, the energy accumulation of the resonant inductor can be fully suppressed. However, the tolerances of circuit components and the parasitic parameters as well as temperature variations may affect the accuracy of the proposed SR control in practical applications, thereby weakening the effect of energy suppression. To further evaluate the impact of the above issues on the accuracy of the proposed method, the sensitivity analysis is carried out.

Since the tolerance of the resonant inductor is unavoidable and relatively large, the sensitivity of the proposed SR control to the tolerance of resonant inductor L_r is analyzed. First, define the actual value of the resonant inductor $L_r{}'$. Therefore, the actual value of the output capacitor discharge time of primary side switches $t_{\text{ramp}}{}'$ can be expressed as follows:

$$t_{\text{ramp}}{}' = 8 f_s C_{\text{oss}} (L_m + L_r{}'). \tag{29}$$

The tolerance of resonant inductor changes the output capacitor discharge process of the primary switch, which in turn leads to changes in the energy accumulation of the resonant inductor during the output capacitor discharge of primary and secondary side switches. Affected by this reason, the power caused by this energy $P_{Lr}{}'$ is expressed as follows:

$$P_{Lr}{}' = \frac{{V_{\text{in}}}^2 [1 - \cos(w t_{\text{ramp}}{}')]^2}{64 f_s L_r{}' w^4 {C_{\text{oss}}}^2 (L_m + L_r{}')^2}. \tag{30}$$

On the other hand, since the output capacitor discharge process of the primary side switches is changed, using the proposed SR control is no longer able to match the output capacitor discharge process of the primary and secondary side switches. As a result, the energy accumulation of the resonant inductor is not fully suppressed. The power caused by the energy accumulation of resonant inductor during output capacitor discharge using the proposed SR control can be expressed as follows:

$$P_{\text{Lr\_error}}{}' = \frac{f_s {V_{\text{in}}}^2 (t_{\text{ramp}}{}' - t_{ramp})^2}{4 L_r{}'}. \tag{31}$$

The $P_{\text{Lr\_error}}{}'/P_{\text{Lr}}{}'$ can be conveniently used to express the effect of the proposed SR control on energy accumulation suppression of resonant inductor to evaluate the impact of the resonant inductor tolerance.

Similarly, the sensitivity of the proposed method to the tolerance of SR output capacitor is analyzed. Define the actual value of the SR output capacitor $C_{\text{SR\_oss}}{}''$ and $C_{\text{SR}}{}'' = 2C_{\text{SR\_oss}}{}''/n^2$. Hence, the actual value of the angular frequency of the resonant circuit in Fig. 2(d) w'' can be expressed as follows:

$$w'' = n/\sqrt{2(L_m // L_r) C_{\text{SR\_oss}}{}''}. \tag{32}$$

Affected by the tolerance of SR output capacitor, the power caused by the energy accumulation of resonant inductor $P_{\text{Lr}}{}''$ can be expressed as follows:

$$P_{\text{Lr}}{}'' = \frac{{V_{\text{in}}}^2 [1 - \cos(w'' t_{\text{ramp}})]^2}{64 f_s L_r w''^4 {C_{\text{oss}}}^2 (L_m + L_r)^2}. \tag{33}$$

For the proposed SR control, the SR output capacitor tolerance not only affects the angular frequency of the resonant circuit, but also changes the predesigned SR output capacitor discharge rate, resulting in a mismatch in the output capacitor discharge processes of primary and secondary side switches. Affected by the SR output capacitor tolerance, the drain-source voltage change rate of SR can be expressed as follows:

$$\left| \frac{dV_{ds}}{dt} \right|'' = \frac{(V_{\text{CC}} - V_{\text{th}})\, g_{fs}}{2C_{\text{SR\_oss}}{}'' + g_{fs} C_{gd} R_g}. \tag{34}$$

Based on (34), the actual value of the output capacitor discharge time of secondary side switches is expressed as follows:

$$t_{\text{ramp\_max}}{}'' = \frac{V_o (2C_{\text{SR\_oss}}{}'' + g_{fs} C_{gd} R_g)}{g_{fs} (V_{\text{CC}} - V_{\text{th}})}. \tag{35}$$

According to (7), (9), (10), and (35), the power caused by the energy accumulation of resonant inductor during output capacitor discharge using the proposed SR control considering

the SR output capacitor tolerance can be expressed as follows:

$$P_{\mathrm{Lr\_error}}'' = \frac{f_s {V_{\mathrm{in}}}^2 (t_{\mathrm{ramp\_max}} - t_{\mathrm{ramp\_max}}'')^2}{4L_r} \tag{36}$$

The $P_{\mathrm{Lr\_error}}''/P_{\mathrm{Lr}}''$ can be used to describe the effect of the proposed SR control on energy accumulation suppression of resonant inductor to evaluate the sensitivity of the SR output capacitor tolerance.

In addition, the sensitivity to the tolerance of the output capacitor of primary side switches is analyzed. Define the actual value of the output capacitor of primary side switches $C_{\mathrm{P\_oss}}'''$ and $C_{\mathrm{oss}}''' = 2C_{\mathrm{P\_oss}}'''$. Therefore, the actual value of the output capacitor discharge time of primary side switches t_{ramp}''' can be expressed as follows:

$$t_{\mathrm{ramp}}''' = 8 f_s C_{\mathrm{oss}}'''(L_m + L_r). \tag{37}$$

Affected by the tolerance of output capacitor of primary side switches, the power caused by the energy accumulation of resonant inductor P_{Lr} can be expressed as follows:

$$P_{\mathrm{Lr}}''' = \frac{{V_{\mathrm{in}}}^2 [1 - \cos(w t_{\mathrm{ramp}}''')]^2}{64 f_s L_r w^4 {C_{\mathrm{oss}}''}^2 (L_m + L_r)^2}. \tag{38}$$

Similarly, the power caused by the energy accumulation of resonant inductor during output capacitor discharge using the proposed SR control considering the output capacitor tolerance of primary side switches can be expressed as follows:

$$P_{\mathrm{Lr\_error}}''' = \frac{f_s {V_{\mathrm{in}}}^2 (t_{\mathrm{ramp\_max}} - t_{\mathrm{ramp\_max}}''')^2}{4L_r}. \tag{39}$$

And the $P_{\mathrm{Lr\_error}}'''/P_{\mathrm{Lr}}'''$ is used to express the effect of output capacitor tolerance on the proposed SR on-time control.

According to the above analysis, the error of the proposed SR on-time control is mainly caused by the error of the output capacitor discharge time of the primary side switches and the SR output capacitor discharge time. SR output capacitor discharge time is determined by SR characteristics and gate resistor, independent of resonant capacitor. And the output capacitor discharge time of the primary side switches satisfies (1) and (3) under light load conditions where the proposed SR control is applied, so it is not affected by the resonant capacitor tolerance. In summary, the proposed SR on-time control has low sensitivity to resonant capacitor tolerance.

On the other hand, the relationship between component tolerance and SR on-time error can reflect the influence of component tolerance on the proposed SR on-time control. Define the ratio of SR on-time error caused by component tolerance to SR on-time as e. To this end, e_{Lr} represents the error caused by resonant inductor tolerance, $e_{\mathrm{SR\_oss}}$ represents the error caused by SR output capacitor tolerance, and $e_{\mathrm{P\_oss}}$ represents the error caused by output capacitor of primary side switches tolerance, which can be expressed as follows:

$$e_{\mathrm{Lr}} = \frac{L_r' - L_r}{L_r' + L_m} \tag{40}$$

$$e_{\mathrm{SR\_oss}} = \frac{2(C_{\mathrm{SR\_oss}}'' - C_{\mathrm{SR\_oss}})}{2C_{\mathrm{SR\_oss}}'' + g_{fs} C_{gd} R_g} \tag{41}$$

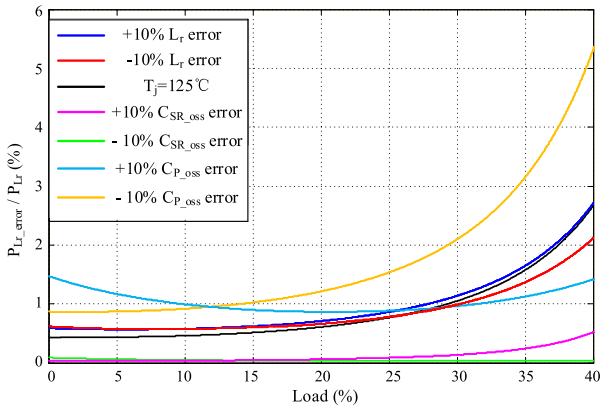

Fig. 10. Sensitivity analysis of different parameters for proposed SR control.

$$e_{\mathrm{P\_oss}} = \frac{C_{\mathrm{P\_oss}}''' - C_{\mathrm{P\_oss}}}{C_{\mathrm{P\_oss}}'''}. \tag{42}$$

Based on the above formulas, the proposed SR on-time control is less sensitive to the resonant inductor tolerance than the output capacitor tolerance of the switches. Combined with $P_{\mathrm{Lr\_error}}/P_{\mathrm{Lr}}$ analysis and the SR on-time error analysis, the negative impact of the tolerances of L_r, $C_{\mathrm{SR\_oss}}$ and $C_{\mathrm{P\_oss}}$ on the proposed SR on-time control is acceptable and does not affect the overall performance of the *LLC* resonant converter.

Furthermore, the circuit parameters may change when temperature increases, so the sensitivity of proposed SR control to temperature is analyzed. It is noted that a low temperature coefficient resistor can be used for the turn-ON gate resistor of SR to avoid parameter changes caused by temperature. In addition, since the air gap reluctance of the inductor is much greater than the core reluctance, it is less affected by temperature. Therefore, the changes in parasitic parameters of switches caused by temperature are mainly analyzed.

For switching components, the forward transfer admittance and the gate threshold voltage are temperature-sensitive parameters, which generally decrease with increasing temperature. For the proposed method, the forward transfer admittance and the gate threshold voltage of SR affect its output capacitor discharge rate. On this basis, the temperature sensitivity of the proposed SR control is analyzed using the foresaid analysis method. Based on the parameters shown in Table I, the sensitivity analysis results of the proposed method on different parameters at the maximum input voltage and rated output voltage are shown in Fig. 10.

It can be seen that when the temperature is 125 °C, the error of the proposed SR control gradually increases as the load increases. However, even under 40% load conditions, the error of the proposed method is still less than 3%. Therefore, the proposed method has low sensitivity to temperature. When $C_{\mathrm{P\_oss}}$ has a deviation of 10%, the maximum error of the proposed method is less than 6%. Furthermore, when L_r and $C_{\mathrm{SR\_oss}}$ have a deviation of 10%, the maximum error of the proposed method is less than 3%. Especially for $C_{\mathrm{SR\_oss}}$, the maximum error is less than 1%. Therefore, the negative impact of the tolerances of

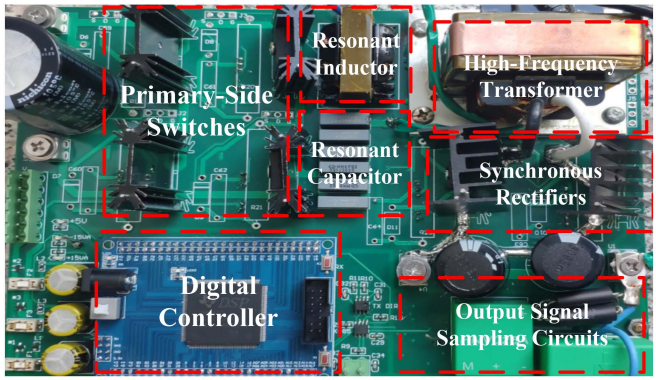

Fig. 11. Full-bridge LLC prototype converter.

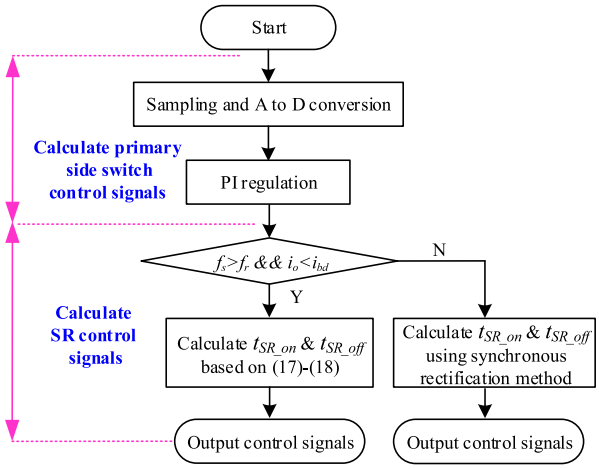

Fig. 12. Flowchart of the closed-loop control system in the LLC prototype.

$C_{\mathrm{P\_oss}}$, L_r and $C_{\mathrm{SR\_oss}}$ on the proposed SR control is acceptable and does not affect the overall performance. Furthermore, it is worth noting that the $C_{\mathrm{SR\_oss}}$ with a deviation of -10% generally have smaller errors than the $C_{\mathrm{SR\_oss}}$ with a deviation of +10%. As a result, it is appropriate to use slightly larger parameters of $C_{\mathrm{SR\_oss}}$ than those in the datasheet of components for driver circuit design. On the contrary, C_{P_oss} with a deviation of -10% generally have greater errors than the parameter with a deviation of +10%. Hence, the output capacitance of primary side switches is recommended to be a smaller value than the theoretical value.

IV. Experimental Verification

To verify the proposed SR control, a full-bridge *LLC* prototype converter is built, as shown in Fig. 11. The key parameters of the prototype are shown in Table I, which are designed using classical design method based on FHA. The digital signal processor (DSP) TMS320F28335 is used to generate SR control signal. The maximum clock frequency is set to 150 MHz. As a result, the minimum adjustment time of control signal is 6.67 ns. According to the parameters shown in Table I, the on-time of SR control signal Δt_{SR} is 300 ns, and the range of turn-ON instant of SR $t_{\mathrm{SR\_on}}$ can be calculated based on (27). The flowchart of the closed-loop control system in *LLC* prototype is shown in Fig. 12. The SR control signals are calculated based on the

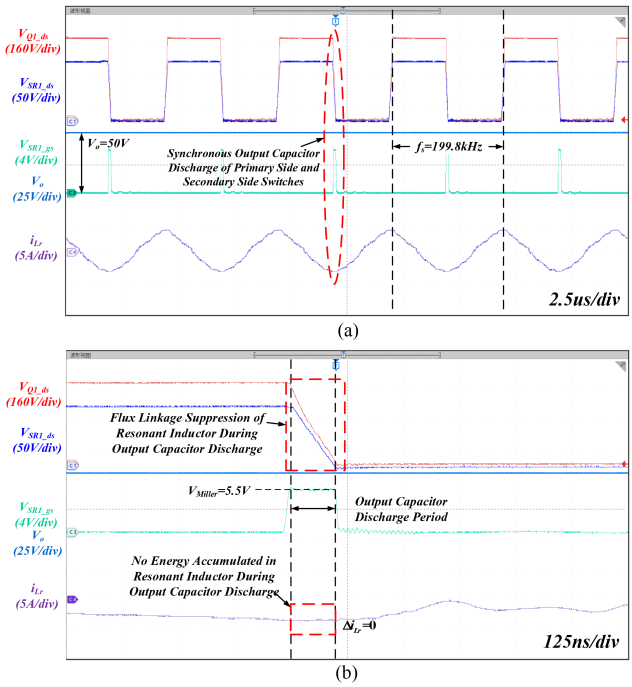

Fig. 13. Waveforms under 1% load condition with $V_{\mathrm{in}} = 440\,V$: (a) Macroscopic switching period. (b) Zoomed output capacitor discharge period.

of SR is designed to be 12 Ω based on the design guideline. In order to highlight the impact of the proposed SR on-time control on light-load performance and improve the readability of the experimental waveforms, this article captured all experimental waveforms of the proposed SR on-time control with the conventional synchronous rectification control disabled. To determine the boundary load condition of proposed SR control, we have tested the *LLC* prototype under different load conditions at maximum input voltage. The switching frequency is close to the system upper limit under 40% load condition, so the 40% load condition is selected as the boundary load condition.

First, the light-load performance of the prototype with different input voltages was tested. Fig. 13 shows the waveforms using proposed SR control under 1% load condition with $V_{\mathrm{in}} = 440$ V. It can be seen that the output voltage is well regulated to 50 V, which is the rated output voltage. And the switching frequency is 199.8 kHz. Hence, *LLC* resonant converter using the proposed SR control can effectively achieve voltage regulation even under harsh working condition, i.e., maximum input voltage and very light load condition. Further, the switching frequency does not reach the designed maximum switching frequency, which means that the prototype has the potential to operate at a lighter load. Based on the zoomed waveforms in Fig. 13(b), the drain-source voltage of primary side switch has a decreasing tendency similar to that of ramp voltage source, which confirms the theoretical analysis. The drain-source voltage of SR decreases rapidly when its gate-source voltage is equal to the Miller voltage. By using the proposed SR control, the voltage decreasing process of primary-side switch is synchronized with SR, thereby suppressing the energy accumulation of resonant inductor during

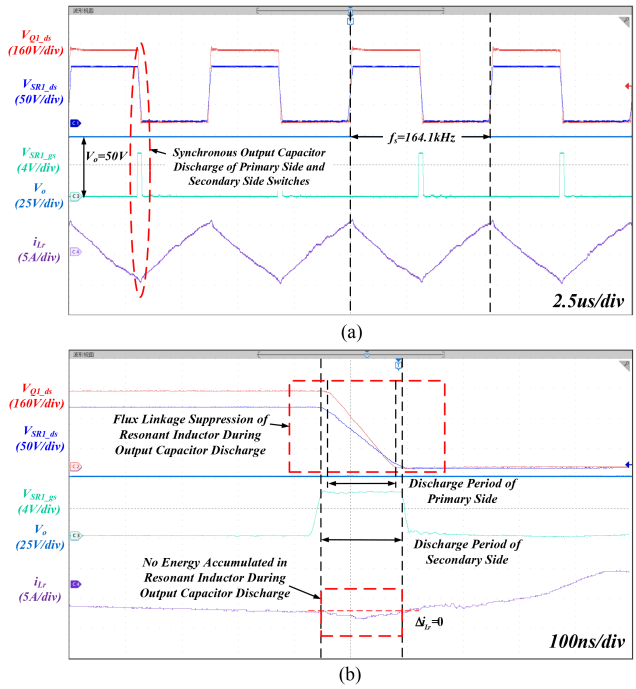

Fig. 14. Waveforms under 1% load condition with $V_{\text{in}} = 400\,V$: (a) Macroscopic switching period. (b) Zoomed output capacitor discharge period.

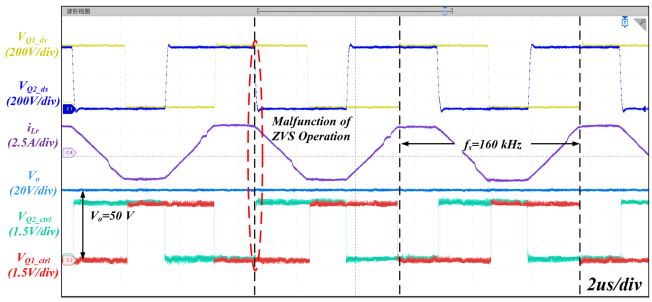

Fig. 15. Waveforms under 1% load condition with $V_{\text{in}} = 440\,V$ using PSM control.

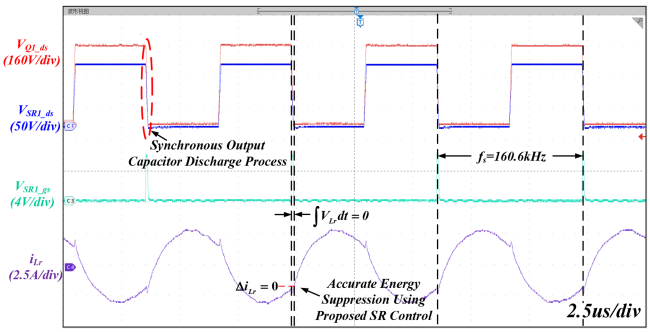

Fig. 16. Waveforms under 20% load condition with $V_{\text{in}} = 400\,V$.

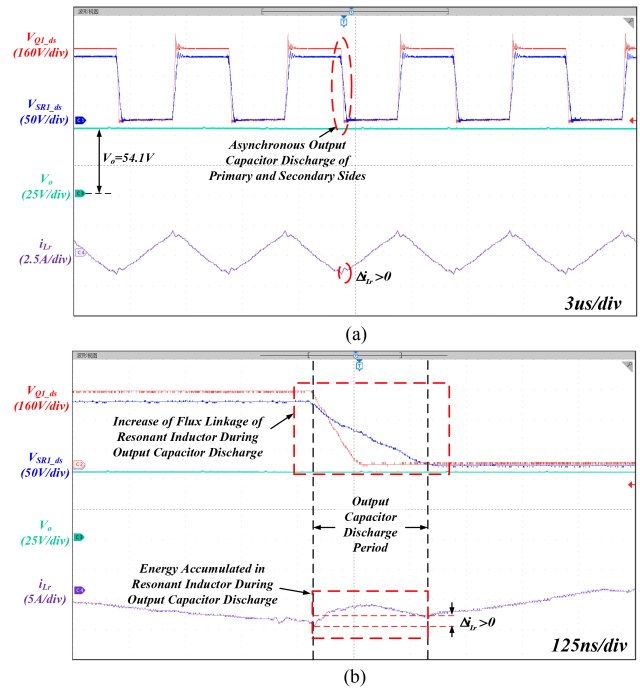

Fig. 17. Waveforms without using proposed SR control under 1% load condition with $V_{\text{in}} = 400$ V and $f_s = 164.1$ kHz: (a) Macroscopic switching period. (b) Zoomed output capacitor discharge period.

Fig. 14 shows the key waveforms under 1% load condition with $V_{\text{in}} = 400$ V. Likewise, the output voltage is regulated to its rated voltage and the switching frequency is 164.1 kHz. It is noted that the output capacitor discharge process of secondary side takes longer time than that of primary side under this switching frequency, which is in well accordance with the SR gate resistor design guideline. To suppress the energy accumulation of resonant inductor, the start moment of output capacitor discharge of secondary side is controlled to be ahead of primary side, while its ending moment lags behind that of primary side. With this effect, the resonant current is approximately constant before and after output capacitor discharge, thus eliminating the load-independent energy to be transmitted to output.

The key waveform of *LLC* resonant converter using the PSM control under 1% load condition is shown in Fig. 15. During PSM control, the *LLC* prototype operates at the resonant frequency. Different from the PFM control, the resonant current waveform with PSM control is similar to the trapezoid wave at light load. This is because when the upper or lower switches of the two bridge arms in *LLC* resonant converter are simultaneously conducted, the voltage of resonant inductor and magnetizing inductor is close to zero, so the resonant current change rate is close to zero during this period. It can also be seen from this figure that the output voltage is regulated to the rated voltage. However, the large phase shift angle causes the malfunction of the ZVS operation of primary side switches, which leads to the additional turn-ON loss. Furthermore, the PSM control can only be used in full-bridge topology, thus limiting its application scope.

Then the performance of prototype operating under other light load conditions was tested to further verify the effectiveness of proposed SR control. Fig. 16 represents the key waveforms of prototype under 20% load condition with $V_{\text{in}} = 400$ V. As shown here, the output voltage is well regulated and the switching frequency is 160.6 kHz. Thus, the proposed SR control is effective over a wide load range.

To intuitively evaluate the effect of proposed SR control, Fig. 17 shows the waveforms without using proposed SR control.

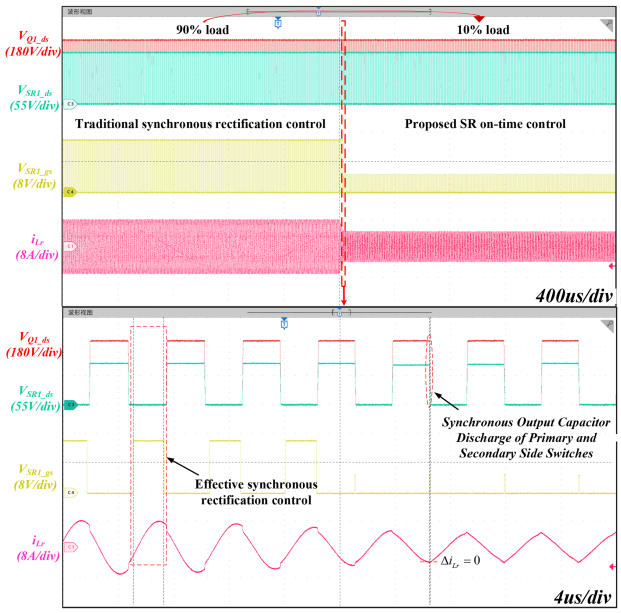

Fig. 18. Waveforms during load change: 90% load to 10% load.

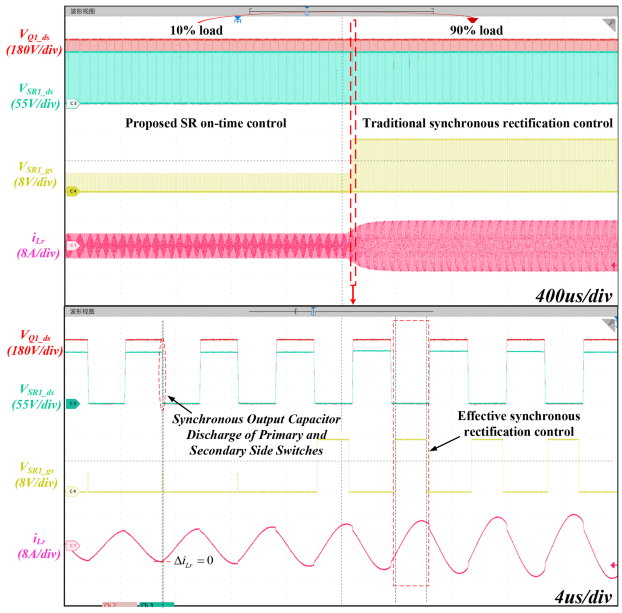

Fig. 19. Waveforms during load change: 10% load to 90% load.

In order to make a fair comparison, its test condition is the same as Fig. 14. It can be seen that the output capacitor discharge processes of primary and secondary sides are asynchronous. The output voltage is 54.1 V, which is higher than that using proposed SR control. For the zoomed waveforms shown in Fig. 17(b), the relationship between the flux linkage of resonant inductor and the energy accumulation of resonant inductor during output capacitor discharge can be clearly observed, which further verifies the analysis. The energy accumulated in resonant inductor causes the nonmontonic voltage gain. By comparing Figs. 14 and 17, it can be concluded that the proposed SR control can effectively reduce output voltage under light load conditions.

Fig. 18 shows the transient waveforms from 90% load to 10% load. The SRs are controlled by the traditional synchronous rectification control method at heavy load, thereby reducing the conduction loss caused by the large current. At this time, the resonant current changes during output capacitor discharge of switches due to the asynchronous output capacitor discharge processes between the primary side and secondary side. Affected by this, the energy accumulated in resonant inductor increases. However, this energy accounts for a low proportion of output load and therefore does not affect the monotonicity of the voltage gain. As the load decreases and the switching frequency increases, the proposed SR on-time control works instead of traditional synchronous rectification control. In this case, the energy accumulation of resonant inductor is fully suppressed during output capacitor discharge, thereby normalizing the voltage gain, which facilitates voltage regulation and improves light-load efficiency. Fig. 19 shows the transient waveforms from 10% load to 90% load. When the *LLC* resonant converter works at light load, the proposed SR on-time control operates to synchronize the output capacitor discharge process of the primary side and secondary side switches. At heavy load, the proposed SR on-time control stops functioning and SRs are controlled by the traditional synchronous rectification method.

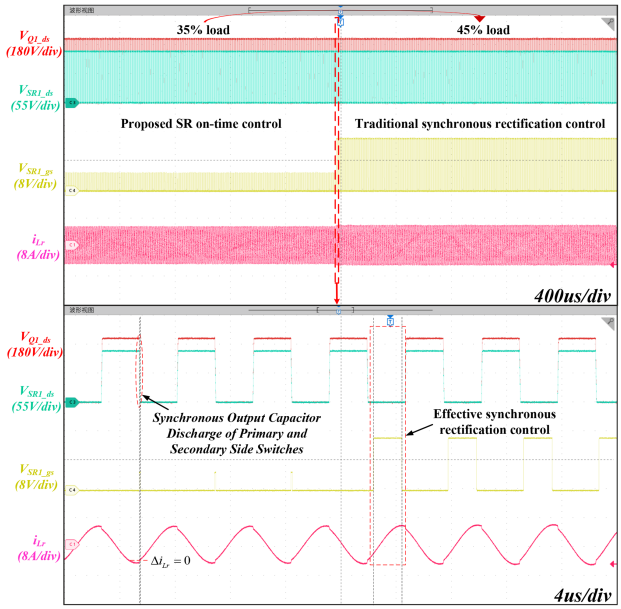

Fig. 20. Waveforms during load change: 35% load to 45% load.

In these dynamic changes, the operation of the proposed SR on-time control tracks load changes, which verifies that the proposed SR on-time control is effective in the transient.

Figs. 20 and 21 show the transient waveforms near the switching point. It can be seen that the traditional synchronous rectification control and the proposed SR on-time control switch smoothly with the load change. This is because near the switching point, the output capacitance of the switches has a low effect on the voltage gain due to the low proportion of the energy accumulated by the resonant inductor during output capacitor discharge process to the load. Therefore, the change of SR control method will not cause switching frequency mutation. In addition, the switching oscillation of the SR control methods

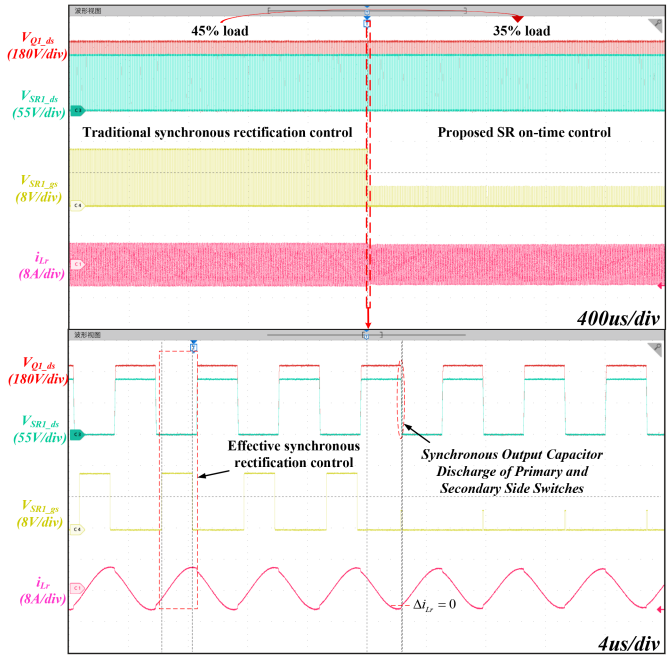

Fig. 21. Waveforms during load change: 45% load to 35% load.

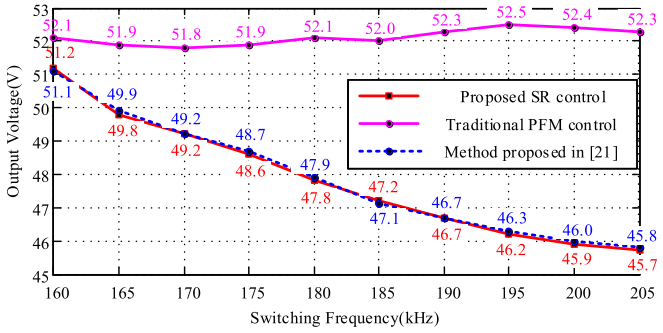

Fig. 22. Comparison of light-load voltage regulation capability.

near the switching point and the gain curve discontinuity caused by switching SR control methods can be avoided by setting a reasonable hysteresis load and switching frequency region.

To compare the performance of the proposed SR control and existing methods, the traditional PFM control method and the method proposed in [21] are implemented to perform some additional tests on the LLC prototype, respectively. Fig. 22 shows the output voltage versus switching frequency with $V_{\text{in}} = 400\,V$ and 1% load condition. Obviously, the curve of traditional PFM control is higher than those of other methods. The proposed SR control and the method proposed in [21] have similar curves. From the perspective of monotonicity, the traditional PFM control curve is nonmonotonic, which means that it cannot effectively regulate voltage at very light load, while others decrease monotonously with the increase of switching frequency. Consequently, the proposed method can effectively regulate output voltage under light load conditions.

To further demonstrate the effectiveness of the proposed SR control, Fig. 23 shows the output voltage versus load regulation

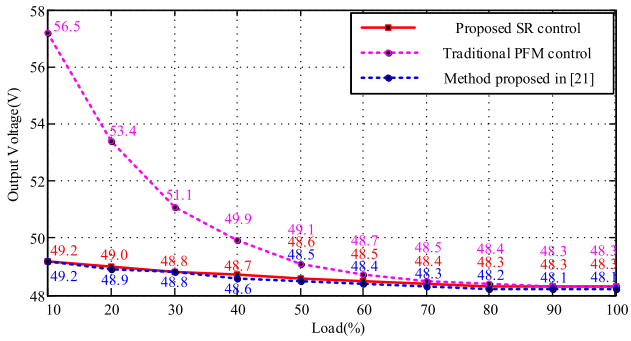

Fig. 23. Comparison of output voltage versus load regulation curves.

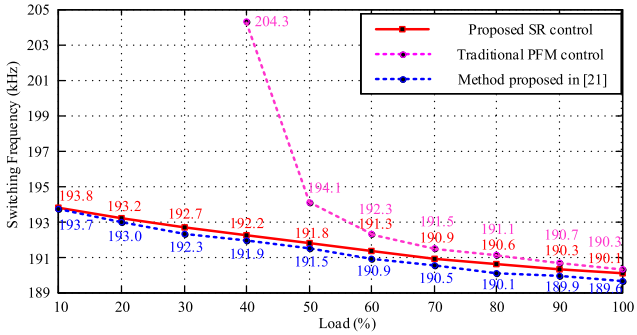

Fig. 24. Comparison of switching frequency versus load regulation curves.

curves measured through different methods under open-loop condition at maximum input voltage and switching frequency. In this test, the proposed SR control works without the limitation of boundary load condition. It can be seen that when using the traditional PFM control, the output voltage increases significantly as load decreases. When using the proposed SR control, the output voltage changes less as load decreases. This shows that the proposed SR control can effectively suppress the impact of load reduction on output voltage, thereby improving the light-load voltage regulation capability of *LLC* resonant converter.

Fig. 24 shows the switching frequency versus load regulation curves under open-loop condition at maximum input voltage and rated output voltage. To comprehensively observe the performance of the proposed SR control, the proposed SR control also works without the limitation of boundary load condition. When the load condition is lower than 40%, the switching frequency of the *LLC* prototype using traditional PFM control reaches the system upper limit, and the output voltage cannot be effectively adjusted to the rated value. For the same load conditions, both the proposed SR control and the method proposed in [21] can regulate the output voltage to the rated value and the switching frequency is lower than the system upper limit, which verifies the effectiveness of the proposed SR control. At 40% load and the same output voltage, the switching frequency of the proposed SR control is 12.1 kHz lower than that of the traditional PFM control, thus reducing the power loss at light-load. As the load increases, the switching frequency of the proposed SR control gradually approaches the switching frequency of traditional PFM control. It is noted that the switching frequency of the method proposed

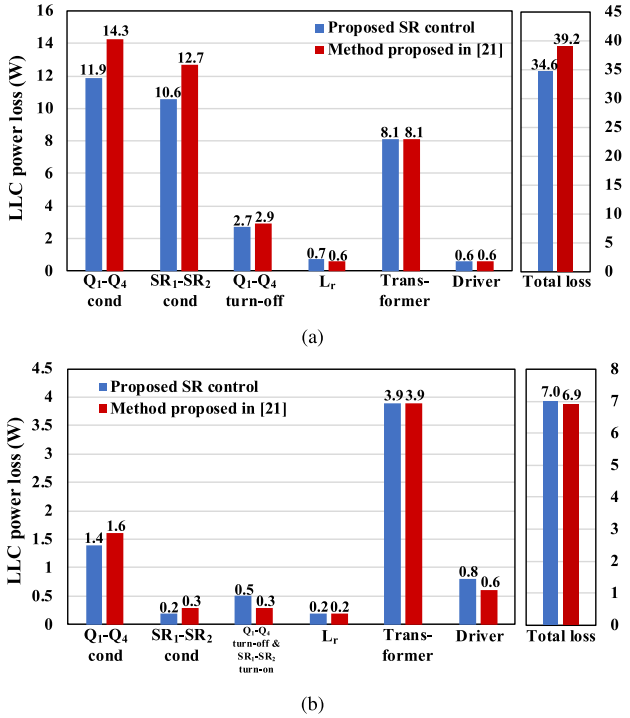

Fig. 25. Main loss breakdown of *LLC* prototype using different methods: (a) At full load. (b) At 10% load.

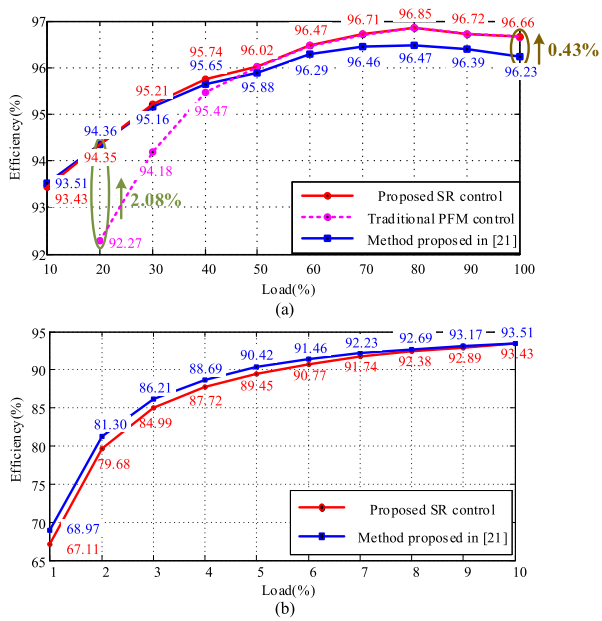

Fig. 26. Comparison of efficiency performance: (a) 10% load to full load. (b) 1% load to 10% load.

in [21] is slightly lower than that of the proposed SR control, especially at heavy-load. This is because the method proposed in [21] reduces the effective conduction time of the switching components, resulting in an increase in their conduction voltage. Affected by this reason, the converter needs to appropriately reduce the switching frequency to compensate for the voltage loss.

The main loss breakdown of the *LLC* prototype at rated input voltage and rated output voltage is shown in Fig. 25 under different load conditions. At full load, the *LLC* prototype using the proposed SR control only operates the traditional PFM control, which is the same as the method proposed in [21]. However, the method proposed in [21] has a larger conduction current even though their output power is the same. This is because the extra parallel capacitor in [21] reduces the effective on-time of the switches. With this effect, the conduction loss of *LLC* prototype using the proposed SR control is lower than that of the method proposed in [21]. Obviously, the conduction loss dominates the total loss at heavy load. Therefore, the proposed SR control has higher efficiency than the method proposed in [21] at full load. Although the conduction loss of the proposed SR control at light load is still lower than that of the method proposed in [21], the SR on-time control increases the turn-ON loss of SRs and the driver loss. Nonetheless, the proposed SR control has similar efficiency to the method proposed in [21] at light load. This is because the losses of the magnetic components dominate the total loss at light load and are almost identical for both methods.

The efficiency curves with rated input voltage and rated output voltage are shown in Fig. 26. Since the traditional method cannot regulate output voltage to 50 V under load conditions below 20%, its efficiency under these load conditions is not compared. The efficiency of traditional method is the lowest under 20%∼30% load conditions because it operates at a high switching frequency to achieve voltage regulation. For the proposed SR control, its efficiency is similar to [21] at light load. This is because these two methods can effectively reduce the excessive switching loss at light load, and the additional loss caused by these methods accounts for a lower proportion of the total loss. At heavy load, the efficiency of the proposed SR control is higher than that in [21], which is improved by 0.43% at full load. This is because the additional conduction loss and turn-OFF loss caused by the method in [21] increase with load and account for a higher proportion of the total loss at heavy load, which reduces the efficiency. In contrast, the proposed method only introduces additional SR turn-ON loss at light load and no additional power loss at heavy load. Therefore, compared with the method in [21], the proposed method has higher heavy-load efficiency while having similar light-load efficiency. Although the efficiency of the proposed method is lower than that of the method in [21] at 1% load, it has less impact on the overall performance of *LLC* resonant converter due to its low power loss value. Compared with traditional PFM control, the proposed SR control improves the efficiency by up to 2.08% at light-load. Compared with the method in [21], the proposed method has similar light-load performance and higher heavy-load efficiency. In addition, the proposed method does not require additional auxiliary components, thus not increasing the cost and volume of the converter. In summary, the proposed method enables voltage regulation over a wide load range with high efficiency. It is suitable for wide load range applications such as data center power supply, PV, and EV auxiliary power module.

Table II provides comparison of light-load performance enhancement methods for *LLC* resonant converter. Because the

TABLE II
COMPARISON OF LIGHT-LOAD PERFORMANCE ENHANCEMENT METHODS FOR LLC RESONANT CONVERTER

Category	Reference	Additional Components	Topology Limitation	ZVS Range	Voltage Ripple	Effective On-time	Voltage Regulation
PSM Control	[8]–[9]	None	**Full-bridge**	**Narrow**	**Medium**	**Medium**	Strong
VFDCM Control	[10]	None	**Full-bridge**	**Medium**	**Medium**	**Medium**	Strong
Burst Control	[11]–[13]	None	None	Wide	**High**	**Medium**	Strong
Circuit Reconfiguration	[15]	**Switch**	**Full-bridge**	Wide	Low	High	**Weak**
Burst PSM Control	[17]	None	**Full-bridge**	Wide	**Medium**	High	Strong
Damping Split Inductor	[19]–[20]	**Capacitor / Resistor**	None	Wide	Low	High	**Medium**
External Capacitor of Switches	[21]–[22]	**Capacitor**	None	**Medium**	Low	**Low**	**Medium**
Proposed SR On-time Control		**None**	**None**	**Wide**	**Low**	**High**	**Medium**

proposed SR control improves the light-load performance by eliminating the output capacitance effect of the primary and secondary side switches, it has relatively weak light-load voltage regulation capability compared with the phase shift control, which directly adjusts the voltage gain. However, the proposed SR control has the advantages of not being limited by topology, wide ZVS range, and low output voltage ripple. Furthermore, effective on-time of switches has an important effect on conduction loss of *LLC* resonant converter, especially at heavy load. Compared with the methods proposed in [21] and [22], the proposed method requires no additional components and preserves effective on-time of switches, thus guaranteeing the heavy load efficiency of *LLC* resonant converter. In summary, the proposed SR control achieves comprehensively excellent performance in terms of light-load performance enhancement of *LLC* resonant converters.

V. CONCLUSION

This article proposes an adaptive SR on-time control within dead-time for *LLC* resonant converters operating at light-load. The energy-based analysis reveals that the root cause of non-monotonic light-load voltage gain of *LLC* resonant converter is the energy accumulated in resonant inductor due to mismatched output capacitor discharge between primary and secondary side switches. Therefore, an adaptive SR on-time control within dead-time is developed to synchronize the output capacitor discharge processes by accelerating and designing the discharging rate of SR under different load conditions and switching frequencies. Experimental results at light load demonstrate that by using the proposed SR on-time control, the energy accumulation of resonant inductor is effectively suppressed during dead-time and the output voltage is well regulated with a normal switching frequency. Meanwhile, the voltage gain of *LLC* resonant converter is monotonic even at 1% load, thus ensuring effective light-load voltage regulation. With the proposed SR control, the efficiency is increased by 2.08% at 20% load compared with traditional PFM control, and increased by 0.43% at full load in comparison to the method in [21]. Hence, the proposed SR control enables voltage regulation over a wide load range with high conversion efficiency, and is suitable for data center power supply, PV, and EV auxiliary power module applications.

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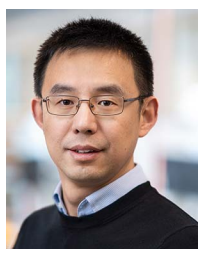

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