A Modular Interline Power Flow Controller for Meshed Multiterminal DC Grids

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***Abstract*—In meshed multiterminal direct current (MTDC) grids, it is not possible to independently regulate all line currents via terminal controllers. To address this issue, the dc power flow controllers (DCPFCs) are introduced. However, most power flow controllers previously proposed have a small current regulation range. This article proposes a modular interline power flow controller (IDCPFC) topology with a wide current adjustment range. It can be easily expanded into a multiport IDCPFC due to its modularity and scalability. The current adjustment range of the proposed IDCPFC can be improved due to the modular structure and optimized control method. Meanwhile, the topology, operation principle, and control strategy of the proposed topology are explained in this article. The comparison with DCPFC topologies previously proposed demonstrates the advantages of a wider adjustment range, lower cost, and higher efficiency. Simulations performed in PSCAD/EMTDC and experiments based on a down-scaled prototype are completed. Simulation and experiment results validate the operation principle, control strategy, and theoretical analysis results.**

***Index Terms*—Adjustment range, dc power flow controllers (DCPFCs), down-scaled prototype, multiterminal direct current (MTDC) grids, PSCAD/EMTDC.**

I. Introduction

In THE past decades, the renewable energy sources have gained increasing attention and growing penetration [1], [2], [3]. Meanwhile, high-voltage dc (HVdc) transmission based on a voltage-source converter (VSC) has made significant progress due to its advantages such as high voltage, large capacity, and long transmission distance [4], [5], [6], [7], [8], [9], [10]. Then, the concept of the meshed multiterminal direct current (MTDC) grid has received extensive consideration from both academia and industry. However, if there are N individual VSCs and M ($M \geq N-1$) lines in a meshed MTDC grid, only $N-1$ different dc line currents can be regulated by the VSC controllers. There may be some line currents that cannot be controlled actively, leading to unnecessary power losses and overloads of transmission lines. To solve this problem, the DCPFC is introduced to regulate the line currents precisely in the dc grids.

Generally, the DCPFC topologies are divided into four types: 1) series variable resistance (SVR); 2) dc transformer (DCT); 3) interline dc power flow controller (IDCPFC); 4) series adjustable voltage source (SAVS).

The SVR-type DCPFCs regulate the line currents by inserting adjustable resistances into the transmission lines [11]. However, they cannot increase the line current value or change the direction of the line current because the inserted resistor can only be increased. The power losses increase due to the external line resistances. Besides, the external equipment is required to avoid the overheating issue.

The DCT-type DCPFCs regulate the line currents by adjusting the voltage at the node of the transmission line [12], [13]. The DCT-type DCPFCs are suitable for situations where the terminal voltages can be at different voltage levels. Nevertheless, the dc transformer is required to withstand the terminal voltages. Therefore, the DCT-type DCPFCs have the disadvantages of high costs, high power losses, and high component stresses, especially when the rated voltages of the terminals are the same.

The SAVS-type DCPFCs adjust the line currents by inserting equivalent variable voltage sources into the transmission lines [14], [15], [16], [17], [18], [19], [20]. Besides the main circuits, which regulate the line current, they usually require auxiliary circuits and external sources to keep the energy balance. The SAVS-type DCPFCs have the advantages of lower costs and power losses compared to the dc transformer. Meanwhile, the costs and losses of these DCPFCs are still high due to the complex structure.

The IDCPFCs regulate the line currents by inserting small variable voltage sources into the lines. Different from the SAVS-type DCPFCs, the IDCPFCs do not require external sources and the inserted voltage sources exchange energy with each other [21], [22], [23], [24], [25], [26], [27], [28], [29]. Therefore, the IDCPFCs require fewer semiconductor switches leading to lower costs and lower power losses.

However, as the transmission distance increases, the resistance of transmission line also increases. It requires a wider range of inserted voltage to achieve the expected current regulation range. Therefore, many traditional IDCPFC topologies are not suitable due to the insufficient adjustment ranges. Therefore, some IDCPFC topologies are composed of modular multilevel

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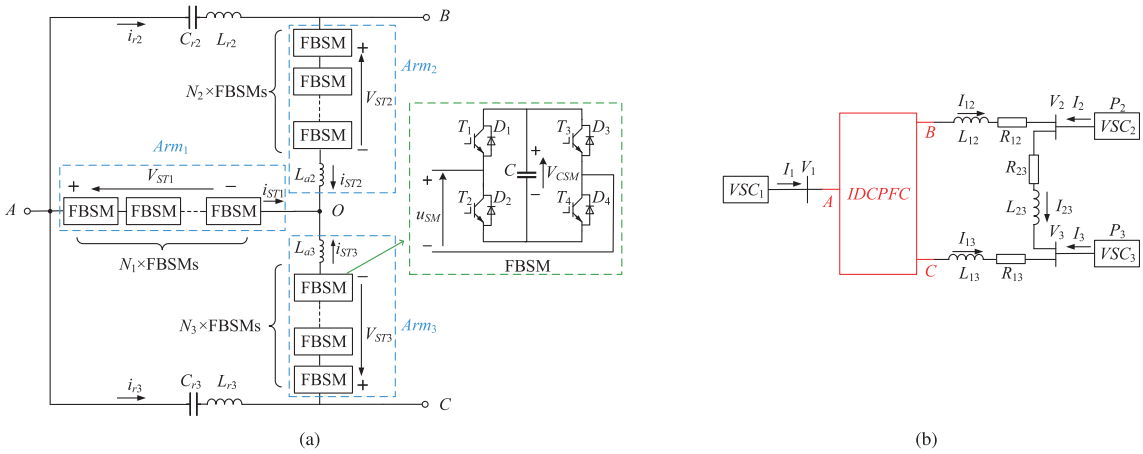


Fig. 1. Topology of the proposed IDCPFC in a three-terminal dc transmission system. (a) Topology of the proposed IDCPFC. (b) Structure of the three-terminal HVdc system with the proposed IDCPFC.

converter (MMC) arms, which consist of series-connected submodules (SMs). They can improve the current adjustment range by increasing the ranges of inserted voltages. They usually realize the power exchange of the inserted voltage sources via an ac transformer or circulating current. According to this, these topologies can be divided into two types. The first type of topology is typically composed of two MMCs that are connected in a front-to-front configuration. The ac transformers are required to realize the power exchange [30]. The second type of topology consists of MMC arms, which are directly connected to each other. The power exchange is realized via the circulating currents instead of the ac transformers [31], [32], [33]. Nevertheless, these topologies proposed previously require lots of semiconductor devices or bulky magnetic elements. It will lead to high costs and high power losses.

This article proposes a bidirectional interline current flow controller based on MMC arms. It adjusts the line currents by inserting equivalent variable voltage sources into the transmission lines. The adjustment range is very wide because the range of inserted voltage can be changed by adjusting the SM number in the arms. The proposed topology can be employed in medium-voltage (MV) or HVdc systems because it does not need to withstand system voltage. It can be flexibly expanded to regulate more line currents by changing the number of resonant tanks and arms according to the number of line currents needed to be controlled. The topology, operation principle, and control strategy of the proposed topology are described in Section II. The theoretical analysis and parameter design of this topology are illustrated in Section III. The comparison results are shown in Section IV. The simulation results and the experiment results are presented in Sections V and VI, respectively. Finally, Section VII concludes this article.

II. Topology, Operation Principle, and Control Strategy

A. Topology

The topology of the proposed IDCPFC and the structure of a three-terminal dc system are shown in Fig. 1. As shown in Fig. 1(a), the proposed IDCPFC is composed of three arms (Arm_1, Arm_2, and Arm_3) and two resonant tanks. Each arm contains one stack (Stack_1, Stack_2, or Stack_3), while only Arm_2 and Arm_3 contain arm inductors (L_{a2} and L_{a3}). The stacks consist of series-connected full-bridge submodules (FBSMs) because they need to generate negative voltage levels. The quantities of FBSMs in the Stack_1, Stack_2, and Stack_3 are N_1, N_2, and N_3, respectively. Each FBSM consists of four IGBTs and one capacitor and the output voltage can be V_{CSM}, 0 or $-V_{\text{CSM}}$. The other arms are connected to both ends of Arm_1 through resonant tank and arm inductors, separately. The resonant tank is composed of a capacitor (C_{r2} or C_{r3}) and an inductor (L_{r2} or L_{r3}). The number of arms and resonant tanks can be flexibly adjusted in accordance with the number of the dc lines requiring power flow regulation.

Fig. 1(b) shows the typical structure of a three-terminal dc system that employs the proposed IDCPFC topology. In this dc grid, there are three terminals, which are represented by VSC_1, VSC_2, and VSC_3, respectively. The terminal voltages are V_1, V_2, and V_3 and the terminal currents are I_1, I_2, and I_3, respectively. The line resistances on the lines (line_{12}, line_{13}, and line_{23}) are R_{12}, R_{13}, and R_{23}. The VSC_1 is controlled as a dc voltage regulator and the rated voltage is V_1. While the VSC_2 and VSC_3 are controlled as power regulators. The rated powers of VSC_2 and VSC_3 are P_2 and P_3, respectively.

B. Operation Principles

To ensure the IDCPFC works functionally, it is necessary to achieve line current regulation and energy balance. The line currents are determined by the terminal voltages and the line resistances. Therefore, the proposed IDCPFC regulates the line currents by inserting variable dc voltage sources into the lines. Since this IDCPFC does not have an external source, the energy balance and voltage stability are realized by changing the power between the inserted voltage sources.

The equivalent circuits of the proposed topology are shown in Fig. 2. Each stack voltage can be represented by an ac voltage

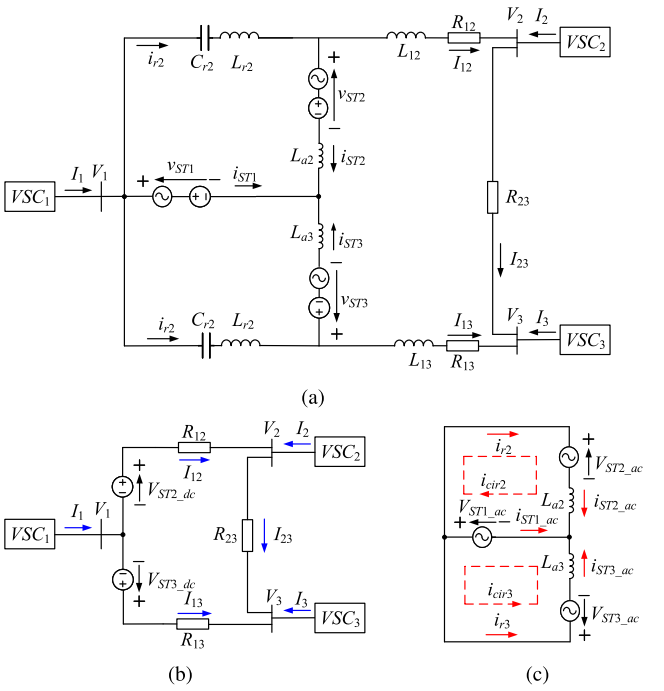


Fig. 2. Equivalent circuits. (a) Equivalent circuit of the proposed topology. (b) Equivalent circuit of the DC components. (c) Equivalent circuit of the AC components.

with a dc offset. Thus, the stack voltages can be obtained

$$v_{\mathrm{ST}i} = V_{\mathrm{ST}i\_\mathrm{dc}} + v_{\mathrm{ST}i\_\mathrm{ac}} \tag{1}$$

where $i = 1, 2,$ and 3.

Then, the equivalent circuits of the dc components and ac components are shown in Fig. 2(a) and 2(b), separately. The regulation of the line currents is realized via changing the values of dc voltage components. While the power exchange between the inserted voltage sources is achieved via adjusting the initial phases of the ac voltage components.

The dc voltage component of Arm_1 is set as 0 to simplify the control strategy. Then, the inserted voltages are determined by the dc voltage components of Arm_2 and Arm_3

$$\begin{cases} V_{\mathrm{ST1\_dc}} = 0 \\ V_{\mathrm{ST2\_dc}} = V_{x12} \\ V_{\mathrm{ST3\_dc}} = V_{x13}. \end{cases} \tag{2}$$

One of the dc voltage components of Arm_2 and Arm_3 is used to regulate the line currents, while the other is used to keep the total energy of all the stacks balanced. It is realized by the control strategy.

The amplitudes ($V_{\mathrm{ST\_ac}}$) of ac voltage components are the same for all stacks and they are related to the modulation indexes (m_1, m_2, and m_3) of stacks. The initial phases of the stacks are 0, φ_2, and φ_3. Thus, the ac voltage components of the stacks can be obtained as

$$\begin{cases} v_{\mathrm{ST1\_ac}}(t) = V_{\mathrm{ST\_ac}} \sin(\omega t) \\ v_{\mathrm{ST2\_ac}}(t) = V_{\mathrm{ST\_ac}} \sin(\omega t + \varphi_2) \\ v_{\mathrm{ST3\_ac}}(t) = V_{\mathrm{ST\_ac}} \sin(\omega t + \varphi_3) \end{cases} \tag{3}$$

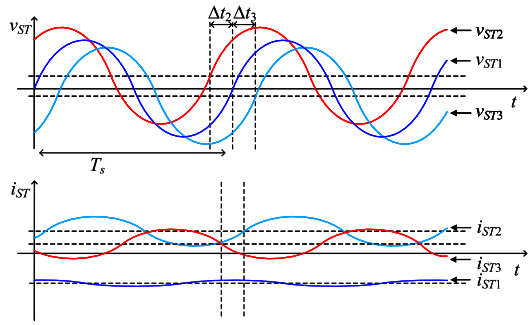


Fig. 3. Waveforms of the stack voltages and stack currents.

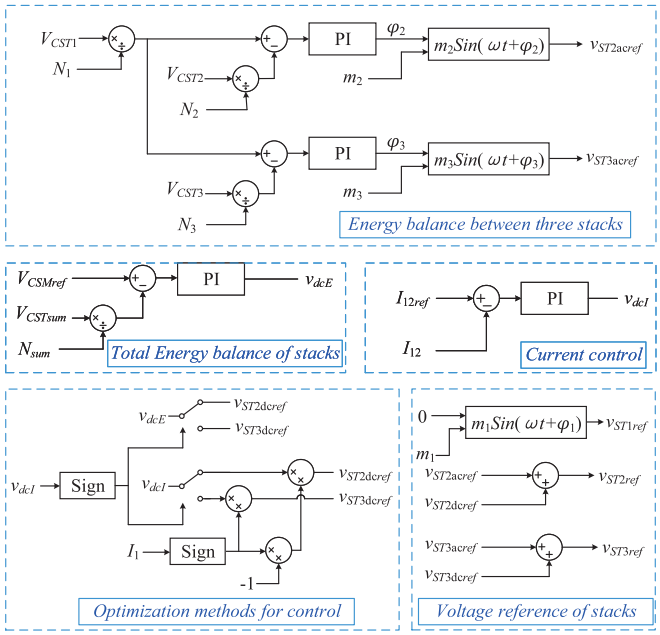


Fig. 4. Control strategy of the proposed IDCPFC topology.

$$V_{\mathrm{ST\_ac}} = m_1 N_1 V_{\mathrm{CSM}} = m_2 N_2 V_{\mathrm{CSM}} = m_3 N_3 V_{\mathrm{CSM}} \tag{4}$$

where the $\omega = 2\pi f_{\mathrm{ac}}$, and f_{ac} is the frequency of ac voltage components.

Since the initial phases of the ac stack voltage components are different, there are ac power exchanges between the stacks. Therefore, the energy balancing of the stacks can be realized by adjusting the initial phases (φ_2 and φ_3). The theoretical waveforms of the stack voltages and stack currents are shown in Fig. 3.

C. Control Strategy

The control strategy diagram is shown in Fig. 4. The reference current of line_{12} is $I_{12\mathrm{ref}}$ and the measured value of line_{12} current is I_{12}. The references to the three stack voltages are represented by V_{ST1ref}, V_{ST2ref} and V_{ST3ref}. The reference of single FBSM capacitor voltage is represented by V_{CSMref}. The sums of the measured values of SM capacitor voltages in the stacks are V_{CST1}, V_{CST2}, and V_{CST3}, respectively. The sum of the measured value of all the SM capacitor voltages in the three stacks is

V_{CSTsum} and the number of all the SMs in the three stacks is N_{sum}.

The control strategy of the proposed topology can be divided into five parts. In the first part, the energy balance between the three stacks is realized. The average SM voltage of all the stacks is controlled to be equal to that of Stack_1. The SM capacitor voltages in the stacks are adjusted by changing the corresponding phase shifts of ac voltage components of stacks. The voltage balance between the SMs in the same stack is realized by the modulation, such as nearest level modulation (NLM) and carrier phase shift pulsewidth modulation (CPS-PWM). Then, in the second part, the total energy balance of the stacks is realized. The sum of all the FBSM capacitor voltages in the three stacks is adjusted by changing the dc component of one stack voltage. In the third part, the regulation of line_{12} current is realized by changing the dc component of another stack voltage. In the fourth part, the optimal control strategy is realized according to the analysis results. The arm voltage utilized to control the line current and the arm voltage used to control the total energy of stacks is determined in this part. Finally, the references of the stack voltages can be obtained according to the dc components and ac components obtained in the previous four parts.

III. Circuit Analysis and Parameter Design

In this section, a detailed theoretical analysis was conducted on the proposed topology, mainly including line current regulation, energy balance, capacitor voltage ripple, and parameter design. There are two general assumptions in the following analysis: 1) stacks generate ideal sinusoidal ac voltage components; and 2) parasitic resistance terms are neglected.

A. Line Currents Regulation

The line current regulation is achieved via changing the inserted voltages, which are determined by the dc voltage components of the stacks. The dc component current of Stack_1 equals the terminal current I_1 of VSC_1 and the dc component currents of Stack_2 and Stack_3 equal the line currents (I_{12} and I_{13}), separately. Then they can be obtained as

$$\begin{cases} I_{\text{ST1\_dc}} = I_1 = I_{\text{ST2\_dc}} + I_{\text{ST3\_dc}} \\ I_{\text{ST2\_dc}} = I_{12} \\ I_{\text{ST3\_dc}} = I_{13}. \end{cases} \tag{5}$$

Without the IDCPFC, the natural currents of line_{12}, line_{13}, and line_{23} are I'_{12}, I'_{13}, and I'_{23}. Then the line current variation caused by the IDCPFC can be obtained ($I_{x12} = I_{12} - I'_{12}$, $I_{x13} = I_{13} - I'_{13}$, $I_{x23} = I_{23} - I'_{23}$).

According to the system parameters and the Ohm's law, then the following can be obtained:

$$\begin{cases} V_2 = V_1 + V_{x12} - I_{12}R_{12} \\ V_3 = V_1 + V_{x13} - I_{13}R_{13} \\ V_2 - V_3 = I_{23}R_{23} \\ P_2 = V_2 I_2 = V_2(I_{23} - I_{12}) \\ P_3 = V_3 I_3 = V_3(-I_{23} - I_{13}). \end{cases} \tag{6}$$

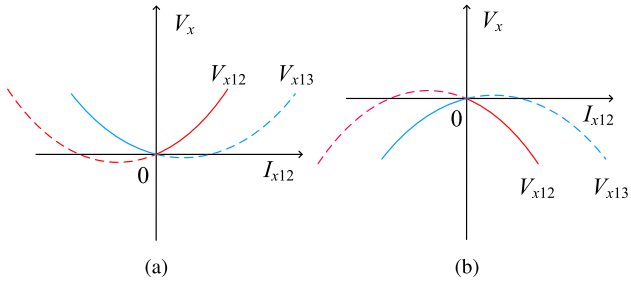


Fig. 5. Relationships of I_{x12}, V_{x12}, and V_{x13} under two conditions. (a) $I_1 > 0$. (b) $I_1 < 0$.

Meanwhile, the dc powers absorbed by Stack_1, Stack_2, and Stack_3 can be obtained as

$$\begin{cases} P_{\text{ST1\_dc}} = 0 \\ P_{\text{ST2\_dc}} = I_{12} \cdot V_{x12} \\ P_{\text{ST3\_dc}} = I_{13} \cdot V_{x13}. \end{cases} \tag{7}$$

To keep the energy balance, the sum of dc power of all the stacks is zero. Then the following can be obtained:

$$P_{\text{ST1\_dc}} + P_{\text{ST2\_dc}} + P_{\text{ST3\_dc}} = V_{x12}I_{12} + V_{x13}I_{13} = 0. \tag{8}$$

According to (6) and (8), the relationships between I_{x12} and V_{x12}, as well as between I_{x12} and V_{x13} can be obtained, which are shown in Fig. 5. It can be seen that the two lines are not linear or monotonic. In addition, the V_{x12} and V_{x13} are both 0 when I_{x12} is 0. Therefore, to enlarge the adjusting area, the variable ($V_{\text{dc}I}$) used to regulate the line current should be selected from V_{x12} and V_{x13}, which depends on the I_{x12}. For example, the relationship between the line current change and inserted voltages is shown in Fig. 5(a) when the line currents are positive ($I'_{12} \geq 0$ and $I'_{13} \geq 0$). The line current variation (I_{x12}) is regulated by adjusting the V_{x13} when $I_{x12} \leq 0$ and by adjusting the V_{x12} when $I_{x12} \geq 0$.

B. Energy Balance

The energy balance of the proposed topology is realized by the circulating currents, which are generated by the ac components of stack voltages. According to (3), the ac components of the stack voltages and arm currents are shown in Fig. 6. Then, the ac current components of the Stack_2 and Stack_3 can be calculated as

$$\begin{aligned} i_{\text{ST2\_ac}}(t) &= \frac{1}{L_{a2}} \int (v_{\text{ST1\_ac}}(t) - v_{\text{ST2\_ac}}(t))\text{d}t \\ &= -\frac{2V_{\text{ST\_ac}} \sin(\frac{\varphi_2}{2})}{\omega L_{a2}} \sin\left(\omega t + \frac{\varphi_2}{2}\right) \end{aligned} \tag{9}$$

$$\begin{aligned} i_{\text{ST3\_ac}}(t) &= \frac{1}{L_{a3}} \int (v_{\text{ST1\_ac}}(t) - v_{\text{ST3\_ac}}(t))\text{d}t \\ &= -\frac{2V_{\text{ST\_ac}} \sin(\frac{\varphi_3}{2})}{\omega L_{a3}} \sin\left(\omega t + \frac{\varphi_3}{2}\right). \end{aligned} \tag{10}$$

According to the Kirchhoff current law (KCL), the ac current component of Stack_1 can be obtained as

$$i_{\text{ST1\_ac}}(t) = -i_{\text{ST2\_ac}}(t) - i_{\text{ST3\_ac}}(t). \tag{11}$$

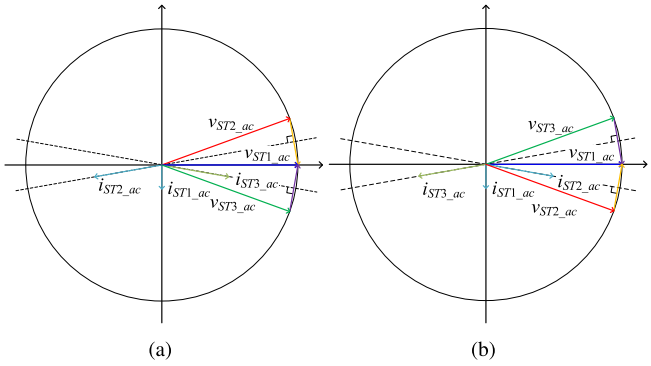


Fig. 6. Analysis of stack currents under two conditions. (a) $\varphi_2 > 0$. (b) $\varphi_2 < 0$.

Then, the ac power components of the stacks can be calculated as

$$\begin{cases} P_{\text{ST1\_ac}} = -\frac{V_{\text{ST\_ac}}^2}{2\omega}\left(\frac{\sin\varphi_2}{L_{a2}} + \frac{\sin\varphi_3}{L_{a3}}\right) \\ P_{\text{ST2\_ac}} = -\frac{V_{\text{ST\_ac}}^2}{2\omega L_{a2}}\sin\varphi_2 \\ P_{\text{ST3\_ac}} = -\frac{V_{\text{ST\_ac}}^2}{2\omega L_{a3}}\sin\varphi_3. \end{cases} \tag{12}$$

To keep the balance of the stack energy, the ac power component and the dc power component of each stack should be equal. Then, it can be presented as

$$P_{\text{ST}i\text{\_ac}} = P_{\text{ST}i\text{\_dc}} \tag{13}$$

where $i = 1, 2$, and 3.

Since the dc power component ($P_{\text{ST1\_dc}}$) of Stack$_1$ is 0, the ac power component ($P_{\text{ST1\_ac}}$) of Stack$_1$ is 0, too. Thus, according to (12), it can be derived as

$$\frac{\sin\varphi_2}{L_{a2}} + \frac{\sin\varphi_3}{L_{a3}} = 0. \tag{14}$$

Generally, since all the ac component voltages are same, all the arm inductances are set as same ($L_{a2} = L_{a3} = L_a$). Then it can be obtained as

$$\varphi_2 = -\varphi_3. \tag{15}$$

Then, substituting (9), (10), and (15) into (11), then it can be calculated as

$$i_{\text{ST1\_ac}}(t) = \frac{4V_{\text{ST\_ac}}\sin^2\left(\frac{\varphi_2}{2}\right)}{\omega L_a}\sin\left(\omega t + \frac{\pi}{2}\right). \tag{16}$$

In addition, the resonant currents (i_{r2} and i_{r3}) are equal to the ac current components of corresponding stacks. Thus, it can be obtained as

$$i_{r2} = i_{\text{ST2\_ac}} \tag{17}$$

$$i_{r3} = i_{\text{ST3\_ac}}. \tag{18}$$

Besides, the resonant frequency (f_r) can be obtained as

$$f_r = f_{\text{ac}} = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{19}$$

C. Capacitor Ripple

The stability of SM capacitor voltages is essential for the proposed power flow controller to operate functionally and stably. Therefore, it is important to select an appropriate SM capacitance to meet the voltage ripple requirements. This section analyzes and calculates the ripples of the SM capacitor voltages in the proposed power flow controller. It is believed that the voltages of SM capacitors in the arms are balanced via the modulation. The number of capacitors in the arm is represented by N_C, and the capacitance value is C_{SM}. The dc component of a single capacitor voltage is V_C, and the ripple is $v_{C\_\text{rip}}(t)$.

The energy stored in the stack is related to the SM capacitor voltage, which can be expressed as

$$e_{\text{ST}}(t) = \frac{1}{2}CN_C\left[V_C + v_{C\_\text{rip}}(t)\right]^2. \tag{20}$$

Simplifying (20) and ignoring the very small quadratic term, the voltage ripple of the capacitor can be obtained as

$$v_{C\_\text{rip}}(t) = \frac{e_{\text{ST\_ac}}(t)}{CN_C V_C}. \tag{21}$$

Normally, the fluctuation of SM capacitor voltage can be represented as

$$\xi = \frac{v_{C\max} - v_{C\min}}{V_C}. \tag{22}$$

Meanwhile, the energy stored in the arm can also be represented by the absorbed power. Therefore, it can be obtained as

$$e_{\text{ST}}(t) = \int_0^t v_p(t)\cdot i_p(t)\mathrm{d}t. \tag{23}$$

The voltages and currents of stacks have been obtained in the previous section. The ac components of the total energy stored in the stacks are represented as $e_{\text{ST1\_ac}}$, $e_{\text{ST2\_ac}}$, and $e_{\text{ST3\_ac}}$. Then, they can be calculated as

$$e_{\text{ST1\_ac}}(t) = \frac{V_{\text{ST\_ac}}}{\omega}\cdot A_1(t) \tag{24}$$

$$e_{\text{ST2\_ac}}(t) = \frac{V_{\text{ST\_ac}}}{\omega}\cdot A_2(t) \tag{25}$$

$$e_{\text{ST3\_ac}}(t) = \frac{V_{\text{ST\_ac}}}{\omega}\cdot A_3(t) \tag{26}$$

where $A_1(t) = \frac{V_{\text{ST\_ac}}\sin^2\frac{\varphi_2}{2}}{\omega L_a}\cos(2\omega t)$, $A_2(t) = \frac{2V_{x12}\sin\frac{\varphi_2}{2}}{\omega La}\cdot\cos(\omega t + \frac{\varphi_2}{2}) - I_{12}\sin(\omega t + \varphi_2) + \frac{V_{\text{ST\_ac}}\sin\frac{\varphi_2}{2}}{2\omega La}\sin(2\omega t + \frac{3\varphi_2}{2})$, $A_3(t) = \frac{2V_{x12}\sin\frac{\varphi_3}{2}}{\omega La}\cdot\cos(\omega t + \frac{\varphi_3}{2}) - I_{12}\sin(\omega t + \varphi_3) + \frac{V_{\text{ST\_ac}}\sin\frac{\varphi_3}{2}}{2\omega La}\sin(2\omega t + \frac{3\varphi_3}{2})$.

The SM capacitances in the three stacks are represented as C_1, C_2, and C_3. The ac components of the SM capacitor voltages are represented as $\tilde{v}_{\text{CST1}}(t)$, $\tilde{v}_{\text{CST2}}(t)$, and $\tilde{v}_{\text{CST3}}(t)$. Then, they can be calculated as

$$\tilde{v}_{\text{CST1}}(t) = \frac{V_{\text{ST\_ac}}}{\omega C_1 N_1 V_{\text{CSM}}}\cdot A_1(t) \tag{27}$$

$$\tilde{v}_{\text{CST2}}(t) = \frac{V_{\text{ST\_ac}}}{\omega C_2 N_2 V_{\text{CSM}}}\cdot A_2(t) \tag{28}$$

$$\tilde{v}_{\mathrm{CST3}}(t) = \frac{V_{\mathrm{ST\_ac}}}{\omega C_3 N_3 V_{\mathrm{CSM}}} \cdot A_3(t). \tag{29}$$

D. Parameter Design

Taking a three-terminal system as an example, this section introduces the parameter design method of the proposed power flow controller.

First, the line resistance can be estimated based on the line parameters. Typically, the line resistance will increase by 1.2 Ω when the line length increases by 100 km. Then, the system parameters are substituted into (6) and (7). The relationship between the current change I_x and the inserted voltage can be obtained, which is similar to Fig. 5.

Assuming that the line current adjustment range are $[I_{x\min}, I_{x\max}]$, the range of the inserted voltage can be obtained as $V_{x12} \in [V_{x12\min}, V_{x12\max}]$ and $V_{x13} \in [V_{x13\min}, V_{x13\max}]$.

By taking a certain margin α, the maximum values ($V_{\mathrm{ST2\_dc\,max}}$ and $V_{\mathrm{ST3\_dc\,max}}$) of the inserted voltage dc component can be obtained

$$V_{\mathrm{ST2\_dc\,max}} = \max\{|V_{x12\min}|, |V_{x12\max}|\} \cdot (1+\alpha) \tag{30}$$

$$V_{\mathrm{ST3\_dc\,max}} = \max\{|V_{x13\min}|, |V_{x13\max}|\} \cdot (1+\alpha). \tag{31}$$

Generally, the amplitude ($V_{\mathrm{ST\_ac}}$) of the ac component voltage equals to the maximum value of $V_{\mathrm{ST2\_dc\,max}}$ and $V_{\mathrm{ST3\_dc\,max}}$. The rated voltage of the stack SM capacitors is determined by the parameters of the semiconductor devices and it is generally set as 2 kV. The modulation indexes m_1, m_2, m_3 are generally all set as 1. The numbers of SMs in stacks can be calculated according to the value ranges of the stack voltages. Then, they can be obtained as

$$N_1 \geq \frac{V_{\mathrm{ST\_ac}}}{m_1 V_{\mathrm{CSM}}} \tag{32}$$

$$N_2 \geq \frac{m_2 V_{\mathrm{ST2\_dc\,max}} + V_{\mathrm{ST\_ac}}}{m_2 V_{\mathrm{CSM}}} \tag{33}$$

$$N_3 \geq \frac{m_3 V_{\mathrm{ST3\_dc\,max}} + V_{\mathrm{ST\_ac}}}{m_3 V_{\mathrm{CSM}}}. \tag{34}$$

The arm inductors are used for ac power transmission of the stacks, which ensures the energy balance between the stacks. Therefore, the value of arm inductance is determined by the required maximum ($|P_{\mathrm{ST2\_ac}}|_{\max}$) of the ac power transferred between the stacks. According to (12), the value of the arm inductance can be obtained

$$L_a \leq \frac{V_{\mathrm{ST\_ac}}^2 \sin\varphi_{2\max}}{2\omega\,|P_{\mathrm{ST2\_ac}}|_{\max}}. \tag{35}$$

The maximum value ($|P_{\mathrm{ST2\_ac}}|_{\max}$) of ac component of Stack_2 can be obtained according to (6) and (7). The maximum ($\varphi_{2\max}$) phase can be set according to the system requirement ($-\varphi_{2\max} \leq \varphi_2 \leq \varphi_{2\max}$). In practical applications, $|P_{\mathrm{ST2\_ac}}|_{\max}$ is difficult to calculate. Due to $|P_{\mathrm{ST2\_ac}}|_{\max} \leq V_{\mathrm{ST2\_dc\,max}} \cdot |I_{12}|_{\max}$, in order to simplify the calculation, the requirement of L_a can also be obtained as

$$L_a \leq \frac{V_{\mathrm{ST\_ac}}^2}{2\omega V_{\mathrm{ST2\_dc\,max}} \cdot |I_{12}|_{\max}} \sin\varphi_{2\max}. \tag{36}$$

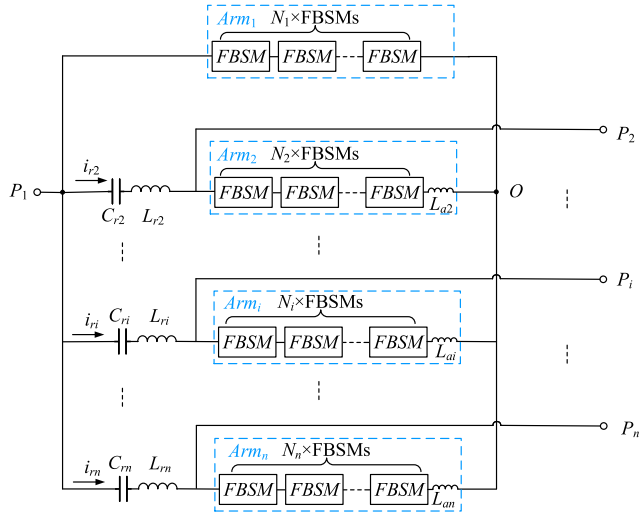


Fig. 7. Topology applied in dc grid with n terminals.

When phase shift angle φ_2 is set as $\varphi_{2\max}$, the ripple of $A_1(t)$, $A_2(t)$, and $A_3(t)$ can be calculated as $\Delta A_1, \Delta A_2$, and ΔA_3. Assuming that the fluctuation requirement of the SM capacitor voltage is $\xi_{\max}$. Then, the capacitances of the SM capacitors can be obtained

$$C_1 \geq \frac{V_{\mathrm{ST\_ac}} \Delta A_1}{\omega \xi_{\max} N_1 V_{\mathrm{CSM}}^2} \tag{37}$$

$$C_2 \geq \frac{V_{\mathrm{ST\_ac}} \Delta A_2}{\omega \xi_{\max} N_2 V_{\mathrm{CSM}}^2} \tag{38}$$

$$C_3 \geq \frac{V_{\mathrm{ST\_ac}} \Delta A_3}{\omega \xi_{\max} N_3 V_{\mathrm{CSM}}^2}. \tag{39}$$

The resonant frequency of the resonant tank should be consistent with the frequency of the ac component

$$L_r C_r = \frac{1}{4\pi^2 f_{\mathrm{ac}}^2}. \tag{40}$$

E. Future Configuration

In the future, the structure of dc power grids will become more complex. In order to meet the needs of power flow controllers, the topology proposed in this article can be extended to a multiport topology, as shown in Fig. 7.

For each additional port, only one resonant tank and one arm need to be added, which are series-connected. They also connect with Arm_1 in parallel. Besides, replacing IGBT with SiC switching devices can further improve the adjustment range of the proposed power flow controller.

IV. Comparison

A. Comparison of Different Types DCPFCs

This section provides a brief comparison between the proposed topology and other four DCPFCs. They are the typical topologies of various types of DCPFCs, including SVR [11],

TABLE I
COMPARISON OF DIFFERENT TYPES OF DCPFCS

Topology		SVR [11]	DCT [12]	SAVS [16]	Classic IDCPFC [24]	Proposed IDCPFC
Technical	Structure	+	+++++	++++	++	+++
	Control	+	+++++	++++	++	+++
Economic	Cost	+	+++++	++++	++	+++
	Efficiency	+	++	+++	+++++	++++
Adjustment capability	Amplitude	↓	↑/↓	↑/↓	↑/↓	↑/↓
	Direction	+/-	+/-	+/-	+/-	+/-
	Adjustment range	+	+++++	++	++	+++++
	Freedom	$n-1$	$n-1$	$n-1$	$n-2$	$n-2$
Application	Terminal voltage	Low	Different	Any	Any	Any
	External source	No	No	Yes	No	No
	Single line	Yes	Yes	Yes	No	No
	Multiple line	Yes	Yes	Yes	Yes	Yes

The + represents the degree of structure complexity, control complexity, cost, power loss, and adjustment range. The ↑/↓ represent the increase and decrease, separately. The +/– represent the positive and negative, respectively.

DCT [12], SAVS [16], and classic IDCPFC [24]. The comparison mainly focuses on four aspects including technical, economic, adjustment capability, and application. The comparison results are given in Table I.

First, the comparison of technologies is mainly reflected in the complexity of circuit structures and control strategies. The SVR-type DCPFC has the simplest topology and control strategy. The structure and control strategy of the proposed topology are more complex than those of the classic IDCPFC but simpler than those of DCT and SAVS-type DCPFCs.

Second, economic comparison mainly considers the cost and efficiency. The classic IDCPFC and proposed IDCPFC do not need to withstand system voltage compared to DCT and SAVS-type DCPFCs. As a result, the two IDCPFCs can reduce a lot of devices. The SVR-type DCPFC has the lowest cost. However, the cost of the proposed topology is higher than the cost of classic IDCPFC due to the employment of arms, but much lower than the costs of DCT and SAVS-type DCPFCs. Only the efficiency of the classic IDCPFC is higher than that of the proposed IDCPFC. Meanwhile, DCT and SAVS-type DCPFCs have higher power losses because they require a large number of semiconductor devices.

Third, the comparison of adjustment capability is completed in terms of regulation amplitude and direction, regulation range, and freedom degree. Due to SVR-type DCPFC increasing resistance in the line to regulate current, the amplitude of the line current can only be lower than the amplitude of the natural line current, and the direction of the line current cannot be changed. However, the other three topologies achieve current regulation by inserting variable voltage in the line. Therefore, they can adjust both the amplitude and direction of the line currents. The adjustment range of the power flow controller usually depends on the value ranges of the inserted voltages. Therefore, the DCT-type DCPFC and proposed power flow controller can realize a wide range of current regulation. The main circuit of the SAVS-type DCPFC and the classic IDCPFC are both composed of switches or series-connected switches instead of MMC arms, causing the adjustment range to be small. Since inserting larger resistors into the line will lead to significant losses and overheating, SVR-type DCPFC cannot achieve a wide range of current regulation. The freedom degree of a power flow controller represents the number of line currents that can be controlled actively and independently. Since inserted voltages exchange energy with each other through circulating currents, the classic IDCPFC and the proposed topology cannot adjust all line currents independently. Assuming that there are n terminals and $n-1$ line currents need to be regulated in the system, the two IDCPFCs can only control $n-2$ of them actively, the last one would be regulated passively. While the other three topologies can adjust all the line currents actively.

Finally, the application scenarios of the four topologies are summarized. The SVR-type DCPFC is suitable for low-voltage and low-power scenarios due to its significant power losses and overheating. Besides, it cannot adjust the direction of line current, which is a limitation for the practical applications. The DCT-type DCPFC is suitable for scenarios where the voltage levels of the dc terminals are different. Since SAVS-type DCPFCs and the two IDCPFCs do not need to withstand system voltage, they are suitable for any voltage level. SAVS-type DCPFC requires an additional voltage source, which will limit the installation location. Meanwhile, the classic IDCPFC and proposed IDCPFC cannot be used to adjust the current of a single line. Different from the classic IDCPFC, the proposed IDCPFC can be employed to adjust the line currents when a wide adjustment range is required. All types of DCPFC topologies can be extended to multiport topologies to control the currents of multiple lines.

B. Comparison With Another IDCPFC Topology

To demonstrate the advantages and characteristics of the proposed topology, it is compared with another modular IDCPFC topology proposed previously based on costs, current stresses, and power losses in this section [31]. The system parameters are shown in Tables II and III. The VSC_1 is controlled as a dc voltage regulator and the rated dc voltage is 400 kV. The VSC_2 and VSC_3 are controlled as power regulators and the rated active powers are 300 MW and 500 MW. The line resistances (R_{12}, R_{13}, and R_{23}) of $line_{12}$, $line_{13}$, and $line_{23}$ are 3.6 Ω, 1.8 Ω, and 2.4 Ω. The line inductances (L_{12}, L_{13}, and L_{23}) of $Line_{12}$, $Line_{13}$, and $Line_{23}$ are 30 mH, 15 mH, and 20 mH.

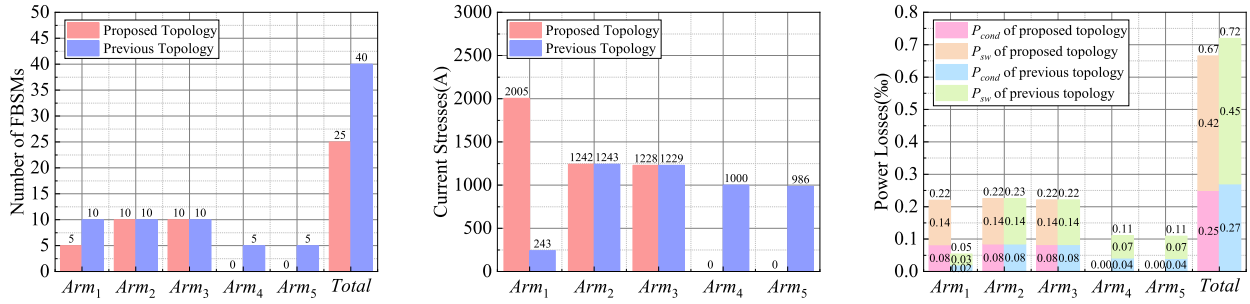


Fig. 8. Comparison of the proposed topology and the previous topology. (a) Costs. (b) Current stresses. (c) Power losses.

TABLE II
TERMINALS PARAMETERS IN SIMULATION

Terminals	Control mode	P(MW)	Q(Mvar)	V_{dc}(kV)
VSC_1	V_{dc}/Q	–	0	400
VSC_2	P/Q	300	0	–
VSC_3	P/Q	500	0	–

TABLE III
LINE PARAMETERS IN SIMULATION

Lines	Length (km)	R (Ω)	L (mH)
$line_{12}$	300	3.6	30
$line_{13}$	150	1.8	15
$line_{23}$	200	2.4	20

1) Cost: The semiconductor switches are selected as ABB 5SNA3000K452300 and the rated SM capacitor voltage is set as 2 kV. Then the FBSM numbers of the two topologies are shown in Fig. 8(a). It can be seen that the FBSM numbers of Arm_2 and Arm_3 of the two topologies are the same. However, the number of FBSMs in Arm_1 in the proposed topology is half of the previous topology. Besides, the proposed topology does not require the Arm_4 and Arm_5 in the previous topology. Therefore, the total FBSM numbers of the proposed topology and the previous topology are 25 and 40, respectively. It means that the total cost of the proposed topology is about 37.5% lower than that of the previous topology.

2) Component Stresses: The current stresses of semiconductor switches are shown in Fig. 8(b). It can be seen that the current stresses of the IGBTs in Arm_2 and Arm_3 of the two topologies are nearly the same, which are 1243 A and 1228 A, respectively. However, the current stresses of the IGBTs in Arm_1 of the proposed topology are higher than the current stresses of the IGBTs in Arm_1 of the previous topology, which are 2005 A and 243 A, separately. Besides, the current stresses of Arm_4 and Arm_5 in the previous topology are 1000 A and 986 A, while the proposed topology does not require the Arm_4 and Arm_5.

3) Efficiency: The power losses of the two topologies are shown in Fig. 8(c). It can be seen that the power losses of the semiconductor devices in Arm_2 and Arm_3 of the two topologies are basically the same, which are all about 0.022%. However, the power losses of the semiconductor devices in Arm_1 of the proposed topology are higher than the power losses of the semiconductor devices in Arm_1 of the previous topology, which are 0.022% and 0.005%, respectively. Besides, the power losses of the semiconductor devices of Arm_4 and Arm_5 in the previous topology are 0.011% and 0.011%, while the proposed topology does not require the Arm_4 and Arm_5. Therefore, the total power losses of the two topologies are 0.067% and 0.072%, which means that the power loss of the proposed topology is 6.94% lower than that of the previous topology.

TABLE IV
SIMULATION PARAMETERS

Symbol	Description	Value
N_1	Number of FBSMs in Arm_1	5
N_2	Number of FBSMs in Arm_2	10
N_3	Number of FBSMs in Arm_3	10
L_{a2}, L_{a3}	Arm inductance in the stacks	1 mH
$Lr2, Lr3$	Resonant inductance	1 mH
$Cr2, Cr3$	Resonant capacitance	100 μF
f_{ac}	ac frequency	500 Hz
V_{CSM}	rated voltage of SM capacitors	2 kV
C	SM capacitance	5000 μF

In summary, the proposed topology can significantly reduce the cost compared to the previous topology. Both the two topologies have low power losses, while the proposed topology has relatively lower power losses. The current stresses of the Arm_2 and Arm_3 in the two topologies are the same. However, the proposed topology has higher current stresses of Arm_1 because it does not require Arm_4 and Arm_5.

V. SIMULATION RESULTS

A simulation model of the IDCPFC shown in Fig. 1 is built in PSCAD/EMTDC to verify the operation principle, control strategy and theoretical analysis results. The detailed parameters of the converter in simulation are shown in Table IV. The proposed IDCPFC is employed to regulate the line currents I_{12}. The simulation results presented in Figs. 9 and 10 show the performance of the proposed IDCPFC under steady state conditions and dynamic response conditions.

Fig. 9(a) shows the voltages of the stacks in the three arms. The amplitudes of ac voltage components in the three arms are the same, and there are phase shifts among the ac voltage components of the three stacks. The phase of V_{ST2_ac} is ahead of that of V_{ST1_ac}, and the phase of V_{ST3_ac} lags behind that of

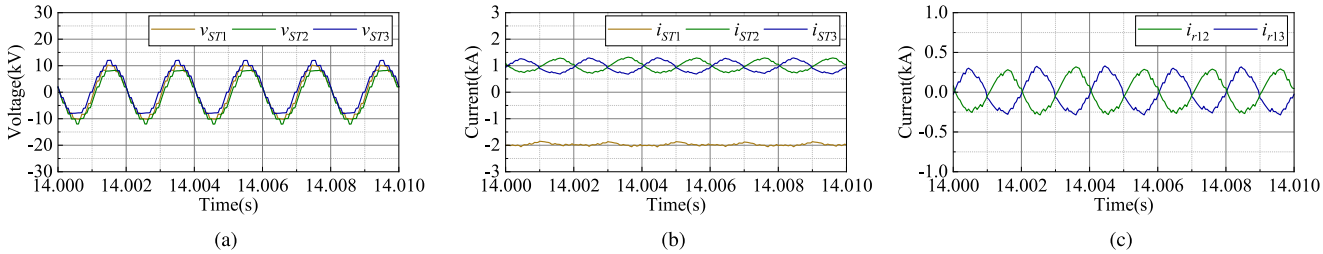


Fig. 9. Simulation results under steady-state conditions. (a) Stack voltages. (b) Stack currents. (c) Resonant currents.

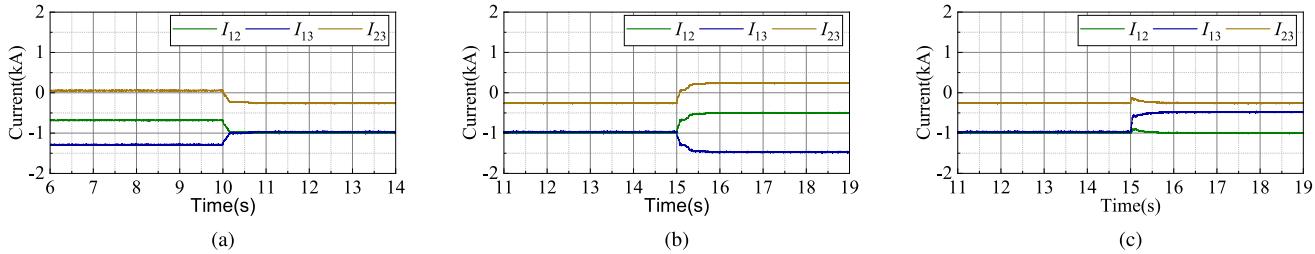


Fig. 10. Simulation results under dynamic response. (a) Line currents when the I_{12} is reduced. (b) Line currents when the I_{12} is increased. (c) Line currents when the P_3 is reduced.

$V_{\mathrm{ST1\_ac}}$. The dc voltage component of Arm_1 is 0 ($V_{\mathrm{ST1\_dc}} = 0$). The dc voltage component of Arm_2 is negative ($V_{\mathrm{ST2\_dc}} < 0$) and the dc voltage component of Arm_3 is positive ($V_{\mathrm{ST3}\_dc} > 0$). Therefore, the inserted voltage in line_{12} is negative and the inserted voltage in line_{13} is positive, which means that the current of line_{12} is decreased and the current of line_{13} is increased after the regulation of the proposed IDCPFC.

Fig. 9(b) shows the currents of the three stacks. The amplitude of ac current component in Arm_2 is basically equal to that in Arm_3 and the phase of ac current component in Arm_2 is roughly opposite to that in Arm_3. Since the phase shifts (φ_2 and φ_3) are very small, the amplitude of ac current component of Arm_1 is very small. The dc current components of Arm_1, Arm_2, and Arm_3 are approximately 1986 A, 1000 A, and 986 A, which are equal to the opposite number of line current of line_{12} and line_{13}. The dc current components of Arm_1 are approximately -2000 A, which is equal to the terminal current of VSC_1.

Fig. 9(c) shows the currents of the resonant tanks. The amplitudes of ac currents in the two resonant tanks are basically the same and the phases of ac currents in the two resonant tanks are roughly opposite. Moreover, the current amplitudes of these two resonant tanks are the same as the ac components of the corresponding arm currents.

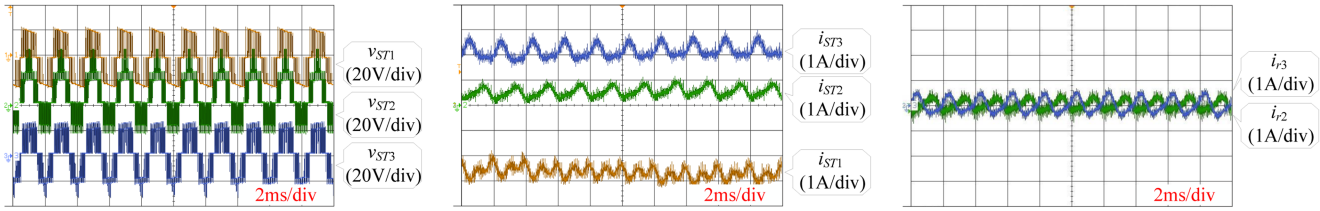
Fig. 10(a) shows the waveforms of line currents when the I_{12} is controlled to reduce. The current (I_{12}) of line_{12} is regulated from the initial current (-0.69 kA) to the reference current (-1 kA) at $t = 10$ s. After about 1.5 s, the line current is adjusted to the reference current and reaches a new steady state. Apart from I_{12}, the I_{13} and I_{23} also change, which means that the part of the terminal current of VSC_3 is controlled to flow into line_{23} and finally flow to line_{13}.

Fig. 10(b) shows the waveforms of line currents when the I_{12} is controlled to increase. The current (I_{12}) of line_{12} is regulated from the original current (-1 kA) to the reference current (-0.5 kA) at $t = 15$ s. The adjustment time of the power flow controller is approximately 1 s. Similarly, the part of the terminal current of VSC_3 is controlled to flow into line_{23} and finally flow to line_{13}. Therefore, the I_{13} and I_{23} also are changed.

Fig. 10(c) shows the waveforms of line currents when the P_3 is controlled to decrease suddenly. The power (P_3) of terminal VSC_3 is changed from the rated power (500 MW) to another power (300 MW) at $t = 15$ s. It can be seen that all the line currents also change a little at $t = 15$ s. After about 1 s, the system reaches a new steady state. The current of line_{12}, which is controlled by the IDCPFC, returns to the reference value. The current of line_{13} changes a lot because the terminal current (I_3) changes. Since the output power of terminal VSC_3 changes, the terminal voltage (V_2) and terminal current (I_2) also change slightly. Therefore, the current of line_{23} also decreases slightly.

VI. Experiment Results

To verify the operation principle and control strategy, a downscaled prototype according to Fig. 1 is built in the laboratory. The experimental platform is displayed in Fig. 12 and the detailed parameters of the experimental system are shown in Table V. The experiment platform contains three terminals (VSC_1, VSC_2, and VSC_3). The VSC_1 is controlled as a dc voltage regulator and the terminal voltage is 100 V. The VSC_2 and VSC_3 are controlled as power regulators and the rated power are both 150 W. The line resistances are all 2 Ω. The experiment results presented in Fig. 11 show the performance of the proposed



(a) (b) (c)

Fig. 11. Experiment results under steady state condition. (a) Stack voltages. (b) Stack currents. (c) Resonant currents.

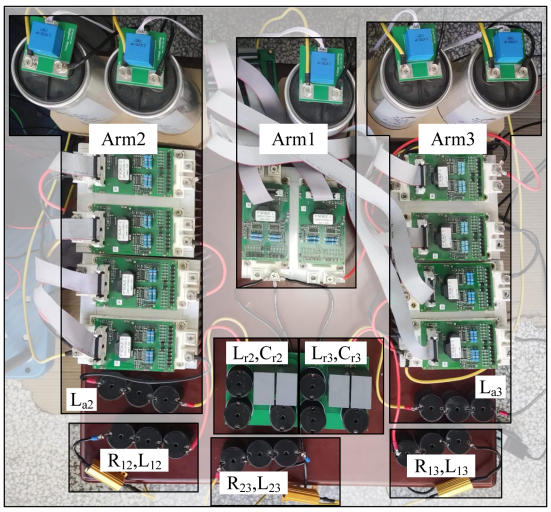


Fig. 12. Experiment platform.

TABLE V
EXPERIMENT PARAMETERS

Symbol	Description	Value
N_1	Number of FBSMs in Arm_1	1
N_2	Number of FBSMs in Arm_2	2
N_3	Number of FBSMs in Arm_3	2
L_{a2}, L_{a3}	Arm inductance in the stacks	1 mH
$Lr2, Lr3$	Resonant inductance	1 mH
$Cr2, Cr3$	Resonant capacitance	100 μF
f_{ac}	ac frequency	500 Hz
V_{CSM}	rated voltage of SM capacitors	20 V
C	SM capacitance	550 μF

IDCPFC under steady-state conditions. Figs. 13 and 14 show the dynamic performance of the proposed IDCPFC under different conditions.

Fig. 11(a) shows the voltages of the stacks in the three arms. There are small phase shifts among the ac voltage components of the three stacks. The dc voltage components of Arm_1, Arm_2, and Arm_3 are 0, positive and negative, separately. It means that the inserted voltage in line_{12} is positive and the inserted voltage in line_{13} is negative. As a result, the current of line_{12} is increased and the current of line_{13} is decreased after the regulation of the proposed IDCPFC.

Fig. 11(b) shows the currents of the three stacks. The amplitude of ac current component in Arm_2 is basically equal to that in Arm_3. Due to the existence of parasitic parameters, the phase of ac current component in Arm_2 is not exactly opposite to that in Arm_3. As a result, the ac current component of Arm_1 is not as small as in the simulation.

Fig. 11(c) shows the currents of the resonant tanks. The two resonant currents are the same as the ac components of the corresponding arm currents. Similarly, the amplitudes are essentially the same and the phases are not completely opposite due to the influence of parasitic parameters.

Fig. 13 shows the dynamic performance when the powers of VSC_2 and VSC_3 are positive ($P_2 = 150$ W, $P_3 = 150$ W). Fig. 13(a) shows the waveforms of line currents when the I_{12} is controlled to decrease. The current (I_{12}) of line_{12} is regulated from the original current (-0.5 A) to reference current (-1.5 A). The adjustment time of the power flow controller is approximately 1.5 s.

Fig. 13(b) shows the waveforms of line currents when the I_{12} is controlled to increase. The current (I_{12}) of line_{12} is regulated from the initial current (-1.5 A) to reference current (-0.5 A). After about 1.5 s, the line current is adjusted to the reference current and reaches a new steady state. Apart from I_{12}, the I_{13} and I_{23} also change, which means that the part of the terminal current of VSC_2 is controlled to flow into line_{23} and finally flow to line_{13}.

Fig. 13(c) shows the waveforms of line currents when the P_2 is controlled to decrease suddenly. The power (P_2) of terminal VSC_2 is changed from 150 W to 100 W. It can be seen that all the line currents change a little when the P_2 decreases suddenly. After about 0.7 s, the system reaches a new steady state. The current of line_{12}, which is controlled by the IDCPFC, returns to the reference value. Similar to the simulation results, the current of line_{13} changes a lot because the terminal current (I_2) changes.

Fig. 14 shows the dynamic performance when the powers of VSC_2 and VSC_3 are negative ($P_2 = -150$ W, $P_3 = -150$ W). Fig. 14(a) shows the waveforms of line currents when the I_{12} is controlled to decrease. The current (I_{12}) of line_{12} is regulated from the original current (1.5 A) to reference current (0.5 A). The adjustment time of the power flow controller is approximately 1 s. Apart from I_{12}, the I_{13} and I_{23} also change, which means that the part of the line current of I_{13} is controlled to flow into line_{23} and finally flow to terminal VSC_2.

Fig. 14(b) shows the waveforms of line currents when the I_{12} is controlled to increase. The current (I_{12}) of line_{12} is regulated from the initial current (0.5 A) to reference current (1.5 A). After about 1.5 s, the line current is adjusted to the reference

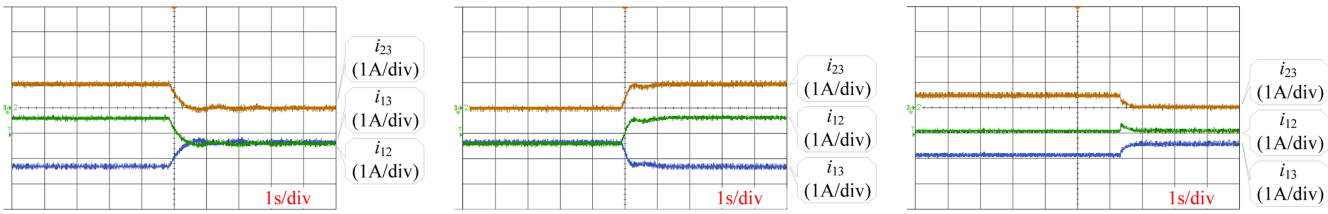


Fig. 13. Experiment results under dynamic response when the powers of VSC_2 and VSC_3 are positive ($P_2 = 150$ W, $P_3 = 150$ W). (a) Line currents when the I_{12} is reduced. (b) Line currents when the I_{12} is increased. (c) Line currents when the P_2 is reduced.

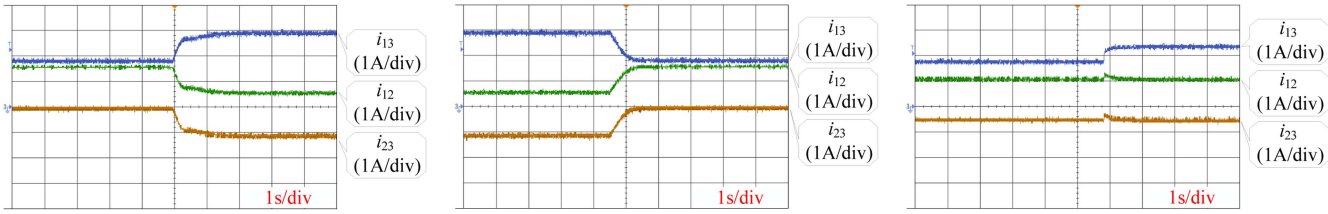


Fig. 14. Experiment results under dynamic response when the powers of VSC_2 and VSC_3 are negative ($P_2 = -150$ W, $P_3 = -150$ W). (a) Line currents when the I_{12} is reduced. (b) Line currents when the I_{12} is increased. (c) Line currents when the P_3 is increased.

current and reaches a new steady state. Similarly, the part of the line current of I_{13}, which flows into $line_{23}$ and finally flow to terminal VSC_2 is decreased.

Fig. 14(c) shows the waveforms of line currents when the P_3 is controlled to increase suddenly. The power (P_3) of terminal VSC_3 is changed from -100 W to -150 W. It can be seen that all the line currents change a little when the P_3 increases suddenly. After about 0.5 s, the system reaches a new steady state. The current of $line_{12}$, which is controlled by the IDCPFC, returns to the reference value. The current of $line_{13}$ changes a lot because the terminal current (I_3) changes.

VII. Conclusion

A novel IDCPFC topology used to regulate the line currents in the meshed multiterminal dc grids is proposed in this article. The current adjustment range is significantly improved due to the employment of MMC arms. It can be easily expanded into multiport topology by changing the number of resonant tanks and arms. It is suitable for applications at various voltage levels because it does not need to withstand the system voltage. The operation principle, control strategy, theoretical analysis, and the merits of the proposed topology are discussed in detail. The comparison with the other four topologies demonstrates its advantages in economy and adjustment capability. The comparison with another modular IDCPFC topology is completed and the results reveal that the proposed topology has the advantages of low cost and high efficiency, but the drawback is the higher device current stresses in Arm_1. Simulations performed in PSCAD/EMTDC and experiments based on a down-scaled prototype are completed. The simulation and experimental results demonstrate the steady-state and dynamic performance under various conditions.

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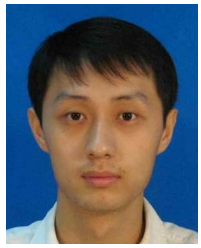

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