A Hybrid Desaturation Fast Detection Circuit for Bridge Leg Short-Circuit Faults

Zicheng Liu, *Senior Member, IEEE*, Jiewei He, *Student Member, IEEE*, Dong Jiang, *Senior Member, IEEE*, Xiangwen Sun, *Student Member, IEEE*, Guang Yang, Hongyang Liu, Peng Li, and Ronghai Qu, *Fellow, IEEE*

***Abstract*—This article proposes an improved hybrid desaturation detection circuit for switching devices, which aims to accelerate the short-circuit (SC) protection for the bridge leg in power converters. The proposed hybrid detection circuit not only retains the linear charging rate of the blanking capacitor voltage like the current source detection circuit, but also obtains the circuit parameters' adjustment capability like the voltage source detection circuit. The mapping between the detected desaturation voltage and the terminal voltage of the semiconductor device can be modified by the proposed solution. Thus, for bridge leg phase SC with a slow current change rate, the proposed circuit can appropriately set the detection threshold to fit the maximum operating current, thereby shortening the peak value and duration of the SC current. Furthermore, the proposed circuit can decouple the detection speed configuration of fault-under-load (FUL) and hard-switching-fault (HSF) states without adding additional detection circuits. Thus, it can accelerate the detection of FUL without shortening the blanking time of HSF, and therefore the shoot-through SC fault of the entire bridge leg can be quickly cutoff. Experimental results verify that the proposed circuit can effectively accelerate the detection and protection process of bridge leg SC faults.**

***Index Terms*—Bridge leg, desaturation detection, detection threshold, fast detection.**

I. Introduction

IN VARIOUS applications, such as motor drives and grid-tied converters, power semiconductor devices are commonly used in pairs as bridge legs. Short-circuit (SC) faults pose the most significant risk to bridge legs, as the fault current can rapidly increase to several times of the rated value, causing irreversible damage to the devices and even threatening personal safety. In recent years, wide bandgap (WBG) power semiconductors, such as SiC MOSFETs, have shown obvious advantages of low loss and high-temperature operating capability over silicon-based devices. However, they are less tolerant of SC faults. Therefore, there is an urgent demand for fast detection ability of SC faults to ensure the reliability of bridge legs [1], [2].

Manuscript received 19 October 2023; revised 28 February 2024; accepted 4 April 2024. Date of publication 16 April 2024; date of current version 20 June 2024. This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grant 52077088, in part by the Aeronautical Science Foundation of China under Grant 2022Z027079001, and in part by the Key R&D Plan of Hubei Province under Project 2022BAA062. Recommended for publication by Associate Editor D. Xu. *(Corresponding author: Dong Jiang.)*

Zicheng Liu, Jiewei He, Dong Jiang, Xiangwen Sun, and Ronghai Qu are with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: liuzc@hust.edu.cn; he_jiewei@hust.edu.cn; jiangd@hust.edu.cn; sunxw@hust.edu.cn; ronghaiqu@hust.edu.cn).

Guang Yang and Hongyang Liu are with the AVIC Xi'an Flight Automatic Control Research Institute, Xi'an 710065, China (e-mail: liuhy076@avic.com; yangg073@avic.com).

Peng Li is with the Wuhan Second Ship Design and Research Institute, Wuhan 430064, China (e-mail: m202171365@hust.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3389033.

Digital Object Identifier 10.1109/TPEL.2024.3389033

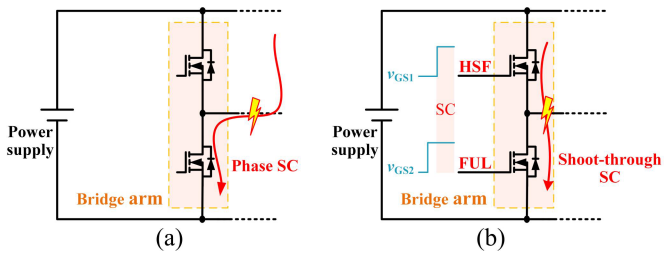


Fig. 1. Two SC situations of the bridge leg. (a) Phase SC. (b) Shoot-through SC.

TABLE I
Types and Characteristics of Bridge Leg SC Faults

Type	Loop inductance	SC device	
Phase SC	μH magnitude	The device in the phase SC loop	
Shoot-through SC	nH magnitude	The device that causes SC due to turn on action	HSF
		The device that was turned on before SC	FUL

According to the location of the SC fault on the bridge leg, as shown in Fig. 1, it can be classified as phase SC and shoot-through SC [3]. The phase SC creates a conduction loop through the midpoint of the bridge leg and has a larger loop inductance compared to the shoot-through SC [4], resulting in a slower rise of the fault current. The shoot-through SC is considered the most hazardous due to the small loop impedance, which causes a rapid increase in fault current after the SC occurs. Under shoot-through SC, the two semiconductor devices in the bridge leg are in different SC states. The device that caused the SC fault due to a turn-ON action belongs to the hard-switching-fault (HSF) state, while another device that was turned ON before the SC moment belongs to the fault-under-load (FUL) state. Types and characteristics of bridge leg SC faults are listed in Table I.

TABLE II
COMPARISON OF THE PROPOSED HYBRID TOPOLOGY WITH CONVENTIONAL TOPOLOGIES

Topology	Capacitor charging rate	Blanking time calculation	Adjustable threshold
Voltage source circuit	Nonlinear	Complex	Yes
Current source circuit	Linear	Simple	No
Proposed hybrid circuit	Linear	Simple	Yes

TABLE III
DETECTION SPEED ADJUSTMENT COMPARISON OF PROPOSED HYBRID TOPOLOGY WITH EXISTING TOPOLOGIES

Topology	Detection unit	Detection speed of FUL and HSF	Potential of fast FUL detection
Conventional circuit [13], [14], [15], [16], [17]	Single	Coupling	Not realized
Separate detection circuit [18], [19], [20]	Double	Decoupling	Realized
Proposed hybrid circuit	Single	Decoupling	Realized

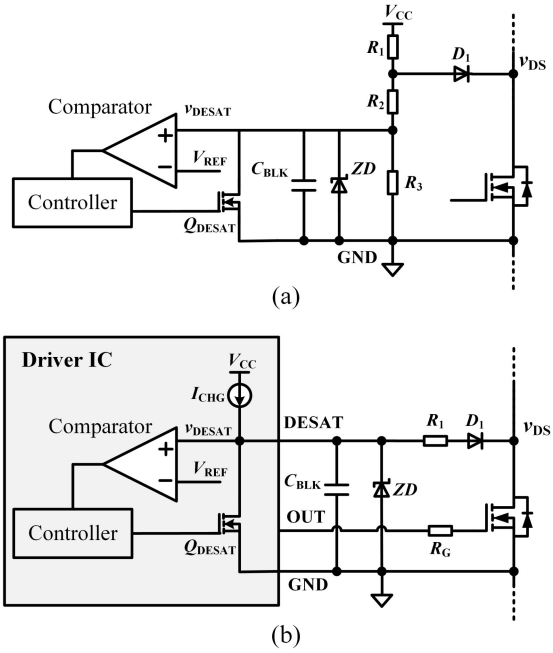


Fig. 2. Two typical desaturation detection circuit topologies: (a) voltage source circuit; (b) current source circuit.

The detection of SC faults represents the first step in the protection process, and several methods have been proposed for power semiconductor SC detection [5]. Some scholars use the parasitic inductance in the circuit for detection [6], [7]. Although this method has fast response performance, its application is limited due to the filtering effect on the dc component. There is also a SC detection method based on the difference between the gate voltage under normal and SC conditions [8], [9], [10], but the circuit design is relatively complicated and the reliability is poor. Integrating a Rogowski coil on a printed circuit board (PCB) can also be used for SC detection [11], [12], but the circuit structure is too complicated to be applied in the industrial field.

Presently, the most commonly used method is desaturation detection [13], [14], [15], [16], [17], [18], [19], [20], [21], which detects the terminal voltage when the device is turned ON. When the terminal voltage is greater than the threshold, it is determined to be a SC situation. The circuit will charge a capacitor (blanking capacitor) to the trigger level and then output a fault signal. Compared with the above detection methods, it has a simpler structure and higher reliability.

The desaturation detection circuit can be divided into two categories as shown in Fig. 2 according to the charging method of the blanking capacitor. The voltage source circuit charges the blanking capacitor through the voltage source to trigger the SC signal [13], [14]. The circuit is built with discrete components and can flexibly adjust parameters, such as the detection threshold. However, the charging rate of the blanking capacitor is non-linear and is related to multiple parameters, thus making the calculation and adjustment of the charging time very difficult.

The current source circuit charges the blanking capacitor through the integrated current source of the gate driver IC [15], [16], [17], which makes the charging rate of the blanking capacitor linear. Compared with voltage source circuits, it has simpler peripheral circuits, and the charging time of the blanking capacitor is easier to calculate and adjust, so it is more widely used in industrial design.

However, major manufacturers' gate driver IC products with the desaturation detection function have a fixed trigger level, which makes it difficult to flexibly adjust the detection threshold in current source circuits [11]. Although the detection threshold can be roughly adjusted by connecting multiple D_1 in series, the adjustment range and accuracy are limited. Moreover, additional components are required, which prevents its application to already-produced PCBs. Therefore, it is difficult for current source circuits to achieve refined detection threshold adjustment according to the actual needs of the application scenarios [16]. An inappropriate fixed threshold may even cause the SC device to burn out [17].

Furthermore, the charging time of the blanking capacitor, also called blanking time, is used to distinguish between normal turn-ON transient and HSF. Although the blanking time avoids false triggering, it slows down the protection speed. Especially for the FUL, the blanking time affects the detection speed, which in fact is not required. In order to achieve fast detection of FUL while distinguishing between HSF and the turn-ON transient, some scholars have adopted two different detection circuits to detect HSF and FUL, respectively [18], [19], [20], the circuits are rather complicated to be practically applied.

In summary, the extensively-used current source desaturation circuit lacks adjustment flexibility. Its fixed detection threshold makes it difficult to adapt to various application requirements. Furthermore, the detection speeds of HSF and FUL states are mutually coupled, limiting the full exploitation of fast-detection capabilities within a specific blanking time.

This article proposes a fast hybrid desaturation detection circuit for bridge leg SC faults. This circuit is as simple to configure

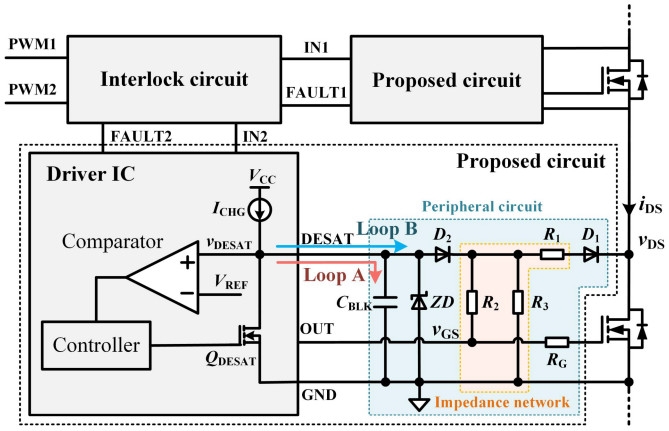


Fig. 3. Proposed hybrid desaturation detection circuit.

as a current source circuit and has the same flexibility as a voltage source circuit. It has a linear blanking capacitor charging rate and a flexibly adjustable relationship between the device terminal voltage and the detection voltage. Comparisons between the proposed circuit and existing circuits are listed in Tables II and III. On the one hand, it allows simple fine-tuning of the detection threshold to adapt to different application requirements. The margin for the current peak can be reduced to speed up detection. On the other hand, it can also accelerate the detection speed of FUL without configuring additional circuits separately. Based on the above two aspects, fast detection of two types of SC faults in the bridge leg can be achieved simultaneously.

II. Proposed Detection Circuit

The topology of the proposed desaturation fast detection circuit using a SiC MOSFET as the object is shown in Fig. 3. Compared with conventional current source circuits, this proposed circuit requires the addition of two resistors (R_2 and R_3) and a diode (D_2), R_2 and R_3 are connected to the G and S poles, respectively, to make the circuit have voltage source circuit characteristics. The addition of D_2 makes C_{BLK} only have a current source as the charging source. Therefore, the proposed circuit has the characteristics of simple configuration of the current source circuit and high flexibility of the voltage source circuit.

The trigger condition for the SC fault signal is that the detection voltage v_{DESAT} of the DESAT pin is higher than the reference voltage V_{REF}. Zener diode ZD is connected in parallel with C_{BLK} to prevent it from overvoltage. When the SiC MOSFET is turned ON, the switch Q_{DESAT} is turned OFF to enable the desaturation detection function. When the SiC MOSFET is turned OFF, the switch Q_{DESAT} is turned ON to disable the desaturation detection function to avoid false triggering. The blanking capacitor C_{BLK} and the charging current source I_{CHG} jointly determine the charging rate of v_{DESAT} and the blanking time T_{BLK}.

The basic principle of desaturation detection is to establish a mapping between v_{DS} and v_{DESAT}, and indirectly realize the detection of i_{DS} through the volt-ampere characteristic curve of the device.

Under steady-state conditions, I_{CHG} flows through loop B. Through the superposition theorem, the contributions of v_{DS}, I_{CHG}, gate turn-ON voltage V_{G}, and diode voltage drops V_{D1} and V_{D2} to v_{DESAT} can be obtained. The relationship between v_{DS} and v_{DESAT} can be expressed as as (1) where G_1, G_2, and G_3 represent the conductances of R_1, R_2, and R_3, respectively

$$G_1 = \frac{1}{R_1}, G_2 = \frac{1}{R_2}, G_3 = \frac{1}{R_3}. \tag{2}$$

It can be seen from (1) shown at the bottom of this page, that the maximum value of v_{DESAT} is $V_{D2} + V_{\mathrm{G}}\frac{G_2}{G_2+G_3} + \frac{I_{\mathrm{CHG}}}{G_2+G_3}$. In order to trigger the SC fault signal, $V_{D2} + V_{\mathrm{G}}\frac{G_2}{G_2+G_3} + \frac{I_{\mathrm{CHG}}}{G_2+G_3}$ needs to be greater than V_{REF}, and D_2 is always turned ON before the SC fault signal is triggered in the circuit

$$V_{D2} + V_{\mathrm{G}}\frac{G_2}{G_2+G_3} + \frac{I_{\mathrm{CHG}}}{G_2+G_3} > V_{\mathrm{REF}}. \tag{3}$$

Rewrite the relationship between v_{DESAT} and v_{DS} when D_2 is turned ON as $v_{\mathrm{DESAT}} = kv_{\mathrm{DS}} + V_B$, then

$$V_{\mathrm{B}} = V_{D2} + \frac{V_{D1}G_1 + V_{\mathrm{G}}G_2 + I_{\mathrm{CHG}}}{G_1+G_2+G_3}, k = \frac{G_1}{G_1+G_2+G_3}. \tag{4}$$

There will be a transient process before entering the steady state. The circuit waveform of the normal conduction transient state of the device is shown in Fig. 4. When the SiC MOSFET is turned ON at t_1, v_{DESAT} is 0 at the beginning. Therefore, D_2 is reversely blocked and the I_{CHG} current flows through loop A. v_{DESAT} continues to rise at a rate of $I_{\mathrm{CHG}}/C_{\mathrm{BLK}}$ while v_{DS} continues to decrease. Until$v_{\mathrm{DESAT}} = kv_{\mathrm{DS}} + V_{\mathrm{B}} - \frac{I_{\mathrm{CHG}}}{G_1+G_2+G_3}$ at t_2, the circuit begins the commutation process. The current flows through loops A and B at the same time. When v_{DESAT} rises to $kv_{\mathrm{DS}}+V_{\mathrm{B}}$ at t_3, commutation is completed and the steady state of current flowing only through loop B is reached. The expression of v_{DESAT} in the commutation process is $v_{\mathrm{DESAT}} = kv_{\mathrm{DS}} + V_{D2} + \frac{I_{\mathrm{CHG}}}{G_1+G_2+G_3}(1 - e^{-\frac{t(G_1+G_2+G_3)}{C}})$. It can be seen that the voltage rise rate is less than $I_{\mathrm{CHG}}/C_{\mathrm{BLK}}$. This will delay the protection detection time of the circuit, so the $\frac{I_{\mathrm{CHG}}}{G_1+G_2+G_3}$ component should be controlled very small so that the commutation process can be ignored.

In the steady state (loop B), (1) indicates that the proposed circuit can flexibly adjust the mapping relationship between v_{DS}

$$v_{\mathrm{DESAT}} = \begin{cases} V_{D2} + (v_{\mathrm{DS}} + V_{D1})\frac{G_1}{G_1+G_2+G_3} + V_{\mathrm{G}}\frac{G_2}{G_1+G_2+G_3} + \frac{I_{\mathrm{CHG}}}{G_1+G_2+G_3} \\ (v_{DS} < V_{D2} + V_{\mathrm{G}}\frac{G_2}{G_2+G_3} + \frac{I_{\mathrm{CHG}}}{G_2+G_3}, D_1 \text{ is forward conducting}) \\ V_{D2} + V_{\mathrm{G}}\frac{G_2}{G_2+G_3} + \frac{I_{\mathrm{CHG}}}{G_2+G_3} \\ (v_{DS} \geq V_{D2} + V_{\mathrm{G}}\frac{G_2}{G_2+G_3} + \frac{I_{\mathrm{CHG}}}{G_2+G_3}, D_1 \text{ is reverse blocking}) \end{cases} \tag{1}$$

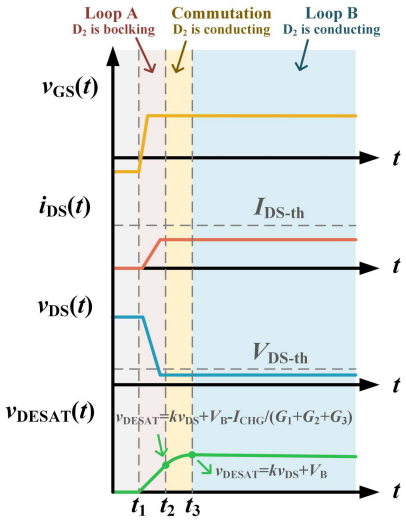


Fig. 4. Normal conduction transient waveform.

and v_{DESAT} by configuring the impedance network composed of R_1, R_2, and R_3. This shows the most fundamental distinction from conventional circuits. Specifically, the values of k and V_{B} in conventional current source circuits are determined as follows:

$$V_{\mathrm{B}} = V_{D1} + \frac{I_{\mathrm{CHG}}}{G_1}, k = 1. \tag{5}$$

Ignoring the I_{CHG}/G_1 component, which is typically controlled to be very small to shorten the current commutation process, the mapping relationship between v_{DS} and v_{DESAT} in conventional current source circuits is fixed and cannot be flexibly adjusted. In contrast, the proposed hybrid circuit provides greater flexibility while retaining the advantages of current source circuits, which brings interesting advantages at the application level. The fast detection of both the phase SC and shoot-through SC in the bridge leg can thus be achieved.

III. Fast SC Detection for Bridge Leg

A. Lower Detection Threshold for Phase SC

When phase SC occurs in the bridge leg, the fault current rise rate is relatively slow. As depicted in Fig. 5(a), after a short transient state (t_1) when the SiC MOSFET is turned ON, v_{DESAT} will continually track the variation of v_{DS} according to (1). When v_{DESAT} reaches V_{REF}, the fault signal will be triggered, turning OFF the device after a short chip delay (t_{d}). The corresponding V_{DSth} is calculated as follows:

$$V_{\mathrm{DSth}} = \frac{V_{\mathrm{REF}} - V_{\mathrm{B}}}{k}. \tag{6}$$

To simplify the calculation, components generated by V_{D1}, V_{D2}, and I_{CHG}, which account for a low proportion in V_{B}, are ignored

$$V_{\mathrm{B}} = V_{\mathrm{G}} \frac{\mathrm{G}_2}{G_1 + G_2 + G_3}, \quad V_{\mathrm{G}} \frac{G_2}{G_2 + G_3} > V_{\mathrm{REF}}. \tag{7}$$

Then, V_{DSth} can be expressed as

$$V_{\mathrm{DSth}} = V_{\mathrm{REF}} - (V_{\mathrm{G}} - V_{\mathrm{REF}}) \frac{G_2}{G_1} + V_{\mathrm{REF}} \frac{G_3}{G_1}. \tag{8}$$

By substituting the inequality in (7), it can be seen that

$$V_{\mathrm{DSth}} < V_{\mathrm{REF}}. \tag{9}$$

This illustrates the high flexibility of the V_{DSth} value. V_{DSth} can be adjusted simply by changing the resistance of the impedance network. Setting an appropriate smaller value to make the corresponding i_{DS} close to the rated value can shorten the duration of SC and reduce the peak current value.

B. Short FUL Detection Delay for Shoot-Through SC

When handling shoot-through SC, it is crucial for the protection circuit to rapidly detect and clear the fault to prevent the device from being damaged by the rapidly increasing current. However, even though the device is turned ON during the normal conduction transient, v_{DS} still needs a period to drop from the bus voltage, which may cause the desaturation circuit to be falsely triggered. In order to distinguish between the normal turn-ON transient state and HSF state, the circuit needs an appropriate C_{BLK} to limit the rising rate of v_{DESAT}, which has a negative impact on detection speed. T_{BLK} represents the time for v_{DESAT} to rise from 0 to V_{REF} when I_{CHG} flows through Loop A

$$T_{\mathrm{BLK}} = \frac{C_{\mathrm{BLK}} V_{\mathrm{REF}}}{I_{\mathrm{CHG}}}. \tag{10}$$

In order to avoid false triggering, T_{BLK} should exceed the drop time of v_{DS} from the bus voltage to V_{DSth} during the normal conduction transient. This time is related to many factors, such as switch device characteristics, temperature, and bus voltage. The specific value of T_{BLK} should consider both reliability and speed.

As shown in Fig. 1(b), when shoot-through SC occurs in the bridge leg, the SiC MOSFET initially turned on will be in the FUL state, and the SiC MOSFET that is short-circuited because of its turn-ON action will be in the HSF state. Fig. 5(b) and (c) shows the timing diagram of the proposed circuit that detects these two states, respectively.

Under HSF state, the fault signal is triggered when v_{DESAT} rises to V_{REF} after T_{BLK}. For FUL, the rising rate is limited by C_{BLK}, resulting in a delay in detection even though it does not need to be distinguished from the turn-ON transient state

$$T_{\mathrm{delay}} = \frac{C_{\mathrm{BLK}}(V_{\mathrm{REF}} - kV_{\mathrm{DS-on}} - V_{\mathrm{B}})}{I_{\mathrm{CHG}}} \tag{11}$$

where $V_{\mathrm{DS\text{-}on}}$ represents the voltage drop of the SiC MOSFET before the SC fault. Considering the worst case that $V_{\mathrm{DS\text{-}on}}$ is 0

$$T_{\mathrm{delay}} = \frac{C_{\mathrm{BLK}}(V_{\mathrm{REF}} - V_{\mathrm{B}})}{I_{\mathrm{CHG}}} \tag{12}$$

Unlike T_{BLK}, T_{delay} has no theoretical minimum limit. The optimal T_{delay} should be as small as possible while ensuring anti-noise performance. However, the fixed small V_B value in the conventional detection circuit causes T_{delay} to be close to T_{BLK}, and the fast detection potential of FUL is not fully realized. The

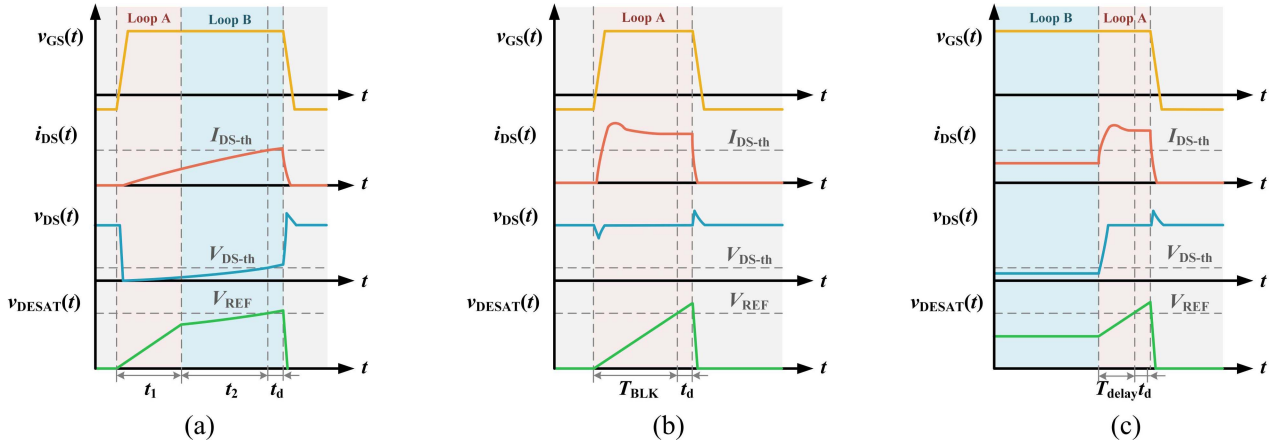


Fig. 5. Timing diagram for processing different states. (a) Phase SC. (b) HSF under shoot-through SC. (c) FUL under shoot-through SC.

proposed circuit can flexibly adjust V_B through the impedance network to achieve the decoupling of Tdelay and T_{BLK} settings. By adjusting the initial value of v_{DESAT} in the steady state (loop B) before FUL, a shorter T_{delay} is achieved for fast FUL detection.

Although it is infeasible to determine the specific SC states of the two SiC MOSFETs in one bridge leg before shoot-through SC occurs, it is certain that one SiC MOSFET is in HSF state and the other is in FUL state. Fast detection of FUL state enables prompt protection of the entire bridge leg. To practically implement this protection mechanism, an additional set of the interlock circuit is included to enable the removal of the entire bridge leg whenever FUL can be fast detected. There are also bridge dual-channel driver chips that integrate the interlocking function inside the chip.

C. Limitations Between V_B and V_{DSth} Settings

It can be seen from the above analysis that the proposed circuit has a beneficial effect on the fast detection of phase SC and shoot-through SC of the bridge leg. Although the impedance network enables the flexible configuration of both V_{B} and V_{DSth}, not all combinations of the two are available. It can be seen from (9) that V_{DSth} can only take a value below V_{REF}. In addition, according to (6) and (7), the limiting relationship between V_{B} and V_{DSth} can be obtained

$$V_{\mathrm{B}}V_{\mathrm{DSth}} \le V_{\mathrm{G}}(V_{\mathrm{B}} + V_{\mathrm{DSth}} - V_{\mathrm{REF}}). \tag{13}$$

Fig. 6 illustrates the range of values for one parameter of V_{B} and V_{DSth} when the other parameter is fixed.

D. Impact of dv_{DS}/dt on FUL Detection

When a FUL fault occurs in a conventional circuit or the proposed circuit, the original forward conducting diode D_1 will be blocked due to the rapid rise of v_{DS}. As shown in Fig. 7, high $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ will generate displacement current through the parasitic parameters of the circuit and interfere with v_{DESAT}, causing the actual detection time to deviate from the theoretical calculation time. In severe cases, it may even cause false triggering.

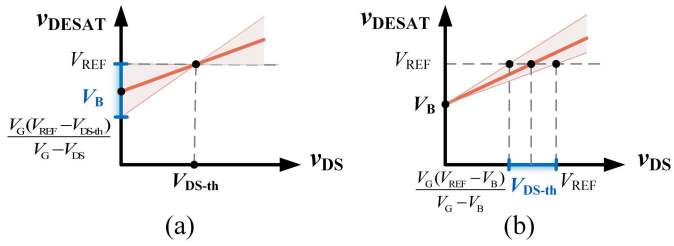


Fig. 6. (a) Value range of V_{B} when V_{DSth} is fixed. (b) Value range of V_{DSth} when V_{B} is fixed.

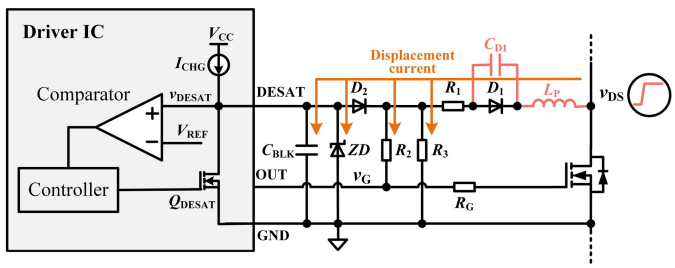


Fig. 7. Displacement current caused by $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ in the proposed detection circuit.

At present, there is still no quantitative systematic analysis of the noise generated by parasitic parameters, which is still a hot spot in current research [21], [22]. The most closely-related parameters to the displacement capacitance are the parasitic capacitance C_{D1} of D_1 and the parasitic inductance L_{p} of the circuit. Usually, multiple fast recovery diodes can be connected in series as D_1 to reduce their influence.

IV. Experimental Results

In order to verify the fast protection performance of the proposed hybrid circuit, a bridge leg SC fault test platform as shown in Fig. 8 was built. The Infineon 1ED3321MC12N gate driver IC was chosen, with a desaturation function current source of 500 μA and a trigger level of 9 V. IMZ120R140M1H

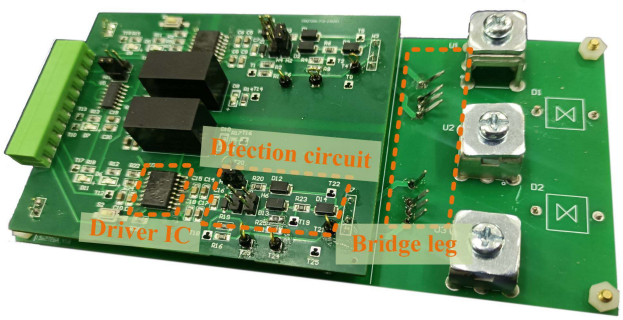


Fig. 8. Bridge leg SC detection platform.

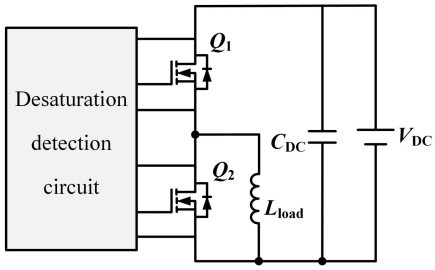


Fig. 9. Bridge leg SC test circuit topology.

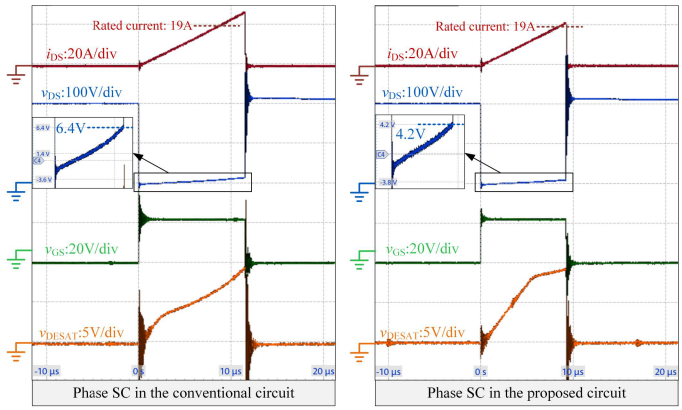


Fig. 10. Phase SC detection results.

TABLE IV
PHASE SC EXPERIMENTAL RESULTS.

Topology	Threshold	Current peak	Current exceeding the rated value	SC duration
Conventional circuit	6.4 V	26.49 A	39.5%	11.7 µs
Proposed hybrid circuit	4.2 V	21.2 A	11.6%	9.2 µs

SiC MOSFETs with a rated current of 19 A were used as test devices. The turn-ON voltage V_G of the drive circuit is 16 V. The designed PCB has two types of desaturation peripheral circuits, the conventional current source circuit and the proposed hybrid circuit, which can be easily switched.

The main purpose of the circuit proposed in this article is not to pursue absolutely fast detection at the expense of noise immunity for specific applications, but to improve the conventional circuit at a small cost to achieve faster detection with the same blanking time. So for a fair comparison, both circuits take the same blanking capacitor value of 220 pF. In the conventional current source circuit, R_1 is selected as 1 kΩ. D_1 is composed of four fast recovery diodes connected in series, with a total conduction voltage drop of 2.38 V. When selecting the proposed hybrid circuit parameters, many factors should be considered comprehensively, including the rapidity, noise immunity, SC withstand ability, etc. A suitable set of parameters is chosen as a particular case to verify the capability of the proposed circuit, with 2.7 kΩ for R_1 and R_2, and 4.7 kΩ for R_3. The conduction voltage drops of D_1 and D_2 are 0.76 and 0.33 V, respectively.

A. Bridge Leg Phase SC Rapid Detection Experiment

Phase SC can be divided into two types: those caused by the SiC MOSFET turn-ON action and those caused by the external load action. Compared with the latter, the former will have a conduction transient process before entering the steady state and tracking v_{DS} changes according to (1). So it is more representative and is used for testing in this chapter. The test circuit to simulate phase SC fault is shown in Fig. 9. The loop inductance in phase SC is mainly determined by the load side, and it has a large value range. In this particular case, the loop inductance is set to about 43.25 μH. The bus voltage is set to 100 V. The upper SiC MOSFET in the bridge leg is used as the test object. The V_{DSth} in the two circuits are 6.12 and 4.08 V, respectively.

The test waveform is shown in Fig. 10, and the results are listed in Table IV. As the upper SiC MOSFET turns ON at t = 0 s, the i_{DS} and v_{DS} of the SiC MOSFET begin to rise. When v_{DS} reaches the threshold, the SC fault is detected and the SiC MOSFET is turned OFF. The errors between the actual value and the theoretically calculated value of V_{DSth} for the conventional circuit and the proposed circuit are only 4.58% and 2.94%, respectively. The peak current of the conventional circuit exceeds the rated value by 39.5%, while in the proposed circuit it is only 11.6%. Furthermore, The SC duration of the proposed circuit is 21.4% shorter than that of the conventional circuit.

Experimental results show that the phase SC detection threshold can be flexibly predetermined near the rated current value through the proposed hybrid circuit. It can reduce the peak current and shorten the SC duration. The proposed circuit can be better suitable for threshold-sensitive situations.

B. Bridge Leg Shoot-Through SC Rapid Detection Experiment

The circuit topology shown in Fig. 9 is also used to simulate the bridge leg shoot-through SC fault. After the lower SiC MOSFET is completely turned ON, the shoot-through SC is created by turning ON the upper SiC MOSFET. At this time, the upper and lower SiC MOSFETs are in the HSF and FUL states, respectively. The theoretical T_{delay} of the two circuits in this special case can be calculated from (10) to be 2.69 and 1.19 μs, respectively. Experiments were conducted under four bus voltages of 100, 200, 400, and 600 V. The experimental waveforms are shown in Fig. 11. Experimental data are listed in Table V.

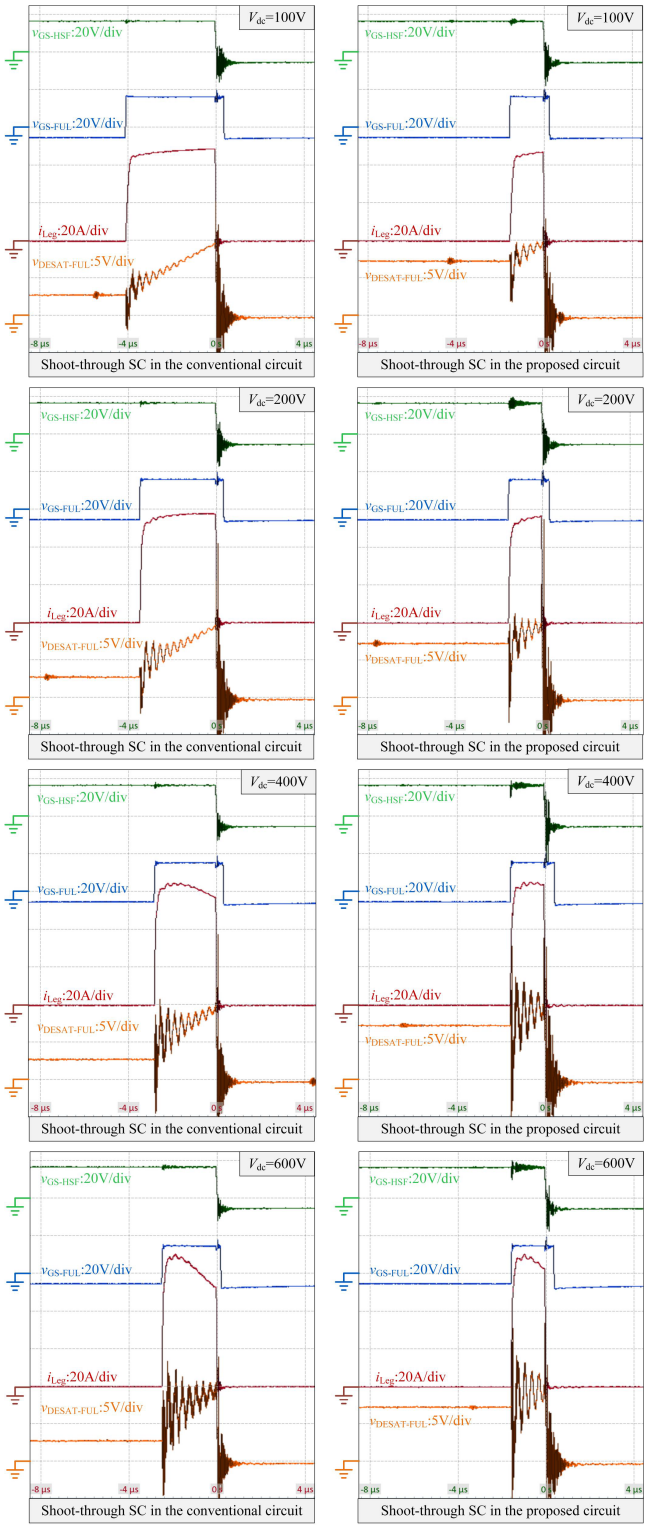


Fig. 11. Shoot-through SC detection test results.

It can be seen from the experimental waveform that when the upper SiC MOSFET is turned ON, the bridge leg current quickly rises to the saturation value. Since the v_{DESAT} of the proposed circuit has a larger initial level, it can reach V_{REF} in a shorter time, which can effectively shorten the detection time of the shoot-through SC fault. Since the time T_{delay} for detecting the FUL state is less than the blanking time T_{BLK} for detecting HSF, the lower SiC MOSFET will detect the fault signal first, and then the interlock circuit will quickly turn off the upper SiC MOSFET within 300 ns to realize the fast protective cutoff of the entire bridge leg.

TABLE V
SHOOT-THROUGH SC EXPERIMENTAL RESULTS

Bus voltage	Conventional circuit		Proposed circuit		Duration reduction
	SC duration	Error with calculation	SC duration	Error with calculation	
100 V	4.00 µs	48.7%	1.46 µs	22.7%	63.5%
200 V	3.42 µs	27.1%	1.48 µs	24.4%	56.7%
400 V	2.77 µs	3.0%	1.51 µs	26.9%	45.5%
600 V	2.45 µs	8.9%	1.51 µs	26.9%	38.4%

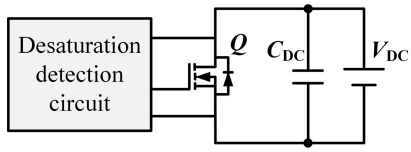


Fig. 12. Single device HSF test circuit topology.

Under the bus voltage of 100 V, the SC duration of the proposed hybrid circuit can be shortened by 63.5% compared with the current source circuit with the same blanking time. In addition, as the bus voltage increases, the noise impact of the displacement current caused by high $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ becomes more obvious. When the bus voltage is 600 V, the SC duration of the proposed hybrid circuit can be shortened by 38.4%. The error between experimental results and theory mainly comes from the parasitic parameters of the circuit. Experimental results show that compared with the current source detection circuit, the proposed hybrid detection circuit can achieve fast detection of the bridge leg shoot-through SC by shortening the detection time of FUL.

C. Comparison of HSF Noise Immunity of Single Device

The main source of circuit noise comes from high $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ during device short circuits or normal switching transients. For the detection of FUL faults, the v_{DESAT} value of the proposed circuit will be higher than that of the conventional current source circuit before SC, which will speed up the detection of FUL status, but will also weaken the noise immunity of the circuit. However, in the FUL state, the device has been fully turned ON, and the weakening of noise immunity will not have a significant impact at this time. However, the detection of HSF needs to be distinguished from the normal turn-ON transient, which may cause false triggering due to the high $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ of the normal turn-ON transient, so it has higher requirements for noise immunity.

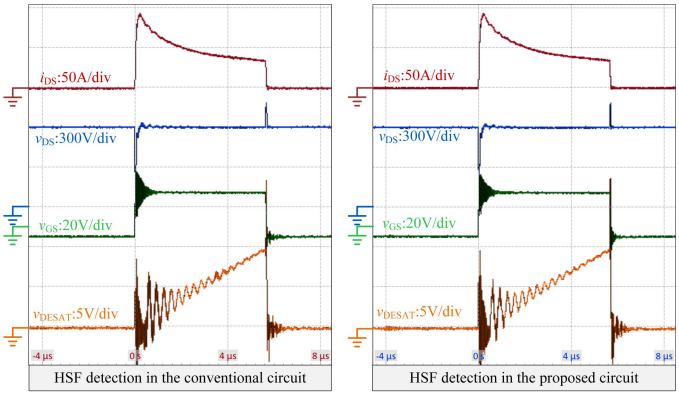


Fig. 13. HSF detection test results.

The circuit topology shown in Fig. 12 is applied to test the HSF detection noise immunity of the conventional current source detection circuit and the hybrid detection circuit proposed in this article. Turning ON the SiC MOSFET when the bus voltage is 600 V generates HSF. The experimental waveform is shown in Fig. 13. It can be seen that the v_{DESAT} waveforms of both circuits are basically the same, and the proposed circuit does not deteriorate the noise immunity of HSF.

V. Conclusion

This article proposes a hybrid desaturation detection circuit, which can be applied to the bridge leg of semiconductor devices to achieve fast SC detection and protection. This circuit has the following advantages.

1) The proposed hybrid desaturation circuit not only has the convenience to calculate and set the blanking time as the current source detection circuit, but also has the same flexible adjustability as the voltage source detection circuit. The proposed circuit can simply and flexibly set the mapping relationship between the detection voltage and the device terminal voltage through the impedance network.
2) For the phase SC of the bridge leg, the proposed circuit can simply set the detection threshold close to the maximum operating current, thereby reducing the peak current and duration of phase SC.
3) The proposed circuit can decouple the detection speed configuration of HSF and FUL without adding additional detection circuits. Therefore, it can accelerate the detection of FUL, without shortening the blanking time of HSF. The rapid FUL detection enables rapid protection of the whole bridge leg.

Experiments show that for two kinds of bridge leg SC faults, the proposed circuit can achieve faster detection and protection, compared with the current source detection circuit with the same blanking time, and there is no obvious deterioration in noise immunity.

Experiments show that compared with the widely-used current source detection circuit with the same blanking time, the proposed circuit can achieve faster SC fault detection and protection of the bridge leg under both phase SC and shoot-through SC.

The proposed circuit has flexible SC protection adjustment capability and a simple circuit structure, which indicates its great potential in WBG devices.

References

[1] H. Qin et al., "A comprehensive study of the short-circuit characteristics of SiC MOSFETs," in *Proc. IEEE 12th Conf. Ind. Electron. Appl.*, 2017, pp. 332–336.
[2] D. Xing et al., "1200-V SiC MOSFET short-circuit ruggedness evaluation and methods to improve withstand time," in *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5059–5069, Oct. 2022.
[3] W. Yang et al., "Overview of SiC MOSFET short circuit protection technology," *Trans. China Electrotechnical Soc.*, vol. 37, no. 10: pp. 2538–2548, 2022.
[4] J. C. Iglesias-Rojas, E. Velázquez-Lozada, and R. Baca-Arroyo, "Online failure diagnostic in full-bridge module for optimum setup of an IGBT-based multilevel inverter" energies," vol. 15, no. 14, 2022, Art. no. 5203.
[5] R. Miftakhutdinov, X. Li, R. Mukhopadhyay, and G. Wang, "How to protect SiC FETs from short circuit faults-overview," in *Proc. 20th Eur. Conf. Power Electron. Appl. (EPE'18 ECCE Europe)*, 2018, pp. 1–10.
[6] K. Sun, J. Wang, R. Burgos, and D. Boroyevich, "Design, analysis, and discussion of short circuit and overload gate-driver dual-protection scheme for 1.2-kV, 400-A SiC MOSFET modules," in *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3054–3068, Mar. 2020.
[7] K. Ghosh, S. S. S., D. S., K. Hatua, and A. Mitra, "Design of a parasitic inductance based shoot-through protection scheme for SiC MOSFET gate driver," in *Proc. IEEE 1st Ind. Electron. Soc. Annu. -Line Conf.*, 2022 pp. 1–6.
[8] S. Yano, Y. Nakamatsu, T. Horiguchi, and S. Soda, "Development and verification of protection circuit for hard switching fault of SiC MOSFET by using gate-source voltage and gate charge," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019 pp. 6661–6665.
[9] T. Horiguchi, S. -i. Kinouchi, Y. Nakayama, and H. Akagi, "A fast short-circuit protection method using gate charge characteristics of SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 4759–4764.
[10] X. Li, D. Xu, H. Zhu, X. Cheng, Y. Yu, and W. T. Ng, "Indirect IGBT over-current detection technique via gate voltage monitoring and analysis," in *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3615–3622, Apr. 2019.
[11] S. Mocevic et al., "Comparison and discussion on shortcircuit protections for silicon-carbide MOSFET modules: Desaturation versus Rogowski switch-current sensor," in *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2880–2893, May–Jun. 2020.
[12] J. Wang, Z. Shen, R. Burgos, and D. Boroyevich, "Design of a high-bandwidth Rogowski current sensor for gate-drive shortcircuit protection of 1.7 kV SiC MOSFET power modules," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, 2015, pp. 104–107.
[13] S. Ji et al., "Short-circuit characterization and protection of 10-kV SiC mosfet," in *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1755–1764, Feb. 2019.
[14] X. Huang et al., "A robust 10 kV SiC MOSFET gate driver with fast overcurrent protection demonstrated in a MMC submodule," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 1813–1820.
[15] R. Graves, A. Lemmon, and L. Gant, "Fast, configurable over-current protection for high-power modules," in *Proc. IEEE Electric Ship Technol. Symp.*, 2015, pp. 332–336.
[16] B. Wittig, M. Boettcher, and F. W. Fuchs, "Analysis and design aspects of a desaturation detection circuit for low voltage power MOSFETs," in *Proc. 14th Int. Power Electron. Motion Control Conf. EPE-PEMC 2010*, 2010, pp. T1–T7–T1–12.
[17] S. Mocevic et al., "Comparison between desaturation sensing and Rogowski coil current sensing for shortcircuit protection of 1.2 kV, 300 A SiC MOSFET module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2666–2672.
[18] T. Bertelshofer, A. Maerz, and M. Bakran, "Design rules to adapt the desaturation detection for SiC MOSFET modules," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2017, pp. 1–8.

[19] Q. Wang, F. Iannuzzo, J. Zhang, Y. Jiang, and F. He, "Improved drain-source voltage detection method for short-circuit protection of SiC MOSFET," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, 2022 pp. 1–4.
[20] Q. Wang, J. Zhang, F. Iannuzzo, Y. Jiang, W. Zhang, and F. He, "Short-circuit fault Adaptive analysis and protection for SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 5, pp. 4867–4881, Oct. 2023.
[21] X. Huang et al., "Comprehensive analysis and improvement methods of noise immunity of desat protection for high voltage SiC MOSFETs with high DV/DT," in *IEEE Open J. Power Electron.*, vol. 3, pp. 36–50, 2021.
[22] S.-S. Min and R.-Y. Kim, "Improved gate-voltage-driven desaturation short-circuit protection circuit with robust switching noise immunity for WBG power semiconductors," in *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 2535–2544, Jun. 2023.

Zicheng Liu (Senior Member, IEEE) received the B.S. degree in hydropower engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2011, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2016.

During 2014 to 2015, he was a Visiting Student with Purdue University, West Lafayette, IN, USA. During 2016 to 2018, he was a Postdoc Researcher with Beijing Jiaotong University, Beijing. He is currently an Associate Professor with HUST. His research interests include multiphase motor control systems and transportation electrification.

Dr. Liu was the recipient of the best letter award of IEEE TRANSACTIONS ON POWER ELECTRONICS, the second-place prize paper award of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and three prize paper awards in IEEE conferences. He is the Vice Chair of IEEE Power Electronics Society Wuhan Chapter.

Jiewei He (Student Member, IEEE) was born in Nanchong, China, in 2001. He received the B.S. degree in hydraulic and hydropower engineering in 2022 from the Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include converter short-circuit fault detection and fault-tolerant control issues.

Dong Jiang (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2005 and 2007, respectively, and the Ph.D. degree in power electronics and motor drives from the University of Tennessee, Knoxville, TN, USA, in 2011.

From January 2012 to July 2015, he was with the United Technologies Research Center, East Hartford, CT, USA, as a Senior Research Scientist/Engineer. Since July 2015, he has been with the Huazhong University of Science and Technology, Wuhan, China, as a Professor. He has authored or coauthored more than 200 published IEEE journal and conference papers and more than 70 granted patents in his research fields. His research interests include power electronics and motor drives.

Dr. Jiang is an Associate Editor for IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He was the recipient of several best paper awards in IEEE conferences. He is the Chair of IEEE PELS Wuhan Chapter.

Xiangwen Sun (Student Member, IEEE) was born in Hubei, China, in 1997. He received the B.S. degree in electrical engineering in 2019 from the Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electronic and Electrical Engineering.

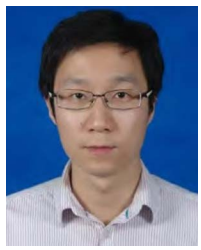
His research interests include inverter topology and control of multiphase machines.

Guang Yang received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, the other one from the University of Birmingham, Birmingham, U.K., in 2011, and the M.S. degree in electrical and electronic engineering from the University of Southampton, Southampton, U.K., in 2013.

He is currently working in AVIC Xi'an Flight Automatic Control Research Institute, Xi'an, China. His main research directions include actuator control and ac motor drive.

Hongyang Liu received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2011, and the M.S degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2014.

He is currently working in AVIC Xi'an Flight Automatic Control Research Institute, Xi'an, China. His main research directions include actuator control and ac motor drive.



Peng Li received the B.S. and M.S. degree in automatization engineering from the Department of Electrotechnical Theory and New Technology, Huazhong University of Science and Technology, Wuhan, China, in 2011.

He is currently working with Wuhan Second Ship Design and Research Institute, Wuhan. His research interests include the control of PMSM and health management of electric drive system.

Ronghai Qu (Fellow, IEEE) was born in China. He received the B.E.E. and M.S.E.E. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1993, 1996, respectively, and the Ph.D. degree in electrical engineering from the University of Wisconsin– Madison, Madison, WI, USA, in 2002.

Dr. Qu is a Full Member of Sigma Xi. He was the recipient of several awards from the GE Global Research Center since 2003, including the Technical Achievement and Management Awards, the 2003 and 2005 Best Paper Awards, and the third prize, from the Electric Machines Committee of the IEEE Industry Applications Society (IAS) at the 2002 and 2004 IAS Annual Meeting, respectively.