Novel Carrier Redistribution Pulsewidth Modulation and Active Voltage Balancing for Five-Level SM Converter With Low-Frequency Voltage Ripple Suppression

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***Abstract*—This study proposes a novel carrier redistribution pulsewidth modulation (CRPWM) technique and its associated active voltage balancing method with low-frequency voltage ripple suppression for the five-level stacked multicell (SM) converter. While CRPWM offers simplicity and ease of implementation with optimal harmonics, it encounters significant neutral point (NP) voltage imbalance issues, particularly at low power factors. NP voltage imbalance is a primary cause of low-frequency voltage ripples in dc-link capacitors. Therefore, the proposed CRPWM utilizes new switching states to minimize NP current generation and ensures the natural voltage balance of floating capacitors to minimize voltage ripples. Consequently, NP current significantly diminishes at low power factors, and unbalanced NP current is almost completely suppressed under the active voltage balancing method theoretically. The proposed CRPWM method, with lower unbalanced NP current and equivalent line voltage harmonic performance compared with other CRPWM methods, exhibits the lowest low-frequency voltage ripples with optimal output performance. Experimental results reveal about 88% and 65% reduction in low-frequency voltage ripples, and about 0.5% and 0.02% reduction in line voltage total harmonic distortion, particularly at lower power factors and highest modulation index with fundamental frequencies of 10 and 50 Hz, respectively.**

***Index Terms*—Active voltage balancing, carrier redistribution, neutral point (NP) voltage, stacked multicell (SM) converter.**

I. Introduction

MULTILEVEL converters have been extensively studied for medium- and high-voltage applications due to their favorable harmonic performance, low voltage stress across switches, and high equivalent switching frequency [1], [2], [3], [4]. Among multilevel converters, clamped converters adopt active switches or diodes to clamp the neutral point (NP) voltage, minimizing the need for capacitors on the floating side and leading to a smaller system weight and volume, particularly in high-voltage scenarios [5]. Several academically accepted clamped converters, such as neutral point clamped (NPC) converters [6], [7], active neutral-point-clamped (ANPC) converters [8], [9], hybrid clamped (HC) converters [5], [10], and stacked multicell (SM) converters [11], [12], find recommendations for industrial applications.

The SM converter, a hybrid clamped converter, comprises three-level flying-capacitor (FC) converters stacked together with NP voltage clamped by bidirectional switches. It inherits the advantages of FC converters, allowing easy expansion to high output voltage levels through cell stacking, eliminating the need for multiple independent dc power supplies, and offering various redundant switches for flexible control. In addition, it requires less energy storage in floating capacitors, significantly reducing capacitor volume and size and enhancing converter power density [13], [14], [15]. Compared with the ANPC converter, the SM converter ensures consistent switching frequencies for switching devices and greater control flexibility through diverse switching states [16]. It also eliminates high-voltage capacitors on the floating side and mitigates split capacitors in the dc-link compared with the HC converter, resulting in a smaller system size and reduced control complexity. Therefore, SM converters are highly attractive for high-voltage and high-power applications [17].

Similar to HC and ANPC converters, the SM converter encounters voltage imbalances in dc-link and floating capacitors. While capacitor voltages can be naturally balanced [18], [19], external factors, such as dead time, line impedance, and control delays can induce voltage divergence. This divergence may lead to distorted output waveforms, increased voltage stress across switches, and potential converter damage. Therefore, active voltage balancing methods are employed using defined pulsewidth modulation (PWM) to enhance the capacitor's voltage balancing performance significantly. Based on hybrid phase

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disposition and phase-shifted PWM (PD+PS PWM), diverse active voltage balancing approaches are implemented for the five-level SM converter. In [19], [20], [21], simple voltage balancing methods are proposed, involving slight adjustments in duty cycles to regulate floating capacitor voltages, while zero-sequence voltage (ZSV) is injected for NP voltage balancing. However, this approach leads to low-frequency voltage ripples in dc-link capacitors due to inadequate NP current regulation by the ZSV. To mitigate these low-frequency voltage ripples, a hybrid dual modulation voltage method is proposed [17]. This approach regulates floating capacitor voltages and NP voltage independently based on the clamping conditions of modulation voltages. However, it necessitates a higher switching frequency.

PD+PS PWM ensures the natural voltage balance of capacitors, but it inherits the PS-PWM method's drawback of increased line voltage harmonics. By contrast, PD-PWM, another widely adopted method for five-level SM converter, achieves optimal line voltage harmonic performance [22], [23], but fails to attain natural voltage balance [22]. In [24], a state machine decoder is employed to achieve active voltage balancing of capacitors with optimal modulation, avoiding the narrow switching pulses. Another approach involves the development of a cost function to balance capacitor voltages through optimal switching states in various voltage levels [23]. Similarly, fast-processing modulation and logic-form-equation approaches are also proposed in [25] and [26] to determine the optimal switching states, but both methods introduce a considerable computational burden.

Space vector PWM is recommended for the five-level SM converter [13], [16], [27], but its computational intensity and implementation complexity limit its widespread application. An alternative, carrier redistribution PWM (CRPWM), offers a simple and easily implementable approach. CRPWM inherits the pros of PS-PWM and PD-PWM, achieving natural voltage balance of capacitors and optimal line voltage harmonic performance simultaneously. Traditional CRPWM, originally proposed for the FC inverter, redistributes base carriers based on the switching sequence and phase output voltage [28]. However, this redistribution results in an uneven utilization of carriers, making conventional CRPWM more sensitive to time-varying currents and causing slight deviations in floating capacitor voltages from normal values. To mitigate voltage offset issues, a symmetric CRPWM is proposed in [29]. This approach symmetrically distributes carriers over two fundamental periods, suppressing voltage offsets of floating capacitors within every two fundamental periods. Furthermore, a modified CRPWM is proposed in [22] for the five-level SM converter, where carriers are symmetrical over every two carrier periods, almost eliminating voltage offsets.

CRPWM provides optimal harmonic performance and better voltage balance performance; however, it struggles to suppress low-frequency voltage ripples, particularly in low-power factor applications. Although dual modulation waveform PWM [17] and fast processing modulation [26] can suppress low-frequency voltage ripples for the five-level SM converter, these methods introduce heavy computational loads, the need for higher switching frequencies, and compromised harmonic performance [22]. Therefore, this study proposes a novel CRPWM and its active voltage balancing method for the five-level SM converter, focusing on low-frequency voltage ripple suppression. The proposed CRPWM maintains simplicity and ease of implementation, defining a new switching sequence for various output phase voltage levels to minimize the generation of NP current. Subsequently, the three-phase average NP current is significantly reduced, particularly at low power factors. In addition, the low-frequency voltage ripples are almost eliminated under the active voltage balancing method, enhancing harmonic performance. The rest of this article is organized as follows. Section II presents a theoretical analysis of the five-level SM converter under PS+PD PWM, traditional CRPWM, symmetric CRPWM, modified CRPWM, and proposed CRPWM, and introduces the impact of various modulation approaches on NP current. Section III analyzes the effect of active voltage balancing on NP current suppression under various modulation approaches. Sections IV and V present the simulation and experimental results, respectively. Finally, Section VI concludes this article.

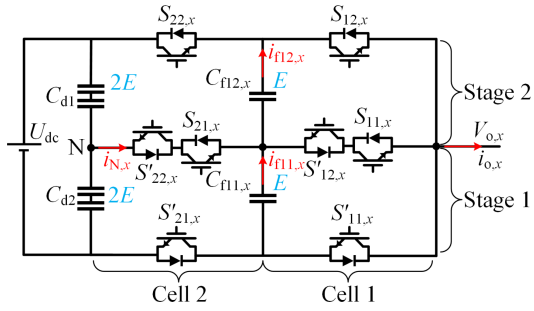

Fig. 1. Single phase circuit of the five-level SM coverter.

II. Five-Level SM Converter and Proposed CRPWM Strategy

A. Five-Level SM Coverter

The single-phase circuit of the five-level SM converter as shown in Fig. 1 comprises a stack of two cells and two stages, each featuring a complementary pair of switches and capacitors, respectively. The dc-link, shared by three phases, is split into two parts with a NP N. The output currents from capacitors $C_{f11,x}$ and $C_{f12,x}$ are denoted as $i_{f11,x}$ and $i_{f12,x}$, respectively, where the currents flowing out of N are denoted as $i_{N,x}$. The output phase current and instantaneous output phase voltage are denoted as $i_{o,x}$ and $V_{o,x}$, respectively, where x represents phase a, b, or c.

According to the operating rules of the five-level SM converter, switches $S_{11,x}$, $S_{12,x}$, $S_{21,x}$, and $S_{22,x}$ must operate in strictly complementary states corresponding to switches $S'_{11,x}$, $S'_{12,x}$, $S'_{21,x}$, and $S'_{22,x}$, respectively. Switches $S_{22,x}$ and $S'_{21,x}$ cannot be turned ON simultaneously, following the same operating rules for switches $S_{12,x}$ and $S'_{11,x}$. We assume normal voltages for the floating capacitors and dc-link capacitors as E and $2E$, respectively, with the negative terminal of the dc-link designated as the voltage zero point. The five-level SM converter can output five voltage levels: 0, E, $2E$, $3E$, and $4E$. The switching states of the five-level SM converter corresponding to the operating rules and output voltage levels are listed in Table I.

TABLE I
SWITCHING STATES OF FIVE-LEVEL SM COVERTER

$S_{22,x}$	$S_{12,x}$	$S_{21,x}$	$S_{11,x}$	$i_{\mathrm{N},x}$	$i_{\mathrm{f11},x}$	$i_{\mathrm{f12},x}$	$V_{o,x}$	switching states
1	1	1	1	0	0	0	$4E$	15
1	0	1	1	0	0	-$i_{o,x}$	$3E$	11
0	1	1	1	$i_{o,x}$	0	$i_{o,x}$	$3E$	7
1	0	1	0	0	-$i_{o,x}$	-$i_{o,x}$	$2E$	10
0	1	0	1	0	$i_{o,x}$	$i_{o,x}$	$2E$	5
0	0	1	1	$i_{o,x}$	0	0	$2E$	3
0	0	1	0	$i_{o,x}$	-$i_{o,x}$	0	E	2
0	0	0	1	0	$i_{o,x}$	0	E	1
0	0	0	0	0	0	0	0	0

Defining the switches turn ON represents 1, otherwise it represents 0. According to Table I, the relationship between the switching states and instantaneous output phase voltage level is

$$V_{o,x} = (S_{22,x} + S_{21,x} + S_{12,x} + S_{11,x}) \cdot E. \tag{1}$$

The instantaneous current flowing out of $C_{\mathrm{f11},x}$ can be expressed as

$$i_{\mathrm{f11},x} = (S_{11,x} - S_{21,x}) \cdot i_{o,x}. \tag{2}$$

Similarly, for $C_{\mathrm{f12},x}$, the instantaneous current is

$$i_{\mathrm{f12},x} = (S_{12,x} - S_{22,x}) \cdot i_{o,x}. \tag{3}$$

The instantaneous current flowing out of NP is

$$i_{\mathrm{N},x} = (S_{21,x} - S_{22,x}) \cdot i_{o,x}. \tag{4}$$

B. Traditional CRPWM for Five-Level SM Converter

The CRPWM approach involves redistributing carriers based on different output voltage levels and defined switching sequences. This approach retains the capacitor voltage natural balancing of the PS-PWM and the optimal total harmonic distortion (THD) performance of the PD-PWM for the FC converter. The five-level SM converter comprises two three-level FC converters stacked together. Therefore, the traditional CRPWM method is easily extended and applied to the five-level SM converter.

Traditional CRPWM comprises an extension of PD+PS PWM, where carriers are redistributed to optimize THD. PD+PS PWM has four carriers $C_{11,x}$, $C_{21,x}$, $C_{12,x}$, and $C_{22,x}$ as shown in Fig. 2(a), which are compared with reference modulation voltage $u_{\mathrm{r},x}$ to obtain gate signals of the corresponding switches. These carriers are phase-shifted in different cells of the five-level SM converter, while they are level-shifted in various stages.

When the carrier frequency significantly exceeds the fundamental frequency, the reference modulation voltage $u_{\mathrm{r},x}$ remains approximately invariant within a carrier period. Therefore, the duty cycles of switches can be expressed as

$$D_{11,x} = D_{21,x} = \begin{cases} 2u_{\mathrm{r},x} & (0 \le u_{\mathrm{r},x} < 1/2) \\ 1 & (1/2 \le u_{\mathrm{r},x} \le 1) \end{cases} \tag{5a}$$

$$D_{12,x} = D_{22,x} = \begin{cases} 0 & (0 \le u_{\mathrm{r},x} < 1/2) \\ 2u_{\mathrm{r},x} - 1 & (1/2 \le u_{\mathrm{r},x} \le 1) \end{cases} \tag{5b}$$

where $D_{11,x}$, $D_{21,x}$, $D_{12,x}$, $D_{22,x}$ are the duty cycles of $S_{11,x}$, $S_{21,x}$, $S_{12,x}$, $S_{22,x}$ in a carrier period.

Analogously, the output phase current $i_{o,x}$ remains constant over a carrier period. Consequently, (2) and (3) can be reformulated as average value models

$$\bar{i}_{\mathrm{f11},x} = (D_{11,x} - D_{21,x}) \cdot i_{o,x} \tag{6a}$$

$$\bar{i}_{\mathrm{f12},x} = (D_{12,x} - D_{22,x}) \cdot i_{o,x}. \tag{6b}$$

Following (5) and (6), the average values of currents flowing through floating capacitors are zero; thus, the floating capacitor voltages naturally remain balanced over a carrier cycle, enhancing the five-level SM converter's output performance. However, the PD+PS PWM approach inherits the drawbacks of the PS-PWM method, generating three adjacent voltage levels in the line voltage and resulting in increased harmonics. Therefore, the CRPWM method, an enhancement of the PD+PS method, is proposed to improve the THD performance for the five-level SM converter while preserving the voltage natural balancing characteristics of floating capacitors.

In the traditional CRPWM method Fig. 2(b), carriers $C_{11,x}$ and $C_{21,x}$ located in the [0.25, 0.5] interval are redistributed by phase-shifting $-\pi/2$ or $\pi/2$. Similarly, carriers $C_{12,x}$, $C_{22,x}$ located in the [0.75, 1] interval are phase-shifted $-\pi/2$ or $\pi/2$. The carriers undergo redistribution, but the phase shift between the two carriers remains unchanged. Therefore, the duty cycles of switches align with (5) within a carrier period, and the floating capacitor voltages can naturally balance. Due to the consistent double Fourier series results with the PD-PWM method, the traditional CRPWM method exhibits superior THD performance compared with the PD+PS PWM method. Each line voltage segment of the five-level SM converter comprises only two adjacent voltage levels.

Despite the imbalance in carrier utilization, the traditional CRPWM method introduces slight voltage deviations in the floating capacitors. Therefore, the symmetric CRPWM method is proposed to address the voltage offset issue. The carriers are symmetrical in adjacent fundamental periods as shown in Fig. 2(c), compensating for the floating capacitor voltage deviations in the last fundamental period during the next fundamental period.

While the symmetric CRPWM method enhances the balancing ability of capacitor voltages over two fundamental periods,

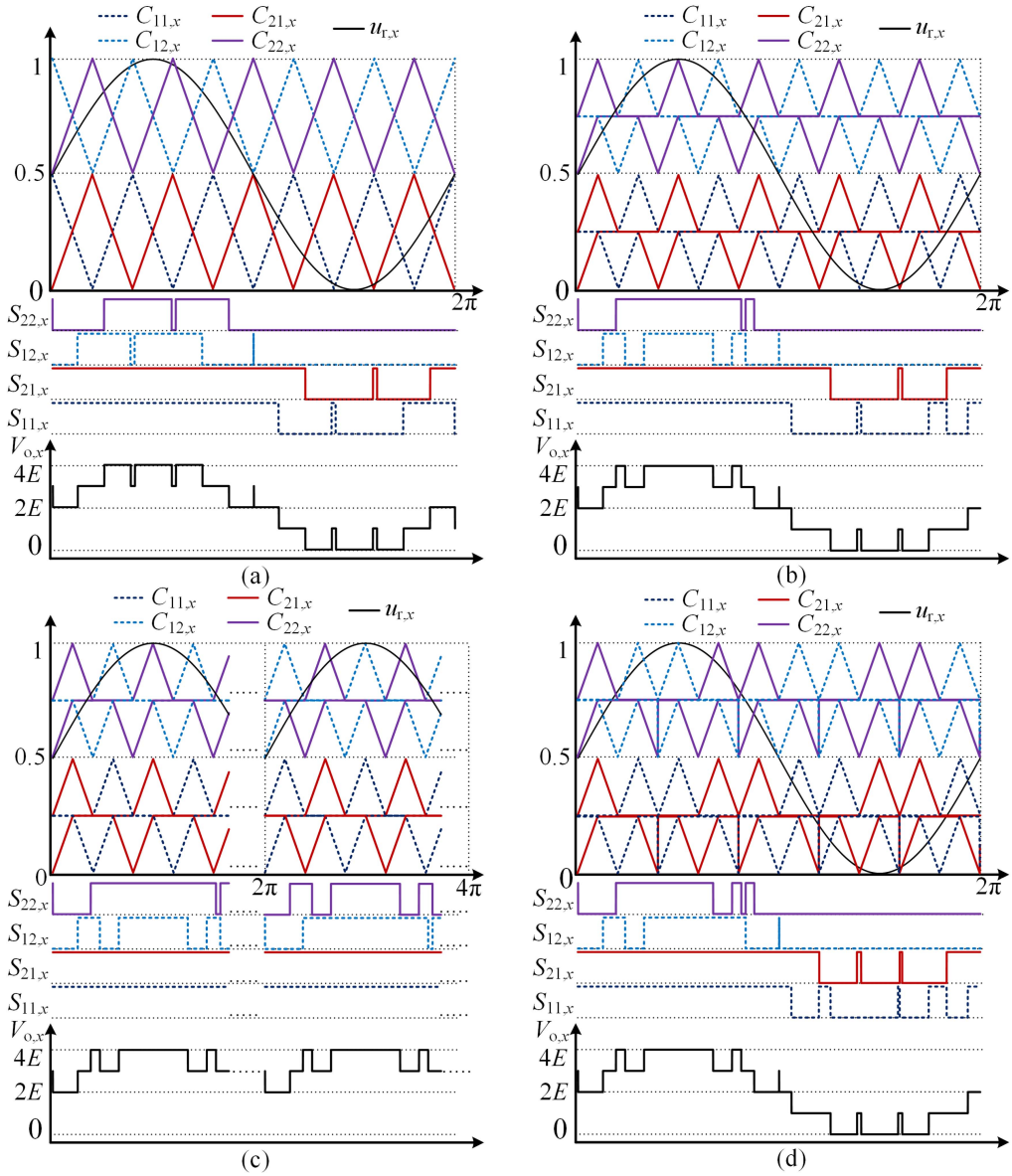

Fig. 2. PD+PS PWM and CRPWMs for five-level SM converter. (a) PD+PS PWM. (b) Traditional CRPWM. (c) Symmetric CRPWM. (d) Modified CRPWM.

a large fundamental period can lead to significant voltage ripples in the floating capacitors. To mitigate this drawback, the modified CRPWM method is introduced as shown in Fig. 2(d), where the carriers are further modified and disposed of symmetrically within every two carrier periods. Correspondingly, the minimum capacitor voltage balance period is reduced from two fundamental periods to two carrier periods, significantly enhancing the floating capacitor voltage balancing performance of the modified CRPWM method.

C. Proposed CRPWM for Five-Level SM Converter With NP Current Reduction

Among the discussed modulation approaches, the modified CRPWM method exhibits superior performance, inheriting the excellent THD performance of the PD-PWM method with the shortest floating voltage balancing period. Nevertheless, these approaches share the same switching states, differing only in their sequences. Therefore, the duty cycles of individual switches remain equal in a carrier period, expressed as (5), and the average NP current can be computed from the average value model in (4)

$$\bar{i}_{\mathrm{N},x} = (D_{21,x} - D_{22,x}) \cdot i_{o,x}. \tag{7}$$

Combining (5) and (7), the average NP current can be expressed as

$$\bar{i}_{\mathrm{N},x} = \begin{cases} 2u_{\mathrm{r},x} \cdot i_{o,x} & (0 \le u_{\mathrm{r},x} < 1/2) \\ (2 - 2u_{\mathrm{r},x}) \cdot i_{o,x} & (1/2 \le u_{\mathrm{r},x} \le 1) \end{cases}. \tag{8}$$

Following (8), the PD+PS PWM and CRPWM methods generate NP current, leading to NP voltage imbalance. However, the five-level SM converter employs active switches to clamp NP to

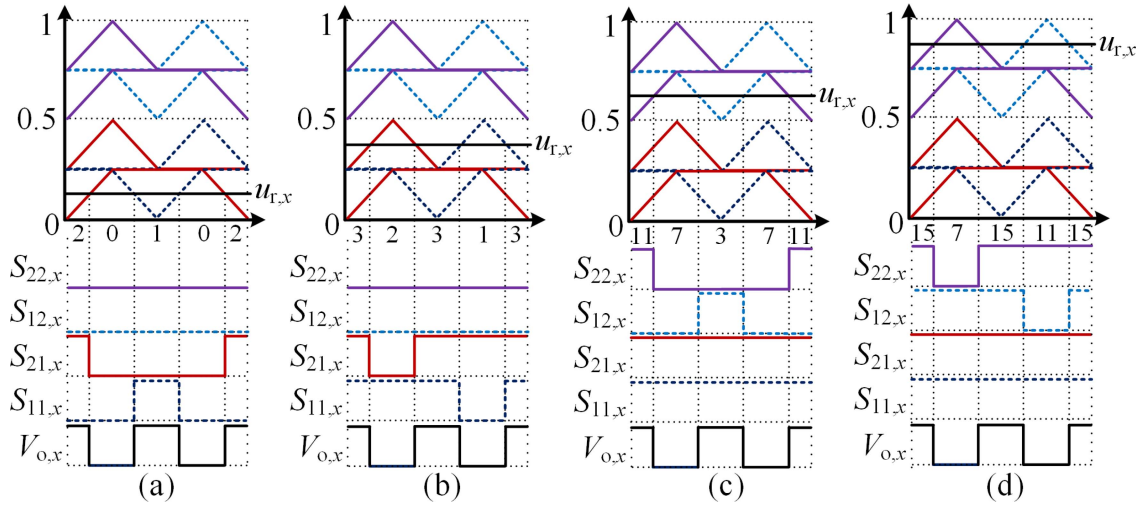

Fig. 3. Pulse models of modified CRPWM method. (a) $0 \le u_{r,x} < 1/4$. (b) $1/4 \le u_{r,x} < 1/2$. (c) $1/2 \le u_{r,x} < 3/4$. (d) $3/4 \le u_{r,x} \le 1$.

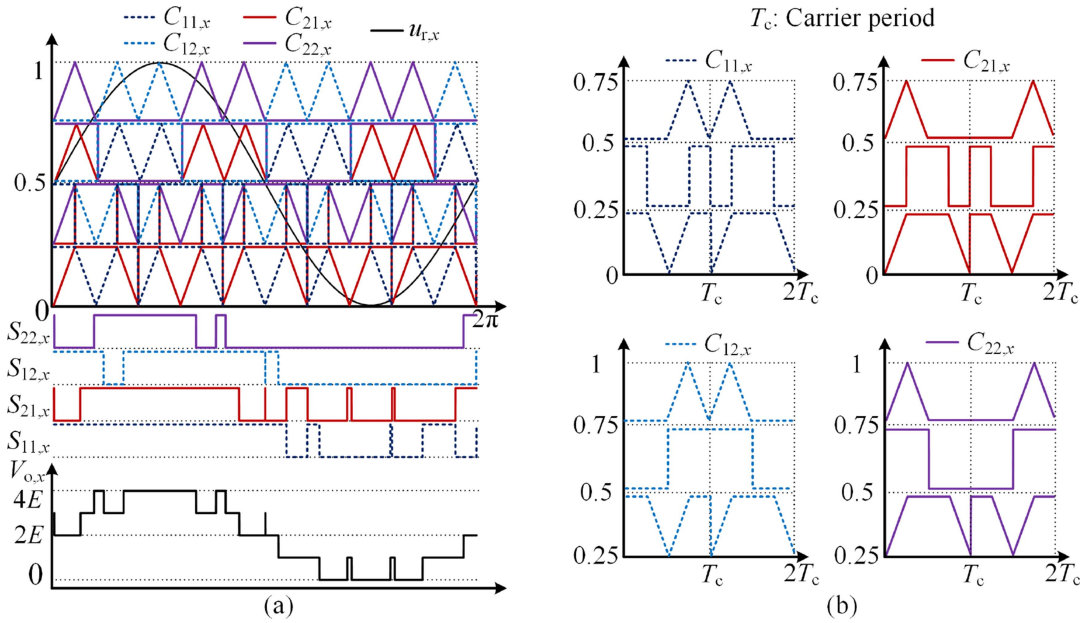

Fig. 4. Proposed CRPWM for five-level SM converter. (a) Proposed CRPWM for obtaining phase voltage. (b) Carriers of proposed CRPWM.

reduce the number of capacitors. Therefore, some NP current is inevitable, making minimization of NP current a crucial concern.

Since PD+PS PWM and CRPWM methods employ the same switching states with different sequences, we comprehensively analyze the modified CRPWM method as an example. The pulse model of the modified CRPWM method is depicted in Fig. 3. When $0 \le u_{r,x} < 1/4$ and $3/4 \le u_{r,x} \le 1$, switching states 2 and 7 generate NP current, but these states need to cooperate with switching states 1 and 11, respectively, to achieve a natural balance of the floating capacitor voltage, and no additional redundant switching states are introduced. Therefore, NP currents generated within these regions are unavoidable. By contrast, when $1/4 \le u_{r,x} < 1/2$ and $1/2 \le u_{r,x} < 3/4$, only switching state 3 is selected for the output voltage level of $2E$, resulting in a maximum NP current as $u_{r,x}$ approaches 1/2 and partly leading to significant low-frequency voltage ripples in the dc-link capacitors. However, switching states 5 and 10 can also output a voltage level of $2E$ without generating NP current. Both switching states should have the same dwell time to ensure the natural voltage balancing of the floating capacitors.

To alleviate the low-frequency voltage ripple problem for the five-level SM converter, we propose the CRPWM method with NP current reduction is shown in Fig. 4. The obtained phase voltages align with other CRPWM methods, ensuring excellent THD performance. Similar to the modified CRPWM method, the proposed CRPWM method redistributes carriers in adjacent carrier cycles, balancing voltage deviations caused by uneven carrier utilization over two carrier cycles.

The pulse models of the proposed CRPWM method are presented in Fig. 5. The difference between the proposed CRPWM method and the modified CRPWM method lies primarily in the region of $1/4 \le u_{r,x} < 3/4$, where new and simple carrier

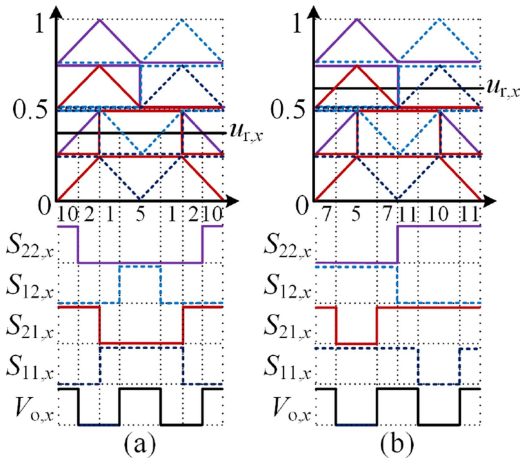

Fig. 5. Pulse models of proposed CRPWM method. (a) $1/4 \le u_{r,x} < 1/2$. (b) $1/2 \le u_{r,x} < 3/4$.

shapes are introduced into the original carriers to achieve switching states 5 and 10, eliminating switching state 3. In addition, when switches $S_{11,x}$ and $S_{21,x}$ change states simultaneously, switches $S_{12,x}$ and $S_{22,x}$ remain turned OFF. Conversely, when switches $S_{12,x}$ and $S_{22,x}$ change states simultaneously, switches $S_{11,x}$ and $S_{21,x}$ are kept turned ON. This approach prevents nonideal switching states caused by switching delays or dead time that are not included in Table I.

The harmonic characteristics of the output voltage are determined through a double Fourier series analysis. As shown in Figs. 2–5, the proposed CRPWM, modified CRPWM, and other CRPWM methods have the same output voltage pulse models, leading to identical double Fourier series results of line voltage. Therefore, the double Fourier series results of line voltage for the proposed CRPWM align with those of modified CRPWM and PD-PWM, which can be referred to [22], indicating that the proposed CRPWM exhibits comparable harmonic performance to PD-PWM.

Compared with PD+PS PWM or other CRPWM methods, the proposed scheme introduces new switching states, where switches $S_{22,x}$ and $S_{12,x}$ undergo additional state changes in the region of $1/4 \le u_{r,x} < 1/2$, while switches $S_{21,x}$ and $S_{11,x}$ experience additional state changes in the region of $1/2 \le u_{r,x} < 3/4$. These changes lead to increased turn-ON and turn-OFFlosses in the power switches, contributing to lower efficiency. Consequently, the duty cycles of switches for the proposed CRPWM method can be expressed as

$$D_{11,x} = D_{21,x} = \begin{cases} 2u_{r,x} & (0 \le u_{r,x} < 1/4) \\ 1/2 & (1/4 \le u_{r,x} < 1/2) \\ 2u_{r,x} - 1/2 & (1/2 \le u_{r,x} < 3/4) \\ 1 & (3/4 \le u_{r,x} \le 1) \end{cases} \tag{9a}$$

$$D_{12,x} = D_{22,x} = \begin{cases} 0 & (0 \le u_{r,x} < 1/4) \\ 2u_{r,x} - 1/2 & (1/4 \le u_{r,x} < 1/2) \\ 1/2 & (1/2 \le u_{r,x} < 3/4) \\ 2u_{r,x} - 1 & (3/4 \le u_{r,x} \le 1) \end{cases}. \tag{9b}$$

According to (7) and (9), the average NP current for proposed CRPWM method is

$$\bar{i}_{N,x} = \begin{cases} 2u_{r,x} \cdot i_{o,x} & (0 \le u_{r,x} < 1/2) \\ (1 - 2u_{r,x}) \cdot i_{o,x} & (1/4 \le u_{r,x} < 1/2) \\ (2u_{r,x} - 1) \cdot i_{o,x} & (1/2 \le u_{r,x} < 3/4) \\ (2 - 2u_{r,x}) \cdot i_{o,x} & (3/4 \le u_{r,x} \le 1) \end{cases}. \tag{10}$$

Equation (10) highlights a significant reduction in NP current in the region of $1/4 \le u_{r,x} < 3/4$, alleviating NP voltage imbalance. For a three-phase system, the reference modulation voltages and the corresponding output currents can be expressed as

$$\begin{cases} u_{r,a} = 1/2 + m \cdot \sin(\theta)/2 \\ u_{r,b} = 1/2 + m \cdot \sin(\theta - 2\pi/3)/2 \\ u_{r,c} = 1/2 + m \cdot \sin(\theta + 2\pi/3)/2 \end{cases} \tag{11a}$$

$$\begin{cases} i_{o,a} = I_o \cdot \sin(\theta + \varphi) \\ i_{o,b} = I_o \cdot \sin(\theta - 2\pi/3 + \varphi) \\ i_{o,c} = I_o \cdot \sin(\theta + 2\pi/3 + \varphi) \end{cases} \tag{11b}$$

where m denotes modulation index and φ signifies power factor angle.

The total average NP current is

$$\bar{i}_N = \bar{i}_{N,a} + \bar{i}_{N,b} + \bar{i}_{N,c}. \tag{12}$$

Following (8) and (10)–(12), the influence of various modulation methods on the total average NP current is demonstrated in Fig. 6 with $m = 1$. The proposed CRPWM method demonstrates a significantly reduced NP current, particularly at low power factors. By contrast, PD+PS PWM and other CRPWM methods further deteriorate the NP current at low power factors. In addition, integrating NP current affects the NP voltage, implying that a low fundamental frequency amplifies the disparity in NP voltage balance performance.

III. Active Capacitor Voltage Balancing Method and Its Effect on NP Current Suppression

The active balancing method enhances the voltage balancing performance of capacitors significantly without balancing booster or auxiliary circuits. It effectively suppresses voltage deviations caused by uneven carrier utilization, turn-ON delay, dead time, and other nonideal conditions. Similar to other clamped converters, ZSV injection is a common technique to balance the NP voltage, while duty cycles are slightly modified to balance the floating capacitors.

A. Active Voltage Balancing for DC-Link Capacitors

NP voltage imbalance is a primary cause of low-frequency voltage ripples and voltage divergence in dc link capacitors. Typically, ZSV injection serves as a common method to suppress NP voltage imbalance actively. To prevent overmodulation, ZSV is constrained to

$$-\min(u_{r,x}) \le u_z \le 1 - \max(u_{r,x}). \tag{13}$$

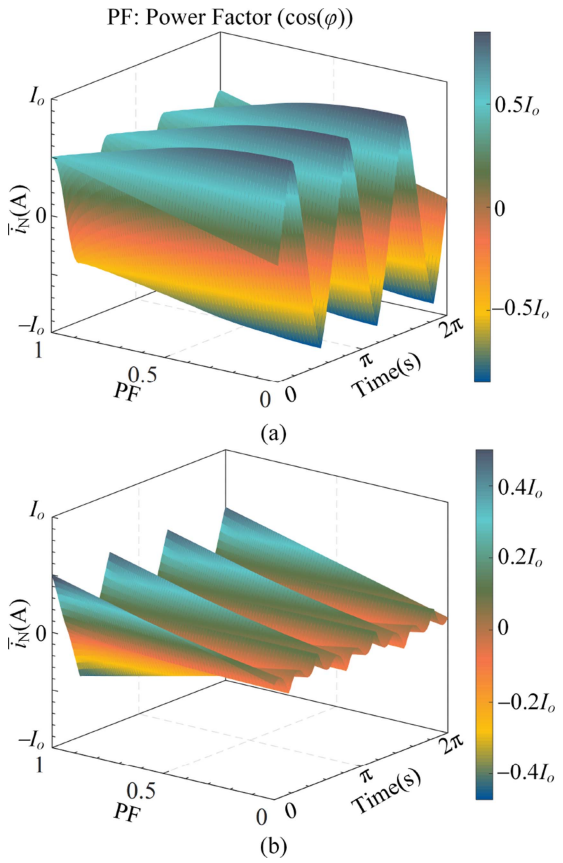

Fig. 6. Different methods effect on the total average NP current. (a) PD+PS PWM and other CRPWMs. (b) proposed CRPWM.

Then the reference modulation voltage is redefined with ZSV injection

$$u'_{\mathrm{r},x} = u_{\mathrm{r},x} + u_{\mathrm{z}}. \tag{14}$$

Taking $u'_{\mathrm{r},x}$ into (10) and (12), the total average NP current can be rewritten as

$$\bar{i}'_{\mathrm{N}} = \bar{i}'_{\mathrm{N,a}} + \bar{i}'_{\mathrm{N,b}} + \bar{i}'_{\mathrm{N,c}}. \tag{15}$$

The required NP current to suppress the NP unbalanced voltage is

$$\bar{i}_{\mathrm{rN}} = C_{\mathrm{d}} \frac{u_{\mathrm{d2}} - u_{\mathrm{d1}}}{T_c} \tag{16}$$

where T_c denotes the carrier period, u_{d1} and u_{d1} denote the voltages of dc-link capacitors C_{d1} and C_{d2} respectively, C_{d} denotes the capacity of dc-link capacitors.

Following (10) and (13)–(16), balancing the NP voltage involves identifying u_{z} that yields $\bar{i}'_{\mathrm{N}}$ closest to $\bar{i}_{\mathrm{rN}}$. The optimal ZSV $u_{\mathrm{z,o}}$ can be determined through the following steps:

Step I: ZSVs are selected equidistantly within the limit of (13) and denoted as $u_{\mathrm{z},k}$.

Step II: $\bar{i}'_{\mathrm{N},k}$ are computed based on $u_{\mathrm{z},k}$ using (10), (11), (14), and (15), whereas $\bar{i}_{\mathrm{rN}}$ is determined using (16).

Step III: Comparing each $\bar{i}'_{\mathrm{N},k}$ with $\bar{i}_{\mathrm{rN}}$, the ZSV is selected, which generates $\bar{i}'_{\mathrm{N}}$ closest to $\bar{i}_{\mathrm{rN}}$ as $u_{\mathrm{z,o}}$.

B. Active Voltage Balancing for Floating Capacitors

The required currents for voltage balancing can be derived from the capacitor voltage ripple models

$$\Delta i_{\mathrm{f11},x} = C_{\mathrm{f11},x} \frac{u_{\mathrm{f11},x} - E}{T_c} \tag{17a}$$

$$\Delta i_{\mathrm{f12},x} = C_{\mathrm{f12},x} \frac{u_{\mathrm{f12},x} - E}{T_c} \tag{17b}$$

where $u_{\mathrm{f11},x}$ and $u_{\mathrm{f11},x}$ denote the voltages of floating capacitors $C_{\mathrm{f11},x}$ and $C_{\mathrm{f12},x}$ respectively, $C_{\mathrm{f11},x}$ and $C_{\mathrm{f11},x}$ denote the capacity of floating capacitors, respectively.

Equation (6) highlights that the currents of floating capacitors can be actively influenced by modifying $D_{11,x}$, $D_{12,x}$, $D_{21,x}$, and $D_{22,x}$. We assume that the required duty cycle adjustments $\Delta D_{11,x}$, $\Delta D_{12,x}$, $\Delta D_{21,x}$, and $\Delta D_{22,x}$ are integrated to $D_{11,x}$, $D_{12,x}$, $D_{21,x}$, and $D_{22,x}$, respectively. Combined with (9), the required duty cycle adjustments can be determined from the required currents

$$\Delta i_{\mathrm{f11},x} = (\Delta D_{11,x} - \Delta D_{21,x}) \cdot i_{o,x} \tag{18a}$$

$$\Delta i_{\mathrm{f12},x} = (\Delta D_{12,x} - \Delta D_{22,x}) \cdot i_{o,x}. \tag{18b}$$

To mitigate any impact on the output voltage, the following conditions must be satisfied:

$$\Delta D_{21,x} + \Delta D_{11,x} = 0 \tag{19a}$$

$$\Delta D_{22,x} + \Delta D_{12,x} = 0. \tag{19b}$$

According to (17), (18), and (19), the required duty cycle adjustments are

$$\Delta D_{11,x} = -\Delta D_{21,x} = C_{\mathrm{f11},x} \frac{u_{\mathrm{f11},x} - E}{2 i_{o,x} \cdot T_c} \tag{20a}$$

$$\Delta D_{12,x} = -\Delta D_{22,x} = C_{\mathrm{f12},x} \frac{u_{\mathrm{f12},x} - E}{2 i_{o,x} \cdot T_c}. \tag{20b}$$

The voltages of dc-link capacitors are balanced with optimal ZSV following (10) and (13)–(16). The required duty cycle adjustments $\Delta D_{11,x}$, $\Delta D_{12,x}$, $\Delta D_{21,x}$, and $\Delta D_{22,x}$ are computed based on (20) and added to (9) for active voltage balancing of floating capacitors. Subsequently, the reference modulation voltages of the switches with active capacitor voltage balancing are

$$\begin{cases} u_{\mathrm{r11},x} = u'_{\mathrm{r},x} + C_{\mathrm{f11},x} \frac{u_{\mathrm{f11},x} - E}{4 i_{o,x} \cdot T_c} \\ u_{\mathrm{r21},x} = u'_{\mathrm{r},x} - C_{\mathrm{f11},x} \frac{u_{\mathrm{f11},x} - E}{4 i_{o,x} \cdot T_c} \\ u_{\mathrm{r12},x} = u'_{\mathrm{r},x} + C_{\mathrm{f12},x} \frac{u_{\mathrm{f12},x} - E}{4 i_{o,x} \cdot T_c} \\ u_{\mathrm{r22},x} = u'_{\mathrm{r},x} - C_{\mathrm{f12},x} \frac{u_{\mathrm{f12},x} - E}{4 i_{o,x} \cdot T_c} \end{cases}. \tag{21}$$

C. Effect of Active Capacitor Voltage Balancing on NP Current Suppression

The NP voltage imbalance is suppressed through ZSV injection, whether the proposed CRPWM method or not. The distinction lies in how ZSV is calculated: the proposed CRPWM method utilizes (10) and (13)–(16), whereas PD+PWM and other CRPWM methods employ (8) and (13)–(16). Therefore,

the relationships between $u_{\mathrm{r},x}$ and $\bar{i}_{\mathrm{N},x}$ in (8) and (10) determine NP voltage balance performance for various approaches.

The total average NP current can be actively adjusted through ZSV injection following (10), (11), and (13)–(15). The maximum total average NP current regulated by ZSV and the minimum total average NP current, denoted as $\bar{i}'_{\mathrm{Nmax}}$ and $\bar{i}'_{\mathrm{Nmin}}$, respectively, are determined in *Step II* and correspond to the maximum and minimum values of $\bar{i}'_{\mathrm{N},k}$. If ZSV injection fully suppresses $\bar{i}_{\mathrm{N}}$, the unbalanced total average NP current is expressed as zero; otherwise, it is expressed as the current that cannot be suppressed. Finally, the unbalanced total average NP current can be expressed as

$$\bar{i}'_{\mathrm{Nimb}} = \begin{cases} 0, & \text{if } \bar{i}_{\mathrm{N}} \geq 0 \text{ and } \bar{i}'_{\mathrm{Nmin}} \leq 0 \\ \bar{i}'_{\mathrm{Nmin}}, & \text{else if } \bar{i}_{\mathrm{N}} \geq 0 \text{ and } \bar{i}'_{\mathrm{Nmin}} > 0 \\ 0, & \text{else if } \bar{i}_{\mathrm{N}} < 0 \text{ and } \bar{i}'_{\mathrm{Nmax}} \geq 0 \\ \bar{i}'_{\mathrm{Nmax}}, & \text{otherwise.} \end{cases} \tag{22}$$

In (21), the reference modulation voltage undergoes further modification after ZSV injection to achieve floating capacitor voltage balance, influencing the calculated total average NP current. Following (7), (9), (20), and (21), the derived average NP current for the proposed CRPWM method with dc-link upper and lower capacitor voltage balance and floating capacitor voltage balance is

$$\bar{i}''_{\mathrm{N},x} = \begin{cases} \bar{i}'_{\mathrm{N},x} + \Delta D_{21,x} \cdot i_{o,x} & (0 \leq u_{\mathrm{r},x} < 1/2) \\ \bar{i}'_{\mathrm{N},x} - \Delta D_{22,x} \cdot i_{o,x} & (1/4 \leq u_{\mathrm{r},x} < 1/2) \\ \bar{i}'_{\mathrm{N},x} + \Delta D_{21,x} \cdot i_{o,x} & (1/2 \leq u_{\mathrm{r},x} < 3/4) \\ \bar{i}'_{\mathrm{N},x} - \Delta D_{22,x} \cdot i_{o,x} & (3/4 \leq u_{\mathrm{r},x} \leq 1) \end{cases}. \tag{23}$$

The duty cycle adjustments $\Delta D_{21,x}$ and $\Delta D_{22,x}$ are computed from the floating capacitor voltages, but they are typically limited to 10% of the original reference modulation voltages [30]. Consequently, the impact of floating capacitor voltage balance control on dc-link upper and lower capacitor voltage balance control is weak and often negligible [5], [19], [30], [31], [32]. This limited effect extends to the unbalanced total average NP current, determined using (22).

Based on (22), the impact of active capacitor voltage balancing on NP current suppression with $m = 1$ is illustrated in Fig. 7. All methods demonstrate excellent ability to suppress unbalanced NP current at extremely high power factors. However, with decreasing power factors, the distinction becomes more pronounced. PD+PS PWM and other CRPWM methods struggle to suppress NP current, resulting in a rapid increase in the unbalanced NP current as the power factor decreases. This trend persists until a very low power factor is achieved. Consequently, PD+PS PWM and other CRPWM methods exhibit limitations in suppressing NP currents, particularly at low power factors. This feature leads to larger low-frequency voltage ripples in dc-link capacitors, particularly at lower fundamental frequencies with considerable modulation indices. By contrast, the proposed CRPWM demonstrates a superior rejection of unbalanced NP current. The unbalanced NP current remains stable with decreasing power factors, and its magnitude and area are significantly smaller than other methods. Therefore, the proposed approach alleviates the NP voltage imbalance problem at low power factor and low fundamental frequency, preventing potential issues related to higher voltage stress and device damage caused by low-frequency voltage ripples.

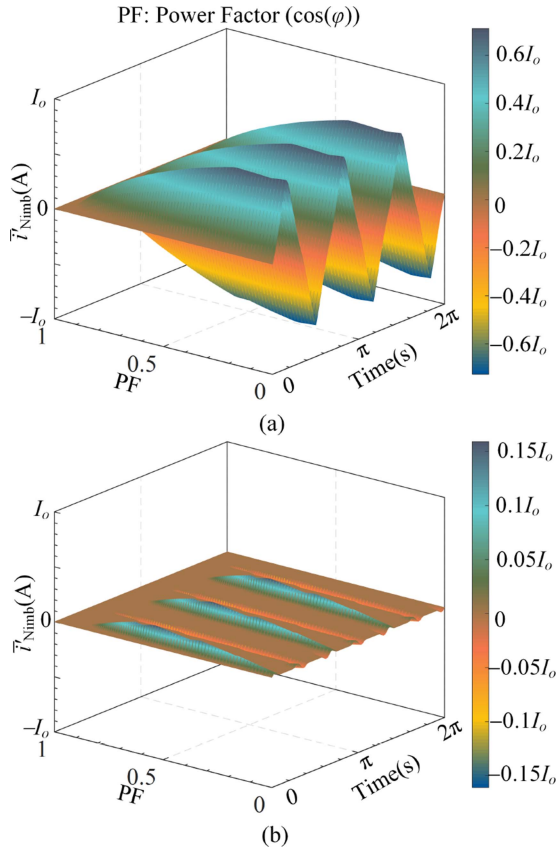

Fig. 7. Effects of active capacitor voltage balancing on NP current suppression, (a) PD+PS PWM and other CRPWMs. (b) proposed CRPWM.

TABLE II
CIRCUIT PARAMETERS OF FIVE-LEVEL SM CONVERTER IN THE SIMULATION AND EXPERIMENT

Parameters	Value
DC-link voltage	U_{dc} = 100 V
DC-link capacitors	$C_{\mathrm{d1}} = C_{\mathrm{d2}}$ = 560 μF
Floating capacitors	$C_{\mathrm{f11},x} = C_{\mathrm{f12},x}$ = 560 μF
Carriers frequency	f_{c} = 4 kHz
Fundamental frequency	f = 50 Hz
R–*L* load	R = 2.5 Ω, L = 40 mH

IV. SIMULATION RESULTS

In the simulation, we constructed a five-level SM converter to validate the feasibility of the proposed CRPWM method at low power factors. Comparative studies are conducted with PS+PD PWM, traditional CRPWM, and modified CRPWM. To ensure balanced capacitor voltages, an active voltage balancing method is implemented. The circuit simulation parameters of the five-level SM converter are detailed in Table II.

A. Simulation Results of Steady-State Performance

The steady-state performances of various modulation approaches under simulation conditions with $m = 1$ are presented in Fig. 8. The proposed CRPWM exhibits superior line voltage performance compared with the four methods. By contrast, the other approaches demonstrate a significant distortion in the line voltage, particularly at PF $=$ 0.23 and $f = 10$ Hz. More pronounced performance differences are observed in the low-frequency voltage ripples of the dc-link capacitors. At PF $=$ 0.2, $f =$ 50 Hz and PF $=$ 0.23, $f =$ 10 Hz, the proposed CRPWM demonstrates low-frequency voltage ripples of 0.44 and 2.14 V, respectively. By contrast, the modified CRPWM, traditional CRPWM, and PS+PD PWM exhibit ripples of 5.5, 5.44, and 5.24 V, and 32.3, 32.2, and 32.5 V, respectively. The low-frequency voltage ripples of the proposed CRPWM are reduced by over 10 times. The THD analysis of the line voltages reveals that the low-frequency voltage ripples introduce significant 5th and 7th harmonic components, while the switching frequency contributes to dominant harmonic frequencies of 8 and 16 k. The proposed CRPWM outperforms other methods in line voltage harmonics with the lowest 5th and 7th harmonic components. At PF $=$ 0.23 and $f = 10$ Hz, modified CRPWM, traditional CRPWM, and PS+PD PWM exhibit substantial 5th harmonic components with amplitudes of 6.1, 6.1, and 6.0 V, respectively, and 7th harmonic components with amplitudes of 1.7, 1.6, and 1.7 V, respectively. By contrast, the proposed CRPWM exhibits the lowest 5th and 7th harmonic components with amplitudes of 0.09 and 0.10 V, respectively. In addition, the dominant harmonics component of the proposed CRPWM at 8 k is comparable to the other approaches, while the higher frequency dominant harmonic component at 16 k accounts for a higher percentage. These higher frequency components can be effectively filtered out by filters to enhance harmonic performance.

B. Simulation Results of Dynamic Performance

The simulation results for dynamic performances with variable voltage and variable frequency (VVVF) control are presented in Fig. 9, where f changes from 0 to 50 Hz linearly, and m increases from 0.25 to 1 with a step size of 0.25, leading to a step change in output voltage. In Fig. 9(b)–(d), at the same value of m, the power factor and impedance increase gradually with increasing f, decreasing low-frequency voltage ripples continuously. For the PS+PD PWM and other CRPWM methods, noticeable low-frequency voltage ripples in the dc-link capacitors appear after $m > 0.5$ and $f > 25$ Hz with a maximum value of about 11 V. Compared with the existing approaches, the proposed CRPWM exhibits negligible low-frequency voltage ripples, showcasing effective balancing of capacitor voltages.

The dynamic performances with a high power factor of 0.85 are illustrated in Fig. 10, where the modulation index changes every 0.04 s, while the parameters are set to $R = 10\ \Omega$ and $L = 20$ mH. Low-frequency voltage ripples of about 1.6 V persist with PS+PD PWM and other CRPWM methods at $m =$ 1. However, these ripples are completely suppressed at $m = 0.8$ and below. By contrast, the proposed CRPWM consistently completely suppresses low-frequency voltage ripples across various modulation indices, showcasing superior performance.

C. Simulation Results of Active Capacitor Voltage Control

The simulation results for the active capacitor voltage control for the proposed CRPWM are depicted in Fig. 11. The voltage references of the capacitors are modified to new values and reverted to normal values after a certain duration. All capacitor voltages exhibit controlled variations with the reference voltages. The proposed CRPWM and active voltage balancing method effectively control the capacitor voltages. The THD of the corresponding line voltage under unequal conditions is illustrated in Fig. 11(b). The voltage imbalance of the dc-link capacitors introduces more harmonics at lower frequencies compared with the floating capacitors, while the voltage imbalance of the floating capacitors produces more harmonics at 2 and 6 kHz near the carrier frequency. The THDs of line voltage are 18.58%, 18.87%, and 19.84% under different conditions, and 1.4%, 1.69%, and 2.66% higher than the normal conditions, respectively.

D. Simulation Results of Grid-Connected Implementation

To simulate grid-connected operations, an active and reactive power (PQ) control strategy with an active damping coefficient is implemented instead of using a simple *RL* load, which is shown in Fig. 12. The SM converter is connected to the point of common coupling (PCC) of the grid via an *L*-filter and operated at low power factors and high modulation indices to induce low-frequency voltage ripples on the dc-link capacitors. Therefore, the voltage root mean square of phase-to-phase voltage is set to 58 V. The active power P_{ref} and reactive power Q_{ref} reference values are set to 120 W and 600 Var, respectively, to operate at a low power factor of 0.2; these values are modified to -600 W and -120 Var, respectively, with a power factor of -0.8. The grid-connected parameters include filter inductor $L_{\mathrm{g}} = 2$ mH and filter winding resistance $R_{\mathrm{g}} = 0.1\ \Omega$; $u_{\mathrm{g,d}}$ and $u_{\mathrm{g,q}}$ denote voltages of PCC in *dq*-axis; $i_{\mathrm{g,d}}$ and $i_{\mathrm{g,q}}$ signify currents of SM converter in *dq*-axis; A_{d} represents active damping coefficient, which is $\alpha \cdot L_g - R_g$; proportional gain for *dq*-axis is $\alpha \cdot L_g$; integral gain for *dq*-axis is $\alpha \cdot \alpha \cdot L_g$, where α is set to 500.

Grid-connected simulation results at a fundamental frequency of 50 Hz are illustrated in Fig. 13. For PS+PD PWM and other CRPWM methods, the five-level SM converter initiates operation with a low power factor of 0.2, resulting in noticeable low-frequency fluctuations in power waveforms and dc-link capacitors. These voltage fluctuations reach about 5 V on dc-link capacitors. By contrast, the proposed CRPWM demonstrates superior performance, showcasing low-frequency voltage fluctuations of 0.84 V on dc-link capacitors. At $t = 0.5$ s, the power factor is changed to -0.8, similar to the high power factor case of 0.8. Low-frequency fluctuations are eliminated for all approaches.

Grid-connected simulation results with a fundamental frequency of 10 Hz are presented in Fig. 14, similar to the conditions in Fig. 13. A key distinction is that, at a low power factor of 0.2,

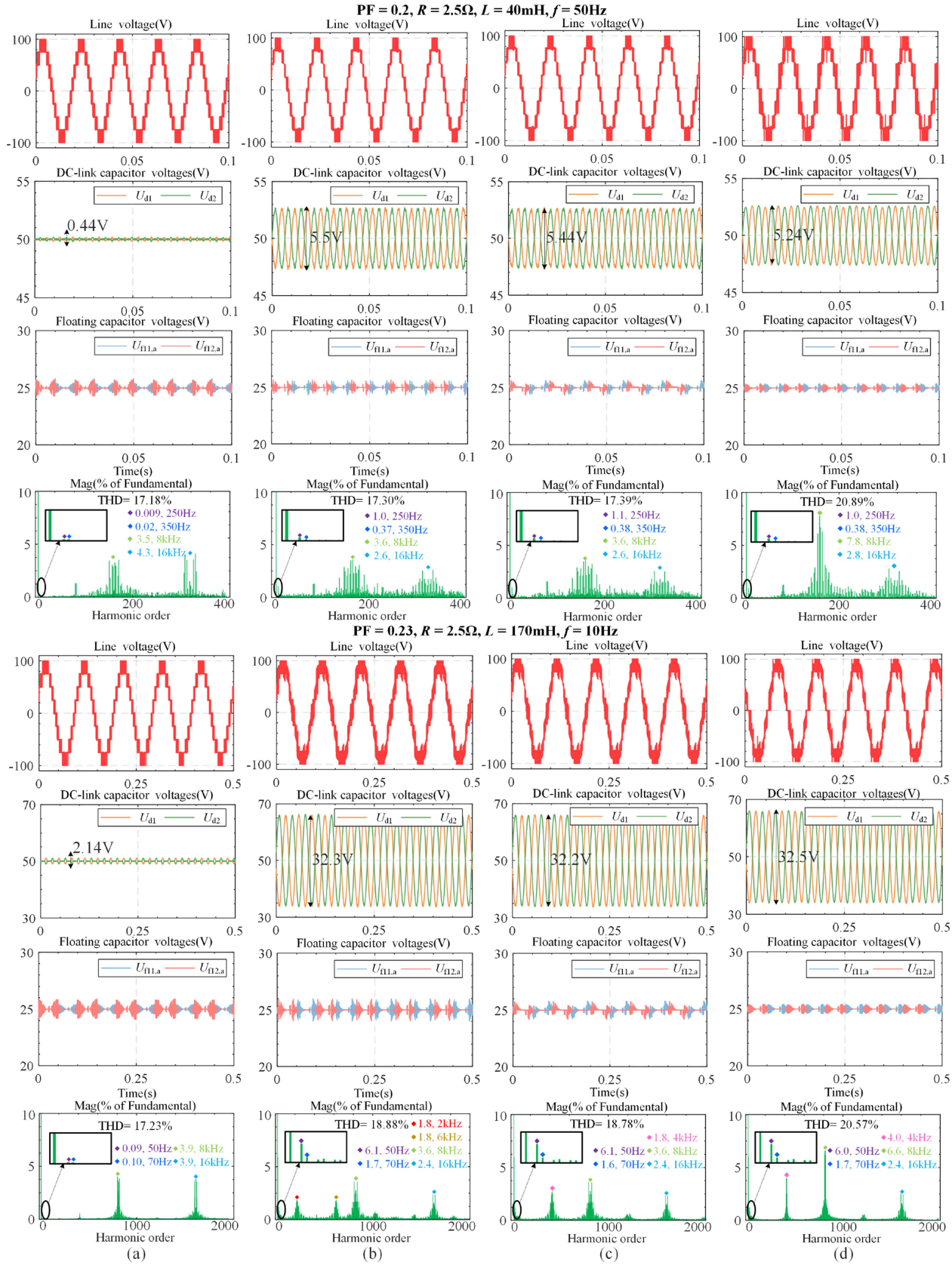

Fig. 8. Steady-state performances of different modulation methods in the simulation. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

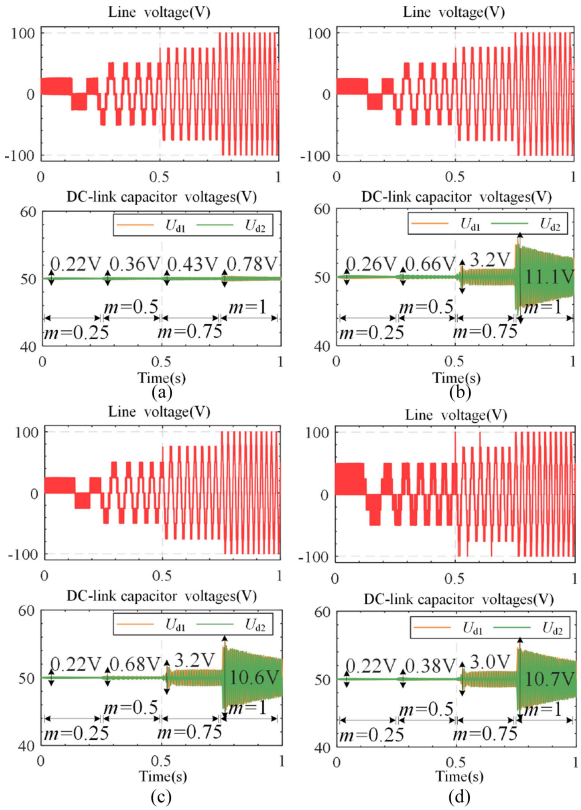

Fig. 9. Dynamic performances with VVVF control in the simulation. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

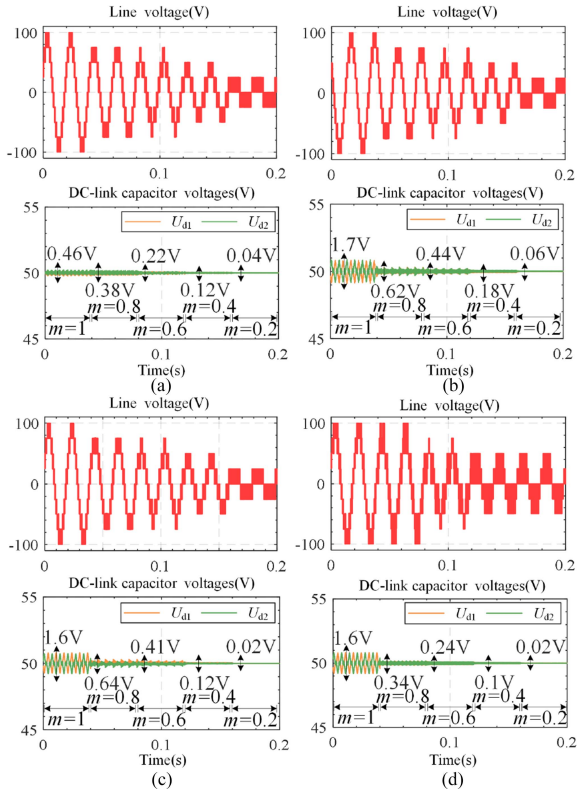

Fig. 10. Dynamic performances with high power factor of 0.85 and different modulation indices in the simulation. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

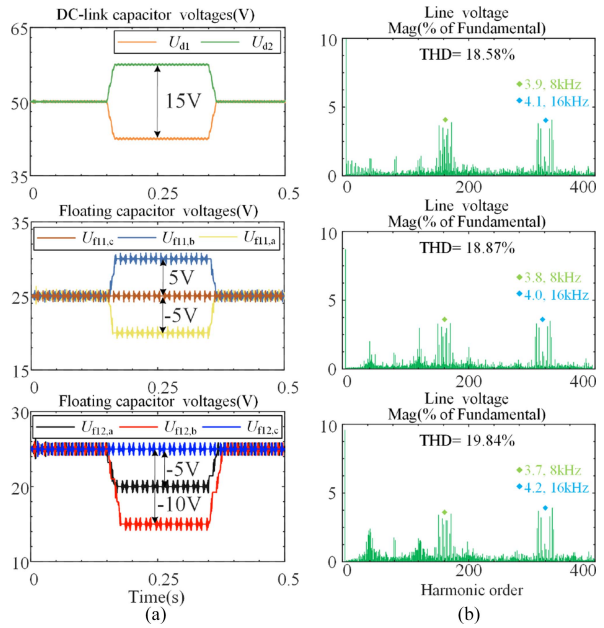

Fig. 11. Active capacitor voltage control for proposed CRPWM in the simulation. (a) Capacitor voltages. (b) THD of the corresponding line voltage.

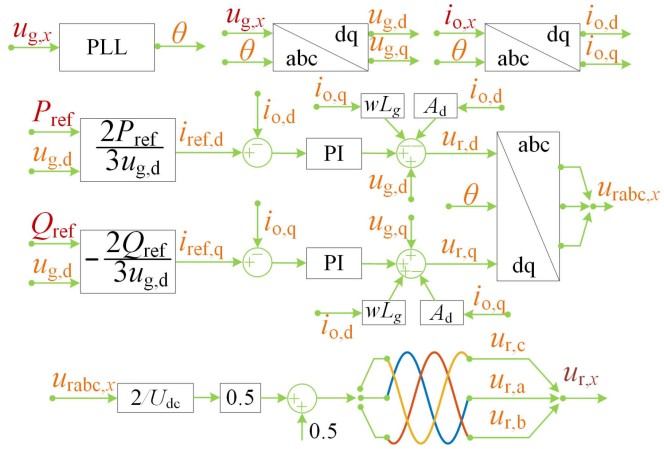

Fig. 12. Block diagram of PQ control strategy for grid-connected implemented in the simulation.

PS+PD PWM and other CRPWM methods exhibit significant distortion in three-phase currents and line voltages compared with the proposed CRPWM. Among all approaches, the proposed CRPWM displays the smallest low-frequency fluctuations in waveforms, showcasing the best performance.

V. Experimental Results

A low-power experimental prototype (see Fig. 15) is constructed to further validate the advantages of the proposed CRPWM with active voltage balancing. The circuit parameters align with those in the simulation. Plexim's RT-BOX1, with an embedded FPGA, is used as a real-time controller for the experimental prototype. It measures voltage and current signals in the prototype and executes the active voltage balancing algorithm and modulation approach to generate gate signals to drive power switches. Fiber optics transmit these gate signals to drive power

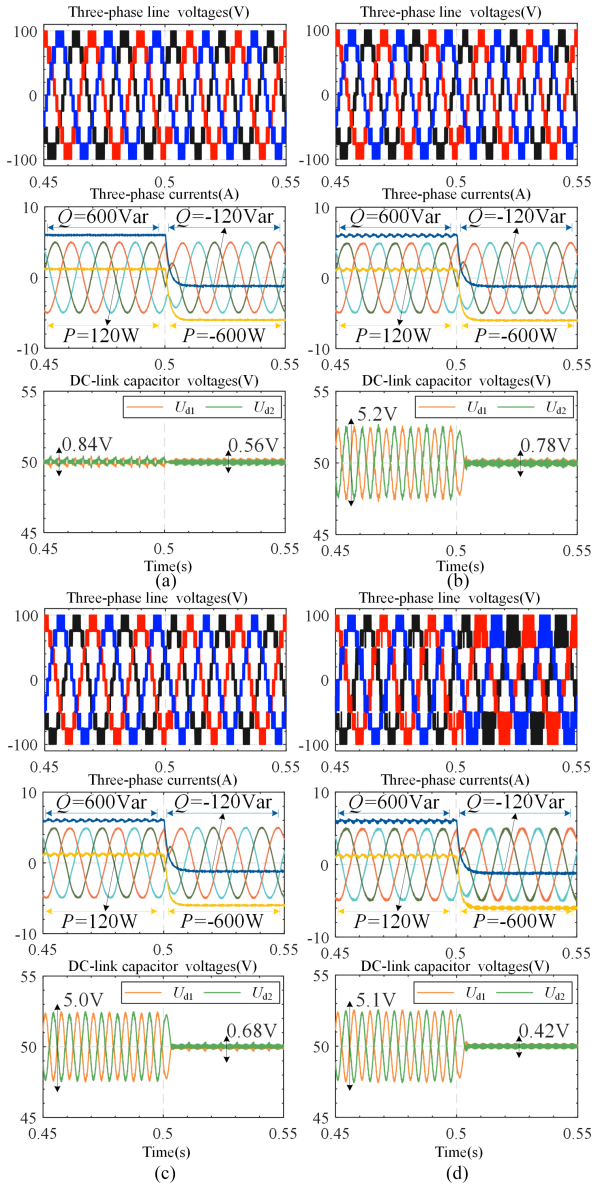

Fig. 13. Grid-connected implementation with 50 Hz in the simulation. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

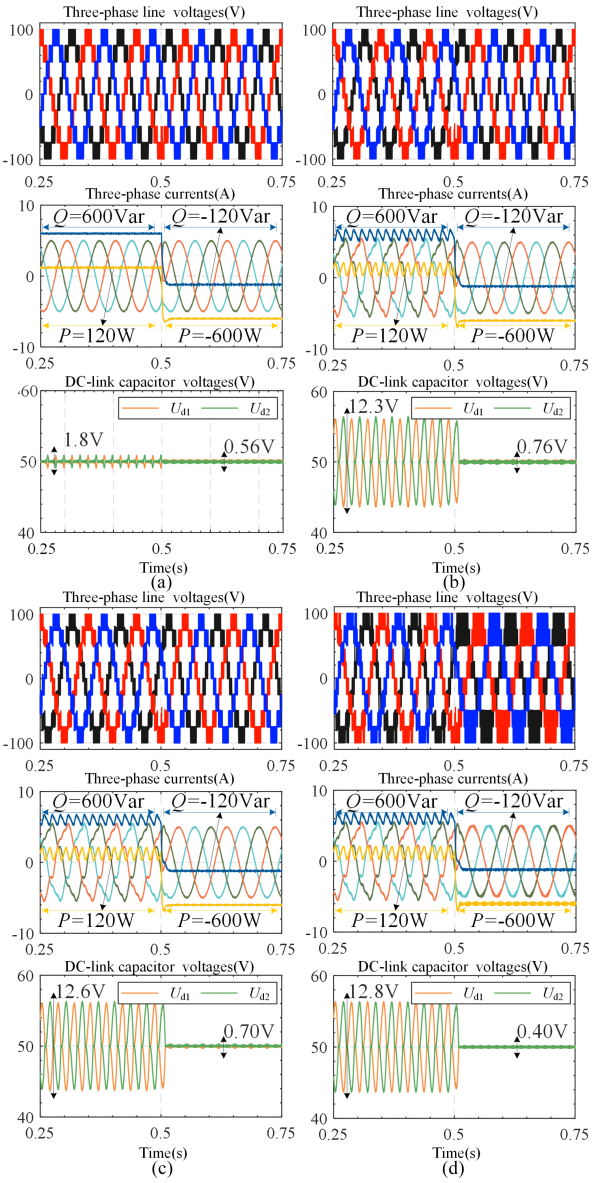

Fig. 14. Grid-connected implementation with 10 Hz in the simulation. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

switches CI60N120SM via gate driver IXDI614YI. The digital implementation for CRPWM can be referred in [22].

A. *Experimental Results of Steady-State Performance*

The steady-state performances of various modulation methods are presented in Fig. 16. In the experiment, similar power factors are maintained, while the fundamental frequencies are set to 50 and 10 Hz. The significant low-frequency voltage ripples occur in modified CRPWM, traditional CRPWM, and PS+PD PWM. By contrast, the proposed CRPWM outperforms other methods with the low-frequency voltage ripples of 1.8 and 3.9 V, representing reductions of about 65% and 88%, respectively, compared with the other three methods. Line voltage THD analysis also supports these findings, revealing that the proposed CRPWM has the lowest 5th and 7th harmonic components with

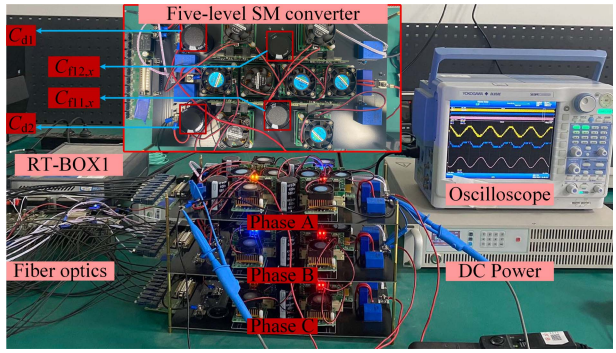

Fig. 15. Prototype of five-level SM converter.

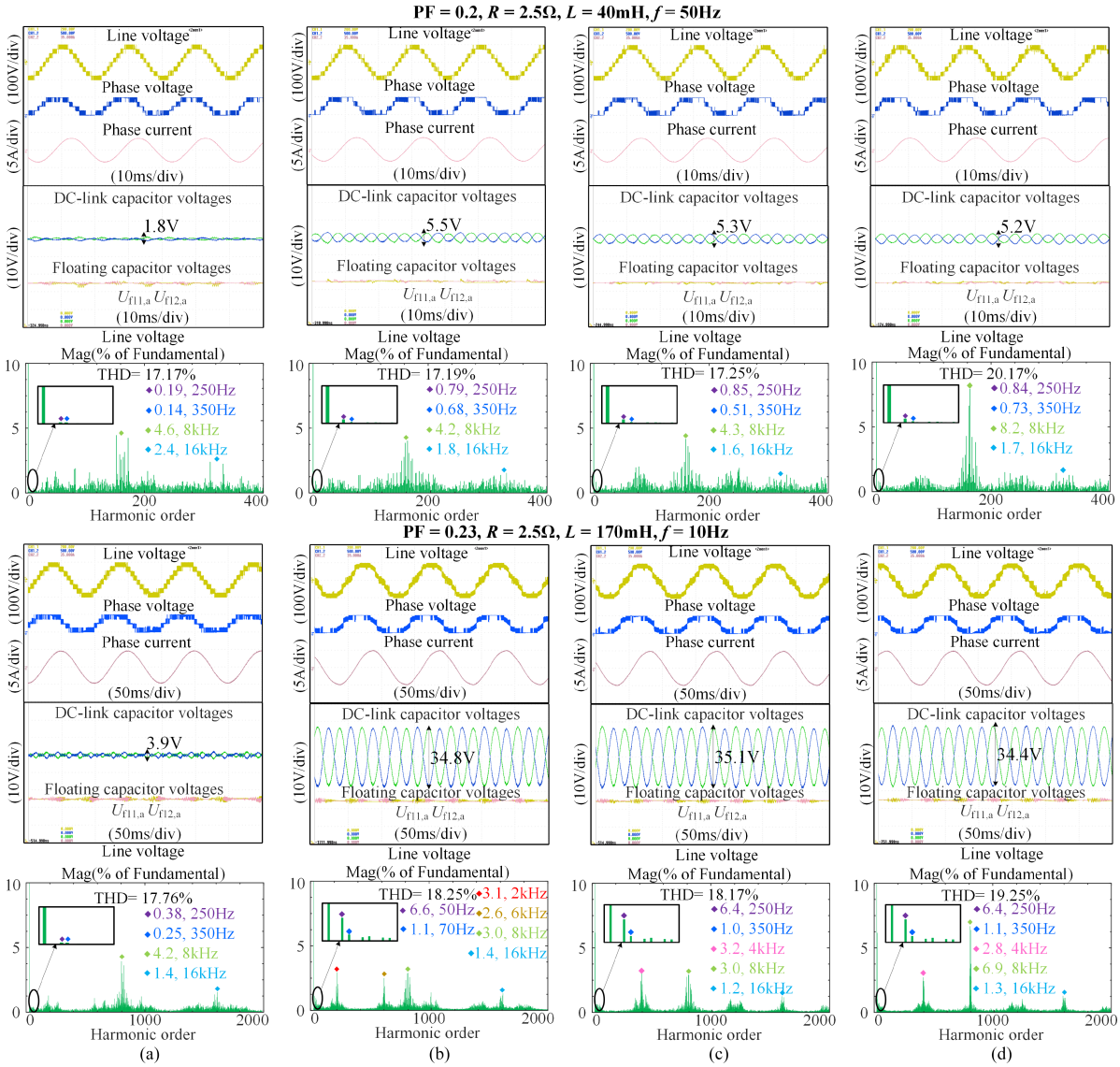

Fig. 16. Steady-state performances of different modulation methods in the experiment. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

amplitudes of 0.19 and 0.14 V, respectively, at PF = 0.2 and $f = 50$ Hz and 0.38 and 0.25 V, respectively, at PF = 0.23 and $f = 10$ Hz. The dominant harmonic components caused by the switching frequency are predominantly concentrated in 8 and 16 k for the proposed CRPWM. By contrast, modified CRPWM, traditional CRPWM, and PS+PD PWM display significant 5th and 7th harmonic components with amplitudes of about 0.8 and 0.6 V, respectively, at PF = 0.2 and $f = 50$ Hz and about 6.5 and 1.1 V, respectively, at PF = 0.23 and $f = 10$ Hz. The dominant harmonic frequencies, attributed to the switching frequency, predominantly manifest at 2 k, 4 k, and 6 k, distributed in lower frequency bands.

The steady-state performances with unbalanced loads in the experiment are illustrated in Fig. 17. The inductance of the c-phase is reduced from 40 to 20 mH, inducing a three-phase unbalanced load. The proposed CRPWM demonstrates a slight 22% increase in low-frequency voltage ripples, while the other three methods exhibit more than 70% increase. The proposed CRPWM outperforms the other methods with unbalanced loads.

B. Experimental Results of Dynamic Performance

The experimental results of dynamic performances with VVVF control (see Fig. 18) are similar to the motor starting process, with m and f changing from 0 to 1 Hz and 0 to 50 Hz, respectively. The other three approaches display significant low-frequency voltage ripples after $f > 35$Hz and $m > 0.7$. By contrast, the proposed CRPWM exhibits minimal low-frequency voltage ripples, almost comparable to those at the carrier frequency.

When the fundamental frequency of the five-level SM converter is modified from 50 to 25 Hz abruptly (see Fig. 19), the low-frequency voltage ripples for the other three methods increase from about 5.3 to 22.5 V, exacerbating the NP voltage

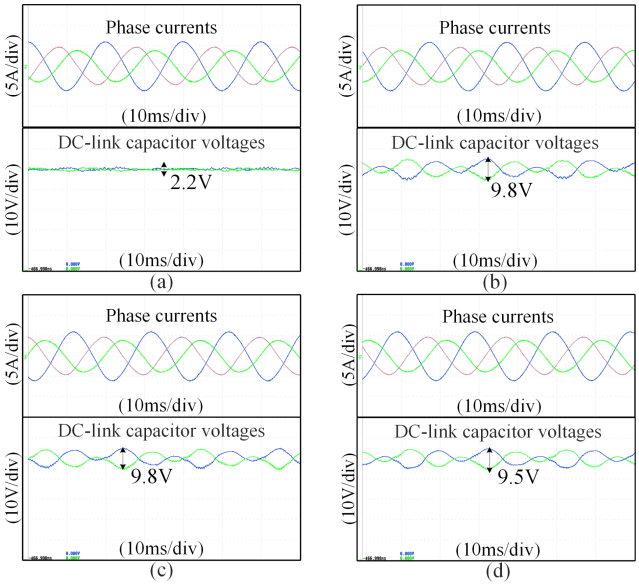

Fig. 17. Steady-state performances with unbalanced load in the experiment. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

imbalance problem drastically. By contrast, the proposed CRPWM shifts low-frequency voltage ripples from 1.8 to 4.4 V, alleviating the NP voltage imbalance problem significantly.

The dynamic performances with varied modulation indices in the experiment are depicted in Fig. 20, where m decreases from 1 to 0.2, with a step size of 0.2. The low-frequency voltage ripples of the other three methods are almost suppressed completely at $m < 0.6$. By contrast, the proposed CRPWM consistently suppresses low-frequency voltage ripples across the entire m range, showcasing superior dynamic performance.

The dynamic performances with a high power factor of 0.85 are presented in Fig. 21, where the modulation index and RL load align with simulation parameters. The floating capacitor voltages are well-balanced for all approaches. However, PS+PD PWM and other CRPWM methods demonstrate larger low-frequency voltage ripples in dc-link capacitors compared with the proposed CRPWM, exhibiting minimal low-frequency voltage ripples.

C. Experimental Results of Active Capacitor Voltage Control

The experimental setup (see Fig. 22) of the active capacitor voltage control for the proposed CRPWM mirrors that of the simulation. The reference voltages of the capacitors are set to new values for a certain duration before being reverted to normal values. Experimental results affirm that all capacitor voltages are controllable under the proposed CRPWM.

D. Experimental Results of THD

The experimental comparison of THD (see Fig. 23) illustrates that when operating at a fundamental frequency of 50 Hz and power factor of 0.2, the fluctuations of low-frequency voltage ripples are relatively small with a high modulation index of 1, having limited impact on the line voltage THD of the SM converter. Consequently, the THD of the proposed CRPWM is only marginally lower than that of modified CRPWM and traditional CRPWM. Conversely, at a higher power factor of 0.85, all approaches exhibit higher THD compared with a power factor of 0.2. Nevertheless, the proposed CRPWM consistently maintains nearly optimal THD performance among all the methods particularly at high modulation indices. At a lower fundamental frequency of 10 Hz, where suppressing low-frequency voltage ripples for the other three methods becomes more challenging at high modulation index, the proposed method excels in THD performance. Under all load conditions, the proposed approach demonstrates a significant THD performance advantage at low modulation indices, with only a slight increase over modified and traditional CRPWM at medium modulation indices.

The comparison of phase voltage THD in the experiment is depicted in Fig. 24. ZSV is determined at each carrier period based on the voltage difference between upper and lower dc-link capacitors, and it is injected into the reference modulating voltages, and then affecting phase voltage. Consequently, all methods exhibit high THD values for phase voltage, among which the proposed CRPWM presents the highest THD values at $m = 1$ and 0.4 and the best harmonic performance at $m = 0.8$ and 0.6.

E. Experimental Results of Efficiency

The comparative study of efficiency results (see Fig. 25) indicates that all methods exhibit higher efficiency at a high power factor of 0.85 and a fundamental frequency of 50 Hz, while the lowest efficiency is observed at a low power factor of 0.2 and fundamental frequency of 50 Hz. Compared with existing methods, modified CRPWM, traditional CRPWM, and PS+PD PWM approaches share identical switching states and similar efficiencies. By contrast, the proposed CRPWM demonstrates the least efficiency, but the efficiency gap with other methods diminishes at lower fundamental frequencies and higher power factors.

F. Experimental Results of Low-Frequency Voltage Ripples

Comparing low-frequency voltage ripple differences in dc-link capacitors (see Fig. 26) reveals that the three alternative methods demonstrate significant ripples, particularly at high modulation indices and low fundamental frequencies. The ripples are suppressed completely only at lower modulation indices and a high power factor of 0.85, where ZSV injection is extended. By contrast, the proposed CRPWM consistently outperforms, showcasing minimal low-frequency voltage ripples across the entire modulation index and power factor spectrum.

G. Summarize

A comprehensive overview of the proposed method and other existing approaches is summarized in Table III. PS+PD PWM and other CRPWM methods share the same switching states with fewer switching transitions and less current flow through the floating capacitors. These approaches exhibit higher efficiencies and reduced voltage ripples of floating capacitors compared

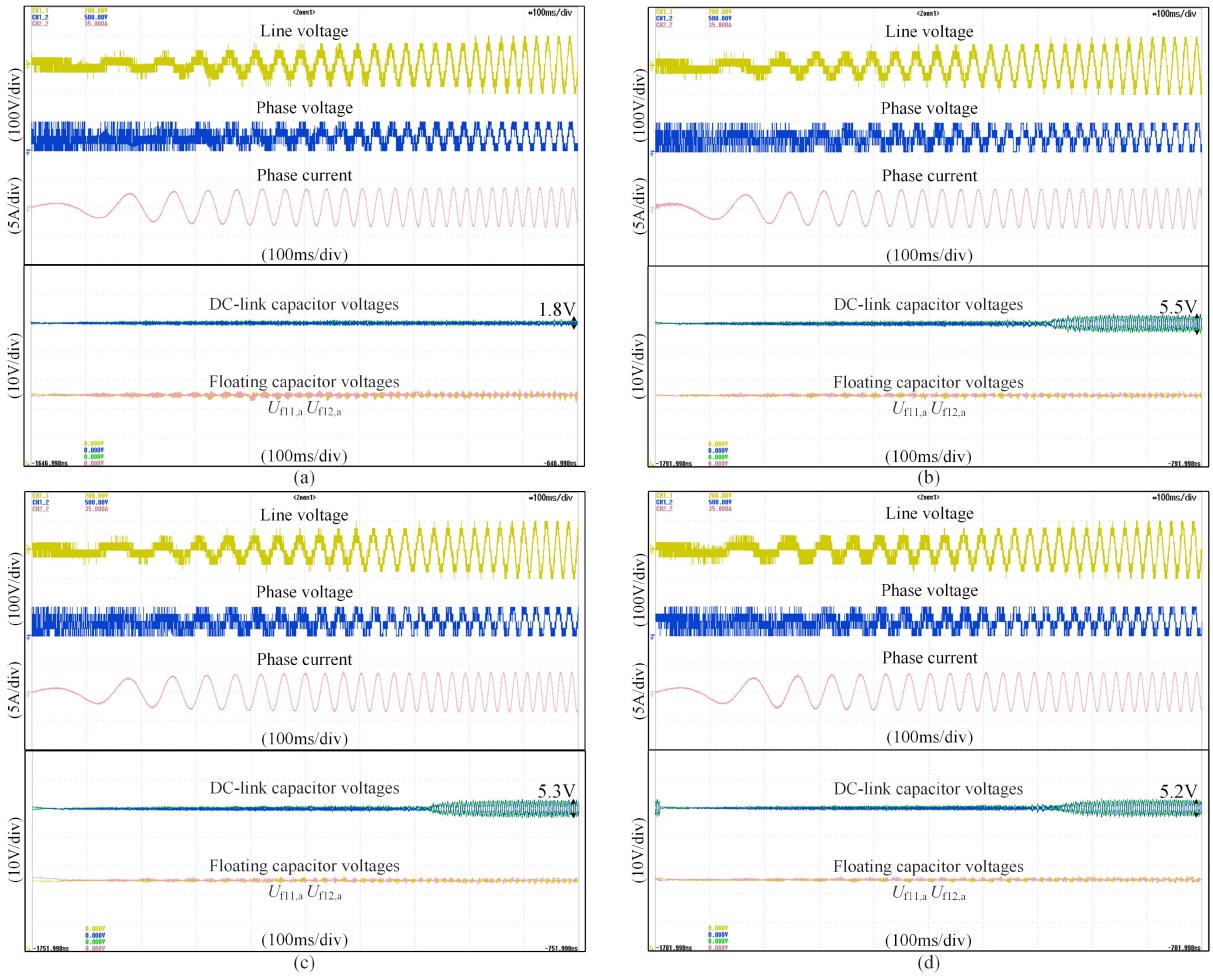

Fig. 18. Dynamic performances with VVVF control in the experiment. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

TABLE III
COMPARISON BETWEEN THE PROPOSED METHOD AND OTHER EXISTING METHODS

	PS+PD PWM	Tra. CRPWM	Sym. CRPWM	Mod. CRPWM	Pro. CRPWM
Voltage ripples of dc-link capacitors	Large	Large	Large	Large	Small
Voltage ripples of floating capacitors	Very small	Very small	Very small	Very small	Small
Harmonic performance of line voltage	Bad	Good	Good	Good	Very good
Harmonic performance of phase voltage	Medium	Medium	Medium	Medium	Medium
Efficiency	High	High	High	High	Medium
Self-balancing period of floating capacitors	Long	None	Medium	Short	Short

with the proposed CRPWM. However, these existing methods generate additional NP currents that are challenging to suppress by ZSV injection, leading to significant low-frequency voltage ripples in dc-link capacitors and increased output voltage harmonic components. PS+PD PWM exhibits the poorest harmonic performance, with more line voltage overlapping within a voltage interval. By contrast, the proposed CRPWM, adept at suppressing low-frequency voltage ripples, exhibits superior harmonic performance of line voltage among all methods. Similar to modified CRPWM, the proposed CRPWM's carriers are also symmetrical over two carrier periods, accelerating the self-balancing of floating capacitors without active voltage control, rendering it particularly suitable for variable frequency applications [22].

The proposed CRPWM introduces the best advantages in terms of suppressing the low-frequency voltage ripples of the dc-link capacitors and improving the THD performance of output line-to-line voltages. However, it compromises the voltage ripples of floating capacitors and the overall efficiency of the system. Typically, the maximum charge/discharge time of the capacitor is the main factor in the selection of the capacitance value [33]. For the other existent methods, the maximum charging/discharging times of floating capacitors are $1/(2f_c)$, which occur at $u_{r,x}$ is 0.25, and 0.75 for $C_{f11,x}$, and $C_{f12,x}$,

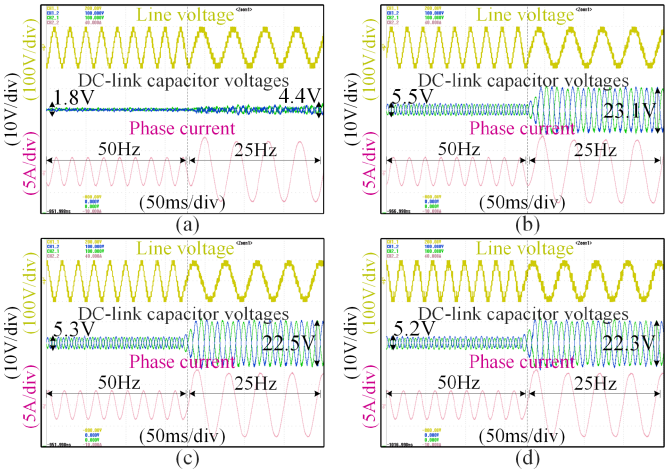

Fig. 19. Dynamic performances for changing the fundamental frequency suddenly in the experiment. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

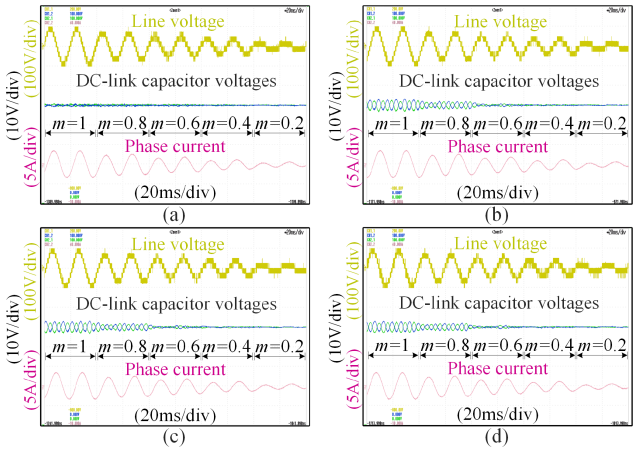

Fig. 20. Dynamic performances with different modulation indexes in the experiment. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

respectively. For the proposed CRPWM, switching states 5 and 10 are introduced instead of switching state 3, so that the maximum charging/discharging times of floating capacitors occur at $u_{r,x}$ is 0.25 to 0.5 for $C_{f11,x}$, and 0.5 to 0.75 for $C_{f12,x}$, respectively. It has a higher charge/discharge frequency, but the maximum charge/discharge times are the same as other methods. As a result, the floating capacitors in the proposed CRPWM have a higher frequency of voltage fluctuation but the maximum amplitude of voltage fluctuation is the same compared to other methods. Therefore, the proposed CRPWM does not affect the selection of the capacitance values of floating capacitors, and the growing frequency of the floating capacitor voltage fluctuation is mainly concentrated in the switching frequency, which is easily filtered out by the output filters. In addition, experimental results of the proposed CRPWM reveal about 88% and 65% reduction in low-frequency voltage ripples of dc-link capacitors at lower power factors and highest modulation index with fundamental frequencies of 10 and 50 Hz, respectively. This ensures that

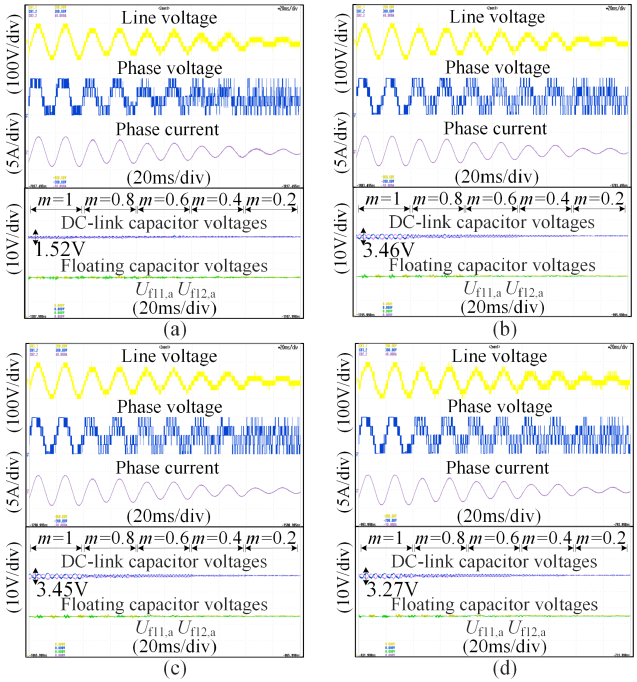

Fig. 21. Dynamic performances with high power factor of 0.85 and different modulation indices in the experiment. (a) Proposed CRPWM. (b) Modified CRPWM. (c) Traditional CRPWM. (d) PS+PD PWM.

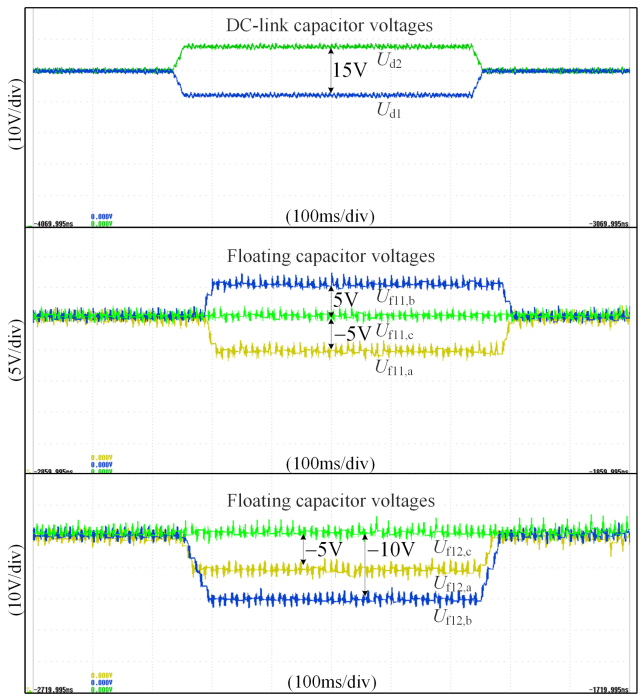

Fig. 22. Active capacitor voltage control for proposed CRPWM in the experiment.

the safe operation of the system is prioritized over the efficiency of the system, avoiding overvoltage and even damage to devices caused by severe low-frequency voltage ripples. The grid-connected implementation simulation also demonstrates that low-frequency fluctuations can also deteriorate the grid-connected power and current waveforms, which significantly

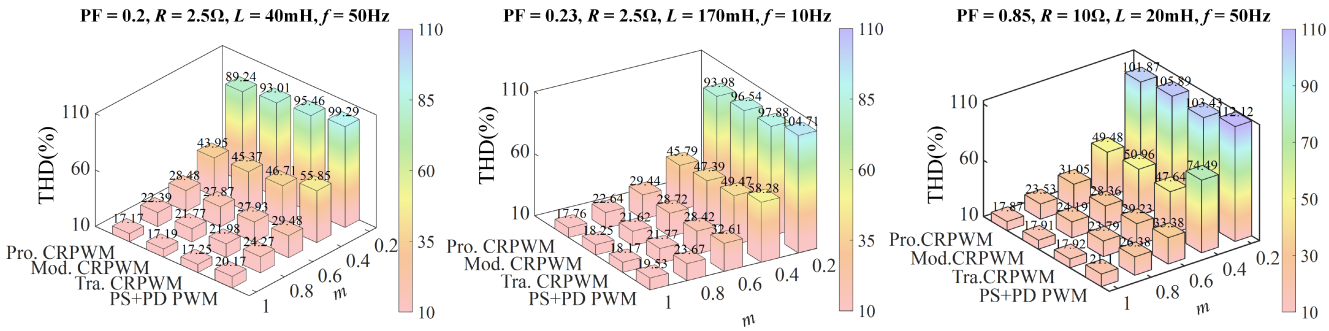

Fig. 23. Comparison of line voltage THD in the experiment.

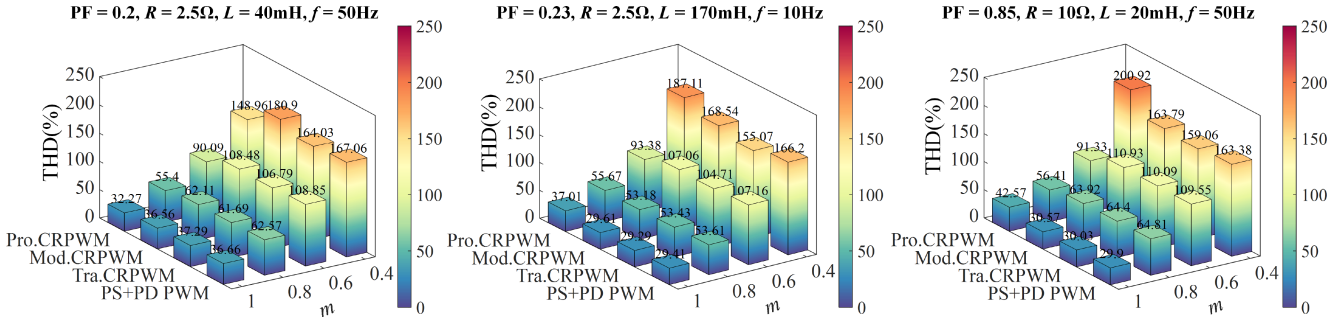

Fig. 24. Comparison of phase voltage THD in the experiment.

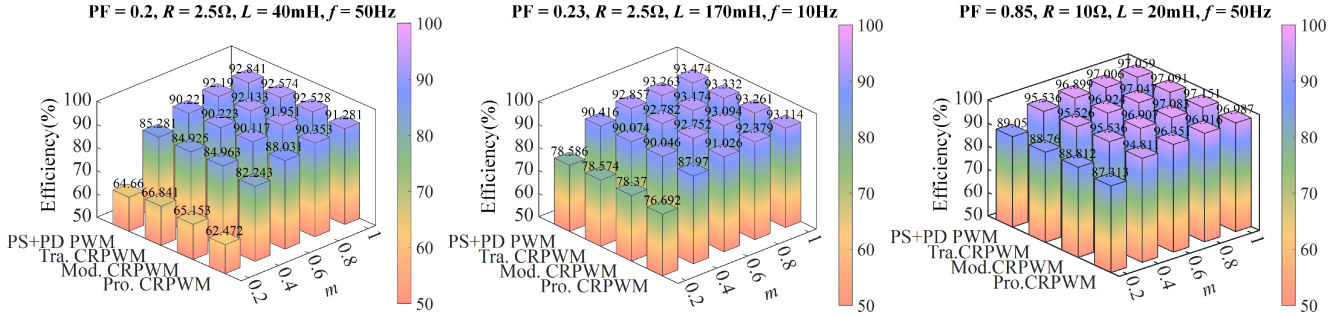

Fig. 25. Comparison of efficiency in the experiment.

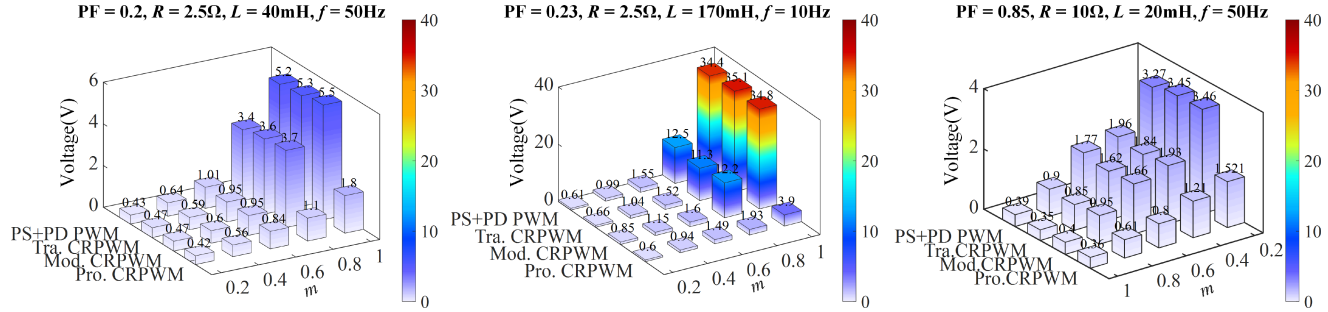

Fig. 26. Comparison of low-frequency voltage ripples in the experiment.

affects the power quality and system stability. Therefore, the proposed CRPWM can better suppress the low-frequency voltage ripples to enhance the safety and stability of the system, which is usually prioritized over system efficiency.

VI. Conclusion

This study proposes a novel CRPWM and its active voltage balancing method for the five-level SM converter to suppress low-frequency voltage ripples of dc-ink capacitors. The study analyzes the impact of various modulation strategies on NP current reduction and capacitor voltage active balancing methods in suppressing unbalanced NP currents. Among all discussed methods, the proposed CRPWM yields the lowest NP current and superior suppression of unbalanced NP current through ZSV injection theoretically, demonstrating enhanced capability in addressing low-frequency voltage ripple issues. Experimental and simulation results affirm that the proposed CRPWM exhibits the lowest efficiency, but smallest low-frequency voltage ripple in static and dynamic evaluations, and optimal harmonic THD performance, particularly at low power factor and low fundamental frequency with substantial modulation index. Therefore, the proposed CRPWM is a viable solution for mitigating low-frequency voltage ripples of dc-ink capacitors and enhancing the output performance of the five-level SM converter in specialized applications.

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