In Situ Detection of GaN $C_{\rm oss}$ Changes Due to Aging for Device State-of-Health Determination in DC–DC Converters

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***Abstract*—Detecting the power-device state-of-health (SOH) during converter operation can enhance the overall system reliability by predicting imminent failure scenarios. While various aging indicators for gallium nitride (GaN) devices have been demonstrated in the literature, few are practically measurable in an active converter. This article demonstrates that the large-signal device output capacitance ($C_{\rm oss}$) is a reliable indicator of short-circuit (SC) aging, and proposes an in situ measurement technique to capture its value by leveraging the operational waveforms of soft-switching converters. The method relies only on the converter operating condition along with the switching modulation and does not require direct measurement of the inductor current. Experimental results for three different GaN devices show a 5%–10% decrease in the large-signal $C_{\rm oss}$ after 5000 SC cycles, proving the usefulness of this parameter as an SOH indicator. The in situ measurement technique is demonstrated in a synchronous buck converter operating in discontinuous conduction mode, successfully capturing the SC-aging-induced change in $C_{\rm oss}$. The presented results and proposed measurement technique pave the way for system-level monitoring of power-device SOH and self-calibrating operation.**

***Index Terms*—Aging precursor, dc-dc power converters, device capacitance measurement, gallium nitride (GaN) power device, in-situ condition monitoring.**

I. Introduction

GALLIUM nitride (GaN) semiconductor technology has gone through remarkable advancements in recent years, driving market adoption. In 2021, the GaN semiconductor market reached a valuation of $126 M, a testament to its growing significance. Furthermore, the market is expected to continue to grow to $2B by 2027 [2]. This growth is, in part, due to the outstanding performance characteristics of GaN devices. In particular, the $R_{\rm DS,on}Q_g$ figure-of-merit for 650 V GaN devices is approximately $13\times$ lower than similar silicon devices [3], [4]. This intrinsic advantage enables GaN converter operation at megahertz frequencies and switching dv/dt values that exceed 100 V/ns [5]. GaN devices have already permeated the consumer electronics market, particularly in phone and laptop power adapters, as well as high-quality audio products [6]. While anticipated growth in the GaN market is expected to stem from the automotive and telecom sectors, particularly with the increasing adoption of electric vehicles and the roll-out of 5G technology [7], it faces ongoing challenges in meeting the high device reliability standards demanded by these applications. GaN high-electron-mobility transistors (GaN HEMTs) exhibit distinct failure modes, activation energies, and accelerating factors compared to silicon MOSFETs [8]. This requires special attention to operate GaN transistors within their safe operating area, given their unique physical structure and sensitive gate. In practice, device failure can occur within 1 μs for repetitive short-circuit (SC) events at typical operating voltages [9], [10], [11], [12].

To assess the state-of-health (SOH) of GaN devices, it is possible to measure their dynamic electrical parameters in real-time during converter operation. For instance, SOH monitoring has been successfully implemented for power MOSFETs by observing the on-resistance [13], [14]. This data can be used to flag errors during operation and transition into fail-safe "limp" modes at the application level, where the load power is curtailed and the overall performance is limited. Furthermore, the extracted SOH data can be uploaded to the cloud to monitor aging trends, inform maintenance scheduling, and support postmortem analysis for quality assurance, as illustrated in Fig. 1.

Due to their shorter history of field use compared to silicon devices, the key factors leading to failure in GaN power devices are currently under active investigation in the literature. Several parameters have been suggested as potential precursors to device failure including the threshold voltage ($V_{\rm th}$), the on-resistance ($R_{\rm DS,on}$), the gate-source leakage current ($I_{\rm gss}$), the gate-drain capacitance ($C_{\rm gd}$), and the output capacitance ($C_{\rm oss} = C_{\rm ds} + C_{\rm gd}$) [15], [16], [17]. $C_{\rm oss}$ is a small-signal value with a highly nonlinear relationship with the drain–source voltage, $v_{\rm DS}$.

The effects of aging on the device electrical parameters can vary depending on the type of stress the device undergoes. For

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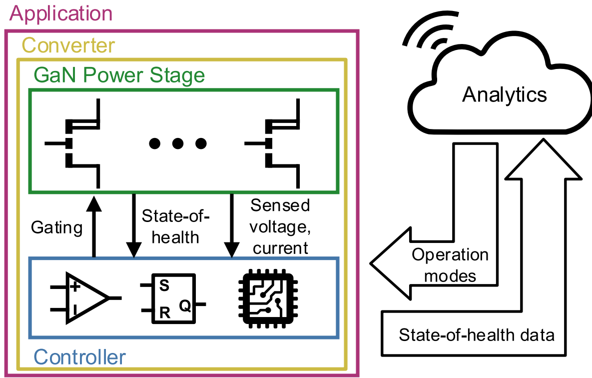

Fig. 1. Conceptual system architecture illustrating the utility of collecting device SOH data.

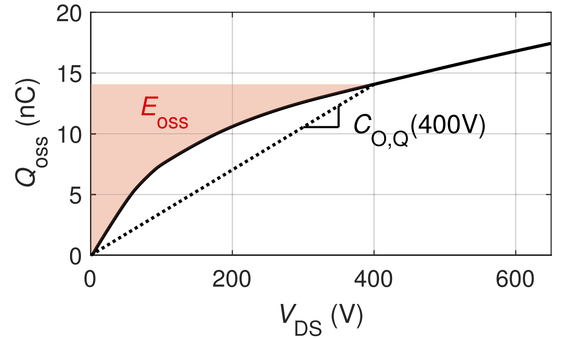

Fig. 2. Definition of the charge-equivalent linear capacitor $C_{\mathrm{O,Q}}$, illustrated at 400 V.

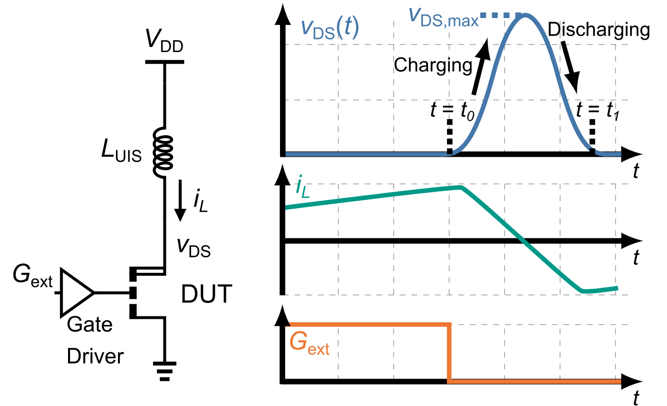

Fig. 3. Test setup and ideal waveforms for a UIS test on a GaN device used to extract large-signal $C_{\mathrm{O,Q}}$.

power devices, typical stress mechanisms include gate overvoltage, drain overvoltage, SC events, and high temperatures. In high-frequency converters, it is possible for SC events to occur during operation due to gating errors, parasitic HEMT turn-ON, or faulty load conditions [17]. Repetitive SC stress has been shown to cause damage to the aluminium gallium nitride/gallium nitride (AlGaN/GaN) region under the field plates [15]. The high-electric field and high current during SC events can produce electrons with sufficient energy to be injected from the channel to the AlGaN/GaN barrier or the surface and become trapped or induce lattice damage [18]. Successive SC events gradually fill the trap states and influence the electric field distribution within the device [19]. This change in electric field due to the traps accumulating negative charge alters the device parameters including V_{th}, $R_{\mathrm{DS,on}}$, and C_{oss}. It has been observed that some of the damage can partially recovery either under a relaxation period at room temperature, or a high-temperature soak [17], [20]. However, it is important to note that not all aspects of degradation are recoverable, underscoring the complexity of GaN device reliability [21]. In addition, the damage to the AlGaN/GaN region from SC events is more pronounced under high-voltage stress even for the same total energy, likely owing to higher electric fields and peak power [22]. The density of trapped charges in the AlGaN barrier layer is proportional to C_{oss}, with additional SC damage leading to a reduction in the measured value of C_{oss} [23].

Performing in situ C_{oss} extraction for SOH monitoring is challenging, since during converter operation, large-swing, high-dv/dt signals are applied to the power device output capacitance [24]. Because of the large-signal nature of the device v_{DS}, a charge-equivalent linear capacitance, $C_{\mathrm{O,Q}}$, is often defined to perform charge-based calculations in converter applications. $C_{\mathrm{O,Q}}$, is defined as

$$C_{\mathrm{O,Q}}(v_{\mathrm{DS,max}}) = \frac{Q_{\mathrm{oss}}(v_{\mathrm{DS,max}})}{v_{\mathrm{DS,max}}} = \frac{\int_0^{v_{\mathrm{DS,max}}} C_{\mathrm{oss}}(v)dv}{v_{\mathrm{DS,max}}} \quad (1)$$

which is illustrated in Fig. 2. $C_{\mathrm{O,Q}}(v_{\mathrm{DS,max}})$ is a lumped measurement that gives the same charging time as $C_{\mathrm{oss}}(v)$ while the drain voltage rises from zero to a selected voltage, $v_{\mathrm{DS,max}}$ [25]. Given the relationship between $C_{\mathrm{O,Q}}$ and C_{oss}, it is desirable to demonstrate that $C_{\mathrm{O,Q}}$ also decreases with SC stress and can be used as an aging indicator. Measuring $C_{\mathrm{O,Q}}$ during converter operation is more straightforward than measuring C_{oss}, since the large voltage swings experienced by the devices are key to capturing $C_{\mathrm{O,Q}}$.

Prior works have shown that unclamped inductive switching (UIS) conditions enable the estimation of GaN $C_{\mathrm{O,Q}}(v_{\mathrm{DS,max}})$ [26]. A typical UIS test circuit and resulting waveform are shown in Fig. 3. Representing the OFF-state device with an equivalent capacitance of $C_{\mathrm{O,Q}}$, the expression for $V_{\mathrm{DS}}(s)$ is derived to be

$$V_{\mathrm{DS}}(s) = \frac{1}{1 + s^2 L_{\mathrm{UIS}} C_{\mathrm{O,Q}}(v_{\mathrm{DS,max}})}. \quad (2)$$

Thus, the corner frequency of this second-order system is

$$w_o = \sqrt{\frac{1}{L_{\mathrm{UIS}} \cdot C_{\mathrm{O,Q}}(v_{\mathrm{DS,max}})}} \quad (3)$$

which can be related to $(t_1 - t_0)$ in Fig. 3 as

$$t_1 - t_0 = \frac{2\pi}{2w_o} = \pi\sqrt{L_{\mathrm{UIS}} \cdot C_{\mathrm{O,Q}}(v_{\mathrm{DS,max}})}. \quad (4)$$

This can be rearranged to estimate the large-signal $C_{\rm O,Q}$, with

$$C_{\rm O,Q}(v_{\rm DS,max}) = \frac{1}{L_{\rm UIS}}\left(\frac{t_1 - t_0}{\pi}\right)^2 \quad (5)$$

where the peak of the resonant voltage corresponds to the $v_{\rm DS}$ where $C_{\rm O,Q}$ is estimated.

The UIS test setup is suitable for measuring $C_{\rm O,Q}$ to demonstrate its viability as an aging indicator. However, performing this measurement in a converter during operation is challenging as it requires accurate, high-bandwidth measurements ranging up to 650 V. For in situ measurements, the principle of finding the charge-equivalent capacitance can be applied to a soft-switching converter with a linear inductor. In order to achieve zero-voltage switching (ZVS), energy balance is required between the inductor and the switch-node capacitance. For a half-bridge with equally-sized switches, the capacitance seen at the switch-node is equal to twice the device $C_{\rm O,Q}$, assuming a negligible contribution from the parasitic components.

In the past works of [15] and [23], the effect of aging on $C_{\rm oss}$ was discussed primarily within the context of modeling the device's operational lifetime. However, there has been no exploration of measuring this parameter during converter operation and the extension of aging analysis from $C_{\rm oss}$ to $C_{\rm O,Q}$ has not been addressed.

Monitoring GaN aging precursors during converter operation is the focus of the work in [27] and [28], but neither approach uses $C_{\rm O,Q}$ as the SOH indicator. A custom silicon integrated circuit (IC) for measuring the gradual rise in GaN dynamic on-resistance, denoted as $r_{\rm DS,on}$, which occurs as a result of aging, is presented in [27]. It is possible to use $r_{\rm DS,on}$ to provide SOH information; however, measuring $r_{\rm DS,on}$ requires temperature monitoring and a sophisticated machine learning algorithm to estimate device health. Similarly, Du et al. [28] also presented a custom silicon IC for monitoring GaN aging and dielectric breakdown. The switching turn-ON time, $T_{\rm ON}$, is chosen as the SOH indicator as it has minimal temperature dependence. Accurately measuring $T_{\rm ON}$ is challenging due to GaN devices' high switching speeds. Measurement error can be mitigated through a closed-loop solution, however, this approach is limited as switching speeds continue to increase. In [29], a GaN IC monitors the voltage applied to the gate during turn-ON to provide feedback to the driver to avoid damage caused by overvoltage. While this approach showcases the feasibility of utilizing monolithic GaN to capture device parameters, it does not address SOH indication.

In this work, the focus is on monitoring the variation in device capacitance, $C_{\rm O,Q}$, as an SOH indicator in GaN converters. To achieve this, two main contributions are highlighted. The first contribution is to characterize $C_{\rm O,Q}$ under SC aging to confirm it is a viable alternative indicator to $C_{\rm oss}$. The second contribution is to propose an in situ method of measuring $C_{\rm O,Q}$ during soft-switching converter operation, without requiring high-bandwidth current or voltage measurements. Compared to our prior literature [1], this article builds on the depth of the results characterizing $C_{\rm O,Q}$ as an aging indicator. GaN devices of different sizes and from multiple manufacturers are characterized. Furthermore, the design considerations for the circuit blocks needed for the in situ $C_{\rm O,Q}$ detection are elaborated on, and the limitations of the $C_{\rm O,Q}$ extraction based on the converter architecture are discussed.

TABLE I
DESCRIPTION OF AGED GAN DEVICES

Manufacturer	Part number	$R_{\rm DS,on}$	Identifier
GaN systems	GS-065-008-1-L	225 mΩ	DUT1
GaN systems	GS-065-011-1-L	150 mΩ	DUT2
STMicroelectronics	SGT120R65AL	120 mΩ	DUT3

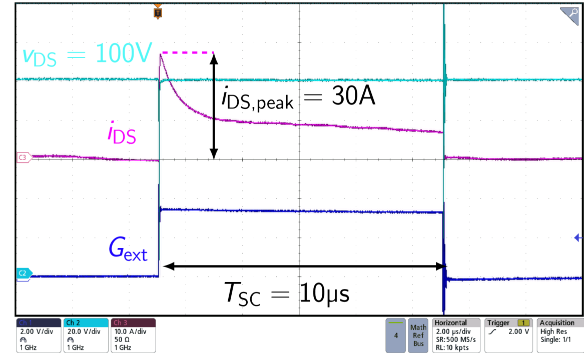

Fig. 4. Measured SC current of DUT1 for a 10 μs pulse at $v_{\rm DS} = 100$ V.

The rest of this article is organized as follows. Aging results to illustrate the usability of $C_{\rm O,Q}$ as an SOH metric are presented in Section II. The description of the converter architecture and control scheme for the proposed in situ aging monitoring is detailed in Section III. The performance of the in situ method is evaluated and verified experimentally in a synchronous buck converter in Section IV. Finally, Section V concludes this article.

II. EXPERIMENTAL AGING OF $C_{\rm O,Q}$ IN GAN

To experimentally demonstrate that $C_{\rm O,Q}$ decreases with SC stress and can be used as an aging indicator, SC aging was performed on the three different 650-V Schottky gate p-GaN HEMTs listed in Table I. The device under test (DUT) identifiers DUT1, DUT2, and DUT3 are used to distinguish between the devices. Two different device manufacturers are represented and the size of the devices increases from DUT1 to DUT3.

To age the devices, multiple SC pulses were performed for each DUT using the setup shown in Fig. 5(a). Each SC pulse had a duration of 10 μs with a duty cycle of 0.05%, for a total single-cycle duration of 20 ms. For the 8 A-rated DUT1 with a $V_{\rm test}$ value of 100 V, the maximum initial current reaches 30 A, as shown in Fig. 4. Due to self-heating, $i_{\rm DS}$ decreases during the SC pulse, with a final value of 6.7 A.

The ability of the devices to withstand SC pulses at increasing voltages was also tested. The $i_{\rm DS}$ during SC pulses at increasing $V_{\rm test}$ values from 50 to 350 V in 50 V increments are shown for DUT1 in Fig. 5(b). Higher $V_{\rm test}$ voltages result in similar peak currents, with decreasing final current values as the device dissipates more power. A 10 μs pulse at $V_{\rm test} = 400$ V was also

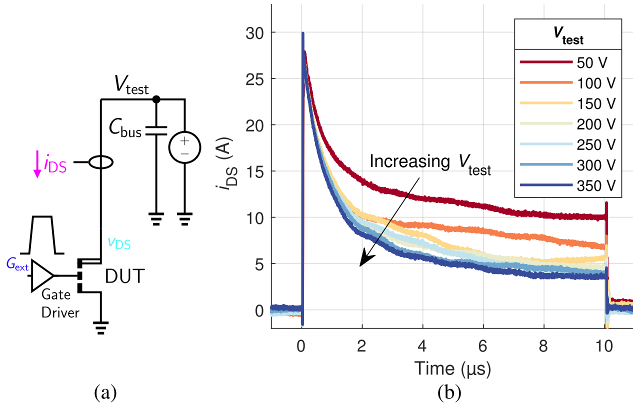

Fig. 5. (a) SC test circuit. (b) Measured SC current of DUT1 for V_{test} increasing in 50 V increments up to 350 V.

TABLE II
400-V SC Withstand Test Results

Identifier	Withstand duration
DUT1	480 ns
DUT2	600 ns
DUT3	800 ns

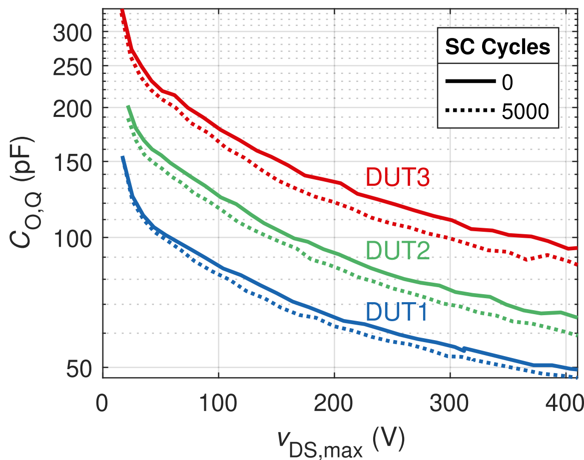

Fig. 6. Measured $C_{O,Q}$ before and after 5000 10 μs, 100 V SC cycles for each DUT.

attempted for all DUTs, resulting in failure for each tested device. Device failure is marked by an abrupt increase in the drain current. The SC withstand duration, defined as the pulse duration until device failure, was measured at $V_{test} = 400$ V for all three DUTs, and the results are presented in Table II.

The large-signal $C_{O,Q}$ for each DUT was measured before any SC pulses, and again after 100, 500, 1500, and 5000 SC pulses of 10 μs duration with a 0.05% duty cycle and $V_{test} = 100$ V. The initial and final $C_{O,Q}$ values are shown in Fig. 6. The measured capacitance increases with device size as expected, and the change in capacitance due to aging becomes slightly more significant at larger device sizes.

$C_{O,Q}$ is calculated by performing 30 independent UIS events with increasing $v_{DS,max}$ and evaluating (5) for each resonant

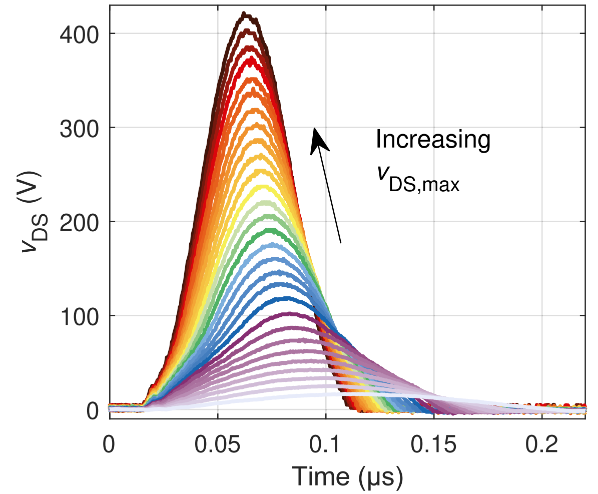

Fig. 7. Measured v_{DS} waveforms from 30 independent UIS events performed on DUT3 used to calculate $C_{O,Q}$ with (5).

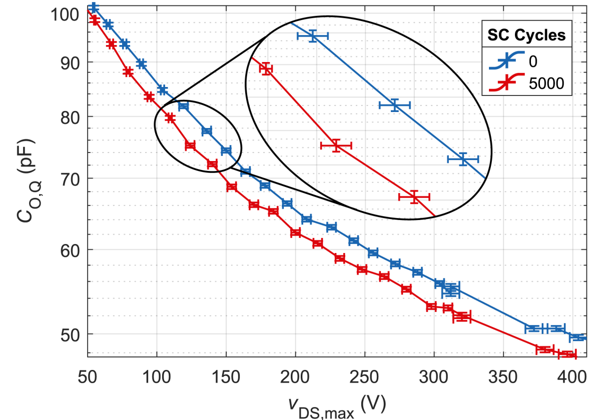

Fig. 8. Measured $C_{O,Q}$ before and after 5000 10 μs, 100 V SC cycles for DUT1 showing the measurement error.

waveform. The measured $v_{DS}(t)$ waveforms for each UIS event performed before any SC cycles on DUT3 are shown in Fig. 7. Notably, the resonant time, $(t_1 - t_0)$, decreases with increasing $v_{DS,max}$ as $C_{O,Q}$ decreases at higher voltages.

The $v_{DS}(t)$ waveforms were captured with a Tektronix MDO34 series oscilloscope. The capacitance for DUT1 in Fig. 6 is repeated in Fig. 8 with error bars associated with the capacitance calculation in (5). Despite the relatively small change in $C_{O,Q}$, there is still sufficient margin to detect aging-induced $\Delta C_{O,Q}$.

The most significant $C_{O,Q}$ decrease occurs during the first 100 SC cycles, as shown in Fig. 9. The $C_{O,Q}$ value continues to decrease with additional SC stress, but at a slower rate. After 5000 SC cycles a lower aged capacitance is measured at $v_{DS,max} = 300$ V than the unaged capacitance measured at $v_{DS,max} = 340$ V.

The relative change in $C_{O,Q}$ with increasing SC cycles is shown for each DUT in Fig. 10. The percent decrease in capacitance at each number of cycles is approximately equal for

TABLE III
AGING METRICS AND IN SITU DETECTION METHODS FOR E-MODE GAN HEMTS

	This work	[27] ISSCC 2020	[28] ISPSD 2022	[11] TIA 2019	[21] TPE 2024	[15] TPE-L 2021
Device class	650-V Schottky-gate e-mode HEMTs	$<$ 100 V e-mode GaN	$<$ 100 V e-mode GaN	650-V e-mode HEMTs	100-V and 40-V rated Schottky-type p-GaN gate HEMTs	650-V Gan Systems GS66504B
Measured in situ?	Yes	Yes	Yes	No	No	No
Aging parameters	$C_{O,Q}$	Dynamic $R_{DS,on}$	T_{on}, I_{gss}	V_{th}, I_{gs}, $R_{DS,on}$, I_{dss}	V_{th}, $I_{d,peak}$, $R_{DS,on}$	C_{oss}, T_{on}, I_{gss}, $R_{DS,on}$, V_{th}
Aging applied	Up to 5000 SC pulses with a 10 µs duration at $V_{DS} = 100$ V	Temperate sweep from 0 °–120 °C	High temperature gate bias test up to 100 °C	A single 3.2 µs SC pulse at $V_{DS} = 300$ V	Up to 100 SC pulses with a 10 µs duration. $V_{DS} =$ 40–70 V and $V_{GS} =$ 4–6 V for different devices	Up to 1000 cycles at $V_{DS} = 100$ V for a 5 µs duration
Parameter shift observed	$C_{O,Q}$ −5% to 13% depending on the device	Dynamic $R_{DS,on}$ changes from 155 mΩ to 238 mΩ across temperature. No shift from aging is investigated	T_{on} +10.3% I_{gss} used to detect dielectric failure	V_{th} +4% I_{gs} -61% $R_{DS,on}$ +5% at $V_{GS} = 2.5$ V I_{dss} −39%	$R_{DS,on}$ +7%–15%, V_{th} +0.31 V–0.88 V, $I_{d,peak}$ −7% to 33%	C_{oss} −10% to 20%, V_{th} +0.43 V, $R_{DS,on}$ +36%, I_{gss} +40 nA–160 nA, T_{on} -8 ns

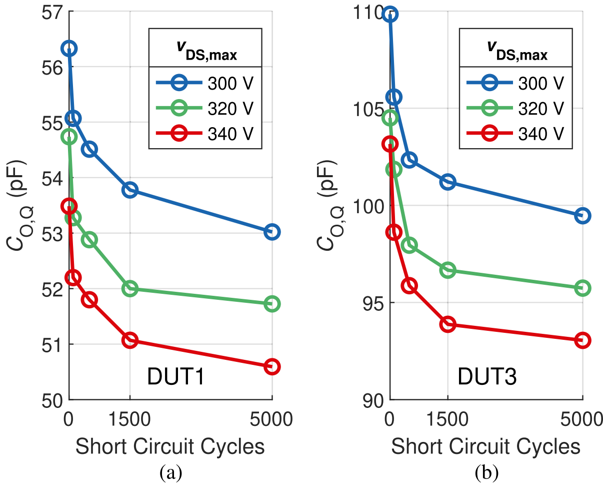

Fig. 9. Change in capacitance with SC cycles at three different $v_{DS,max}$ voltages for (a) DUT1 and (b) DUT3.

voltages beyond $v_{DS,max} = 150$ V. After 5000 cycles, the DUT1 capacitance decreases an average of $-4.9\,\%$ over the 150–420 V range. The average decrease increases to $-8.6\,\%$ for DUT2, and $-9.0\,\%$ for DUT3. The impact of drastically increasing the number of SC cycles to 50 000 is also presented in Fig. 10(c) for DUT2. The $C_{O,Q}$ is found to decrease only slightly more after 50 000 cycles compared to 5000 cycles, an average of $-10.2\,\%$ instead of $-8.6\,\%$. This supports the trend observed at lower SC cycle counts where the largest $C_{O,Q}$ decrease occurs in the initial SC cycles, with a diminishing reduction at higher cycle numbers. Given these results, with a high precision in situ extraction of $C_{O,Q}$ it should be feasible to use the large signal $C_{O,Q}$ as a precursor to aging. A 5%–10% decrease from the initial $C_{O,Q}$ measurement can be used as an indicator of significant stress applied to the device. These results are summarized alongside other metrics used to indicate aging in Table III. While a wide array of electrical parameters undergo change when exposed to SCs, they vary in suitability for in situ extraction. Section III describes a nonintrusive way to extract changes to $C_{O,Q}$ by leveraging soft-switching waveforms.

III. CONVERTER AND CONTROL ARCHITECTURE

To monitor device aging in situ, $C_{O,Q}$ must be extracted during the converter operation. To do this, the energy balance inherent to soft switching can be leveraged. In a synchronous buck converter, for the high-side device to experience ZVS, the inductor must deliver sufficient charge to raise the switch-node voltage to the input voltage, V_{HV}. The ZVS requirement can be expressed as

$$\frac{1}{2}LI_{\text{valley}}^2 \geq \frac{1}{2}Q_x(V_{HV}) \cdot V_{HV} \tag{6}$$

where I_{valley} is the lowest value of the negative inductor current, and Q_x represents the switch-node charge. Q_x can be expressed in terms of the charge-equivalent device capacitance, $C_{O,Q}$ and a layout-dependent parasitic capacitance, C_{par}, (e.g., due to probes, PCB) that is assumed to be constant with respect to applied voltage. For a synchronous buck converter with equally sized switches

$$Q_x = C_x \cdot V_{HV} = (2C_{O,Q}(V_{HV}) + C_{\text{par}})V_{HV}. \tag{7}$$

Combining (6) and (7), this leads to a ZVS requirement of

$$\frac{1}{2}LI_{\text{valley}}^2 \geq C_{O,Q}V_{HV}^2 + \frac{1}{2}C_{\text{par}}V_{HV}^2. \tag{8}$$

By tuning $|I_{\text{valley}}|$ to its minimum value to satisfy (8), $C_{O,Q}$ can be estimated as

$$C_{O,Q}(V_{HV}) = \frac{LI_{\text{valley, min}}^2 - C_{\text{par}}V_{HV}^2}{2V_{HV}^2}. \tag{9}$$

Since the goal of the in situ measurements is to detect aging by extracting a relative change in $C_{O,Q}$, $\Delta C_{O,Q}$, the $|I_{\text{valley}}|$ tuning should be performed at uniform temperature and load conditions. This reduces measurement errors caused by C_{par} when calculating a relative change in capacitance if C_{par} is affected by load or temperature. Calculating $C_{O,Q}$ in this way can be extended to other topologies by accounting for the sum

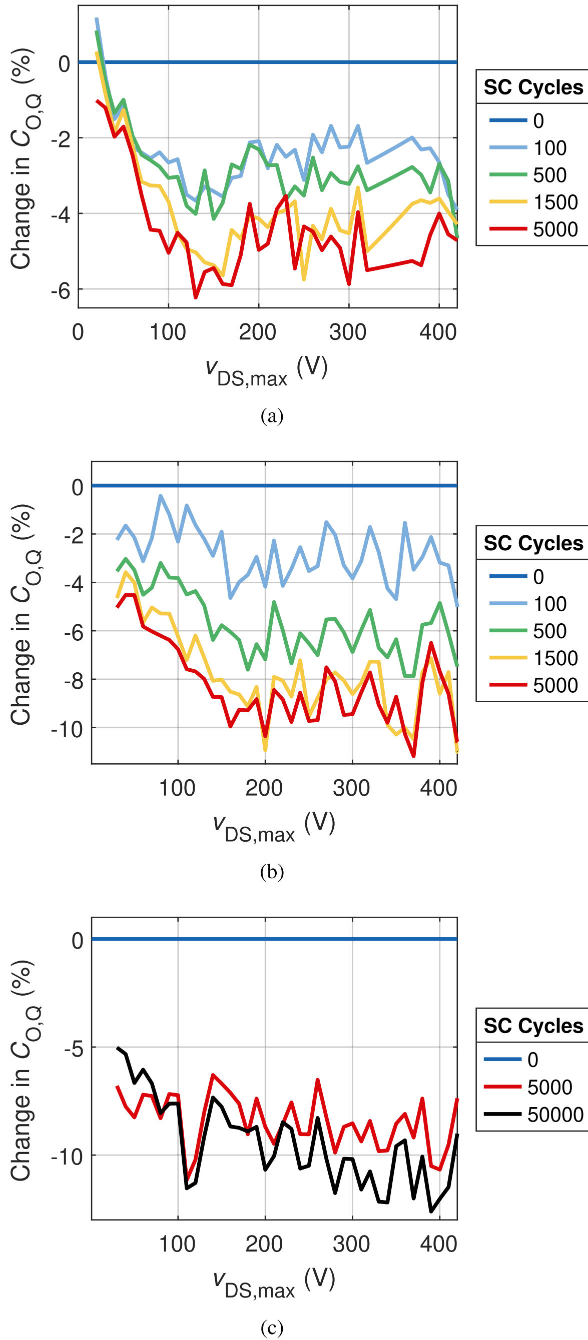

Fig. 10. Measured relative change in $C_{O,Q}$ at various aging levels for (a) DUT1, (b) DUT3, and (c) DUT2.

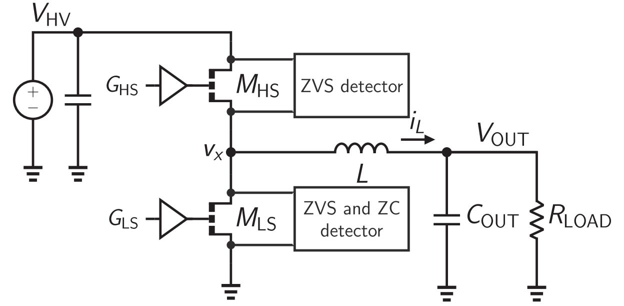

Fig. 11. Synchronous buck converter with additional sensors for operation with $C_{O,Q}$ extraction.

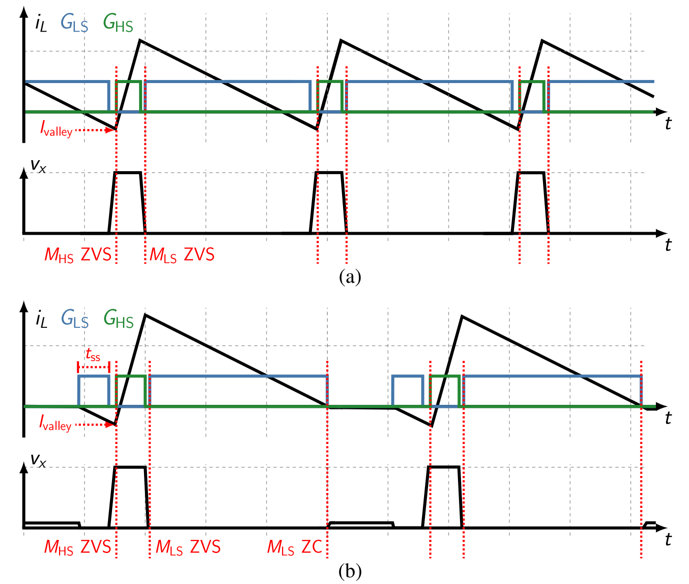

Fig. 12. Typical operating waveforms for (a) synchronous buck converter operating with negative I_{valley}, and (b) proposed control scheme with soft-switching DCM used to accurately tune I_{valley} by adjusting t_{ss}.

of device capacitances at each node that is charged by each inductor current.

For illustrative purposes, the proposed digital $C_{O,Q}$ extraction method is implemented in a synchronous buck converter, as shown in Fig. 11. To achieve ZVS, the converter operates with negative I_{valley}. Theoretical waveforms for typical synchronous-converter soft-switching operation are shown in Fig. 12(a). Using this switching sequence, it is difficult to precisely tune I_{valley} to find $|I_{valley,\,min}|$ to satisfy (8), since I_{valley} is related to the load current and the M_{HS} on-time. As an alternative approach, this work uses a different switching sequence for discontinuous conduction mode (DCM) operation that is detailed in Fig. 12(b). When the falling slope of i_L reaches zero in the proposed DCM sequence, M_{LS} is turned-OFF. Both switches then remain OFF for a period of time, similar to DCM operation in a nonsynchronous converter. Then, M_{LS} is turned back ON to generate the negative I_{valley} needed for M_{HS} soft-switching. The key advantage of the DCM sequence for this application is its additional flexibility and precision for extracting $C_{O,Q}$, since I_{valley} directly correlates with the on-time duration of M_{LS}, denoted as t_{ss}, with

$$|I_{valley}| = \frac{V_{OUT}}{L} t_{ss}. \tag{10}$$

Furthermore, the DCM sequence enables lower operating frequencies during light-load conditions and reduces the effective average current, easing the minimum on-time requirement for the high-side switch. However, there are also drawbacks to this scheme, including higher ΔI, which results in more inductor hysteresis loss, and the additional loss associated with the second turn-ON of M_{LS}. Both switching sequences require

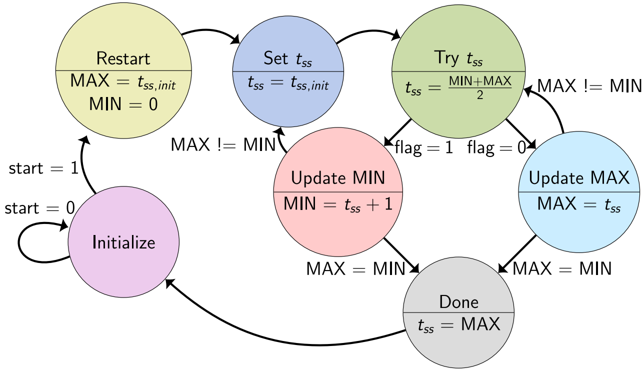

Fig. 13. State diagram of the proposed binary search algorithm.

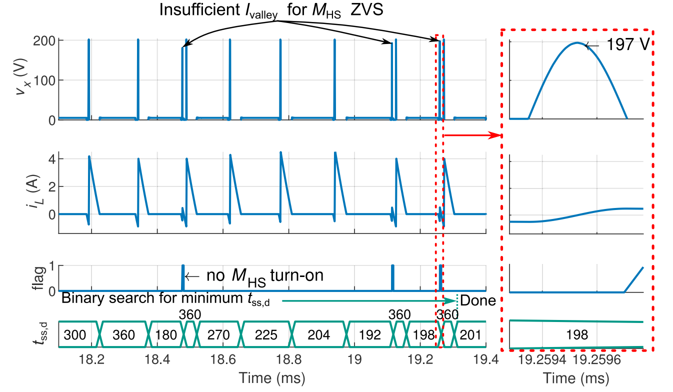

Fig. 14. Simulation waveforms of the proposed binary search algorithm.

sensing circuits to detect M_{HS} and M_{LS} ZVS. However, the DCM sequence also requires M_{LS} zero-current (ZC) sensing. Following the completion of the $C_{\mathrm{O,Q}}$ extraction, it is feasible to revert the converter's operation to the standard synchronous operation depicted in Fig. 12(a). However, the transition process falls outside the scope of this article.

To find the minimum $|I_{\mathrm{valley}}|$ to achieve ZVS for the $C_{\mathrm{O,Q}}$ extraction, a digital binary search is performed. An initial conservative estimate is chosen for $|I_{\mathrm{valley}}|$ that ensures ZVS turn-ON. During the binary search, some of the attempted $|I_{\mathrm{valley}}|$ values are insufficient to produce M_{HS} ZVS. In this case, both switches remain OFF while v_x resonates back to zero, rather than turning ON with partial soft-switching. Then, M_{LS} is turned-ON again for $t_{\mathrm{ss,init}}$ to produce I_{valley}'s initial guess, ensuring ZVS. In this way, the optimal I_{valley} can be found while constraining the deviation of V_{OUT} from the reference.

A state diagram detailing the proposed binary search algorithm is shown in Fig. 13. A missed ZVS turn-ON can be detected by recording the time between G_{LS} turning OFF with I_{valley} and turning ON again with M_{LS} ZVS. The G_{LS} OFF-time is much shorter without the G_{HS} ON-time, and the missed M_{HS} ZVS is recorded with flag $= 1$. This indicates that the algorithm should update the minimum t_{ss} value. If, on the other hand, M_{HS} achieves ZVS, the algorithm reduces the maximum t_{ss} value on the next cycle. This process continues until the minimum t_{ss} and maximum t_{ss} converge to a final value.

The results of a Cadence mixed-signal simulation verifying the algorithm are illustrated in Fig. 14. After startup, the binary search determines the minimum $|I_{\mathrm{valley}}|$ in 11 cycles. The digitized t_{ss} value, denoted as $t_{\mathrm{ss,d}}$ and linked to I_{valley} through (10), begins at 360 and ultimately converges to 201 in the *Done* state, representing the minimum $|I_{\mathrm{valley}}|$. It is worth noting that during the process, there are three instances where $t_{\mathrm{ss,d}}$ values below the final value fail to provide adequate I_{valley} for M_{HS} ZVS. In response, the initial $t_{\mathrm{ss,d}}$ of 360 is repeated after each of these cases, ensuring M_{HS} ZVS.

It is intended that the binary search algorithm used to determine the minimum $|I_{\mathrm{valley}}|$ be run under light-load conditions. Testing the different $t_{\mathrm{ss,d}}$ values disturbs the average current delivered to the load, and V_{OUT} regulation relies on the period when both switches are OFF, as depicted in the alternate switching scheme in Fig. 12(b). If a substantial load-step occurs during the extraction period, the extraction should be aborted to avoid voltage regulation failure.

To calculate $C_{\mathrm{O,Q}}$ using the converter for SOH monitoring, $I_{\mathrm{valley,min}}$ in (9) is replaced using the knowledge of the regulated V_{OUT} and the ON-time of the low-side switch, t_{ss} given in (10). This eliminates the need to measure i_L and gives

$$C_{\mathrm{O,Q}}(V_{\mathrm{HV}}) = \frac{(V_{\mathrm{OUT}}^2 t_{\mathrm{ss}}^2)/L - C_{\mathrm{par}} V_{\mathrm{HV}}^2}{2V_{\mathrm{HV}}^2}. \tag{11}$$

As it is the change in capacitance, $\Delta C_{\mathrm{O,Q}}$, rather than the exact value that is important for device health, the impact of the parasitic capacitance can be eliminated by performing a binary search to find t_{ss} under the same operating conditions. Therefore, the change in capacitance relies only on the converter operating conditions with

$$\Delta C_{\mathrm{O,Q}}(V_{\mathrm{HV}}) = (t_{\mathrm{ss},1}^2 - t_{\mathrm{ss},2}^2)\left(\frac{V_{\mathrm{OUT}}^2}{2V_{\mathrm{HV}}^2\, L}\right). \tag{12}$$

By eliminating the need for current measurement when extracting $\Delta C_{\mathrm{O,Q}}$, this SOH estimation method can operate even at very high-switching frequencies and is suitable for integration as an on-chip solution.

The minimum measurable capacitance difference, $\Delta C_{\mathrm{O,Q}}$, scales with increasing $C_{\mathrm{O,Q}}$ and depends on the converter inductance and operating voltage. The relationship between $\Delta C_{\mathrm{O,Q}}$ and the operating parameters of the converter are shown in Fig. 15 with a 5 ns resolution for the digitized t_{ss}, $t_{\mathrm{ss,d}}$. With $L = 5.6\,\mu$H, $V_{\mathrm{HV}} = 200$ V, $V_{\mathrm{OUT}} = 5$ V, and $C_{\mathrm{O,Q}} = 65$ pF, the minimum measurable $\Delta C_{\mathrm{O,Q}}$ is 0.6 pF. Based on the results of Fig. 9, this resolution is sufficient to detect the decrease in $C_{\mathrm{O,Q}}$ due to aging. For instance, at $V_{\mathrm{HV}} = 200$ V, the $\Delta C_{\mathrm{O,Q}}$ observed after aging with 5000 SC cycles was 3.26 pF for DUT1, 8.13 pF for DUT2, and 13.9 pF for DUT3. It's important to note that in this study, we have used pulsed SCs lasting 10 μs at 100 V with the aim of observing the aging process of the devices for longer, survivable conditions at a lower stress voltage. If the converter experiences a gating error that causes repeated SC events in situ, it is possible for 5000 cycles to occur within a few minutes.

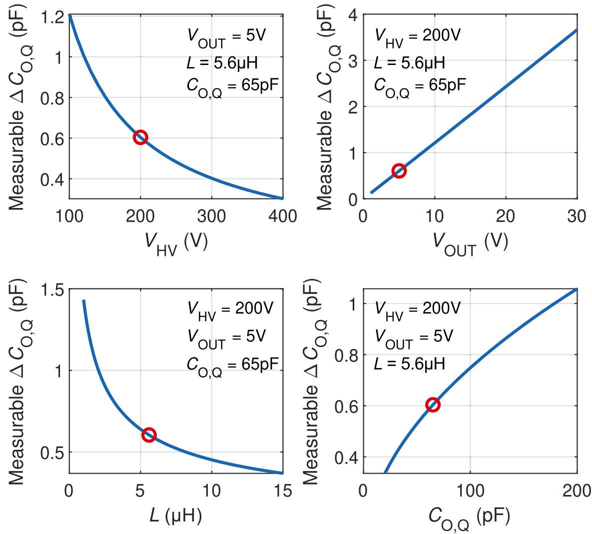

Fig. 15. Relationships between the converter operating parameters and minimum measurable $\Delta C_{\mathrm{O,Q}}$. A common operating point producing a measurable $\Delta C_{\mathrm{O,Q}}$ of 0.6 pF is highlighted in each curve.

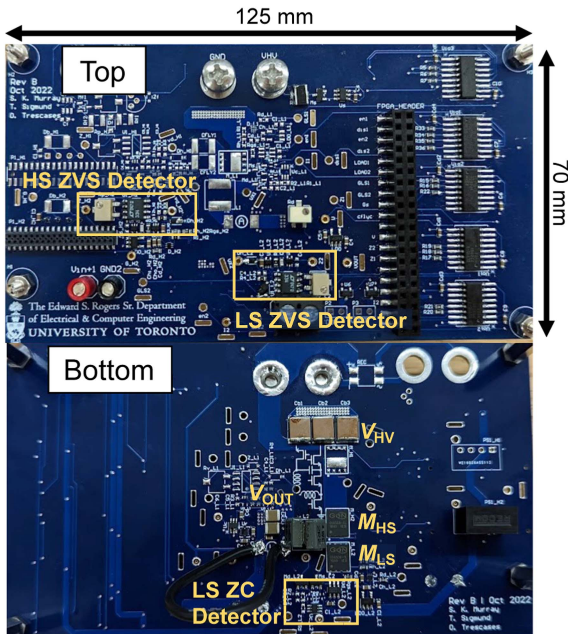

Fig. 16. Experimental prototype of the synchronous buck converter for $C_{\mathrm{O,Q}}$ extraction.

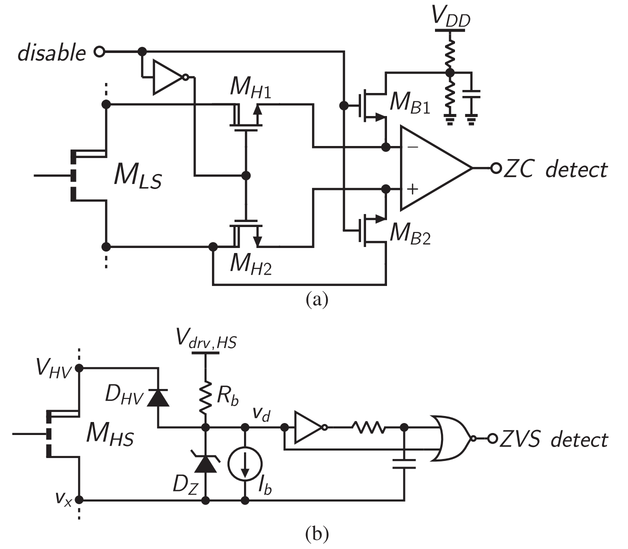

Fig. 17. Circuit implementations of the (a) ZC and (b) ZVS detectors.

TABLE IV
COMPONENT LIST FOR THE $C_{\mathrm{O,Q}}$ EXTRACTION BUCK CONVERTER

Component	**Manufacturer Part number**	**Values**
Gate driver	LMG1020YFFR	n.a.
L_{OUT}	78439346056	5.6 μH / 6.9 A
C_{OUT}	EMK325ABJ107MM-T	2× 100 μF / 16 V
C_{IN}	C5750X7T2J474K250KC	3× 0.47 μF / 630 V
M_{H}	AO3162	600 V / 34 mA
M_{B}	RUM001L02T2CL	20 V / 100 mA
ZC amplifier	TLV3603DCKR	2.5 ns, rail-to-rail
D_{HV}	RFU02VSM6STR	600 V / 0.2 A
L_{Z}	PLZ5V1C-G3/H	5.1 V
ZVS NOT/NOR gate	74LVC1G02Z-7	$t_{\mathrm{pd}} = 1.7$ ns

IV. CONVERTER OPERATION FOR IN SITU $\Delta C_{\mathrm{O,Q}}$ EXTRACTION

The proposed in situ aging detection method is validated in a 200 V-to-5 V synchronous buck converter by extracting the $\Delta C_{\mathrm{O,Q}}$ between new and aged devices. The experimental test setup is shown in Fig. 16. Two GaN Systems GS-065-008-1-L 8 A, 225 mΩ devices (DUT1) are used for the power stage. The detailed schematics of the ZVS and ZC detectors are shown in Fig. 17. The component values used in the buck converter are listed in Table IV.

The ZC detector uses two 600 V-rated MOSFETs, M_{H1} and M_{H2}, to isolate the comparator inputs from the power device during its OFF-state, when the M_{LS} drain is exposed to 200 V. During this time, devices M_{B1} and M_{B2} are ON, establishing a known state for the comparator output. Upon the second activation of M_{LS} with ZVS, the ZC detector is enabled. Subsequently, M_{B1} and M_{B2} are turned-OFF while M_{H1} and M_{H2} are turned-ON, allowing the comparator input to observe the v_{DS} of M_{LS}. The ZC detector triggers as i_L crosses zero, and the drain voltage of M_{LS} falls below its source voltage.

The ZVS detector operation relies on negative current conduction while the GaN devices are OFF. For the M_{HS} ZVS detector, as the switch node, v_x, rises past the input voltage, V_{HV}, the high-voltage blocking diode, D_{HV}, begins to conduct and lowers the v_d node voltage, which is the converted to a pulse by the subsequent falling-edge detection circuitry. The D_{HV} diodes are implemented using the smallest possible devices with sufficient voltage rating, in order to limit capacitive current injection during the switching transients. The discrete implementation of the control and circuit elements for $C_{\mathrm{O,Q}}$ extraction aims to

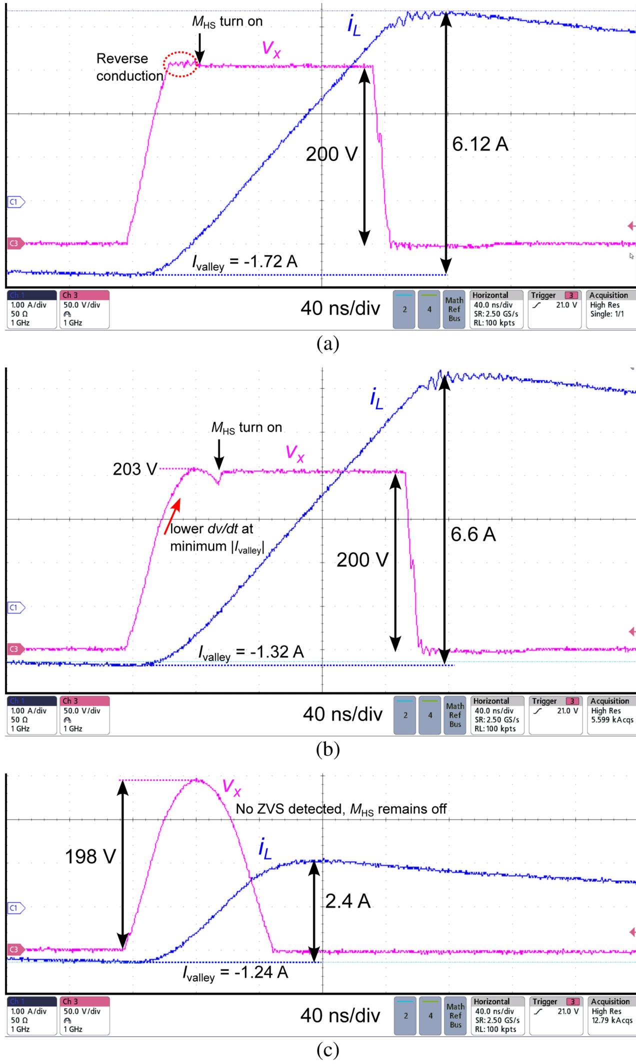

Fig. 18. Measured waveforms for the synchronous buck converter operating at $V_{HV} = 200$ V and $V_{OUT} = 5$ V with (a) excessive $|I_{valley}|$, (b) minimum $|I_{valley}|$, and (c) insufficient $|I_{valley}|$ for M_{HS} ZVS.

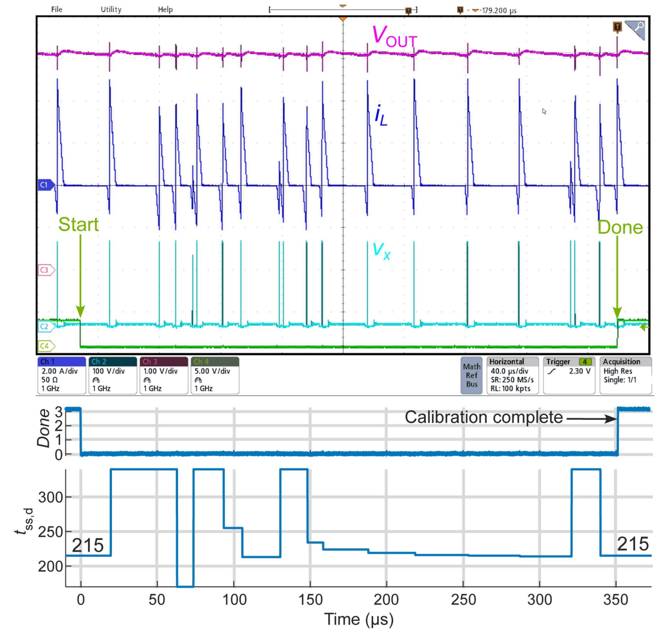

Fig. 19. Measured waveforms for the synchronous buck converter running the binary search algorithm to find the minimum $|I_{valley}|$ used to estimate $C_{O,Q}$. The minimum $|I_{valley}|$ is found after 350 μs.

serve as a proof-of-concept for potential future integration into either a silicon controller IC or a monolithic GaN solution.

The closed-loop converter operation, shown in Fig. 18, highlights the M_{HS} ZVS detection and turn-ON. The difference between excessive, minimal, and insufficient $|I_{valley}|$ for ZVS is illustrated in Fig. 18(a)–(c), respectively. With excessive $|I_{valley}|$, the device remains in reverse conduction once v_x reaches V_{HV}, dissipating the stored energy transferred from the inductor. In contrast, with minimal $|I_{valley}|$ there is limited inductor energy remaining, and the resonant shape of v_x is apparent as the dv/dt of v_x begins to decrease as v_x approaches V_{HV}. For the insufficient $|I_{valley}|$ case, v_x never reaches V_{HV}, so ZVS is not detected and M_{HS} remains OFF. As v_x falls, it resonates with i_L and the peak of i_L is approximately equal to I_{valley}.

The operation of the proposed binary search algorithm for finding minimum $|I_{valley}|$ is experimentally verified and shown in Fig. 19. The oscilloscope screen capture is aligned with data recorded by the FPGA controller to annotate the attempted $t_{ss,d}$ values as the algorithm is executing. In this figure, the algorithm is run a second time after it had already finished once, demonstrating that the algorithm repeatedly converges to the same value of $t_{ss,d} = 215$. The initial guess that is used after a missed M_{HS} turn-ON is $t_{ss,d} = 340$, corresponding to $t_{ss} = 1.7\,\mu$s and $I_{valley} = -2.08$ A. The optimal I_{valley} of -1.32 A is reached in 19 cycles, with three missed turn-ONs due to insufficient inductor energy. The experimental algorithm takes eight additional cycles to converge over the simulation algorithm as the initial t_{ss} guess is repeated twice after a missed M_{HS} turn-ON in the experimental implementation. Additional deviation of V_{OUT} due to the missed M_{HS} turn-ONs is measured to be 28 mV, corresponding to an additional 0.5 % ripple.

To detect device aging, the binary search algorithm for finding the minimum $|I_{valley}|$ was run for different input voltages both before and after the two power devices were exposed to 5000 SC cycles. Aging and $\Delta C_{O,Q}$ extraction were performed for converters operating with M_{HS} and M_{LS} implemented as DUT1, DUT2, and DUT3. The change in capacitance extracted by the converter from before to after aging is depicted in Fig. 20. For DUT1 and DUT2, across different input voltages, V_{HV}, the converter extracted a decrease between 2.0 pF and 4.9 pF. For DUT3, the decrease in capacitance ranged from 4.4 to 8.7 pF. Consistent with the results in Fig. 6, the converter operating with DUT3 experiences the largest $\Delta C_{O,Q}$.

The in situ results follow a similar overall trend to the single-device $\Delta C_{O,Q}$ results in Fig. 5. However, as the V_{DS} of M_{LS} increases while the V_{DS} of M_{HS} decreases, drawing an exact numerical comparison is challenging. The overall accuracy of

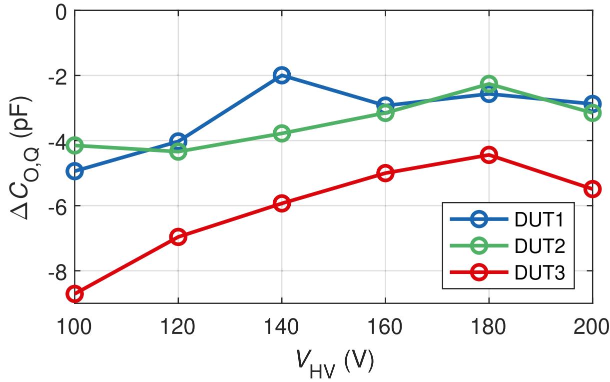

Fig. 20. Change in $C_{\mathrm{O,Q}}$ extracted in situ by operating the minimum $|I_{\mathrm{valley}}|$ algorithm on the synchronous buck converter with new and aged devices.

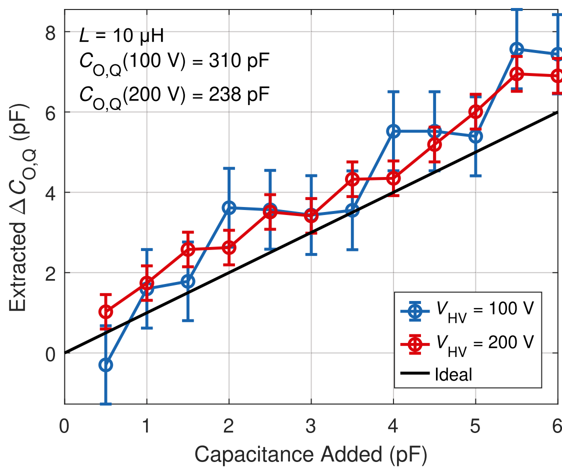

Fig. 21. Measured change in $C_{\mathrm{O,Q}}$ extracted when adding external capacitance to the synchronous buck converter operating the minimum $|I_{\mathrm{valley}}|$ algorithm. The error bars represent the quantization error of $t_{\mathrm{ss,d}}$.

$\Delta C_{\mathrm{O,Q}}$ detection is hindered by using separate PCBs for converter operation and rapid aging via SC stress, due to the large capacitance requirements of SC events.

To assess the sensitivity of the in situ measurement technique, the extracted $\Delta C_{\mathrm{O,Q}}$ is observed when a known capacitance is applied between v_x and ground. The applied capacitance increases in 0.5 pF increments, and the extraction results are presented in Fig. 21. Vertical error bars indicate the $t_{\mathrm{ss,d}}$ quantization error. The converter is operated with $L = 10\,\mu\mathrm{H}$ and with DUT2 for M_{HS} and M_{LS}. The input voltage, V_{HV}, is changed between 100 and 200 V, consequently altering the measured switch node capacitance from 310 to 238 pF. This shift affects the quantization step of the $\Delta C_{\mathrm{O,Q}}$ extraction, as illustrated in Fig. 15, where $\Delta C_{\mathrm{O,Q}}$ detection becomes more sensitive with increasing V_{HV}. The results, while slightly overestimating the added capacitance, follow the expected linear trend. The discrepancies can likely be attributed to additional PCB parasitic capacitance introduced to the switch node when the external capacitors are added. Nevertheless, the results demonstrate that the converter is capable of extracting $\Delta C_{\mathrm{O,Q}}$ values on the order of single-digit picofarads, which is promising for the viability of this in situ SOH estimation technique.

V. Conclusion

An in situ extraction technique to estimate the charge-equivalent device output capacitance in soft-switching converters was experimentally demonstrated. The proposed binary search algorithm for finding $C_{\mathrm{O,Q}}$ was experimentally verified to extract the minimum $|I_{\mathrm{valley}}|$ required for soft-switching of M_{HS}. Under the same operating conditions, temperature, and device age, the algorithm reliably converges to the same $t_{\mathrm{ss,d}}$. Through the use of the DCM control scheme, the minimum $|I_{\mathrm{valley}}|$ is located by tuning $t_{\mathrm{ss,d}}$ and without explicitly measuring the current, which is key for high-frequency operation. The detection of $\Delta C_{\mathrm{O,Q}}$ using the presented $C_{\mathrm{O,Q}}$ extraction method is also experimentally verified by operating the binary search algorithm on both new and aged GaN devices.

The aging behavior of $C_{\mathrm{O,Q}}$ in GaN devices was characterized via repeated SC stress cycles. As GaN devices undergo additional SC stress cycles, measurement results show a detectable decrease in $C_{\mathrm{O,Q}}$. For V_{DS} voltages between 150 and 400 V, the percentage $C_{\mathrm{O,Q}}$ decrease per SC cycle on each of the three devices tested remains stable, presenting a viable indicator of device aging stress.

With a well-characterized impact of aging on $C_{\mathrm{O,Q}}$ and accurate $C_{\mathrm{O,Q}}$ extraction, a $\Delta C_{\mathrm{O,Q}}$ may be observed in situ, indicating a declining SOH. The reported $\Delta C_{\mathrm{O,Q}}$ can be used inform operational changes at the converter or system level to enhance reliability.

Acknowledgment

Extended characterization of the impact of aging on C_{oss} across multiple GaN device manufacturers, analysis of in-situ C_{oss} extraction in the presence of the PCB parasitic capacitance, and a discussion on the minimum detectable change in C_{oss} based on converter operating conditions.

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