Composite Current-Constrained Control of Stand-Alone Three-Phase Inverters Under Multiple Load Conditions

Saijin Huang, Xiangyu Wang, *Senior Member, IEEE*, Guanjun Li, Xinming Wang, *Graduate Student Member, IEEE*, Shihua Li, *Fellow, IEEE*, and Qi Li

***Abstract*—With the growing penetration of renewable energy sources, distribution network protection and stability are of great importance. This article aims to propose a current limiting control scheme with antidisturbance properties to improve the reliability and power quality of stand-alone three-phase inverters under multiple load conditions (including balanced loads, unbalanced loads, and nonlinear loads). A benchmark controller is designed first to achieve voltage regulation and overcurrent protection targets under relatively ideal conditions (e.g., only subject to constant disturbances caused by parameter perturbation or linear balanced load switching). Then, considering the unbalanced and nonlinear load conditions, two composite disturbance observers are constructed to estimate the large-scale, fast-varying harmonic disturbances introduced by the multiple loads. Based on the disturbance estimates and the benchmark controller, a composite current-constrained control scheme with rigorous stability analyses is proposed. The innovative control scheme ensures good output voltage quality and strictly guarantees overcurrent protection, which is validated by the simulations and experiments. Last but not least, extended current limiting control schemes to broaden the application range and enhance the control performance are presented.**

***Index Terms*—Composite control scheme, current limiting, harmonic suppression, mismatched disturbances, multiple load conditions, three-phase inverters, voltage regulation.**

Manuscript received 25 January 2024; accepted 11 March 2024. Date of publication 25 March 2024; date of current version 16 May 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 62373099, Grant 62025302, and Grant 62173221, in part by the Key R&D plan of Jiangsu Province under Grant BE2020082-4, and in part by the Open Fund of Jiangsu Engineering Technology Center for Energy Storage Conversion and Application (China Electric Power Research Institute) under Grant NY80-23-003. Recommended for publication by Associate Editor Y. Xue. *(Corresponding author: Xiangyu Wang.)*

Saijin Huang, Xiangyu Wang, Xinming Wang, Shihua Li, and Qi Li are with the School of Automation, Southeast University, Nanjing 210096, China, and also with the Key Laboratory of Measurement and Control of Complex Systems of Engineering, Ministry of Education, Nanjing 210096, China (e-mail: hsj@seu.edu.cn; w.x.y@seu.edu.cn; wxm_seu@seu.edu.cn; lsh@seu.edu.cn; liqikj@seu.edu.cn).

Guanjun Li is with the School of Automation, Southeast University, Nanjing 210096, China, also with the Key Laboratory of Measurement and Control of Complex Systems of Engineering, Ministry of Education, Nanjing 210096, China, and also with the China Electric Power Research Institute Company, Nanjing 210003, China (e-mail: liguanjun@epri.sgcc.com.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3380322.

Digital Object Identifier 10.1109/TPEL.2024.3380322

I. Introduction

As the foreseen exhaustion of fossil fuels and environmental degradation, considerable worldwide efforts have been made to develop more renewable energy sources (e.g., wind, solar photovoltaics, hydropower, bioenergy, and ocean power). Three-phase inverter-interfaced distributed generation systems have emerged as a practical approach for integrating renewable power generations into the distribution network operating in grid-connected or stand-alone modes [1], [2], [3]. In the grid-connected mode, three-phase inverter systems aim to respond to the power demand from the upstream distribution grid [4], [5], [6]. While during stand-alone operation, three-phase inverters are isolated from the grid, and the highest priority is to supply reliable and high-quality power to local loads [7], [8], [9]. Many advanced control methods have been proposed to enhance regulation efficiency and power quality [10], [11], [12], [13], [14], such as adaptive control, sliding mode control, backstepping control, and observer-based control. Besides voltage regulation and power quality issues, overcurrent protection is necessary for stand-alone three-phase inverters since the overlarge current induced by machine starting or short-circuit fault may damage the power semiconductor devices.

Several current limiting strategies have been proposed for the inverter systems [15], [16], [17], [18], [19], mainly based on the cascade control structure (outer voltage loop and inner current loop). They can be categorized into two groups: instantaneous saturation limit and latched limit. The former limiter prevents overcurrent by placing a saturation unit in the output of the voltage controller and setting prescribed saturation values of the current reference. The latter limiter replaces the current reference with a predefined safe value during overcurrent conditions. Although the two types of current limiting strategies are simple to implement and have broad applications, they still have some defects: 1) During overcurrent stages, the inverter opens the voltage control loop and switches to current control mode (CCM), which loses the voltage controllability and leads to voltage deviations or even overvoltage; 2) In the case of a sinusoidal input signal (including the current reference signals in the natural reference frame (NARF) or the stationary reference frame (STRF) and the signals in the synchronous reference frame (SYRF) during unbalanced conditions), the output is distorted due to crest clipping, which deteriorates the voltage and

current waveforms and causes poor power quality. Therefore, designing a novel current limiting strategy to strengthen the voltage control ability and improve the power quality throughout the operation is essential and investigated emphatically in this article.

Directly voltage-controlled noncascade control structure eliminates the current control loop and can provide direct and continuous voltage control. Compared with the cascade control structure, it is more concise and is expected to have a faster transient response [16], [20], [21]. However, without the inner current control loop, the current limiting task is more challenging. Moreover, multiple load conditions (including balanced loads, unbalanced loads, and nonlinear loads) exacerbate this control problem: 1) Under the noncascade control structure, the inner states (i.e., inductor currents of the three-phase inverter) are difficult to control directly. Overcurrent protection becomes a vital issue [22]. 2) Different loads have different characteristics and affect the system differently. Generally, linear balanced load switching derives constant disturbances, and unbalanced/nonlinear loads introduce large-scale, fast-varying harmonic disturbances [23], [24], [25]. Designing a control scheme that considers these loads simultaneously and maintains good power quality is demanding. In addition, the load disturbances are mismatched under the noncascade control structure, which cannot be directly compensated [26]. 3) The load disturbances inevitably influence the currents via the same channels, and the couplings between currents and disturbances make both overcurrent protection and disturbance rejection more complicated.

To realize overcurrent protection, conventional noncascade control schemes usually select conservative control parameters to avoid excessive currents. However, the dynamic performance is sacrificed [27]. Some elegant noncascade control schemes have been proposed to accomplish control tasks under state constraints, such as invariance set (IS) principle-based control [28], [29], barrier Lyapunov function (BLF) based backstepping control [30], [31], and model predictive control (MPC) [32], [33], [34]. IS principle-based controller constrains states by constructing a particular Lyapunov function. States starting from the IS always stay within it. Because it highly depends on the Lyapunov function, it is skillful to get the maximum positive IS [35]. BLF-based backstepping controller restricts states by designing an appropriate BLF, which contains the constrained states and tends to infinity once the states approach the constraints. Due to the backstepping mechanism, the virtual controllers should be limited within the constrained domain, making the parameter selection considerably conservative [36]. MPC accomplishes the task by minimizing the cost function containing the constrained states. Nevertheless, this way is considered to be soft as it performs an indirect way to constrain states [37].

Nowadays, some simple and effective state-constrained control schemes have been proposed [38], [39]. The constraint mechanism is established by introducing a nonlinear penalty term into controller gains. If the states tend to the constraint boundaries, the penalty term tends to infinity, and the control inputs increase automatically. In this manner, the control action drags back the states and guarantees that the constraint is always satisfied. To promote this method and improve performances under disturbances, several control schemes combining the nonlinear penalty term design method and the feedforward disturbance compensation technology have been put forward [40], [41]. In [40], the speed control of a permanent magnet synchronous motor (PMSM) with current constraints and time-varying disturbances is investigated. Although it addresses the problem well from the application viewpoint, it does not provide rigorous stability analysis. Dai et al. [41] scrutinizes the current constraint and mismatched disturbance rejection problem of PMSMs and provides strict stability analysis. However, only constant disturbances are handled, and the time-varying harmonic disturbances introduced by unbalanced and nonlinear loads can not be well compensated and suppressed.

To tackle the aforementioned problems, a new current limiting control scheme based on the noncascade control structure is designed, including composite disturbance observers (CDOs) and a composite current-constrained controller. Compared with existing results, the main contributions of this article are threefold:

1) A novel current limiting control scheme for three-phase inverters is proposed. Unlike most current limiting strategies that have to switch to CCM and constrain the current reference during overcurrent stages, the proposed scheme inherits a desired current limitation at all times without additional mode switching or saturation unit. Moreover, the proposed scheme ensures that output voltages are always under control, which enhances voltage controllability and improves power quality.
2) Multiple load conditions are analyzed and handled within the current limiting framework. CDOs are constructed to estimate the constant load disturbances and fast-varying harmonics. With the proposed feedforward compensation based on the disturbance estimates, fast voltage recovery, and harmonic suppression under multiple load conditions are achieved.
3) From a theoretical perspective, the proposed control scheme further expands the types of mismatched disturbances (including mismatched constant and time-varying disturbances) handled under the nonlinear penalty term-based control frame. Besides, a novel Lyapunov function is designed to analyze the stability of the closed-loop system with nonlinear penalty terms and mismatched multiple disturbances, which provides a potential analytical tool for similar systems.

The rest of this article is organized as follows. Section II provides some preliminaries. Section III presents the design process in detail. Section IV gives the simulation and experimental results. Finally, Section V concludes this article.

II. Preliminaries

In this section, the dynamic model of the stand-alone three-phase inverter is presented, and the control problems (voltage regulation, overcurrent protection, and multiple load conditions) studied in this article are also described in detail.

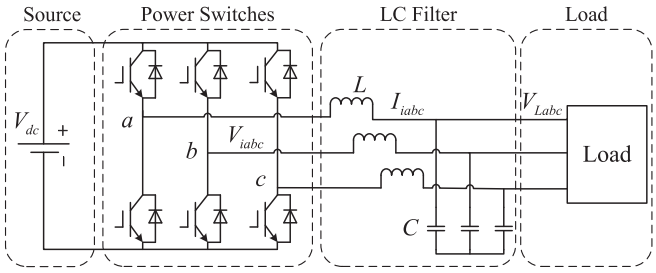

Fig. 1. Circuit diagram of a typical three-phase inverter system.

A. Dynamic Model of Three-Phase Inverters

A typical stand-alone three-phase inverter system is shown in Fig. 1, which is composed of a direct current (DC) voltage source $V_{\rm dc}$, three insulated gate bipolar transistor (IGBT) half-bridges, an output filter (L and C), and local loads.

The dynamic model of the three-phase inverter in the SYRF is formulated as

$$\begin{cases} \dot{v}_{Ld} = \omega v_{Lq} + \frac{1}{C} i_{id} - \frac{1}{C} i_{Ld} \\ \dot{i}_{id} = \omega i_{iq} - \frac{1}{L} v_{Ld} + \frac{1}{L} v_{id} \\ \dot{v}_{Lq} = -\omega v_{Ld} + \frac{1}{C} i_{iq} - \frac{1}{C} i_{Lq} \\ \dot{i}_{iq} = -\omega i_{id} - \frac{1}{L} v_{Lq} + \frac{1}{L} v_{iq} \end{cases} \tag{1}$$

where v_{Ld} and v_{Lq} are the dq-axis load voltages (i.e., controlled outputs), i_{id} and i_{iq} are the dq-axis inductor currents (i.e., constrained states), v_{id} and v_{iq} are the dq-axis inverter voltages (i.e., control inputs), i_{Ld} and i_{Lq} are the dq-axis load currents, ω is the electric angular frequency ($\omega = 2\pi f$), and f is the fundamental frequency.

B. Problem Formulation

1) Overcurrent Stress: In practical operations, overcurrent protection is necessary since the power semiconductor switches are vulnerable and highly susceptible to excessive currents. Meanwhile, machine starting, short-circuit fault, or even large control inputs for fast output regulation make the overcurrent phenomenon appear frequently. Corresponding to the inverter model (1), the control objective for overcurrent protection is to limit the inductor currents i_{id} and i_{iq} flowing through switches within safe constraints throughout the entire operation process.

In the NARF, the maximum current of each phase should be less than the maximum allowable peak current (PC) $I_{\max}$ [4], [5]. $I_{\max}$ is determined during the design process of the inverter and is usually set between two or three times the rated current of the inverter system [15], [16], [17], [18], [19]. In this article, the value is selected as two times the rated current I_N. In the SYRF, the d-axis and the q-axis current limiting values should satisfy: $I_{d-\rm limit}^2 + I_{q-\rm limit}^2 = I_{\max}^2$. In Ref. [18], $I_{d-\rm limit}$ and $I_{q-\rm limit}$ are set as $I_{\max}$ and 0, respectively. In this article, the current constraints are established as

$$\begin{cases} |i_{id}| < I_{d-\rm limit}, |i_{iq}| < I_{q-\rm limit} \\ \text{subject to } \sqrt{I_{d-\rm limit}^2 + I_{q-\rm limit}^2} = I_{\max} = 2I_N \end{cases} \tag{2}$$

Define $-M_1 = M_2 = I_{d-\rm limit}$ and $-M_3 = M_4 = I_{q-\rm limit}$, the current constraints are transformed into $M_1 < i_{id} < M_2$ and $M_3 < i_{iq} < M_4$.

2) Multiple Load Conditions: Stand-alone three-phase inverters have extensive applications, such as aerospace, ship power, microgrids, and household appliances. Different applications require the three-phase inverter to carry different types of loads, which puts higher requirements on the reliability and power quality of the inverter. This article focuses on the performance improvement of inverter systems with different load conditions and tries to enhance the voltage recovery speed after load switchings and the harmonic suppression capability under unbalanced loads and nonlinear loads.

During each load switching, load currents i_{Ld} and i_{Lq} are disturbed first and, in turn, impact the whole system. i_{Ld} and i_{Lq} are regarded as disturbances to model the influence caused by the load variations. For unbalanced loads and nonlinear loads, harmonic load currents are introduced, which in turn induces output voltage distortion. In the SYRF, open-loop controlled three-phase inverters with unbalanced loads output voltages contain DC components and second-order harmonic components, and the output voltages with nonlinear loads contain DC components and $6n$-order harmonic components ($n \in \mathbb{Z}^+$). Controllers should be able to eliminate these fast-varying harmonic components to reduce the total harmonic distortion (THD) value and improve the output voltage quality.

3) Overall Control Objective: According to the above-mentioned, the control objective of this article is to design a control scheme such that the output voltages v_{Ld} and v_{Lq} track reference voltages accurately and quickly, even under multiple load conditions. Meanwhile, overcurrent protection (2) should be always guaranteed.

Denote v_{Ld}^* and v_{Lq}^* as the reference signals, which are DC input signals. Define voltage tracking errors $x_1 = v_{Ld}^* - v_{Ld}$ and $x_2 = v_{Lq}^* - v_{Lq}$. Besides, define $x_3 = -\omega v_{Lq}^* - i_{id}/C$ and $x_4 = \omega v_{Ld}^* - i_{iq}/C$. The system (1) is transformed into

$$\begin{cases} \dot{x}_1 = \omega x_2 + x_3 + d_1 \\ \dot{x}_2 = -\omega x_1 + x_4 + d_2 \\ \dot{x}_3 = \omega x_4 - \frac{1}{CL} x_1 + (\frac{1}{CL} - \omega^2) v_{Ld}^* - \frac{1}{CL} v_{id} \\ \dot{x}_4 = -\omega x_3 - \frac{1}{CL} x_2 + (\frac{1}{CL} - \omega^2) v_{Lq}^* - \frac{1}{CL} v_{iq} \end{cases} \tag{3}$$

where $d_1 = i_{Ld}/C, d_2 = i_{Lq}/C$ are disturbances. d_1 and d_2 are mismatched and cannot be directly compensated for the reason that they are in different channels from the control inputs v_{id} and v_{iq}. Moreover, d_1 and d_2 contain multiple components, which can be decomposed into $d_1 = d_{1c} + d_{1h}$, $d_2 = d_{2c} + d_{2h}$. d_{1c} and d_{2c} are constant components. While, $d_{1h} = A_1 \sin(\alpha_1 \omega t + \varphi_1)$ and $d_{2h} = A_2 \sin(\alpha_2 \omega t + \varphi_2)$ are harmonic components, where A_1, A_2 are unknown amplitudes and φ_1, φ_2 are unknown phases. α_1, α_2 are the orders of these harmonics, which can be obtained by the spectrum analysis technology in practical applications. In addition, because the current states x_3 and x_4 are in the same channels with d_1 and d_2, the couplings between them make the current limiting and antidisturbance targets more challenging.

III. Main Results

This section presents the proposed current limiting control scheme, including two parts. In the first part, a benchmark controller is designed based on the conventional proportional-integral-derivative (PID) control method to realize voltage regulation and overcurrent protection tasks in some scenarios. To further improve power quality and suppress harmonics introduced by unbalanced/nonlinear loads, a composite current-constrained controller is proposed in the second part.

A. Benchmark Controller Design

According to the control-oriented model (3), a PID controller with precise feedback compensation is designed first

$$\begin{cases} v_{id} = f_d(x) + CL\left[k_1 x_1 + k_3 x_3 + k_{I1}\int_0^t x_1(\tau)\mathrm{d}\tau\right] \\ v_{iq} = f_q(x) + CL\left[k_2 x_2 + k_4 x_4 + k_{I2}\int_0^t x_2(\tau)\mathrm{d}\tau\right] \end{cases} \tag{4}$$

where $k_1, k_2 > 0$, $k_{I1}, k_{I2} > 0$, and $k_3, k_4 > 0$ are the control gains of the proportional terms, integral terms, and derivative terms, respectively. $f_d(x) = \omega CLx_4 - x_1 + (1-\omega^2 CL)v_{Ld}^*$ and $f_q(x) = -\omega CLx_3 - x_2 + (1-\omega^2 CL)v_{Lq}^*$ are the feedback compensation terms, which eliminate the effect of ωx_4 on x_3 dynamics and $-\omega x_3$ on x_4 dynamics and help decouple.

From the current constraints (2), $M_1 < i_{id} < M_2$ and $M_3 < i_{iq} < M_4$. For the transformed system (3), the constraints accordingly become $\underline{N}_3 < x_3 < \overline{N}_3$ and $\underline{N}_4 < x_4 < \overline{N}_4$, where $\underline{N}_3 = -\omega v_{Lq}^* - M_2/C$, $\overline{N}_3 = -\omega v_{Lq}^* - M_1/C$, $\underline{N}_4 = \omega v_{Ld}^* - M_4/C$ and $\overline{N}_4 = \omega v_{Ld}^* - M_3/C$.

Based on the basic controller (4) and the nonlinear penalty design idea, the benchmark current limiting controller (CCPID) is designed as

$$\begin{cases} v_{id} = f_d(x) + CL\left\{k_1 x_1 + [k_3 + g_d(x_3)]\, x_3\right\} \\ \qquad +CLk_{I1}\int_0^t x_1(\tau)\mathrm{d}\tau \\ v_{iq} = f_q(x) + CL\left\{k_2 x_2 + [k_4 + g_q(x_4)]\, x_4\right\} \\ \qquad +CLk_{I2}\int_0^t x_2(\tau)\mathrm{d}\tau \end{cases} \tag{5}$$

where $g_d(x_3) = l_1/((\overline{N}_3 - x_3)(x_3 - \underline{N}_3))$ and $g_q(x_4) = l_2/((\overline{N}_4 - x_4)(x_4 - \underline{N}_4))$. The current limiting mechanisms are established through the two nonlinear penalty terms $g_d(x_3)$ and $g_q(x_4)$. When the currents approach the constraint boundaries, the terms become larger automatically, and the gains of the derivative terms increase accordingly. With the increasing effect of lead correction, the current states x_3 and x_4 are dragged away from the boundaries, and overcurrent protection is achieved.

Since the benchmark controller (5) is designed under the directly voltage-controlled noncascade control structure, no mode switching and saturation unit is required, and voltage regulation and overcurrent protection are maintained all the time, which improves the voltage quality and system safety. Moreover, the benchmark CCPID controller is revised based on the PID controller, which is simple to implement.

B. Current Limiting Control Scheme Design

The benchmark CCPID controller (5) can accomplish the control objective in some relatively ideal scenarios as the PID control utilizing feedback regulation achieves zero steady-state error tracking only with constant disturbances (e.g., parameter perturbation or linear balanced load switching). For the large-scale, fast-varying harmonic disturbances caused by unbalanced and nonlinear loads, it is challenging to finish the antidisturbance task directly and quickly, and it fails to stop voltage fluctuations. In this section, a new current limiting control scheme is designed, with voltage tracking and current constraint functionalities as the benchmark controller (5). Furthermore, it enhances antidisturbance capabilities and suppresses harmonics.

1) CDO Design: Based on the transformed system (3), two CDOs are designed for the disturbance estimation of the d-axis subsystem and the q-axis subsystem, respectively.

$$\begin{cases} \dot{\eta}_{i,1} = h_i + \eta_{i,2} + \eta_{i,3} + \beta_{i,1}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,2} = \beta_{i,2}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,3} = \alpha_i\omega\eta_{i,4} + \beta_{i,3}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,4} = -\alpha_i\omega\eta_{i,3} + \beta_{i,4}(x_i - \eta_{i,1}) \end{cases} \tag{6}$$

where $i = 1, 2$, $\eta_{1,1}, \eta_{1,2}, \eta_{1,3}$, and $\eta_{1,4}$ are estimates of d-axis components x_1, d_{1c}, d_{1h}, and $\dot{d}_{1h}/(\alpha_1\omega)$, $\eta_{2,1}, \eta_{2,2}, \eta_{2,3}$, and $\eta_{2,4}$ are estimates of q-axis components x_2, d_{2c}, d_{2h}, and $\dot{d}_{2h}/(\alpha_2\omega)$, $h_1 = \omega x_2 + x_3$, $h_2 = -\omega x_1 + x_4$. $\beta_{i,1}, \beta_{i,2}, \beta_{i,3}, \beta_{i,4}$ are observer gains to be determined.

Denote estimation errors $e_{i,1} = \eta_{i,1} - x_i, e_{i,2} = \eta_{i,2} - d_{ic}, e_{i,3} = \eta_{i,3} - d_{ih}, e_{i,4} = \eta_{i,4} - \dot{d}_{ih}/(\alpha_i\omega)$, $i = 1, 2$. Taking time derivatives of the estimation errors, from (3) and (6), the estimation error systems are obtained

$$\dot{E}_i = H_i E_i + \sigma_i \tag{7}$$

where $i = 1, 2$, $E_i = [e_{i,1}, e_{i,2}, e_{i,3}, e_{i,4}]^T$, $\sigma_i = [0, -\dot{d}_{ic}, 0, 0]^T$ and $H_i = \begin{bmatrix} -\beta_{i,1} & 1 & 1 & 0 \\ -\beta_{i,2} & 0 & 0 & 0 \\ -\beta_{i,3} & 0 & 0 & \alpha_i\omega \\ -\beta_{i,4} & 0 & -\alpha_i\omega & 0 \end{bmatrix}$.

Proposition 1: If the observer gains $\beta_{i,1}, \beta_{i,2}, \beta_{i,3}, \beta_{i,4}$ of the CDOs (6) are selected to make H_i in (7) be Hurwitz matrices, then the estimation errors asymptotically converge to zero, i.e., $\lim_{t\to\infty} e_{i,j}(t) = 0$ $(i = 1, 2,\ j = 1, \ldots, 4)$.

Proof: See Appendix A. □

Remark 1: The observer gains are selected by assigning reasonable observer poles (i.e., p_1 of H_1 and p_2 of H_2). Generally, the farther the poles are set, the faster the disturbances are estimated, but the more noise is introduced accordingly. Moreover, overlarge observer gains may induce overshoot. Therefore, the poles should be assigned appropriately, considering the tradeoff between the estimation speed and these defects.

For simplicity, denote $\hat{d}_1 = \eta_{1,2} + \eta_{1,3}$, $\hat{d}_2 = \eta_{2,2} + \eta_{2,3}$, $e_{d_1} = e_{1,2} + e_{1,3}$, and $e_{d_2} = e_{2,2} + e_{2,3}$.

2) Composite Current-Constrained Controller Design: As the constrained states (x_3 and x_4) and the mismatched disturbances (d_1 and d_2) are both in the dynamics of the voltage tracking error ($\dot{x}_1$ and $\dot{x}_2$), in the steady state, $x_3 = -\omega x_2 - d_1$ and $x_4 = \omega x_1 - d_2$. Overlarge disturbances inevitably lead to

constraint (i.e., $\underline{N}_3 < x_3 < \overline{N}_3$ and $\underline{N}_4 < x_4 < \overline{N}_4$) unsatisfaction. Hence, the following assumption is made for the mismatched disturbances.

Assumption 1: The maximum absolute values of the disturbances ($d_1(t)$ and $d_2(t)$) are smaller than the minimum absolute values of the constraint boundaries ($\min\{|\underline{N}_3|, |\overline{N}_3|\}$ and $\min\{|\underline{N}_4|, |\overline{N}_4|\}$).

Remark 2: For the d-axis subsystem, because the reference voltage of the q-axis is zero, the minimum absolute value of the d-axis constraint boundary equals $I_{d-\text{limit}}/C$ and is defined as N_{3_m}. Based on the inverter system (1), $i^*_{id}/C = i^*_{Ld}/C$ at steady state (i^*_{id} and i^*_{Ld} are the steady-state values under rated conditions). Since the constraint value is two times the rated current, the current induced by the load disturbance d_1 can be two times the nominal load current, which covers a wide range of load conditions. In terms of the q-axis subsystem, $i^*_{iq}/C = \omega v^*_{Ld} + i^*_{Lq}/C$ at steady state under rated conditions. The minimum absolute values of the q-axis constraint boundary is $N_{4\_m} = \omega v^*_{Ld} + I_{q-\text{limit}}/C$, and $d_2 = i_{Lq}/C$. Because of the coupling term ωv^*_{Ld}, the q-axis assumption is more accessible to satisfy than the d-axis.

Based on the benchmark controller (5) and the disturbance estimates obtained from the observers (6), a composite current-constrained controller (CDOB-CC) is designed as

$$\begin{cases} v_{id} = f_d(x) + CL\left\{k_1 x_1 + [k_3 + g_d(x_3)]\,(x_3 + \hat{d}_1) + \dot{\hat{d}}_1\right\} \\ v_{iq} = f_q(x) + CL\left\{k_2 x_2 + [k_4 + g_q(x_4)]\,(x_4 + \hat{d}_2) + \dot{\hat{d}}_2\right\} \end{cases} \tag{8}$$

where k_1, k_2, k_3, k_4, l_1, and l_2 are positive control parameters.

Remark 3: Unlike the benchmark CCPID controller (5), which uses the integral action to eliminate disturbance-induced deviations, the CDOB-CC controller rejects disturbances through feedforward compensation. Without the integral terms of accumulating errors for correction and directly compensating the disturbance estimates into the internal states (i.e., $x_3 + \hat{d}_1$ and $x_4 + \hat{d}_2$), the CDOB-CC controller achieves better disturbance rejection performance. Further, different from the integral action that fails to handle voltage fluctuations caused by harmonics, the CDOB-CC controller can effectively suppress harmonics with harmonic estimation by the CDOs and the feedforward harmonic compensation.

Substituting the controller (8) into the system (3), the closed-loop system is expressed as

$$\begin{cases} \dot{x}_1 = \omega x_2 + \tilde{x}_3 - e_{d_1} \\ \dot{x}_2 = -\omega x_1 + \tilde{x}_4 - e_{d_2} \\ \dot{\tilde{x}}_3 = -k_1 x_1 - \left[k_3 + \frac{l_1}{(\overline{N}_{31} - \tilde{x}_3)(\tilde{x}_3 - \underline{N}_{31})}\right]\tilde{x}_3 \\ \dot{\tilde{x}}_4 = -k_2 x_2 - \left[k_4 + \frac{l_2}{(\overline{N}_{41} - \tilde{x}_4)(\tilde{x}_4 - \underline{N}_{41})}\right]\tilde{x}_4 \end{cases} \tag{9}$$

where $\tilde{x}_3 = x_3 + \hat{d}_1$, $\tilde{x}_4 = x_4 + \hat{d}_2$, $\overline{N}_{31} = \overline{N}_3 + \hat{d}_1$, $\underline{N}_{31} = \underline{N}_3 + \hat{d}_1$, $\overline{N}_{41} = \overline{N}_4 + \hat{d}_2$, $\underline{N}_{41} = \underline{N}_4 + \hat{d}_2$. Denote $X = [x_1, x_2, \tilde{x}_3, \tilde{x}_4]^T$, the closed-loop system (9) is rewritten as

$$\dot{X} = AX + B_1\zeta_3(\tilde{x}_3) + B_2\zeta_4(\tilde{x}_4) + J_1 e_{d_1} + J_2 e_{d_2} \tag{10}$$

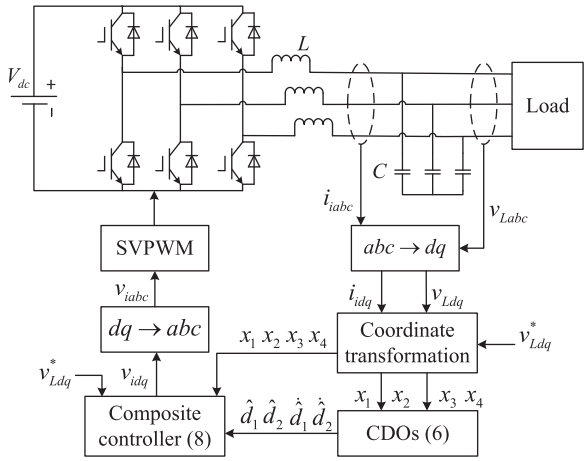

Fig. 2. Control block diagram of the proposed control scheme.

where $A = \begin{bmatrix} 0 & \omega & 1 & 0 \\ -\omega & 0 & 0 & 1 \\ -k_1 & 0 & -k_3 & 0 \\ 0 & -k_2 & 0 & -k_4 \end{bmatrix}$, $B_1 = [0, 0, -l_1, 0]^T$, $B_2 = [0, 0, 0, -l_2]^T$, $J_1 = [-1, 0, 0, 0]^T$, $J_2 = [0, -1, 0, 0]^T$, $\zeta_3(\tilde{x}_3) = \tilde{x}_3/((\overline{N}_{31} - \tilde{x}_3)(\tilde{x}_3 - \underline{N}_{31}))$, $\zeta_4(\tilde{x}_4) = \tilde{x}_4/((\overline{N}_{41} - \tilde{x}_4)(\tilde{x}_4 - \underline{N}_{41}))$. Besides, define $C_1 = [0, 0, 1, 0]$ and $C_2 = [0, 0, 0, 1]$, then $\tilde{x}_3 = C_1 X$ and $\tilde{x}_4 = C_2 X$.

Based on the above control design process, the main result of this article is given as follows.

Theorem 1: Consider the stand-alone three-phase inverter system (1) under the observers (6) and the controller (8). If the initial currents are satisfied $i_{id}(0) \in (M_1, M_2)$, $i_{iq}(0) \in (M_3, M_4)$, the Assumption 1 is met and the observer gains and the control parameters are selected to satisfy the following conditions:

a) the observer gains $\beta_{i,1}, \beta_{i,2}, \beta_{i,3}, \beta_{i,4}$ of CDOs (6) are chosen to make estimation error system matrices $H_i, i = 1, 2$ (in (7)) Hurwitz matrices;
b) the control parameters k_1, k_2, k_3, k_4 of controller (8) are chosen to make the closed-loop system matrix A (in (10)) Hurwitz matrix, and the control parameters l_1 and l_2 are selected to make b (which is given below) positive.

Then, the states of the closed-loop system (10) asymptotically converge to zero. Meanwhile, the current constraints are always guaranteed.

Proof: See Appendix B. □

The control block diagram is shown in Fig. 2.

IV. Simulations and Experiments

In this section, the performances of the proposed current limiting control scheme are tested by simulations and experiments. The benchmark CCPID controller (5) and the CDO-based controller (CDOBC) are also tested. The CDOBC controller is

TABLE I
PARAMETERS OF THE THREE-PHASE INVERTER SYSTEM

Parameters	Symbols	Nominal values
DC voltage	V_{dc} (V)	280
Switching frequency	f_s (kHz)	5
Reference voltage of d-axis	v_{Ld}^* (V)	$110\sqrt{2}$
Reference voltage of q-axis	v_{Lq}^* (V)	0
Fundamental frequency	f (Hz)	50
Filter inductor	L (mH)	10
Filter capacitor	C (μF)	6.67

TABLE II
CONTROLLER PARAMETERS FOR SIMULATIONS

Controllers	Control parameters
CDOB-CC	$p_1 = -5\text{e}3$, $p_2 = -1\text{e}3$, $k_1 = 1\text{e}8$, $k_2 = 1\text{e}7$ $k_3 = 1\text{e}4$, $k_4 = 1\text{e}4$, $l_1 = 1.28\text{e}14$, $l_2 = 1.144\text{e}13$
CDOBC-H	$p_1 = -5\text{e}3$, $p_2 = -1\text{e}3$, $k_1 = 1.1\text{e}8$, $k_2 = 1\text{e}7$ $k_3 = 1.25\text{e}4$, $k_4 = 1.1\text{e}4$
CDOBC-L	$p_1 = -5\text{e}3$, $p_2 = -1\text{e}3$, $k_1 = 0.75\text{e}8$, $k_2 = 0.7\text{e}7$ $k_3 = 0.96\text{e}4$, $k_4 = 1.1\text{e}4$
CCPID	$k_{I1} = 3\text{e}10$, $k_{I2} = 8\text{e}8$, $k_1 = 1\text{e}8$, $k_2 = 1\text{e}7$ $k_3 = 1\text{e}4$, $k_4 = 1\text{e}4$, $l_1 = 1.7\text{e}14$, $l_2 = 1.145\text{e}13$

constructed as

$$\begin{cases} v_{id} = f_d(x) + CL\left[k_1 x_1 + k_3(x_3 + \hat{d}_1) + \dot{\hat{d}}_1\right] \\ v_{iq} = f_q(x) + CL\left[k_2 x_2 + k_4(x_4 + \hat{d}_2) + \dot{\hat{d}}_2\right]. \end{cases} \tag{11}$$

The symbols are consistent with the above. The circuit parameters of the three-phase inverter system are shown in Table I.

The following three cases are implemented, in which Case 1 and Case 2 are tested in simulations, while Case 1 and Case 3 are tested in experiments for space saving.

Case 1: The inverter system no-load starts. A 100Ω balanced resistive load is added at 0.05s, and the resistance monotonically decreases from 100Ω to 80Ω and increases to 100Ω when $0.1\text{s} \le t \le 0.14\text{s}$.

Case 2: The inverter system no-load starts. A nonlinear load (i.e., a diode rectifier composed of a three-phase rectifier bridge, a 10mH inductor, a 680μF capacitor, and a 200Ω resistor) is added at 0.05s and removed at 0.1s.

Case 3: The inverter system no-load starts. A 100Ω unbalanced resistive load (phase a opened) is added at 0.05s and removed at 0.1s.

A. Simulations

The control parameters are listed in Table II, where the CDOBC controller (11) has two groups of parameters. The CDOBC-H controller (i.e., the CDOBC controller with high control gains) aims to achieve rapid dynamic performance regardless of the current constraints. In contrast, the CDOBC-L controller (i.e., the CDOBC controller with low control gains)

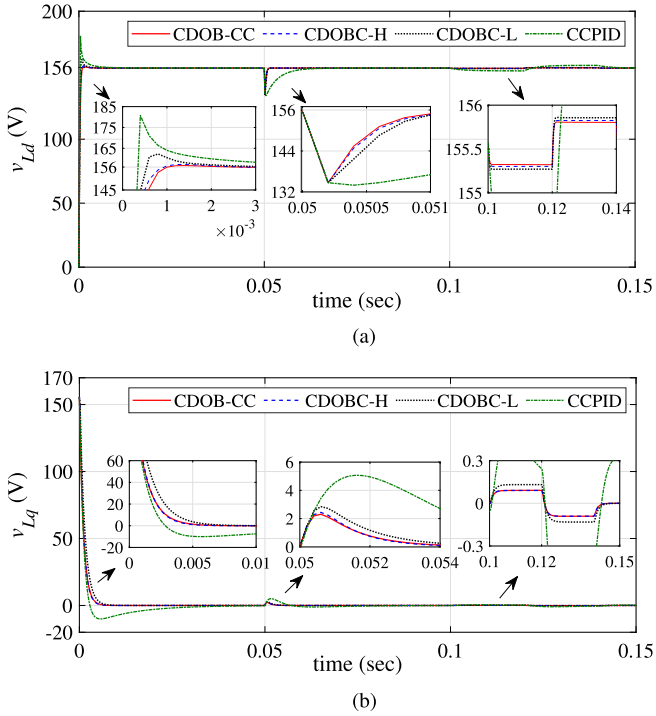

Fig. 3. Output voltage response curves under Case 1. (a) Response curves of d-axis output voltages. (b) Response curves of q-axis output voltages.

satisfies the constraints throughout the process. In addition, to ensure the fairness of comparison, the control parameters are tuned repeatedly to make the control amplitudes of the four controllers at the same level. During simulations, the current constraints are $-M_1 = M_2 = 3.6\text{A}$, $-M_3 = M_4 = 0.6\text{A}$.

1) Case 1: Figs. 3–5 depict the curves of dq-axis output voltages, inductor currents, and control inputs of the closed-loop inverter systems under the above four control schemes. It can be seen from Fig. 3 that the output voltage tracking performances of the proposed CDOB-CC controller are close to the performances of the CDOBC-H controller and are better than those of the CDOBC-L controller. In addition, because the CCPID controller can only suppress disturbances by large integration, the dynamic performances are greatly sacrificed. Moreover, the disturbance rejection and voltage recovery effects are far worse than the three CDO-based control schemes.

Regarding the current constraints, Fig. 4 shows that the dq-axis currents of the CDOB-CC controller, the CCPID controller, and the CDOBC-L controller strictly satisfy the constraints. In contrast, the currents of the CDOBC-H controller far exceed the limitations. Fig. 5 demonstrates similar control amplitudes, which confirms the comparison fairness.

2) Case 2: Figs. 6–8 display the response curves of the inverter system under Case 2. Because of the nonlinear load, $6n$-order harmonic disturbances are introduced into the system. By setting $\alpha_i = 6n\,(n \in \mathbb{Z}^+)$, the time-varying harmonic disturbances can be estimated and suppressed. In this test, by using the fast Fourier transform (FFT), the main components of the disturbances are calculated to be six-order harmonics. Hence, $\alpha_i = 6\,(i = 1, 2)$.

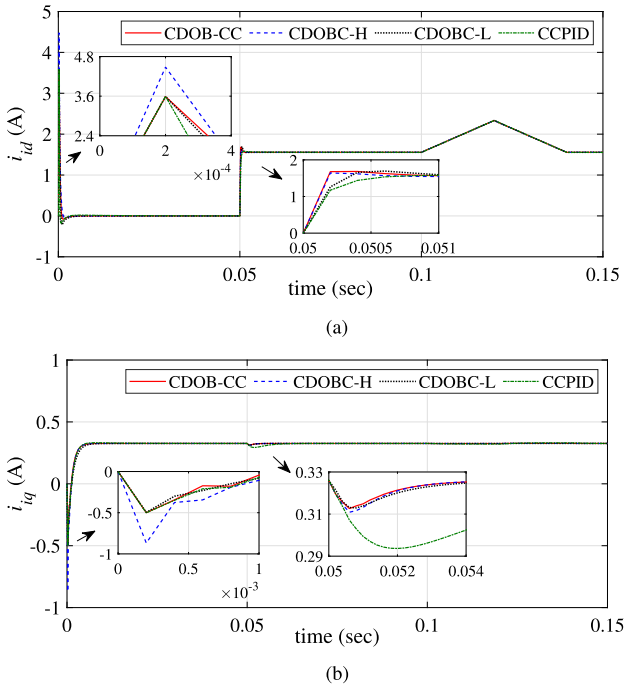

Fig. 4. Inductor current response curves under Case 1. (a) Response curves of d-axis inductor currents. (b) Response curves of q-axis inductor currents.

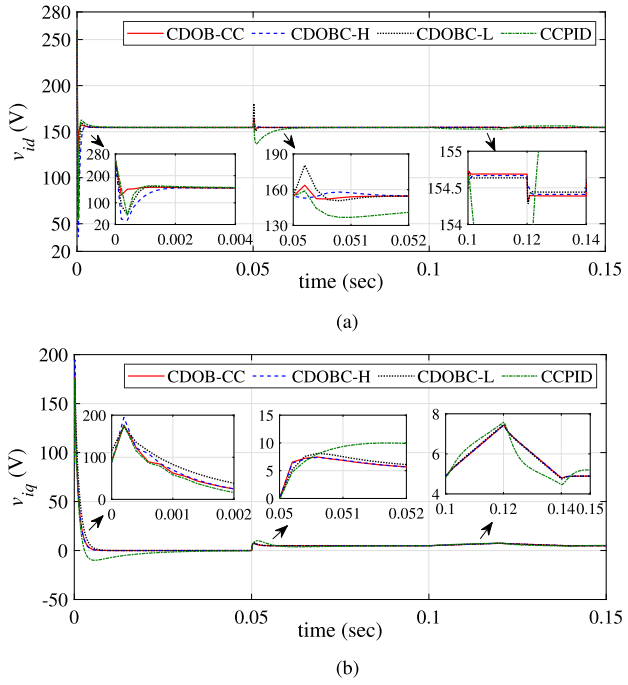

Fig. 5. Control input response curves under Case 1. (a) Time histories of d-axis control inputs. (b) Time histories of q-axis control inputs.

As presented in Fig. 6, owing to the harmonic suppression effect of the proposed control scheme, the steady-state voltage qualities (e.g., the steady-state errors and the recovery time (RT)) of the CDOB-CC controller and the CDOBC-H controller are

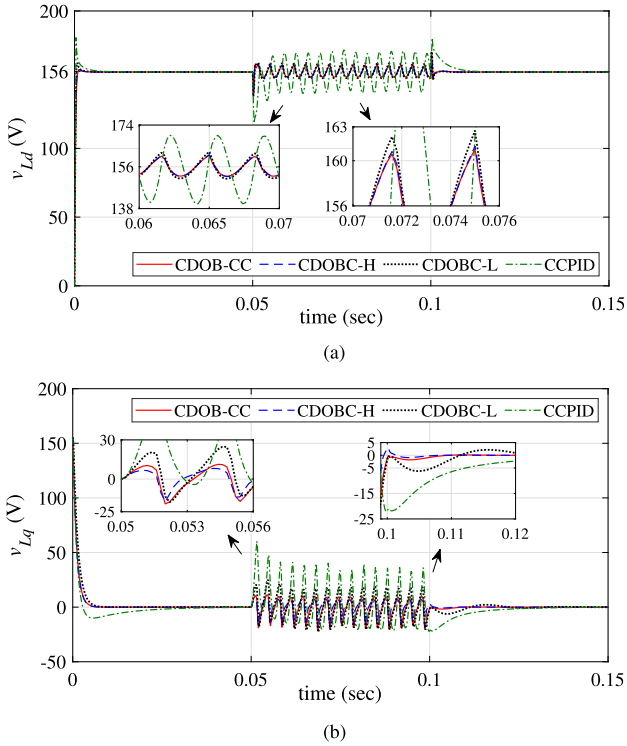

Fig. 6. Output voltage response curves under Case 2. (a) Response curves of d-axis output voltages. (b) Response curves of q-axis output voltages.

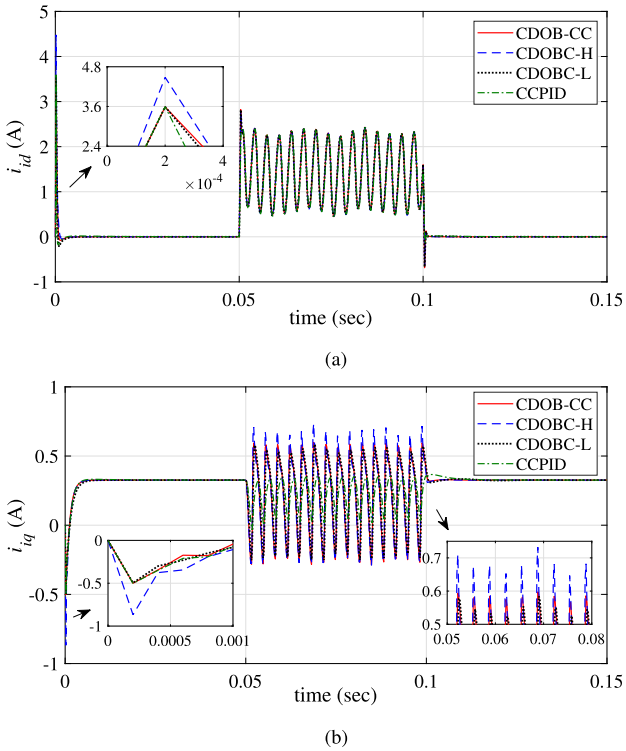

Fig. 7. Inductor current response curves under Case 2. (a) Response curves of d-axis inductor currents. (b) Response curves of q-axis inductor currents.

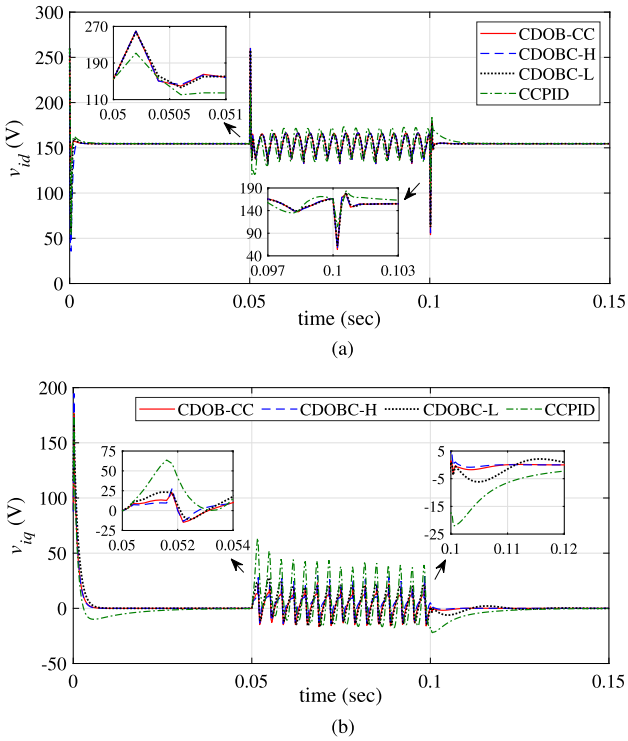

Fig. 8. Control input response curves under Case 2. (a) Time histories of d-axis control inputs. (b) Time histories of q-axis control inputs.

TABLE III
PERFORMANCE COMPARISONS IN SIMULATIONS

Controllers	ST (ms)	PC (A)	RT (ms)	RMSE (V)	THD (%)
CDOB-CC	0.76	3.59	0.70	2.00	2.16
CDOBC-H	0.71	4.48	0.73	2.05	2.21
CDOBC-L	1.27	3.59	0.79	2.53	2.73
CCPID	2.72	3.59	6.84	7.26	7.81

better than the other two controllers. The CDOBC-L controller suffers from conservative control parameters, while the CCPID controller is limited by the integral control mechanism that it can only suppress constant disturbances through cumulative errors. Fig. 7 shows that the dq-axis currents of the CDOBC-H controller are out of the constraints. Conversely, the current constraints of the other three controllers are always satisfied. Specific comparisons of the four controllers are shown in Table III. The performance indices include settling time (ST), PC, RT under Case 1, and root-mean-square steady-state error (RMSE) and THD value under Case 2.

Remark 4: The ST is the time when the output voltage tracking error enters the range of $\pm 2\%$ of the steady-state value and no longer goes out. The PC is the maximum current during the operation. The RT takes from the moment the disturbances are added until the output voltage tracking error returns to the $\pm 2\%$ of the steady-state value and no longer exceeds the threshold. The RMSE value is measured during the disturbance addition phase. The THD values are calculated throughout the entire time interval.

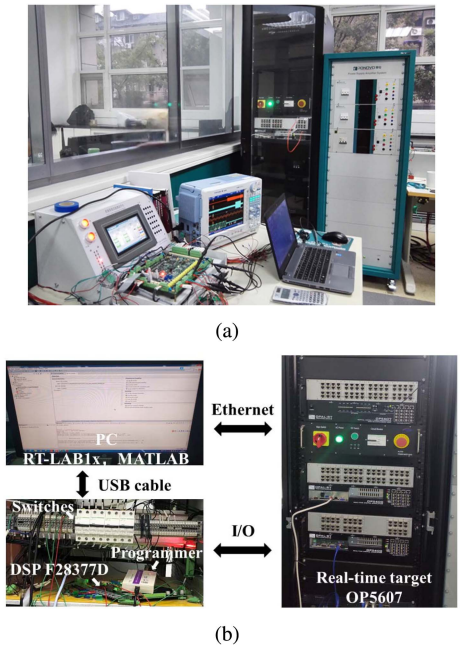

Fig. 9. Experimental platform: (a) overall diagram and (b) specific configuration.

The above simulation results adequately display the performances of the proposed CDOB-CC controller, which obtains good output voltage tracking performances and strictly ensures current constraints. Meanwhile, fast voltage recovery and harmonic suppression under multiple load switching are achieved.

B. Experiments

To further test the proposed current limiting control scheme, hardware-in-the-loop (HIL) experiments have been conducted. Fig. 9 clearly shows the platform, which consists of a computer (equipped with softwares MATLAB and RT-LAB1x), a DSP28377D controller, and an OP5607 real-time target emulator (integrated with a V7 field programmable gate array (FPGA), a 16-bit analog output module, a 32-bit digital input module, and a DB37M signal connection module). The platform enables power electronic simulations at the nanosecond level, and the dead-time of the switch is 0.3μs. The experiments' workflow is as follows: 1) A three-phase inverter is simulated in MATLAB (enhanced with RT-LAB related packets, e.g., RTeGrid Pro), and the inverter's states information (i.e., the output voltages and the inductor currents) is transferred via the Ethernet cable to the emulator for data processing (e.g., D/A conversion); 2) The processed analog states information is sent through the analog output module to the DSP console, and control inputs are calculated by the DSP controller; 3) The control inputs are sent to the controlled inverter to complete the closed-loop control; 4) Real-time operating states of the closed-loop system are monitored and recorded by the RT-LAB1x.

Parameters of the three-phase inverter system are listed in Table I, and the controller parameters are shown in Table IV. The current constraints are set as $-M_1 = M_2 = 3$A and $-M_3 =$

TABLE IV
CONTROLLER PARAMETERS FOR EXPERIMENTS

Controllers	Control parameters
CDOB-CC	$p_1 = -5e3$, $p_2 = -5e3$, $k_1 = 1.6e8$, $k_2 = 1.6e8$ $k_3 = 2e4$, $k_4 = 2.3e4$, $l_1 = 4.5e14$, $l_2 = 7e14$
CDOBC-H	$p_1 = -5e3$, $p_2 = -5e3$, $k_1 = 1.6e8$, $k_2 = 1.6e8$ $k_3 = 2.4e4$, $k_4 = 2.3e4$
CDOBC-L	$p_1 = -5e3$, $p_2 = -5e3$, $k_1 = 8e7$, $k_2 = 1.6e8$ $k_3 = 2e4$, $k_4 = 1e5$
CCPID	$k_{I1} = 7e10$, $k_{I2} = 7e10$, $k_1 = 1.6e8$, $k_2 = 1.6e8$ $k_3 = 2e4$, $k_4 = 2.3e4$, $l_1 = 4.5e14$, $l_2 = 7e14$

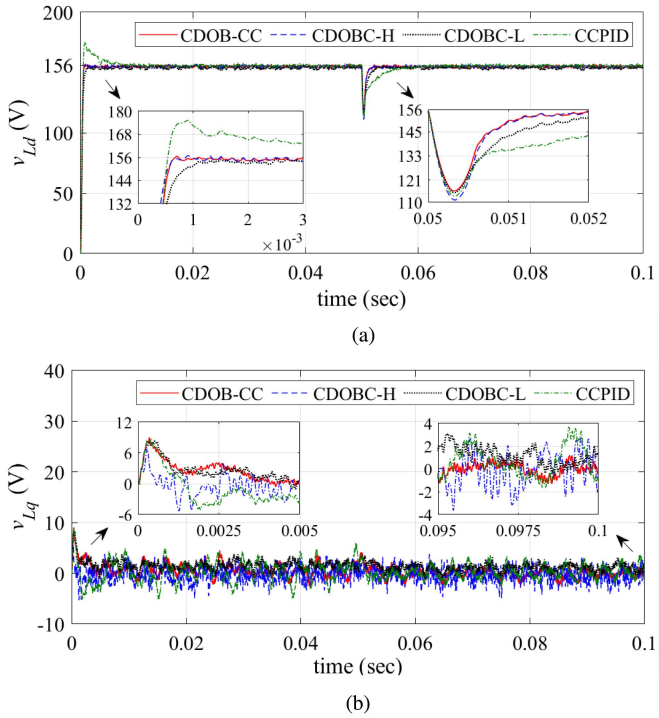

Fig. 10. Output voltage response curves under Case 1. (a) Response curves of d-axis output voltage. (b) Response curves of q-axis output voltages.

$M_4 = 0.6$A. Because of the inability to modify the resistance values monotonically and time-varyingly in the experiments, the conditions of sudden load addition and removal are tested in Case 1.

1) Case 1: Figs. 10–12 display the experimental results under Case 1. As seen from Fig. 10(a), the proposed CDOB-CC controller has nice dynamic and disturbance rejection performances, close to the CDOBC-H controller and far superior to the other two controllers. Moreover, unlike the excessive currents under the CDOBC-H controller, the CDOB-CC controller keeps the currents within the constraints, as shown in Fig. 11(a).

Different from the d-axis subsystem, the q-axis overcurrent problem is mainly induced by the noise. With large penalty term gains (i.e., l_1 and l_2), the CDOB-CC and benchmark CCPID controllers strictly restrict the overcurrent, as shown in

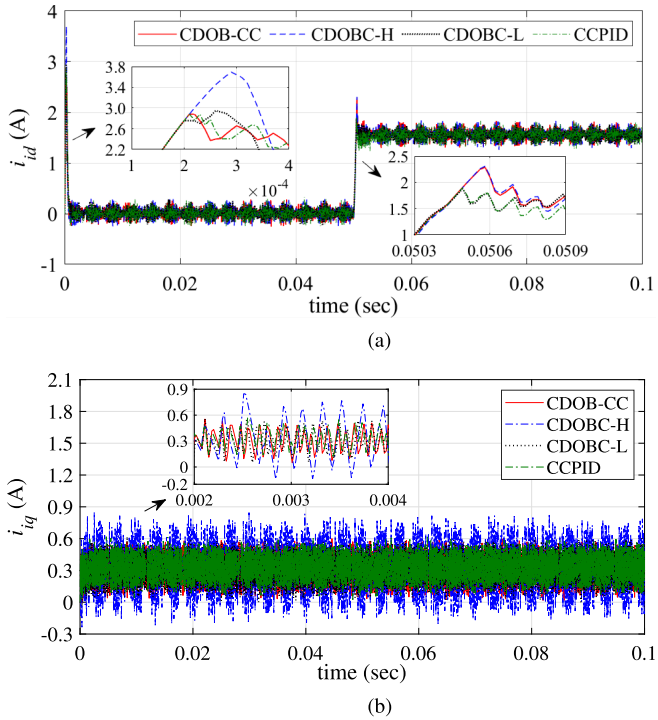

Fig. 11. Inductor current response curves under Case 1. (a) Response curves of d-axis inductor currents. (b) Response curves of q-axis inductor currents.

TABLE V
PERFORMANCE COMPARISONS IN EXPERIMENTS

Controllers	ST (ms)	PC (A)	RT (ms)	RMSE (V)	THD (%)
CDOB-CC	0.63	2.88	1.35	1.35	2.54
CDOBC-H	0.58	3.69	1.31	1.39	2.48
CDOBC-L	1.04	2.95	2.20	2.45	2.73
CCPID	6.43	2.88	6.56	4.04	3.00

Fig. 11(b). The essence of the current limiting mechanism is to enlarge the constraint effect by automatically increasing the gain of the derivative term as the current approaches the constraint boundary. Hence, by setting a relatively large derivative gain, the CDOBC-L controller also maintains the current constraints. However, as shown in Fig. 10(b), a large derivative term also exacerbates noise, resulting in poor output voltage quality. Further improving the voltage quality and constraint capability under noise will be a research focus in future work.

2) Case 3: Figs. 13–15 depict the experimental response curves under Case 3. Consistent with the conclusions reached above, the proposed CDOB-CC control scheme has good dynamic performances and overcurrent protection capability, even with large-scale, fast-varying harmonics induced by unbalanced loads. By contrast, the CDOBC-H control scheme has weak current-constrained performances, while the CDOBC-L control scheme has inferior dynamic performances. Meanwhile, the CCPID control scheme shows relatively poor harmonic suppression capability.

The overall numerical comparisons are shown in Table V. From the above simulation and experimental results, it is verified

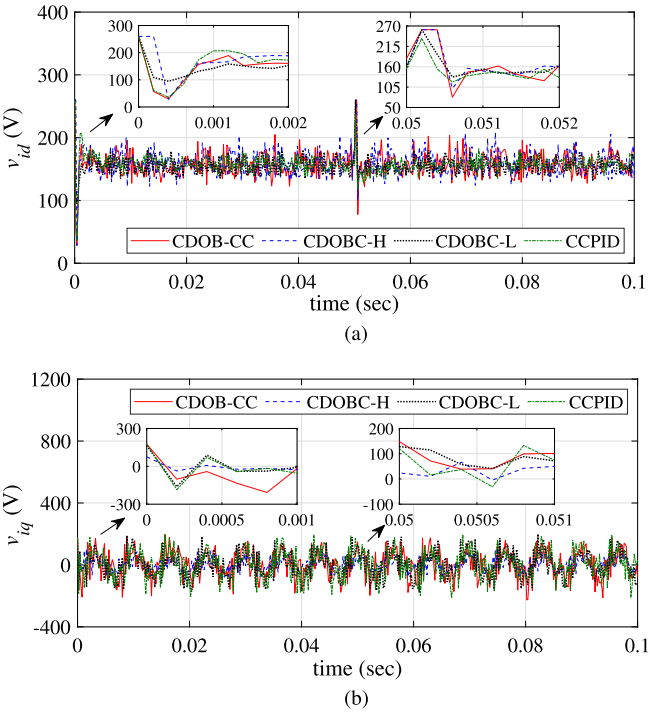

Fig. 12. Control input response curves under Case 1. (a) Time histories of d-axis control inputs. (b) Time histories of q-axis control inputs.

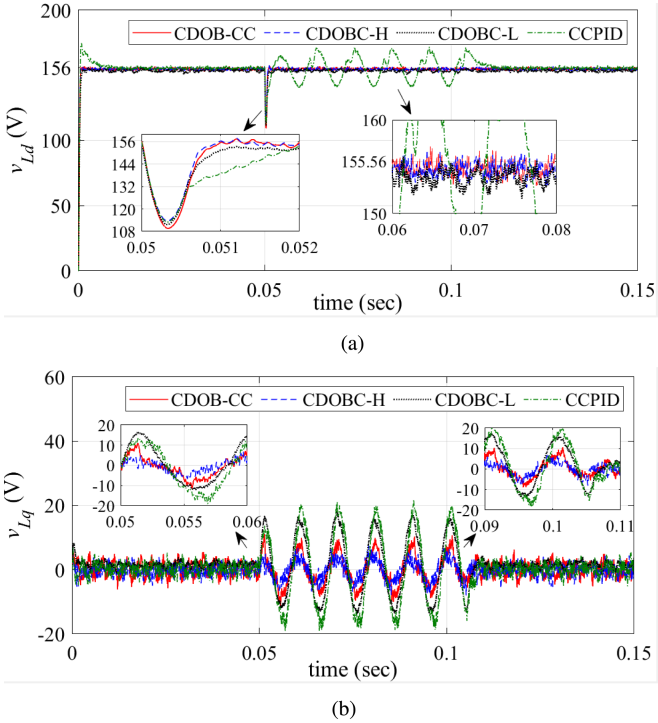

Fig. 13. Output voltage response curves under Case 3. (a) Response curves of d-axis output voltages. (b) Response curves of q-axis output voltages.

that the proposed current limiting control scheme is feasible and effective for the output voltage regulation and overcurrent protection of the three-phase inverter under multiple load conditions.

V. Discussions

A. Extended CDO

The proposed CDOs (6) can be extended to estimate multifrequency harmonics by using the properties of sinusoidal signals (i.e., the second derivative of the signal has a fixed multiple relationship with itself) to model harmonics and inserting the frequency information into the observer design. With this feature, the voltage quality can be improved when various harmonics disturb the inverters. For example, when constant disturbances, second-order harmonics, and sixth-order harmonics simultaneously pollute the system, the following extended CDOs are constructed:

$$\begin{cases} \dot{\eta}_{i,1} = h_i + \eta_{i,2} + \eta_{i,3} + \eta_{i,5} + \beta_{i,1}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,2} = \beta_{i,2}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,3} = 2\omega\eta_{i,4} + \beta_{i,3}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,4} = -2\omega\eta_{i,3} + \beta_{i,4}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,5} = 6\omega\eta_{i,6} + \beta_{i,5}(x_i - \eta_{i,1}) \\ \dot{\eta}_{i,6} = -6\omega\eta_{i,5} + \beta_{i,6}(x_i - \eta_{i,1}) \end{cases} \tag{12}$$

where $i = 1, 2$, corresponding to the observers for the d-axis and q-axis subsystem, respectively. $\beta_{i,1}, \beta_{i,2}, \beta_{i,3}, \beta_{i,4}, \beta_{i,5}$, and $\beta_{i,6}$ are the observer gains. $\eta_{i,2}, \eta_{i,3}$, and $\eta_{i,5}$ are estimates of the constant disturbances, second-order harmonics, and sixth-order harmonics. By integrating these estimates ($\hat{d}_1 = \eta_{1,2} + \eta_{1,3} + \eta_{1,5}$ and $\hat{d}_2 = \eta_{2,2} + \eta_{2,3} + \eta_{2,5}$) and feedforward compensating these harmonics through the proposed CDOB-CC controller, the multifrequency harmonics can be greatly suppressed.

B. Extended Current Limiting Control Scheme in the NARF

To enhance the applicability of the proposed control scheme, the extended current limiting control scheme in the NARF is presented. As the abc three phases have the same system structure, the control scheme for phase a is given as an example. The subsystem is formulated as

$$\begin{cases} \dot{v}_{La} = \frac{1}{C} i_{ia} - \frac{1}{C} i_{La} \\ \dot{i}_{ia} = -\frac{1}{L} v_{La} + \frac{1}{L} v_{ia} \end{cases} \tag{13}$$

where v_{La}, i_{ia}, v_{id}, and i_{La} are the output voltage, inductor current, inverter voltage, and load current, respectively. Denote $x_{1a} = v^*_{La} - v_{La}$ (v^*_{La} is the reference voltage) and $x_{3a} = \dot{v}^*_{La} - i_{ia}/C$, the control-oriented system is obtained

$$\begin{cases} \dot{x}_{1a} = x_{3a} + d_{1a} \\ \dot{x}_{3a} = f_a(x) - \frac{1}{CL} v_{ia} \end{cases} \tag{14}$$

where $d_{1a} = i_{La}/C = d_{1ac} + d_{1ah}$. d_{1ac} represents constant disturbances, and d_{1ac} represents harmonics (γ_1 is its frequency order). $f_a(x) = (v^*_{La} - x_{1a})/(CL) + \ddot{v}^*_{La}$. The constraint is $\underline{N}_{3a} < x_{3a} < \overline{N}_{3a}$.

The CDO is constructed as

$$\begin{cases} \dot{\eta}_1 = x_{3a} + \eta_2 + \eta_3 + \beta_1(x_{1a} - \eta_1) \\ \dot{\eta}_2 = \beta_2(x_{1a} - \eta_1) \\ \dot{\eta}_3 = \gamma_1\omega\eta_4 + \beta_3(x_{1a} - \eta_1) \\ \dot{\eta}_4 = -\gamma_1\omega\eta_3 + \beta_4(x_{1a} - \eta_1) \end{cases} \tag{15}$$

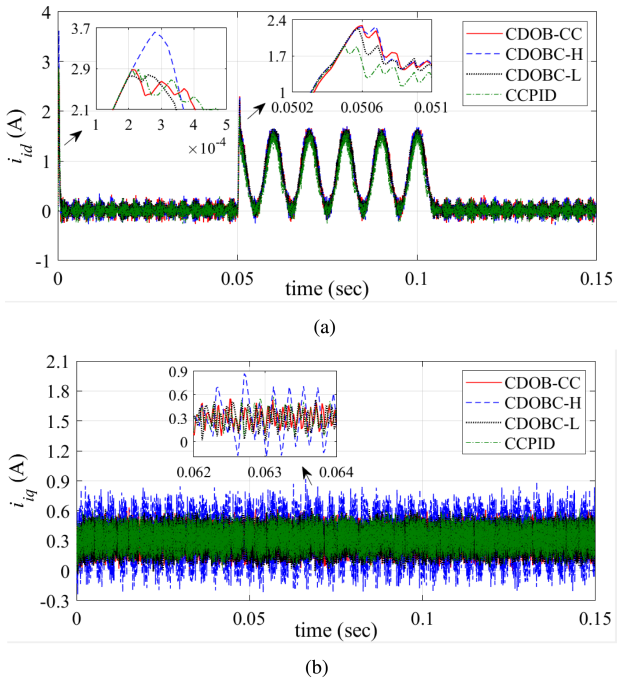

Fig. 14. Inductor current response curves under Case 3. (a) Response curves of d-axis inductor currents. (b) Response curves of q-axis inductor currents.

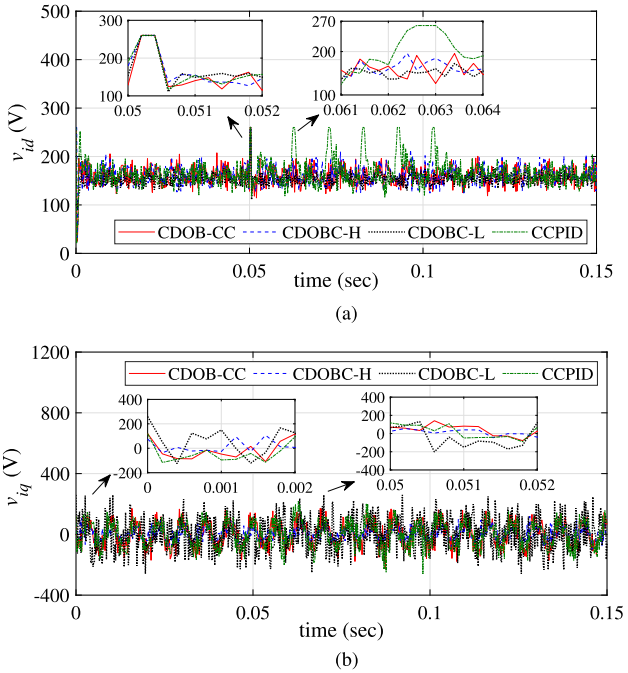

Fig. 15. Control input response curves under Case 3. (a) Time histories of d-axis control inputs. (b) Time histories of q-axis control inputs.

where η_1, η_2, η_3, and η_4 are estimates of x_{1a}, d_{1ac}, d_{1ah}, and $\dot{d}_{1ah}/(\gamma_1\omega)$. $\beta_1, \beta_2, \beta_3, \beta_4$ are observer gains. Denote $\hat{d}_{1a} = \eta_2 + \eta_3$, the current-constrained controller is designed as

$$\begin{aligned} v_{ia} = & CL\left[f_a(x) + k_{1a}x_{1a} + \dot{\hat{d}}_{1a}\right] \\ & + CL\left[k_{3a} + g_a(x_{3a})\right](x_{3a} + \hat{d}_{1a}) \end{aligned} \tag{16}$$

where $g_a(x_{3a}) = l_{1a}/((\overline{N}_{3a} - x_{3a})(x_{3a} - \underline{N}_{3a}))$. k_{1a}, k_{3a}, and l_{1a} are positive control parameters.

Since a large amount of current limiting strategies have been proposed in the NARF and different current limiting values have been set to meet different operating conditions [18], [19], the above control scheme (15), (16) can be directly used to satisfy these limiting values and enhance voltage quality simultaneously.

VI. Conclusion

In this article, the voltage regulation and overcurrent protection control problems have been studied simultaneously for stand-alone three-phase inverters under multiple load conditions. A novel current limiting control scheme with anti-disturbance properties has been proposed based on the CDOs and the composite current-constrained controller. Rigorous stability analysis, simulation, and experimental results have been illustrated to verify the feasibility and effectiveness of the proposed control scheme. In future work, more practical engineering problems (e.g., noise suppression problem, fault ride-through problem) will be investigated to extend the proposed scheme.

Appendix A

Proof of Proposition 1

Based on system (3), the subsystems corresponding to the CDOs (6) are formulated as

$$\begin{cases} \dot{X}_{ei} = A_{ei}X_{ei} + B_{ei}U_{ei} \\ y_{ei} = C_{ei}X_{ei} \end{cases} \tag{17}$$

where $i = 1, 2$, $X_{ei} = [x_i, d_{ic}, d_{ih}, \dot{d}_{ih}/(\alpha_i\omega)]^T$, $y_{ei} = x_i$, $U_{ei} = [h_i, \dot{d}_{ic}]^T$, $A_{ei} = \begin{bmatrix} 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_i\omega \\ 0 & 0 & -\alpha_i\omega & 0 \end{bmatrix}$, $B_{ei} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}^T$, $C_{ei} = [1, 0, 0, 0]$.

The observability matrices of the subsystems (17) are

$$\begin{aligned} Q_{ei} &= [C_{ei}^T, A_{ei}^T C_{ei}^T, (A_{ei}^T)^2 C_{ei}^T, (A_{ei}^T)^3 C_{ei}^T] \\ &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & -\alpha_i^2\omega^2 \\ 0 & 0 & \alpha_i\omega & 0 \end{bmatrix} \end{aligned} \tag{18}$$

where $i = 1, 2$. As the ranks of Q_{ei} are 4, the subsystems (17) are observable [42].

For the estimation error systems (7), treat σ_i $(i = 1, 2)$ as inputs. The reduced systems $\dot{E}_i = H_iE_i$ are globally exponentially stable provided that H_i are Hurwitz matrices. The systems (7) are input-to-state stable (ISS). In addition, the inputs σ_i asymptotically converge to zero owing to the characteristic of the constant disturbances d_{ic}. Then, according to the input-to-state stability theory [43], the system states of (7)

asymptotically converge to zero, that is, $\lim_{t\to\infty} e_{i,j}(t) = 0$ $(i = 1, 2,\ j = 1, \ldots, 4)$. This completes the proof.

APPENDIX B
PROOF OF THEOREM 1

Denote $G_1 = (-\infty, +\infty) \times (-\infty, +\infty) \times (\underline{N}_{31}, \overline{N}_{31}) \times (\underline{N}_{41}, \overline{N}_{41})$. For any given initial states $X(0) \in G_1$, it is assumed that the conditions $x_3(t) \in (\underline{N}_3, \overline{N}_3)$ and $x_4(t) \in (\underline{N}_4, \overline{N}_4)$ are satisfied during $t \in [0, T)$, where T is a positive constant or $T = +\infty$. The proof includes the following three steps.

Step 1 (*Proof of the state boundness*, $t \in [0, T)$)*:* By properly selecting the control parameters k_1, k_2, k_3 and k_4, A can be a Hurwitz matrix. Then for any given symmetric negative-definite matrix $-Q$, there exists a symmetric positive-definite matrix P, which satisfies $A^T P + PA = -Q$.

The candidate Lyapunov function is chosen as

$$V(X) = X^T PX + \int_0^{\tilde{x}_3} \zeta_3(x)\mathrm{d}x + \int_0^{\tilde{x}_4} \zeta_4(x)\mathrm{d}x. \tag{19}$$

Based on the basic inequality $\pm\varrho_1\varrho_2 \le \varrho_1^2/2 + \varrho_2^2/2, \forall \varrho_1, \varrho_2 \in \mathbb{R}$, it infers that

$$\begin{aligned} V(X) &\le \lambda_{\max}(P)||X||_2^2 + |\tilde{x}_3||\zeta_3(\tilde{x}_3)| + |\tilde{x}_4||\zeta_4(\tilde{x}_4)| \\ &\le (\lambda_{\max}(P) + 1/2)||X||_2^2 + \zeta_3^2(\tilde{x}_3)/2 + \zeta_4^2(\tilde{x}_4)/2. \end{aligned} \tag{20}$$

Taking the derivative of $V(X)$ along system (10) in the time interval $[0, T)$, it yields

$$\begin{aligned} \dot{V}(X) &= -X^T QX + 2(B_1^T P + C_1\, A/2)X\zeta_3(\tilde{x}_3) \\ &\quad -l_1\zeta_3^2(\tilde{x}_3) + 2(B_2^T P + C_2\, A/2)X\zeta_4(\tilde{x}_4) \\ &\quad -l_2\zeta_4^2(\tilde{x}_4) + 2J_1^T PXe_{d_1} + 2J_2^T PXe_{d_2} \\ &\le -[\lambda_{\min}(Q) - c]||X||_2^2 - (l_1 - 2)\zeta_3^2(\tilde{x}_3) \\ &\quad -(l_2 - 2)\zeta_4^2(\tilde{x}_4) + e_{d_1}^2 + e_{d_2}^2 \\ &\le -bV(X) + e_{d_1}^2 + e_{d_2}^2 \end{aligned} \tag{21}$$

where $c = \max\{k_1^2/2, k_2^2/2\} + \lambda_{\max}(P_1) + \lambda_{\max}(P_2) + \lambda_{\max}(P_3) + \lambda_{\max}(P_4)$, $P_1 = P^T B_1 B_1^T P$, $P_2 = P^T B_2 B_2^T P$, $P_3 = P^T J_1 J_1^T P$, $P_4 = P^T J_2 J_2^T P$. If the control parameters l_1 and l_2 are selected to make $b = \min\{2l_1 - 4, 2l_2 - 4, (\lambda_{\min}(Q) - c)/(\lambda_{\max}(P) + 1/2)\}$ positive, then according to the Lyapunov theory, the states of the closed-loop system (10) are bounded when $t \in [0, T)$. Thereafter, denote $N_1 = \sup_{t>0} |x_1(t)|$ and $N_2 = \sup_{t>0} |x_2(t)|$, $t \in [0, T)$.

Step 2 (*Proof that the current constraints always hold, i.e.,* $T = +\infty$)*:* Since the proofs of d-axis constraint (i.e., $x_3(t) \in (\underline{N}_3, \overline{N}_3)$) and q-axis constraint (i.e., $x_4(t) \in (\underline{N}_4, \overline{N}_4)$) are similar, only the proof of d-axis is described minutely in this step, which is stated as follows.

Denote $D_1 = \sup_{t>0} |\hat{d}_1(t)|$, by assigning multiple poles of H_1 to calculate the observer gains, $\hat{d}_1(t)$ converges asymptotically from 0 to d_1. Hence, $D_1 < N_{3\_m}$ is obtained. Define $N_{31} = \max\{x_3(0), (a_1\overline{N}_3 + l_1 D_1)/(a_1 + l_1)\}$ and $N_{32} = \min\{x_3(0), (a_1\underline{N}_3 - l_1 D_1)/(a_1 + l_1)\}$, where $a_1 = (k_1 N_1 + D_3 + k_3 D_1)(\overline{N}_3 - \underline{N}_3)$ and $D_3 = \sup_{t>0} |\dot{\hat{d}}_1(t)|$. According to Assumption 1 and the information of control parameters k_1, k_3, l_1 and the boundary values $N_1, \overline{N}_3, \underline{N}_3$, it yields $N_{31} \in (0, \overline{N}_3)$, $N_{32} \in (\underline{N}_3, 0)$.

In order to prove the constraint $x_3(t) \in (\underline{N}_3, \overline{N}_3)$ holds when $t \in [0, T)$, the following two cases are discussed to exhibit the variation trends of x_3 when x_3 approaches the constraint boundaries $\overline{N}_3$ and $\underline{N}_3$.

Case 1: If $x_3(t) \in [N_{31}, \overline{N}_3), t \in [0, T)$, then

$$\begin{aligned} \dot{x}_3 &= -k_1 x_1 - \left[k_3 + \frac{l_1}{(\overline{N}_3 - x_3)(x_3 - \underline{N}_3)}\right](x_3 + \hat{d}_1) - \dot{\hat{d}}_1 \\ &\le k_1 N_1 + D_3 + k_3 D_1 - \frac{l_1(x_3 - D_1)}{(\overline{N}_3 - x_3)(\overline{N}_3 - \underline{N}_3)} < 0. \end{aligned} \tag{22}$$

It indicates that $x_3(t)\dot{x}_3(t) < 0$, which signifies that when x_3 is near the upper boundary $\overline{N}_3$, x_3 will move in a decreasing direction (i.e., away from $\overline{N}_3$) and enter the region of $(0, N_{31})$. This proves that $x_3(t) < \overline{N}_3, t \in [0, T)$ holds.

Case 2: If $x_3(t) \in (\underline{N}_3, N_{32}], t \in [0, T)$, then

$$\dot{x}_3 \ge -k_1 N_1 - D_3 - k_3 D_1 - \frac{l_1(x_3 + D_1)}{(\overline{N}_3 - \underline{N}_3)(x_3 - \underline{N}_3)} > 0. \tag{23}$$

It implies that $x_3(t)\dot{x}_3(t) < 0$, which means that when x_3 is close to the lower constraint boundary $\underline{N}_3$, x_3 will move in a increasing direction (i.e., away from $\underline{N}_3$) and enter the region of $(N_{32}, 0)$. This proves that $x_3(t) > \underline{N}_3, t \in [0, T)$ holds.

For any given initial states $X(0) \in G_1$, $(x_1(t), x_3(t)), t \in [0, T)$ is the solution of the closed-loop system (10) on $G_2 = (-N_1 - 1, N_1 + 1) \times (\underline{N}_3, \overline{N}_3)$. Based on the above analysis, the solution $(x_1(t), x_3(t))$ can be more precisely described as

$$(x_1(t), x_3(t)) \in [-N_1, N_1] \times (N_{31}, N_{32}) \subset G_2. \tag{24}$$

If T is a positive constant, x_3 can continue to extend a time interval and satisfy $x_3(t) \in (\underline{N}_3, \overline{N}_3)$ on the basis of the continuation theorem of solution. However, this contradicts the definition of T. Thus, $T = +\infty$ and $x_3 \in (\underline{N}_3, \overline{N}_3)$ always holds, that is, the d-axis constraint is maintained all the time. Similarly, the q-axis constraint is always ensured.

Step 3 (*Proof that the states are asymptotically convergent*)*:* Based on the analysis of *Step 1* and *Step 2*, the inequality (21) always holds. Then, it yields

$$V(t) \le e^{-bt}V(0) + (1 - e^{-bt})(e_{d_1}^2(t) + e_{d_2}^2(t))/b. \tag{25}$$

From Proposition 1, $\lim_{t\to\infty}(e_{d_1}^2(t) + e_{d_2}^2(t)) = 0$. The right side of the inequality (18) asymptotically converges to zero, which means the states constituting V (i.e., $x_1, x_2, \tilde{x}_3, \tilde{x}_4$) asymptotically converge to zero. Namely, the closed-loop system (10) is asymptotically stable. v_{Ld} and v_{Lq} asymptotically track the reference signals. This completes the proof.

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Saijin Huang received the B.S. degree in automation, in 2019, from Southeast University, Nanjing, China, where he is currently working toward the Ph.D. degree in control science and engineering with the School of Automation.

His research interests include nonlinear control and application in power electronic systems.

Xiangyu Wang (Senior Member, IEEE) received the B.S. degree in mathematics and the Ph.D. degree in control theory and control engineering both from Southeast University, Nanjing, China in 2009 and 2014, respectively.

Since 2014, he has been with the School of Automation, Southeast University, where he is currently a Full Professor. His research interests include nonlinear control, anti-disturbance control, robot control, control and optimization of power systems, and distributed control and optimization of multiagent systems.

He serves as an Associate Editor for the *IET Control Theory and Applications*.

Guanjun Li received the B.S. degree in electric power system and automation and the M.S. degree in power electronics and power transmission both from Southwest Jiaotong University, Chengdu, China, in 2005 and 2008, respectively. He is currently working toward the Doctoral degree in electronic information with the School of Automation, Southeast University.

He is also a Senior Engineer with the China Electric Power Research Institute Company. His main research interests include energy storage control and application technology.

Xinming Wang (Graduate Student Member, IEEE) received the B.E. and M.E. degrees in navigation, guidance and control from the Northwestern Polytechnical University, Xi'an, China, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree in control theory and control engineering from the School of Automation of Southeast University, Nanjing, China.

He has been a Visiting Student with the Department of Aeronautical and Automotive Engineering, Loughborough University, U.K. from 2022 to 2024. His research interests include safety-critical control, disturbance rejection control and its applications to mechatronics systems and flight control systems.

Shihua Li (Fellow, IEEE) received the B.S., M.S., and Ph.D. degrees in automatic control from Southeast University, Nanjing, China in 1995, 1998, and 2001, respectively.

Since 2001, he has been with the School of Automation, Southeast University, where he is currently a Full Professor and the Director of Mechatronic Systems Control Laboratory. His main research interests lie in modeling, analysis and nonlinear control theory with applications to mechatronic systems, including manipulator, robot, ac motor, engine control, power electronic systems and others.

Qi Li received the B.S., M.S., and Ph.D. degrees in automatic control from Southeast University, Nanjing, China, in 1983, 1986, and 1992, respectively.

He was a Visiting Scholar with the Massachusetts Institute of Technology, Cambridge, MA, USA, from 2003 to 2004, joining in the project of Alpha Magnetic Spectrometer, which was sent to the International Space Station later to detect the antisubstance. He has been a Full Professor with Southeast University since 1999. His current research interests include intelligent control, optimal control of complex industrial process, and integration of management and control.