Analytical Model and Safe-Operation-Area Analysis of Bridge-Leg Crosstalk of GaN E-HEMT Considering Correlation Effect of Multi-Parameters

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***Abstract*—Wide band-gap field-effect power devices, such as gallium nitride (GaN) high electron mobility transistors are being widely used for a better system-level performance as a result of superior figure-of-merits in power-conversion application. But they could also suffer from more severe bridge-leg crosstalk issue in fast-switching operation due to their special device features. To suppress the bridge-leg crosstalk, an explicit model and theoretical analysis which could guide collaborative optimization of multiparameter is required. However, the superposition of two noise excitations (*di/dt* and *dv/dt*) and high order circuit structure bring difficulties to modeling and analysis. By the physical behaviors of different switching stages, the generation of crosstalk voltage is analyzed. This article proposes an analytical model of crosstalk voltage, with the explicit representation of parasitic parameters. Based on the model, an exhaustive investigation into the correlation of parameters on the crosstalk voltage is conducted. Further, a scheme for multiparameters collaborative optimization is presented, the safe operational area for crosstalk suppression has been determined. The superiority of the proposed model and the effectiveness of the optimization scheme are verified with simulations and experiments on a double pulse test platform. The model and analysis method can guide the selection of GaN devices and the design of parameters, which is convenient for the pre-test of printed circuit board before power ON.**

***Index Terms*—Analytical model, bridge-leg configuration, crosstalk voltage, gallium nitride high electron mobility transistors (GaN E-HEMTs), safe operational area (SOA).**

I. Introduction

FOR traditional hard-switched bridge-leg circuit with fast-switching device, when the control switch (CtrlTR) turns ON, current commutation and voltage commutation occur quickly, during which the drain-source current of CtrlTR quickly increases and the drain-source voltage of synchronous switch (SyncTR) increases sharply in a sequence [1]. Meanwhile, a false triggering pulse voltage at the gate of SyncTR, named crosstalk voltage, will appear in such a transient. When the crosstalk voltage reaches the threshold voltage for a certain time, the SyncTR will be turned ON unexpectedly and could result into severe shoot-through issue. Bridge-leg crosstalk issue could leave bad impact on system performance, including more severe voltage overshoot [2], additional power loss[3], electromagnetic interference noise [4], shoot-through faults and even device damage [5] in worst cases.

Comparing to their silicon counterparts, gallium nitride high electron mobility transistors (GaN E-HEMTs) have a lower gate-to-source threshold voltage and are prone to being used in fast-switching conditions with much higher *di/dt* and *dv/dt* [6], which make them more sensitive to bridge-leg crosstalk issue [7]. To make matters worse, GaN E-HEMTs has no avalanche breakdown and poor short-circuit withstanding capability [8], [9], [10], resulting with a relatively limited safe operational range in terms of crosstalk affect.

Means to prevent bridge-leg crosstalk from occurring in real applications have been proposed in [8] and [10] by changing gate resistor or other loop parameters to adjust the switching trajectory of CtrlTR so as to weaken crosstalk in terms of noise source. This design idea of electrical anti-interference is worth advocating. However, the adjustment of CtrlTR essentially weakens the *dv/dt* and *di/dt*, which will mostly limit the switching speed at the same time [11]. In practical application, crosstalk suppression methods which limit the *dv/dt* and *di/dt* is playing against to the basic research goal of further improving the power density and switching speed and liberating the potential of GaN devices [12]. Some practical suppression methods of bridge-leg crosstalk issue are application of gate negative bias and implementation of a ferrite bead to attenuate a gate voltage fluctuation [11]. However, these methods require additional circuits or elements. In [13], active gate driving is shown to permit faster switching, whilst still suppressing crosstalk. This kind of method leads to an increase in the number of components and could worsen reliability and the gate loop layout. Therefore, some researchers

Manuscript received 14 July 2023; revised 4 December 2023 and 12 February 2024; accepted 16 March 2024. Date of publication 27 March 2024; date of current version 16 May 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 52107175, in part by the Beijing Nova Program under Grant Z211100002121080, and in part by the project funded by the National Key Laboratory of Operation and Control of New Power Systems of Tsinghua University, China, under Grant SKLD22KM18. Recommended for publication by Associate Editor S. Tian. *(Corresponding author: Xiao Li.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3381638.

Digital Object Identifier 10.1109/TPEL.2024.3381638

focus on optimizing the parameters in the drive loop of SyncTR in order to improving the ability of SyncTR to resist crosstalk. Fortunately, changing the parameters related to SyncTR can effectively improve the immunity to crosstalk against high *dv/dt* and *di/dt* [11], [14]. Bi et al. [15] deduced the relationship between crosstalk voltage amplitude and parameters in the driver loop of SyncTR, which ensure the stability of the system when crosstalk occurs. Through reasonable parameters design, it can prevent false turn-ON under the working conditions of high current, high voltage and fast switching speed, and avoid unstable oscillation of bridge-leg configurations [16], [17]. Efforts should be paid on the collaborative design of crosstalk suppression devices and circuit parameters.

Moreover, a reliable application of GaN HEMT requires a solid design guideline to prevent false turn-ON. To prevent undesirable crosstalk problem from happening, power-supply designers need take parameter influence into consideration, which requires thorough understanding of the problem root cause and their staged effect difference [18], [19], [20]. An effective analytical model considering key parasitic parameters and their staged effect difference helps unbury related mechanism and achieve parameter optimization guidance. Moreover, through analytical model, designer can get a more accurate crosstalk voltage transient waveform. The real crosstalk voltage inside the device package can be described. The influence of various device and circuit parameters could be analyzed. In modeling and analysis of bridge-leg crosstalk, the superposition of dual excitation signals (*dv/dt* and *di/dt*) in time domain and the non-linearity of junction capacitance bring great difficulties, especially for condition with fast-switching GaN device. As far as authors know, in state of art of modeling and analysis on bridge-leg crosstalk of GaN HEMT, it is more often to consider the *dv/dt* during miller stage as excitation signal and then analyze corresponding effects [18]. However, this limits the application of model in other switching stages and could miss other important transient details of crosstalk voltage, which is also sensitive to *di/dt* during switching transient [19]. The correlation of crosstalk voltage with different parameters need to be considered. Thus, a more effective analysis method and explicit model considering key parasitic parameters and their staged effect difference is needed to unbury related mechanism and achieve parameter optimization guidance. Li et al. proposed an analytical model in [20], which takes into account the coupling relationship between *dv/dt* and *di/dt* and overcomes the shortcomings of the simple model. The influence of *di/dt* to crosstalk voltage cannot be ignored for model simplification. Both of the displacement current generated by the miller capacitor C_{gd} and the induced voltage of the common-source inductor L_{cs} contribute to crosstalk voltage [19]. In order to have a further look at staged effect of parameters, more analysis is needed including the coupling effects of C_{gd} and L_{cs} [21]. Fan et al. proposed an improved model in [19], in which the influence of common-source inductance and its coupling effect by *di/dt* in different switching stages was emphasized. In [22], Ishiwaki et al. found that the safe operational range of gate impedance increases with the increase of L_{cs} when the false turn-ON should be avoid. Practical design example revealed that GaN E-HEMTs should not be implemented so that the common-source inductance is extremely small in order to facilitate a design of the gate resistance for avoiding the false turn-ON [23], [24], [25], [26]. Efforts should been paid on the collaborative design of crosstalk suppression devices and circuit parameters [27], [28], [27].

Focusing on the bridge-leg crosstalk of GaN E-HEMTs, this article proposes a segmented, low-order, parameters-explicit analytical model. Different from those established for SiC MOSFETs, this model takes into account the specialty of GaN E-HEMTs. The two excitation signals *di/dt* and *dv/dt* are integrated into just one by considering their staged difference, which shows the potential to investigate the coupling effect between C_{gd} and L_{cs}. Unlike the high-order complex model, which can only be solved numerically, the proposed model is expressed explicitly by parameters, and consequently their effects on crosstalk can be explored much more easily. Further, a scheme for multiparameters collaborative optimization is presented, based on which the SOA for crosstalk suppression is determined for crosstalk prediction and parameter design guidance.

The rest of this article is organized as follows. Section II describes the double pulse test (DPT) circuit and parameters setting. By establishing equivalent circuit, the detailed switching process of GaN E-HEMTs was analyzed. The formation process of crosstalk voltage is explained. Then the crosstalk voltage models were established. In Section III, the effects of key parameters on crosstalk voltage are analyzed, and the multiparameters optimization through a case is presented, with the SOA designs of crosstalk suppression. LTspice simulation and experimental test in Section IV are executed to verify the superiority of the model and the effectiveness of the optimization scheme. Finally, Section V concludes the article.

II. Circuit Derivation and Modeling

A. Double Pulse Testing Equivalent Circuit

Fig. 1 shows the double pulse testing equivalent circuit of GaN E-HEMTs that considers key high-frequency components, especially parasitic parameters. This circuit will be taken as an example to analyze the mechanism of bridge-leg crosstalk and derive the control equations. The crosstalk false turn-ON voltage occurs mainly when CtrlTR Q_2 turns ON and SyncTR Q_1 is freewheeling in the analyzed circuit. The fact remains that crosstalk could also occur when CtrlTR device turns OFF and mainly introduce concern with negative transient gate-source voltage, which could affect device's reliability and even failure to a certain degree. However, at most of time, this case is of less concern, as larger safety margin of transient negative gate-source voltage (e.g., the GS66508B device used is -20 V) than positive safety range could be reached mostly, together with a way to adjust negative turn-OFF gate voltage as people did. In contrast, false turn-ON by crosstalk during CtrlTR device turn ON, which is known as miller turn-ON event, is of more concern of designers in many cases and could result into direct failure or huge power loss. Therefore, in this article, taking as an example, the transient process of CtrlTR turning ON will be analyzed in stages. The symbol definitions used in Fig. 1 are shown as follows.

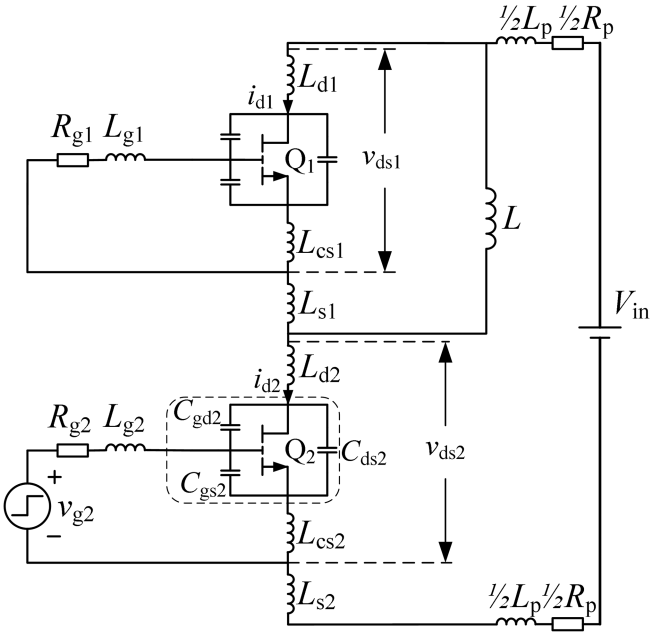

Fig. 1. DPT equivalent circuit of GaN E-HEMTs.

V_{in}	DC-link voltage source.
L	Load inductance.
L_p	Power circuit stray inductance.
R_p	Power circuit stray resistance.
C_{ds1}, C_{ds2}	Drain-source capacitance of Q_1, Q_2.
C_{gd1}, C_{gd2}	Gate-drain capacitance of Q_1, Q_2.
C_{gs1}, C_{gs2}	Gate-source capacitance of Q_1, Q_2.
R_{g1}, R_{g2}	Drive circuit resistance of Q_1, Q_2.
L_{g1}, L_{g2}	Drive circuit parasitic inductance.
L_{cs1}, L_{cs2}	Common-source parasitic inductance.
v_{g2}	Gate drive voltage of CtrlTR.

B. Analytical Model and State Space Model

Fig. 2 shows the typical transient waveforms when CtrlTR turns ON. In Fig. 2, v_{gs1} is gate-source crosstalk voltage of Q_1. U_{DC} is dc power supply voltage. U_{DRV} is the driving voltage. U_{plat} is Miller platform voltage. U_{th} is gate threshold voltage. i_{Lcs1} is the current flowing through L_{cs1}. v_{ds1} and v_{ds2} represent the drain-source voltages. v_{gs2} is gate-source voltage of CtrlTR. The CtrlTR turns ON process can be divided into four switching stages labeled as S_1 to S_4 in Fig. 2, which are analyzed in detail as follows.

1) *CtrlTR Turns On Delay Stage S_1 ($t_0 \le t \le t_1$):* To begin the analysis, SyncTR has turned OFF by negative gate voltage, but it physically operated in reverse conduction condition with load freewheeling through its 2DEG. During S_1, the driving current i_{g2} charges the input capacitor C_{iss2}, and v_{gs2} increases from zero. However, before it reaches U_{th}, CtrlTR Q_2 will not conduct and the drain current i_{d2} remains zero. The equivalent circuit during S_1 is shown in Fig. 3, and the control equation of drive circuit can be obtained as

$$R_{g2}i_{g2} = U_{\text{DRV}} - v_{\text{gs2}} - (L_{\text{cs2}} + L_{g2})\frac{di_{g2}}{dt}. \quad (1)$$

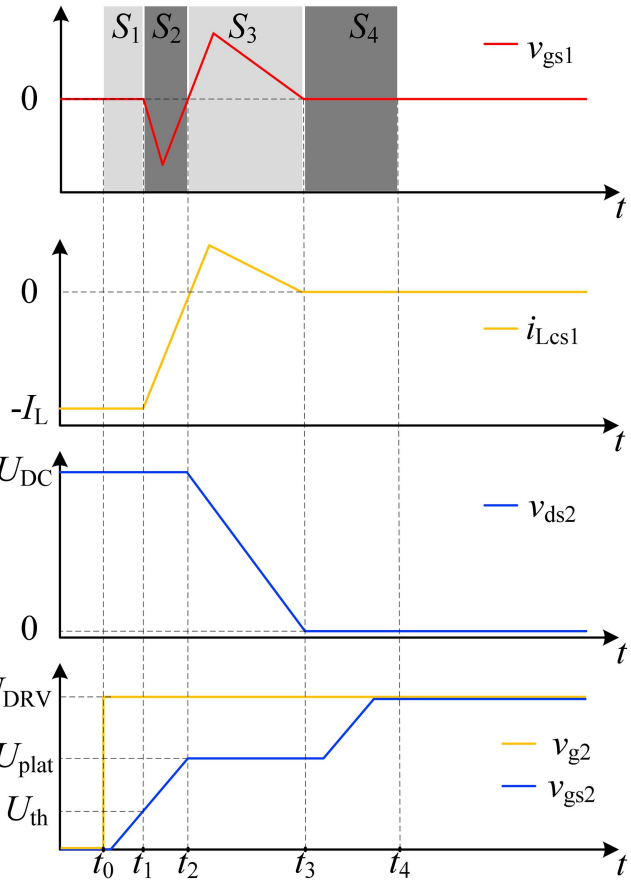

Fig. 2. Timing diagram during CtrlTR turns ON.

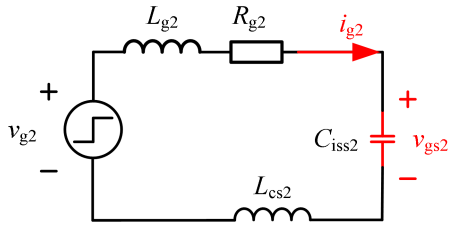

Fig. 3. Equivalent circuit of S_1.

The duration of S_1 is known as delay time

$$T_1 = (t_1 - t_0) = -\tau_1 \cdot \ln\left(\frac{U_{\text{DRV}} - U_{\text{th}}}{U_{\text{DRV}}}\right). \quad (2)$$

In which, $\tau_1 = R_{\text{g2}}C_{\text{iss2}}$ is the time constant of the drive circuit. During S_1, there is no significant gate-source crosstalk voltage.

2) *Current Rise (di/dt) Stage S_2 ($t_1 \le t \le t_2$):* During this stage, CtrlTR is operated in the constant current region, and the equivalent circuit is shown in Fig. 4. The i_{d2} will increase from zero until it reaches the load current I_{L} at time t_2, resulting in a larger *di/dt*. The two-dimensional electron gas current i_{2DEG} can be represented by v_{gs2} and transconductance g_m, and the control equation of i_{d2} can

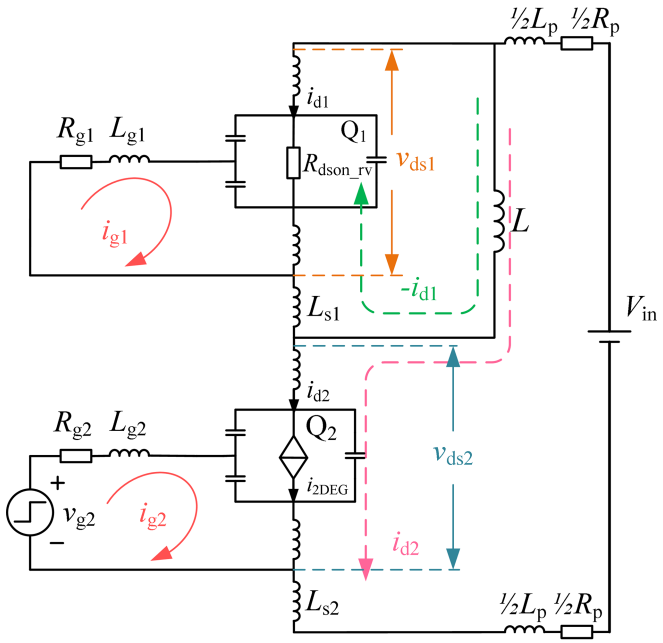

Fig. 4. Equivalent circuit of S_2.

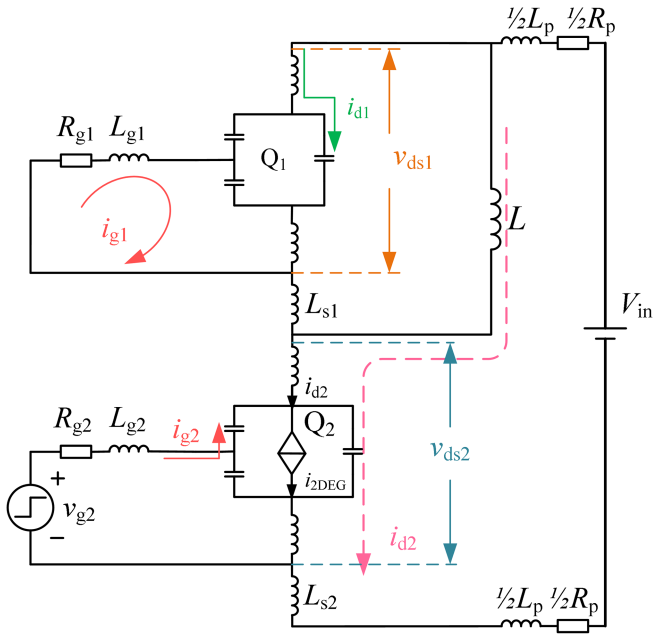

Fig. 5. Equivalent circuit of S_3.

be obtained as

$$i_{2\mathrm{DEG}} = g_m \cdot (v_{\mathrm{gs2}} - V_{\mathrm{th}}) \tag{3}$$

$$i_{d2} = i_{2\mathrm{DEG}} + C_{\mathrm{ds2}}\frac{dv_{\mathrm{ds2}}}{dt} - C_{\mathrm{gd2}}\frac{dv_{\mathrm{gd2}}}{dt}. \tag{4}$$

During S_2, CtrlTR gradually grabs current from SyncTR

$$i_{d1} = i_{d2} - I_L. \tag{5}$$

As for the drive circuit and power circuit, the control equations can be obtained as:

$$R_{g2}i_{g2} = U_{\mathrm{DRV}} - v_{\mathrm{gs2}} - (L_{\mathrm{cs2}} + L_{g2})\frac{di_{g2}}{dt} - L_{\mathrm{cs2}}\frac{di_{d2}}{dt} \tag{6}$$

$$V_{\mathrm{in}} = v_{\mathrm{ds2}} + v_{\mathrm{ds1}} + (L_p + L_{s1} + L_{s2}) \cdot \frac{di_{d2}}{dt} + R_p \cdot i_{d2}. \tag{7}$$

For the SyncTR Q_1, the reverse conduction condition satisfies the following:

$$v_{\mathrm{ds1}} = R_{\mathrm{dson\_rv}} \cdot (i_{d2} - I_L) + v_{\mathrm{gs1}} - V_{\mathrm{gd(th)}}. \tag{8}$$

In (8), $R_{\mathrm{dson\_rv}}$ is the equivalent drain-source resistance for reverse conduction, and $v_{\mathrm{gd(th)}}$ is the reverse conduction threshold voltage. Due to the high symmetry of the physical structure, it is usually

$$R_{\mathrm{dson\_rv}} \approx R_{\mathrm{dson}} \tag{9}$$

$$V_{\mathrm{gd(th)}} \approx V_{\mathrm{th}}. \tag{10}$$

The duration of S_2 can be approximated as

$$T_2 = (t_2 - t_1) = -\tau_1 \cdot \ln\left(\frac{U_{\mathrm{DRV}} - U_{\mathrm{plat}}}{U_{\mathrm{DRV}} - U_{\mathrm{th}}}\right). \tag{11}$$

By the substitution relationship of (5), the key electrical quantities included in the control equations can be quantified and simplified into just seven variables: i_{g1}, i_{g2}, v_{gs1}, v_{gs2}, v_{ds1}, v_{ds2}, and i_{d2}. By combining the control equations of S_2, the state space matrix corresponding to this substage can be obtained as

$$[v_{\mathrm{gs2}}\ v_{\mathrm{gs1}}\ i_{g2}\ i_{g1}\ i_{d2}\ v_{\mathrm{ds2}}\ v_{\mathrm{ds1}}]^T = A_2 \times [v_{\mathrm{gs2}}\ v_{\mathrm{gs1}}\ i_{g2}\ i_{g1}\ i_{\mathrm{d2}}\ v_{\mathrm{ds2}}\ v_{\mathrm{ds1}}]^T + B_2. \tag{12}$$

In which, A_2 and B_2 are shown in the appendix. Due to the presence of multiple energy-storage components (capacitors and inductors) in the circuit, during the process of establishing the state space matrix, the energy within each energy-storage component should be considered in order to achieve time-domain connectivity between models of each sub-stage.

3) *Current Overshoot and Voltage Fall (dv/dt) Stage S_3 ($t_2 \le t \le t_3$):* When v_{gs2} reaches U_{plat}, the Miller process of CtrlTR will start, v_{ds2} will quickly decrease to near zero, and the drain current i_{d2} will make an overshoot. The equivalent circuit of S_3 is shown in Fig. 5. During S_3, the control equations of CtrlTR are the same as which in the previous sub-stage. For SyncTR Q_1, the charging process of C_{oss1} can be expressed as

$$C_{\mathrm{ds1}} \cdot \frac{dv_{\mathrm{ds1}}}{dt} + C_{\mathrm{gd1}} \cdot \frac{dv_{\mathrm{dg1}}}{dt} = i_{d2} - I_L. \tag{13}$$

The duration of S_3 can be approximated as

$$T_3 = (t_3 - t_2) = \frac{Q_{\mathrm{gd2}}R_{g2}}{U_{\mathrm{DRV}} - U_{\mathrm{plat}}}. \tag{14}$$

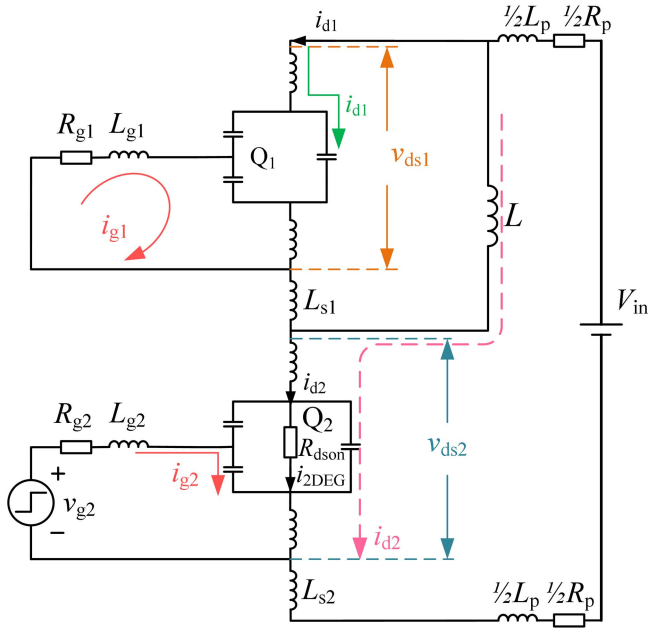

Fig. 6. Equivalent circuit of S_4.

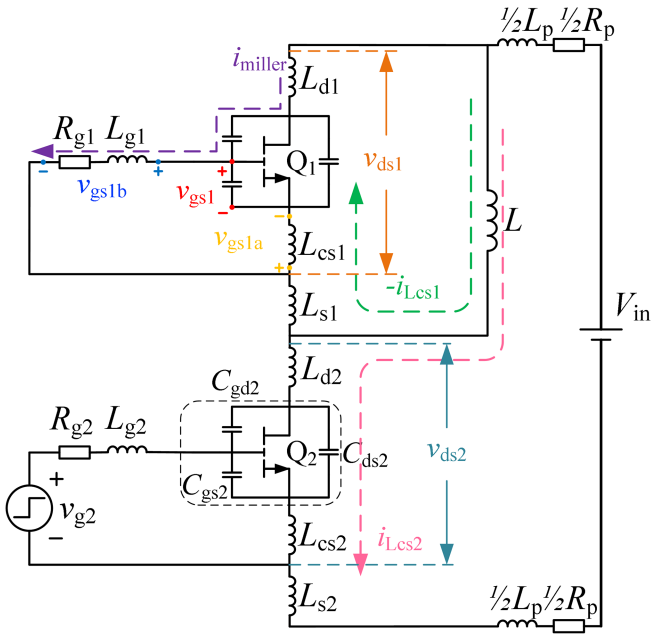

Fig. 7. Crosstalk process of double pulse testing circuit.

By combining the control equations of S_3, the state space matrix of S_3 can be obtained as

$$[v_{gs2}\ v_{gs1}\ i_{g2}\ i_{g1}\ i_{d2}\ v_{ds2}\ v_{ds1}]^T = A_3 \times [v_{gs2}\ v_{gs1}\ i_{g2}\ i_{g1}\ i_{d2}\ v_{ds2}\ v_{ds1}]^T + B_3. \quad (15)$$

In which, A_3 and B_3 are shown in the appendix.

4) *Current and Voltage Oscillation Stage S_4 ($t_3 \geq t$):* During S_4, CtrlTR is operated in the variable resistance region, and the equivalent circuit is shown in Fig. 6. The drain current of CtrlTR can be expressed as

$$i_{d2} = \frac{v_{ds2}}{R_{dson}} + C_{ds2} \cdot \frac{dv_{ds2}}{dt} + C_{gd2} \cdot \frac{dv_{dg2}}{dt}. \quad (16)$$

During S_4, v_{ds1} has increased to close to the dc-link voltage, and the dc component of i_{d1} is considered as zero. High-frequency oscillations can be observed on i_{d1} and v_{ds1}, and the control equation is

$$i_{d1} = C_{oss1}\frac{dV_{ds1}}{dt} - C_{rss1}\frac{dV_{gs1}}{dt}. \quad (17)$$

The state space matrix of this substage

$$[v_{gs2}\ v_{gs1}\ i_{g2}\ i_{g1}\ i_{d2}\ v_{ds2}\ v_{ds1}]^T = A_4 \times [v_{gs2}\ v_{gs1}\ i_{g2}\ i_{g1}\ i_{d2}\ v_{ds2}\ v_{ds1}]^T + B_4. \quad (18)$$

The (12), (15) and (18) constitute the state space model of the CtrlTR turns ON.

C. State Space Core Model Focusing on SyncTR Crosstalk

Observing the mathematical structure of matrix A_n in (12), (15) and (18), it can be found that the control matrix of model is characterized by a high degree of sparsity. When focusing on the bridge-leg crosstalk of SyncTR, more attention should be paid to the electrical variables that have stronger correlation with SyncTR, such as v_{gs1}, i_{g1}, v_{ds1} and i_{d1}. Therefore, the control equations in the state space model would be given different priority after elementary transformation and organization, and secondary meshes can be removed from the state space matrix to obtain the state space core model focusing on SyncTR crosstalk

$$[v_{gs1}\ i_{g1}\ v_{ds1}]^T = A_n^* \times [v_{gs1}\ i_{g1}\ v_{ds1}\ i_{d1}]^T + B_n^*. \quad (19)$$

The $A_n{}^*$ and $B_n{}^*$ ($n = 2 \sim 4$) are shown in appendix. Observing (19), the noise signals *di/dt* and *dv/dt* (i_{d1} and v_{ds1}) that induce crosstalk voltage become the excitation signals of the model directly. Through (19), the two intermediate variables i_{g1} and v_{ds1} can be eliminated, thus the relationship between v_{gs1} and i_{d1} can be directly derived. By the mathematical process, the first model reduction of the higher order analysis model is achieved.

D. Transfer Function Model of Crosstalk Voltage

As shown in Fig. 7, when Q_2 turns ON, the load current commutates from Q_1 [green line -i_{Lcs1}] to Q_2 [pink line i_{Lcs2}]. The current i_{Lcs1} flowing through L_{cs1} rises rapidly from the negative value of load current -I_L which leads to a induced voltage in driver loop [yellow line $v_{gs1\,a}$], resulting in an unexpected negative crosstalk voltage pulse at the gate-source terminal of Q_1. After CtrlTR takes all the load current, v_{gs2} continues to rise which leads to the decrease of v_{ds2}. As the U_{DC} is fixed, v_{ds1} increases rapidly. At the same time the junction capacitances C_{ds1} and C_{gd1} will be charged. The displacement current charging C_{gd1} [purple line i_{miller}] flows into the drive loop of Q_1, resulting in an unexpected triggering voltage pulse [blue line v_{gs1b}] at the gate-source terminal of Q_1. v_{gs1} refers to the real crosstalk voltage on the gate-to-source inside the shell of SyncTR, and the component formula of crosstalk voltage v_{gs1}

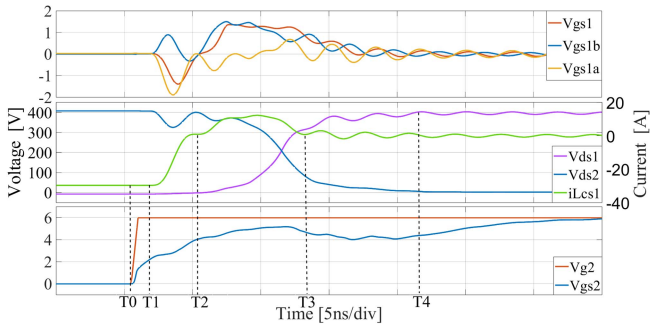

Fig. 8. Waveforms of key electrical quantities during CtrlTR turns ON.

is

$$v_{\mathrm{gs1}} = v_{\mathrm{gs1}a} + v_{\mathrm{gs1}b}. \tag{20}$$

The expression for the two components is

$$v_{\mathrm{gs1}a} = -L_{\mathrm{cs1}} \frac{di_{\mathrm{Lcs1}}}{dt} \tag{21}$$

$$v_{\mathrm{gs1}b} = R_{g1} i_{\mathrm{miller}} + L_{g1} \frac{di_{\mathrm{miller}}}{dt}. \tag{22}$$

The Miller current i_{miller} can be expressed as

$$i_{\mathrm{miller}} = C_{\mathrm{rss1}} \frac{dv_{\mathrm{ds1}}}{dt} - C_{\mathrm{iss1}} \frac{dv_{\mathrm{gs1}}}{dt}. \tag{23}$$

In Fig. 8, SyncTR crosstalk transient waveforms under a specific working condition are presented as an example to show the phase and timing relationship among important electrical variables mentioned above.

During S_1, CtrlTR has not yet been turned-ON and will not generate *di/dt* and *dv/dt* in the power circuit, and there is no obvious crosstalk voltage. So, it is not necessary to modeling at this switching sub-stage. During S_2, significant *di/dt* noise has already appeared on L_{cs1}. Based on the state space core model and (20), a analysis model of crosstalk voltage in the form of transfer function can be established in the frequency domain

$$\begin{aligned} v_{\mathrm{gs1}} &= v_{\mathrm{gs1}a} + v_{\mathrm{gs1}b} \\ &= G_v \cdot v_{\mathrm{ds1}} + G_i \cdot i_{\mathrm{Lcs1}}. \end{aligned} \tag{24}$$

The transfer function of *dv/dt* is G_v, and the transfer function of *di/dt* is G_i

$$G_v = \frac{L_{g1} C_{\mathrm{rss1}} \cdot s^2 + R_{g1} C_{\mathrm{rss1}} \cdot s}{L_{g1} C_{\mathrm{iss1}} \cdot s^2 + R_{g1} C_{\mathrm{iss1}} \cdot s + 1} \tag{25}$$

$$G_i = \frac{-L_{\mathrm{cs1}} \cdot s}{L_{g1} C_{\mathrm{iss1}} \cdot s^2 + R_{g1} C_{\mathrm{iss1}} \cdot s + 1}. \tag{26}$$

In order to establish a single excitation transfer function model for S_2, it is necessary to comprehensive the two noise excitation signals *di/dt* and *dv/dt*. Based on the unique reverse conduction characteristics exhibited by GaN E-HEMTs during S_2, i.e., (8), the relationship between *di/dt* and *dv/dt* can be bridged

$$\frac{dv_{\mathrm{ds1}}}{dt} = \frac{dv_{\mathrm{gs1}}}{dt} + R_{\mathrm{dson\_rv}} \cdot \frac{di_{\mathrm{Lcs1}}}{dt}. \tag{27}$$

Then taking (27) into (24), it can be obtained

$$\begin{aligned} v_{\mathrm{gs1}} = &\frac{(R_{g1} R_{\mathrm{dson\_rv}} C_{\mathrm{rss1}} - L_{\mathrm{cs1}}) \cdot s + (L_{g1} R_{\mathrm{dson\_rv}} C_{\mathrm{rss1}}) \cdot s^2}{1 + [R_{g1} (C_{\mathrm{iss1}} - C_{\mathrm{rss1}})] \cdot s + [L_{g1} (C_{\mathrm{iss1}} - C_{\mathrm{rss1}})] \cdot s^2} \\ &\cdot i_{\mathrm{Lcs1}}. \end{aligned} \tag{28}$$

During S_3, the rapid increase of v_{ds1} is considered as a direct excitation to induce crosstalk voltage. Researchers have also found that current overshoot in the power circuit can also impose significant *di/dt* noise on L_{cs1}. However, due to the lack of theoretical means to bridge the two excitation signals, the role of L_{cs1} is often overlooked in the crosstalk modeling process of S_3. As shown in Fig. 8, there is still a significant difference in the transient details of the waveforms between v_{gs1b} and v_{gs1}. Therefore, ignoring the significant contribution of *di/dt* to the crosstalk voltage component and only considering *dv/dt* excitation in the modeling process will lose the key transient details of crosstalk voltage waveform in most operating conditions and generate certain errors, which is detrimental to the universality and accuracy of the model. Based on the unique reverse recovery characteristics without body diode exhibited by GaN E-HEMTs during S_3, i.e., (13), the relationship between *dv/dt* and *di/dt* can be bridged as

$$i_{\mathrm{Lcs1}} = i_{d1} = C_{\mathrm{oss1}} \frac{dv_{\mathrm{ds1}}}{dt} - C_{\mathrm{rss1}} \frac{dv_{\mathrm{gs1}}}{dt}. \tag{29}$$

Then taking (29) into (24), it can be obtained as

$$v_{\mathrm{gs1}} = \frac{[C_{\mathrm{rss1}} L_{g1} - C_{\mathrm{oss1}} \cdot L_{\mathrm{cs1}}] \cdot s + R_{g1} C_{\mathrm{rss1}}}{k \cdot L_{g1} \cdot s^2 + k \cdot R_{g1} \cdot s + C_{\mathrm{oss1}}} \cdot i_{\mathrm{Lcs1}}. \tag{30}$$

In which $k = C_{\mathrm{iss1}} C_{\mathrm{oss1}} - C_{\mathrm{rss1}} C_{\mathrm{rss1}}$.

During S_4, there are two processes of current oscillation and voltage oscillation simultaneously, and *dv/dt* and *di/dt* still exist simultaneously. The C_{oss1} charging process still meets (13). Therefore, the mathematical form of the single excitation transfer function model during S_4 is the same as that of S_3. The numerical difference is because that nonlinear value of junction capacitance is different from S_3.

The application of GaN E-HEMTs in bridge-leg circuit exhibits two unique characteristics: reverse conduction and quasi-reverse recovery characteristics. The two excitation signals *di/dt* and *dv/dt* in the state space core model are bridged together to form a single excitation signal, which achieving a second time order reduction. A low order, transfer function form crosstalk voltage frequency domain analysis model of a single excitation signal is obtained as shown in (28) and (30).

E. Time Domain Model of Crosstalk Voltage

In order to establish a time-domain model, it is necessary to handle the conversion between the signals in the frequency domain model, and bring the nonlinear capacitance into the model.

Fig. 9(a) depicts the conversion between the key electrical variables during S_2, while Fig. 9(b) focuses on S_3 and S_4. Both subgraphs contain three mathematical calculation processes (current-voltage conversion, Miller current calculation, and Kirchhoff voltage law). However, it is worth noting that the

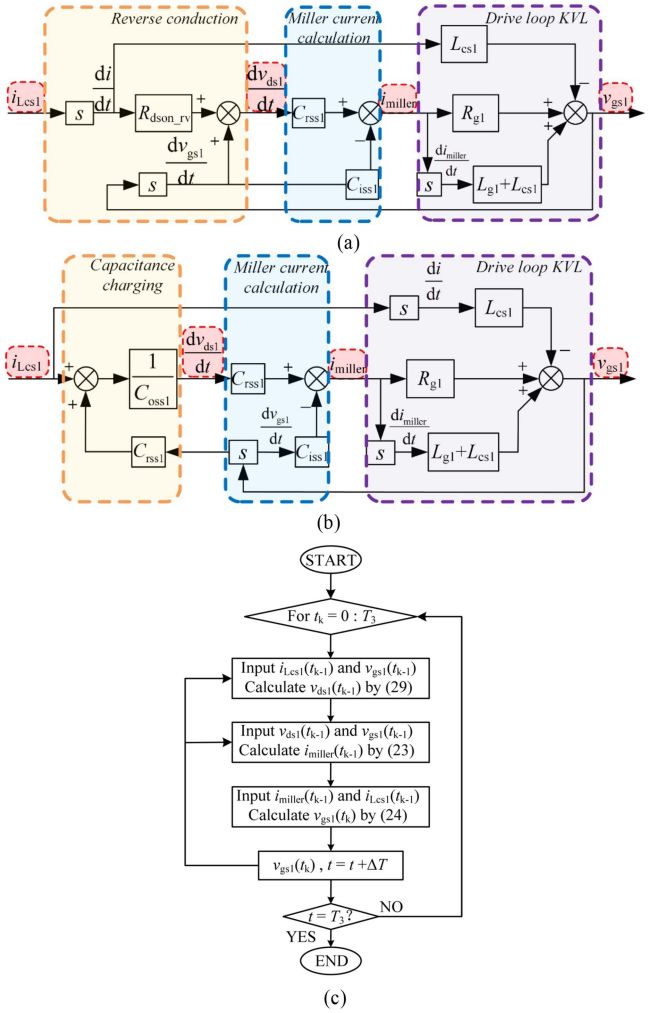

Fig. 9. Signal flow diagram of crosstalk voltage analysis model. (a) Signal flow diagram of S_2. (b) Signal flow diagram of S_3 and S_4. (c) Flowchart of numerical simulation.

current-voltage conversion relationship of the two subgraphs is significantly different. Fig. 9(a) achieves the conversion from current excitation to voltage signal based on (27) of reverse conduction characteristic, while Fig. 9(b) is based on (29) of capacitor charging process. In Fig. 9(c), a flowchart for the numerical simulation based on the model was presented, providing the initial values of each variable for the first iteration.

With the help of data extraction software GetData, data information of the input capacitance $C_{\rm iss}$, the output capacitance $C_{\rm oss}$, and the reverse transfer capacitance $C_{\rm rss}$ of GS66508T (Produced by GaN Systems. Inc) can be converted from the *C–V* characteristic curves. According to the curves, the equation of capacitors can be obtained by fitting. Then the result curves can be obtained by calculating and plotting. Fig. 10 shows the comparisons between fitted curves (solid lines) and datasheet curves (data points) of capacitors. The fitted curves are in good agreement with datasheet curves.

For crosstalk voltage time-domain models containing nonlinear energy-storage components, the relationship between

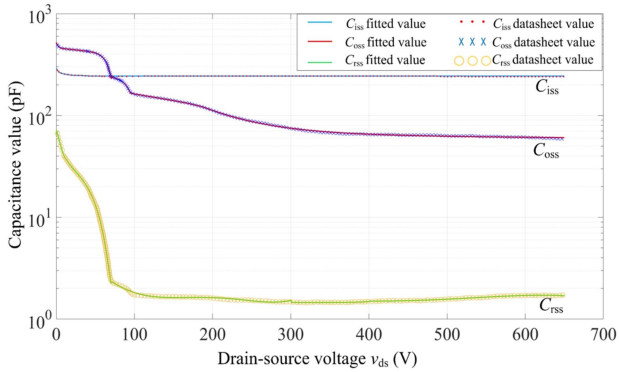

Fig. 10. Comparison between fitted results of capacitance and datasheet.

crosstalk voltage and excitation signal cannot be directly obtained in the form of a constant capacitance model. Therefore, an iterative model or Spice model can be established.

In this article, the crosstalk voltage generated by the circuits containing nonlinear elements can be divided into a great number of computing period. In each period, the capacitance value is a constant, and the model is a linear model. In addition, the initial values of the system are not zero yet, which are determined by the previous period. The crosstalk voltage can be regarded as the full response with zero state response and zero input response. Therefore, by numerical simulation based on the iterative model, the transient waveform of crosstalk voltage can be obtained.

In order to establish a reliable switching model, it is necessary to model the transfer and output characteristics. Transconductance represents the nonlinear relationship between channel current $i_{\rm ch}$ and gate source voltage $V_{\rm gs}$. Conventionally, piecewise fitting method is adopted to fit the transconductance curve, and the fitting equation is as follows:

$$\begin{cases} i_{\rm ch} = 0 & V_{\rm gs} < V_{\rm th} \\ i_{\rm ch} = m(V_{\rm gs} - V_{\rm th})^n, & V_{\rm gs} \le V_{\rm th} \end{cases}. \tag{31}$$

For a more accurate analytical model of switching transient, its temperature dependency were considered. The modeling of transfer characteristics and output characteristics can be obtained through relationship between drain current I_D and gate source voltage $V_{\rm gs}$ and drain source voltage $V_{\rm ds}$. The I_D - $V_{\rm gs}$ curves and the I_D – $V_{\rm ds}$ curve at different temperatures are provided in the datasheet. The curves at two different temperatures can be obtained. Then the relationship between the coefficient of the fitting function and the junction temperature can be obtained by using the linear interpolation method, so as to finally obtain a relationship between I_D, $V_{\rm gs}$, $V_{\rm ds}$ a,nd T_j. The fitting equation same as its SPICE model were taken as reference and the obtained models are as follows, taking example on GS66508T

$$\begin{aligned} I_D = {} & 0.099 \cdot \{-0.391 \cdot [V(T_j) - 25] + 90.8\} \\ & \cdot \ln[1 + e^{26 \cdot (V_{\rm gs} - V_{\rm th})}] \\ & \cdot \frac{v_{\rm ds}}{1 + \max[1.1 + 1.1 \cdot (v_{\rm gs} + 1.0), 0.2] \cdot v_{\rm ds}}. \end{aligned} \tag{32}$$

TABLE I
COMPARISON OF MODELS CONSIDERING NONLINEARITY

Model approach	Nonlinear elements	Parameters to be extracted	State variables	Accuracy
Circuit Model in [29]	8	28	-	More accuracy
Full-parameter analytical model in [30]	8	174	16	Most accuracy
Behavior model in [31]	6	22	-	Accuracy
Time-domain model in [18]	2	16	4	Accuracy
Proposed model	3	7	4	More accuracy

After obtaining the relationship between the above temperature and characteristic parameters, add them to the analytical model for specific analysis and prediction. According to $i_{\mathrm{Lcs}} = I_D$, by combining (32) into the analytical model, the crosstalk voltage waveform at different temperatures can be obtained.

The crosstalk voltage time-domain model proposed in this article preserves nonlinear capacitance, which has a positive impact on simulation accuracy. The number of nonlinear elements, the number of parameters to be extracted, and the number of state variables in the model can be used to describe the complexity of the model. The comparison of the above numbers between different models taking no consideration on temperature effect for all methods is given in Table I. The model proposed in this article can balance the accuracy and complexity of crosstalk voltage simulation.

III. CROSSTALK OPTIMIZATION OF CIRCUIT PARAMETERS AND SAFE OPERATIONAL AREA DESIGN

A. *Influence Analysis of Circuit Parameters on Crosstalk Voltage*

In order to evaluate the correlation of crosstalk voltage to parameters, the proposed model can be used to analyze crosstalk voltage in frequency domain. Actually, the gate impedance can exert different influences on the magnitude of the crosstalk [12], which depends on the contributions of the two critical factors for the crosstalk voltage. When the contribution of C_{gd} is higher than L_{cs}, the crosstalk voltage increases with the increase of the OFF-state impedance. However, with the increase of L_{cs}, the contribution of L_{cs} will also increase and even overcomes the contribution of C_{gd} [24]. The corresponding weighting of circuit parameters and their coupling effect could vary in different switching substages. It is widely recognized by researchers that increasing C_{gd1} by connecting additional capacitors in parallel with gate-drain of SyncTR is generally not conducive for crosstalk suppression, and costly because of the lower switching frequency. Therefore, in order to equivalently explore the effect of C_{gd1}, this article selects the driving loop impedance of Q_1 (R_{g1} and L_{g1}) that convert the displacement current i_{miller} into the component of crosstalk voltage $v_{\mathrm{gs1}\,b}$ as the research object. On the other hand, the contribution of another sub-content of crosstalk voltage $v_{\mathrm{gs1}\,a}$ by L_{cs1} will be explored. Table II gives the circuit parameters applied in this section.

TABLE II
SIMULATION CIRCUIT PARAMETERS

Parameter	Symbol	Value
DC-link voltage	U_{DC}	300 V
Load current	I_{L}	18 A
GaN devices	Q_1, Q_2	GS66508T
Driving voltage	U_{DRV}	6.0 V
Turn-off voltage	U_{g1}	-4.0 V
Turn-on resistance	R_{g2}	10.0 Ω
Drive loop resistance	R_{g1}	3.0 Ω
Drive loop inductance	$L_{\mathrm{g1}}, L_{\mathrm{g2}}$	1.0 nH
Common-source inductance	$L_{\mathrm{cs1}}, L_{\mathrm{cs2}}$	0.2 nH
Stray resistance	R_{p}	80 mΩ
Loop inductance	L_{p}	8.0 nH

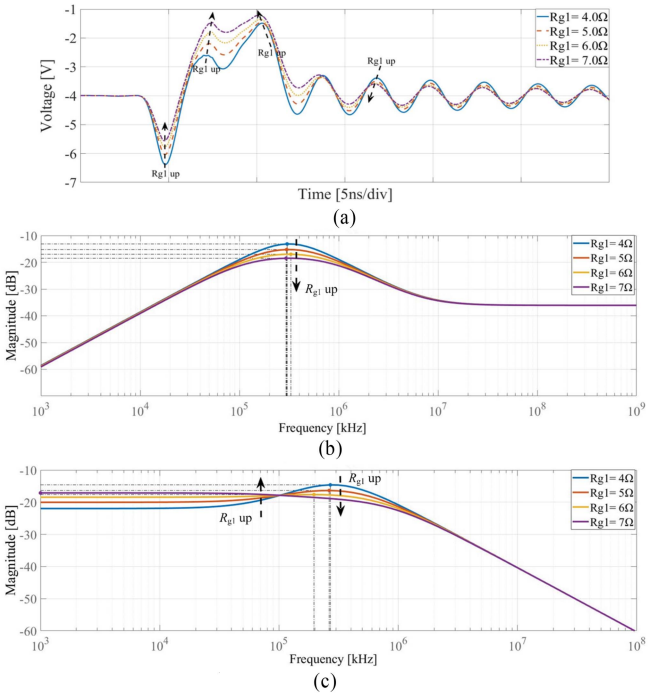

Fig. 11. Effect of drive loop resistance R_{g1} on crosstalk voltage. (a) Time domain simulation waveforms. (b) Model gain curves during S_2. (c) Model gain curves during S_3.

The effect of drive loop resistance R_{g1} on crosstalk voltage is explored in Fig. 11. As shown in Fig. 11(b), during S_2, the increase of R_{g1} will make the model gain decrease at the characteristic frequency(10^5–10^6kHz). That explains the increase of R_{g1} can help in suppressing the amplitude of high-frequency oscillation for negative crosstalk voltage during current rise (*di/dt*) stage which is shown in Fig. 11(a). It should be emphasized that the effect of R_{g1} change on model gain shows a distinct opposite trend between high-frequency band and low-frequency band during S_3 as shown in Fig. 11(c). The gain of low-frequency is positively correlated with the increase of R_{g1}, so that the increase of R_{g1} will be unfavorable to suppress the low-frequency component of crosstalk voltage during the early time of S_3. However, the gain of high-frequency is negatively correlated

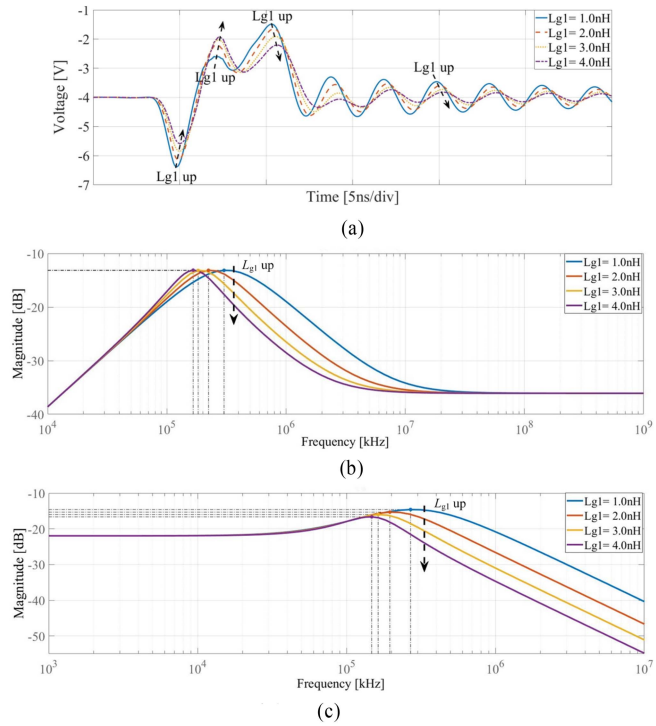

Fig. 12. Effect of drive loop inductance L_{g1} on crosstalk voltage. (a) Time domain simulation waveforms. (b) Model gain curves during S_2. (c) Model gain curves during S_3.

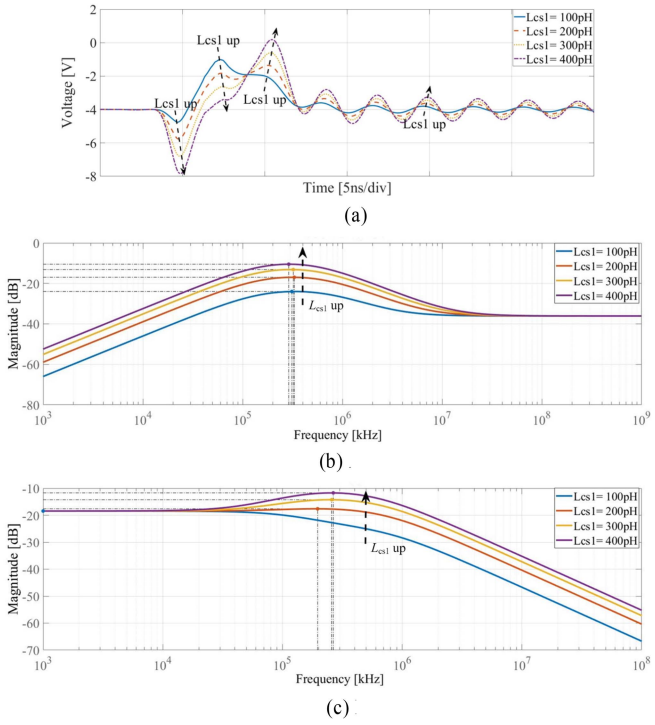

Fig. 13. Effect of common-source inductance L_{cs1}. (a) Time domain simulation waveforms. (b) Model gain curves during S_2. (c) Model gain curves during S_3.

with the increase of R_{g1}, so that the increase of R_{g1} will be help in suppressing the high-frequency component of crosstalk voltage during the later time of S_3 and the whole of S_4. The above frequency domain analysis content matches the time domain waveforms change rule in Fig. 11(a). However, it should be noted that the increase of R_{g1} will also increase the low-frequency crosstalk voltage value caused by the current overshoot during S_3. The different effects between high-frequency component and low-frequency component of crosstalk voltage which R_{g1} contribute should be considered in balance when optimizing the parasitic parameters of circuit.

The effect of drive loop inductance L_{g1} and common-source inductance L_{cs1} are explored in Figs. 12 and 13. As shown in Figs. 12(a) and 13(a), the effect of L_{g1} on the waveforms is weaker than that of L_{cs1}, during no matter S_2, S_3 or S_4.

In Fig. 13(b) and (c), the model gains of both S_2 and S_3 show a strong positive correlation with L_{cs1}. This indicates that the crosstalk voltage waveform is extremely sensitive to L_{cs1}, even a little change on L_{cs1} will make a great impact on the crosstalk voltage waveform. In Fig. 13(a), with the increase of L_{cs1}, the waveforms shift downward during S_2 and prophase of S_3. That results from the fact *di/dt* is positive in these switching stages, and a negative induced voltage $v_{gs1\,a}$ which is proportional to L_{cs1} is generated.

It should be noted that appropriately reducing the L_{cs1} could be beneficial to suppress the oscillation of crosstalk voltage and should be considered more carefully in most cases. Based on time domain waveforms and frequency domain analysis conclusions, it shows that the values design of R_{g1} and L_{cs1} should be given priority when suppressing crosstalk voltage by circuit parameters optimization.

B. Crosstalk Optimization of Circuit Parameters and Safe Operational Area Design

In the process of circuit design and printed circuit board (PCB) layout, a widely recognized method for crosstalk suppression is to minimize L_{cs1} as much as possible. However, due to the packaging technology of GaN E-HEMTs, even for the devices with Kelvin connection, it is very difficult and costly to limit L_{cs1} to a very small value (≤ 0.1nH). In order to cut the cost and find a way out of the crosstalk optimization dilemma cased by L_{cs1}, the idea provided in this article is to increase R_{g1} within a reasonable range to compensate for the negative impact brought by L_{cs1}. The analysis model proposed in this article can guide R_{g1}-L_{cs1} collaborative optimization. Here, a design example of SOA will be provided to illustrate the crosstalk optimization process. The circuit operating conditions of SOA design process are as given in Table II.

The first step in SOA planning is to calibrate the gain curve. First, based on the transfer function, the model gain corresponding to a set of R_{g1}-L_{cs1} values can be calculated. Within the value ranges of R_{g1} and L_{cs1}, changing R_{g1} and L_{cs1} with a fixed step size can obtain the model gain matrix. Using L_{cs1} as the *X*-axis, R_{g1} as the *Y*-axis, and Gain as the *Z*-axis, a model gain curve for the target stage can be drawn. Fig. 14(a), (b), and (c), respectively, depict the gain curves of the proposed model during different switching stages.

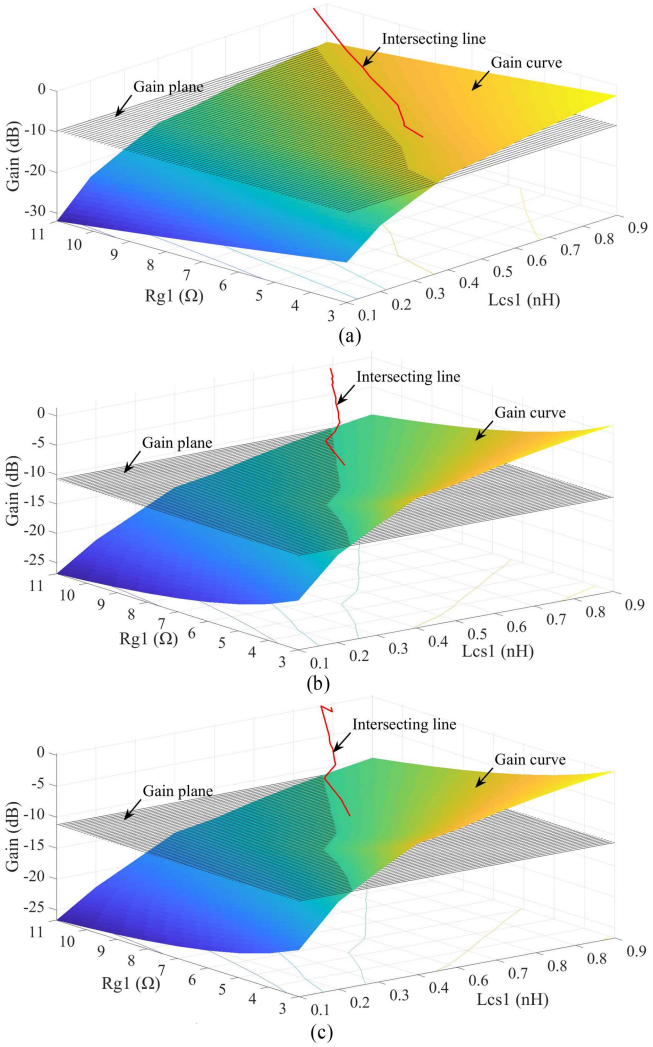

Fig. 14. SOA planning for different sub-stages. (a) Model gain curve calibration of S_2. (b) Model gain curve calibration of S_3. (c) Model gain curve calibration of S_4.

The second step is to design safety objectives. The safety objectives of crosstalk optimization will vary during different stages, reflected in the model, where the gain range limited by crosstalk voltage is different. During S_2, it is necessary to limit the amplitude of negative crosstalk voltage to prevent reverse breakdown or damage to the gate-source structure. The peak of crosstalk voltage usually occurs during S_3, and the safety objective is to limit the peak value below threshold voltage $U_{\rm th}$. When negative voltage turn-OFF technology has been used to suppress crosstalk, the safety objectives of S_3 should be set to a voltage of zero or less than $U_{\rm th}$ according to the application requirements, in order to retain a certain margin. During S_4, the crosstalk voltage waveforms typically have damped oscillation characteristics. The safety objective of S_4 could be set as the peak-to-peak value below $U_{\rm th}$ and retaining a certain margin to prevent false triggering caused by rapid charging and discharging of $C_{\rm gs}$. And according to the datasheet, the typical value of GS66508T's Gate-to-Source threshold voltage is 1.7 V. However, considering that dynamic $U_{\rm th}$ may be affected by operating conditions and there is a risk of $U_{\rm th}$ being too small, a 10% margin more and 1.5 V value have been retained as an example.

TABLE III
SAFETY OBJECTIVES AND GAIN LIMITATIONS

Stages	Safety Objectives	Gain
S_2	Minimum of $v_{\rm gs1} \geq$ -9.0 V	$\leq$-9.8 dB
S_3	Maximum of $v_{\rm gs1} \leq$ 0 V	$\leq$-10.8 dB
S_4	Peak-to-peak of $v_{\rm gs1} \leq$ 1.5 V	$\leq$-11.2 dB

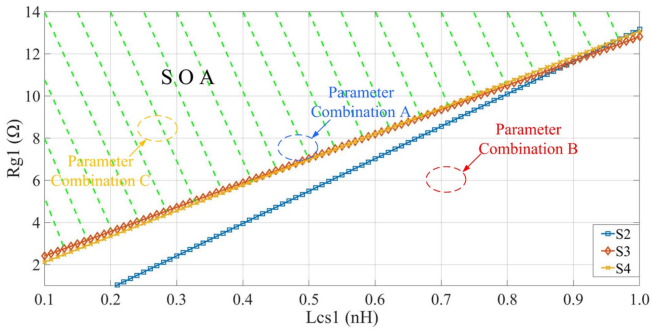

Fig. 15. SOA planning example.

Table III gives the recommended safety objectives and gain limitations in the design example of SOA. It should be emphasized that the safety objectives in Table III have considered turn-OFF voltage of −4.0 V. Draw gain planes perpendicular to the Z-axis in Fig. 14(a), (b), and (c) based on the gain limitations. Each gain curve intersects with a gain plane. The side below the gain plane which was separated by an intersecting line could be considered as the safe parameters area during this stage. The parameters area on the other side is considered to cause dangerous crosstalk and should be avoided.

The third step is to linear programming the total safe operational area. The intersecting lines of stages could be linear fitted to obtain relations between R_{g1} and $L_{\rm cs1}$, as (33). As shown in Fig. 15, taking the intersection of safe parameters areas during different stages, a total SOA can be obtained which meets with total safety objectives. Based on the total SOA, the joint optimization values of R_{g1} and $L_{\rm cs1}$ can be guided as

$$\begin{aligned} {\rm SOA}_2 &: R_{g1} \geq 1.535{\rm e}^{10} \times L_{\rm cs1} - 2.190 \\ {\rm SOA}_3 &: R_{g1} \geq 1.155{\rm e}^{10} \times L_{\rm cs1} + 1.258 \\ {\rm SOA}_4 &: R_{g1} \geq 1.216{\rm e}^{10} \times L_{\rm cs1} + 0.905. \end{aligned} \tag{33}$$

The crosstalk voltage waveforms obtained by combining different R_{g1}-$L_{\rm cs1}$ values is shown in Fig. 16. All combinations of parameters meet the limitations of the SOA planning example. Obviously, it is feasible to offset the deterioration of oscillation and crosstalk caused by larger $L_{\rm cs1}$ by using a larger turn-OFF resistance $R_{\rm g1}$. Optimizing the value of R_{g1} based on SOA planning can also limit the maximum of crosstalk voltage, effectively preventing the false turn-ON.

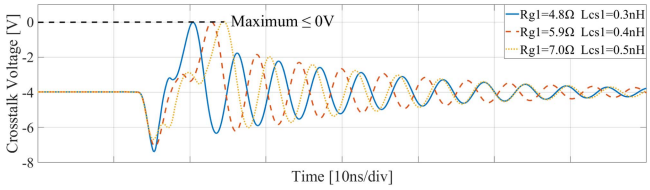

Fig. 16. Crosstalk voltage waveforms of SOA planning example.

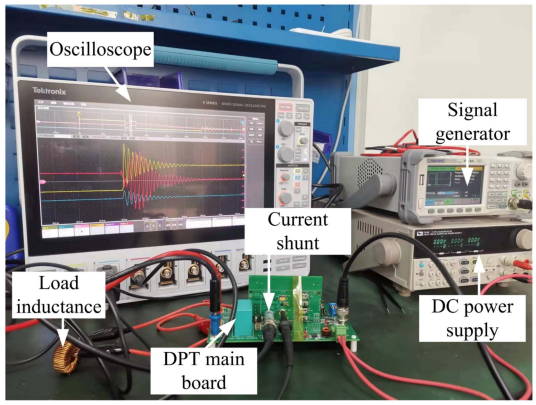

Fig. 17. Experimental platform for DPT.

TABLE IV
EXPERIMENTAL CIRCUIT PARAMETERS

Parameter	Value
DC-link voltage	300 V
Load current	11 A
Turn-off voltage	-4.3 V
Turn-on resistance	10.0 Ω
Drive loop resistance	3.0 Ω
Drive loop inductance	1.88 nH
Common-source inductance	0.23 nH
Loop inductor	14.4 nH

IV. VERIFICATION RESULTS

As shown in Fig. 17, the proposed bridge-leg crosstalk model is validated on a DPT platform. Table IV gives the circuit parameters of the platform. The switching GaN E-HEMTs are GS66508T. The driver IC is ACPL-P346, in order to protect GaN devices from crosstalk voltage, the turn-OFF voltage is set as −4.3V. The v_{gs} is measured by a TPP1000 probe with 1 GHz bandwidth. The load inductance is 200 μH. The dc-link voltage is controlled by dc power supply.

To verify the accuracy of the proposed model, the comparisons of fixed-parameter model, proposed nonlinear capacitances model, and experimental results are shown as Fig. 18. In three subgraphs of Fig. 18, the parameters of circuit are the same as Table IV, except for the dc-link voltage. The parasitic inductances of the DPT platform PCB are mainly obtained by ANSYS Q3D, which are evaluated with experimental results and bench test [24]. As can be seen that the oscillation frequency and peak value of the fixed-parameter model simulation results are close to the experimental results. However, due to the junction capacitances, the decay time is longer than that of experimental results.

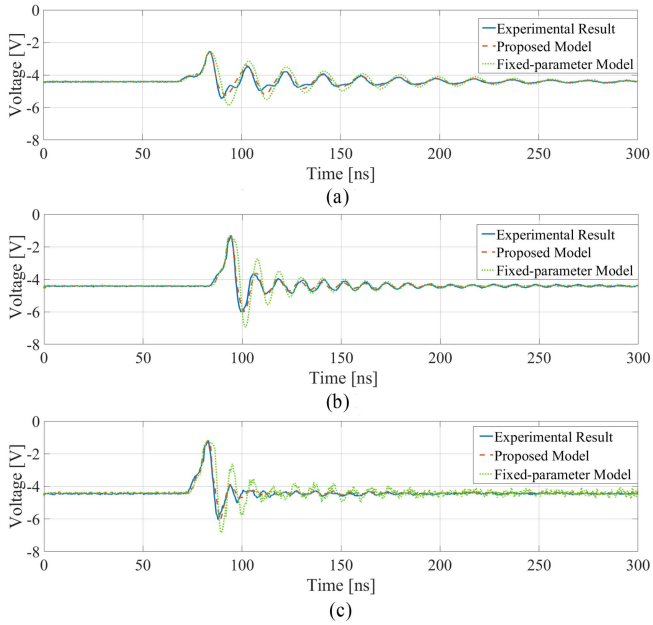

Fig. 18. Comparison of experimental and simulation waveforms of crosstalk voltage in different DC-link voltage with parameters in Table IV. (a) DC-link voltage is 50 V. (b) DC-link voltage is 200 V. (c) DC-link voltage is 300 V.

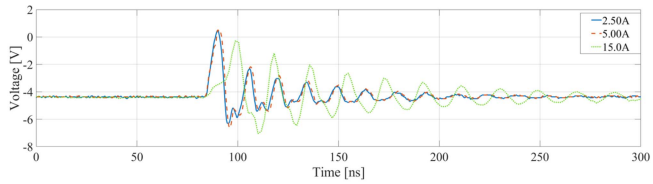

Fig. 19. Experimental waveforms of crosstalk voltage under different load currents with parameters in Table IV.

This situation is more significant when drain–source voltage is over 50 V, because the C_{gd} shows a nonlinear inflection point near 50 V, and changed with voltage significantly within 0–100 V. The proposed model with nonlinear junction capacitances can solve this problem, achieving good precision at different voltage levels and approaching experimental results.

Fig. 19 shows the comparisons of experimental waveforms of crosstalk voltage under different load currents. When the load current changes from 2.5 to 5.0 A, the component generated by voltage noise of the crosstalk voltage still dominates due to the small load current. However, when the load current continues to increase to 15.0 A, due to the large *di/dt* generated by the load current, the component generated by current noise begins to play its main role, and the crosstalk voltage waveform shows the characteristic of reduced amplitude oscillation.

To verify the influence of circuit parameters on crosstalk voltage, the comparisons of experimental results in different circuit parameters are shown in Fig. 20. In Fig. 20(a), the drive loop resistance is adjusted as three levels, and other parameters

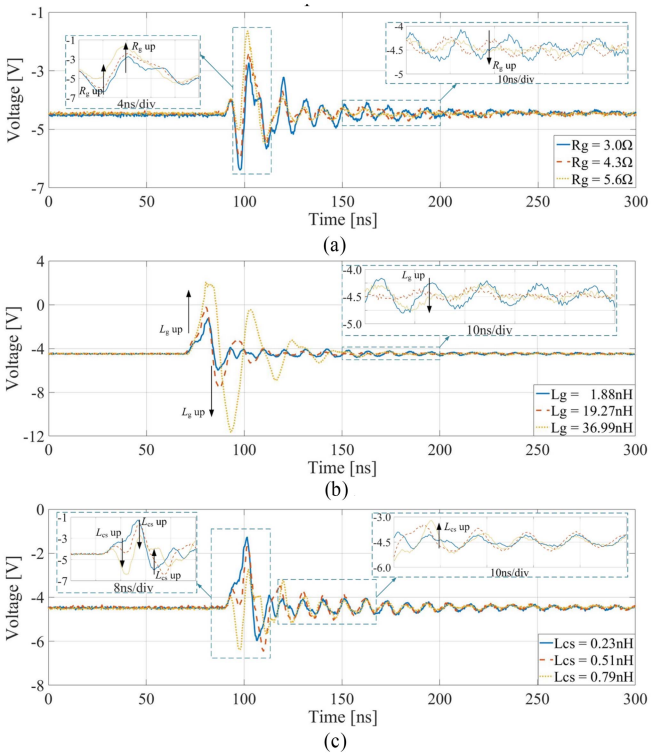

Fig. 20. Comparison of experimental waveforms of crosstalk voltage with different circuit parameters. (a) Drive loop resistance. (b) Drive loop inductance. (c) Common-source inductance.

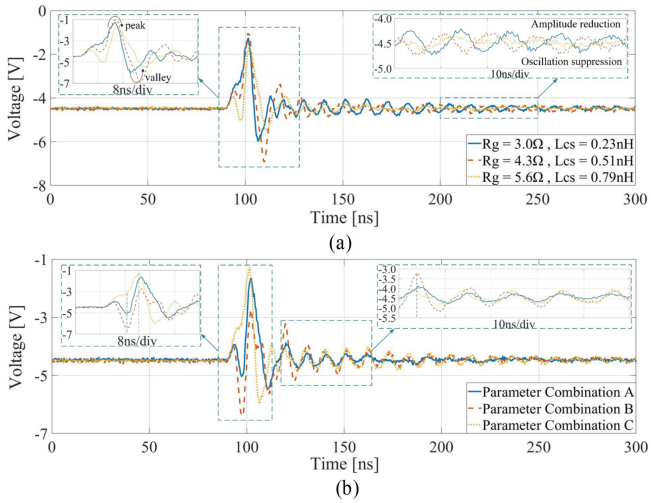

Fig. 21. Experimental waveforms of circuit parameters optimization. (a) Different combinations of R_{g1} and L_{cs1}. (b) Crosstalk voltage waveforms for SOA.

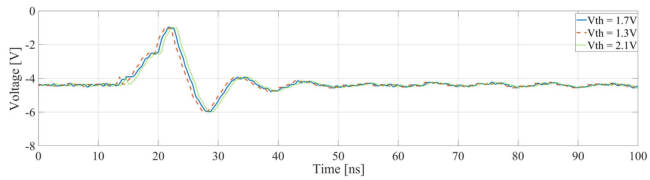

Fig. 22. Crosstalk voltage waveforms considering dynamic gate-threshold voltage.

are the same as these in Table IV. As the resistance increases, negative crosstalk and oscillation are suppressed, but the peak value of crosstalk voltage increases. As shown in Fig. 20(b), excessive L_g can cause false turn-ON, and the amplitude increases with L_g, and oscillation attenuation time reduces. It is necessary to minimize the drive loop inductance to suppress crosstalk voltage. The influence of common-source inductance on the crosstalk voltage is shown in Fig. 20(c). With the increase of L_{cs}, negative crosstalk and oscillation become more severe, because the proportion of crosstalk contribution caused by current noise increases. The influence on crosstalk voltage caused by circuit parameters mentioned above is consistent with the model analysis results.

The experimental waveforms obtained by applying the proposed crosstalk optimization strategy of circuit parameters is shown in Fig. 21. In Fig. 21(a), the drive loop resistance and common-source inductance are designed as three different combinations, and other parameters are the same as these in Table IV. As the L_{cs} increases, increasing the resistance of drive loop, which can suppress negative crosstalk and oscillation while ensuring that the amplitude does not worsen. As shown in Fig. 21(b), crosstalk voltages of different parameter combinations determined based on the SOA design proposed in Fig. 15 are compared. According to the SOA design steps, when common-source inductance are properly compensated by drive loop resistance, a safer crosstalk situation can be achieved.

A conclusion was confirmed in article [24], in which balancing the gate-drain parasitic capacitance and the common source inductance to achieve an appropriate ratio were found to be essential for preventing the oscillatory false triggering. This conclusion indicates that a matchable and reasonable value of L_{cs} by the layout would be more effective than a smaller value for crosstalk suppression in cases. Moreover, in some cases, in order to prioritize meeting the design criteria of switching speed, the adjustable range of gate resistance is often limited. Therefore, optimizing parasitic parameters to suppress crosstalk voltage is more practical in the case.

Recent researches point out that GaN E-HEMT shows the dynamic threshold voltage characteristic. To demonstrate that the proposed model still has a wide application range for prediction of crosstalk voltage when considering dynamic gate-threshold voltage and operation temperature. The comparisons of crosstalk voltage waveforms under different threshold voltages are shown in Fig. 22. When the threshold voltage changes by 0.4 V [25], the crosstalk voltage waveform obtained by the proposed model mainly shifts horizontally. The occurrence of this phenomenon is due to a change in the time when the model reaches the triggering condition. In addition, the dynamic threshold characteristics has obvious part-to-part variation, and its effect on crosstalk would be more obvious for the design of high-voltage switching circuit. Thus, special attention should be paid in high-voltage design and switching test [19].

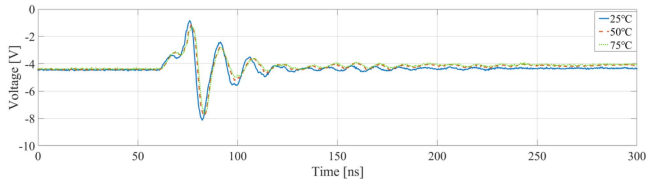

Fig. 23. Crosstalk voltage waveforms at different test temperatures.

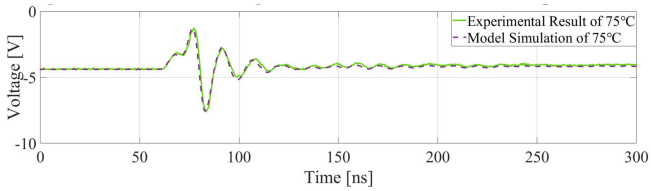

Fig. 24. Comparison of experimental and simulation crosstalk voltage waveforms of 75 °C.

In addition, the comparisons of experimental results under different operation temperature are shown as Fig. 23. As the temperature increases, the maximum value and oscillation of crosstalk voltage are suppressed to a certain extent. However, when the temperature rises above 50 °C, the crosstalk voltage waveform remains almost unchanged as the temperature continues to rise.

In order to provide more application value of the proposed model and consider the influence of temperature on crosstalk, the *I–V* transfer relationship of (3) could be modified in the time-domain model to obtain as

$$\begin{cases} i_d = K_1(T)\cdot \ln\left[1+e^{(v_{\rm gs}-a_0)/b_0}\right] \\ \qquad \cdot \dfrac{(c_0+d_0\cdot v_{\rm gs})\cdot v_{\rm ds}}{1+K_3(T)\cdot(e_0+f_0\cdot v_{\rm gs})\cdot v_{\rm ds}}, \quad v_{\rm ds}>0 \\ i_d = -K_2(T)\cdot \ln\left[1+e^{(v_{\rm gd}-g_0)/h_0}\right] \\ \qquad \cdot \dfrac{v_{\rm sd}}{1+K_4(T)\cdot v_{\rm sd}}, \quad v_{\rm ds}\le 0 \end{cases} \tag{34}$$

in which

$$\begin{cases} K_1(T) = K_1\cdot[1-l_1\cdot(T-25)] \\ K_2(T) = K_2\cdot[1-l_2\cdot(T-25)] \\ K_3(T) = [1-l_3\cdot(T-25)] \\ K_4(T) = [1-l_4\cdot(T-25)] \end{cases}. \tag{35}$$

In the (35), l_1-l_4 is parameters related to temperature characteristics.

In Fig. 24, the model simulation waveform and experimental waveform of crosstalk voltage at 75 °C were compared. The results indicate that the proposed model simulation method is suitable for predicting crosstalk voltage at different temperatures after temperature parameter correction.

V. Conclusion

This article theoretically analyzed the GaN E-HEMT bridge-leg crosstalk behavior in fast switching in details. An explicit analytical model of crosstalk voltage was proposed, with the explicit representation of parasitic parameters and consideration on their staged differences. It is used to evaluate the amplitude and oscillation of crosstalk voltage for guiding GaN device selection and PCB circuit design. Further, based on the theoretical contribution, a scheme of safe operational area design for crosstalk suppression has been determined, which could guide collaborative optimization of multiparameter. The precision of the model is verified through experiments with different circuit conditions. The analysis of crosstalk voltage correlation and sensitivity with circuit parameters and SOA design are also verified through the experimental results and it can contribute to the further study of crosstalk voltage.

Appendix

$$A_2 = \begin{bmatrix} 0 & 0 & -(R_{\rm g2}+sL_{\rm g2}+sL_{\rm cs2}) & 0 & -sL_{\rm cs2} & 0 & 0 \\ 0 & 0 & 0 & -(R_{\rm g1}+sL_{\rm g1}+sL_{\rm cs1}) & -sL_{\rm cs1} & 0 & 0 \\ sC_{\rm iss2} & 0 & 0 & 0 & 0 & -sC_{\rm rss2} & 0 \\ 0 & sC_{\rm iss1} & 0 & 0 & 0 & 0 & -sC_{\rm rss1} \\ g_{\rm m}-sC_{\rm rss2} & 0 & 0 & 0 & 0 & sC_{\rm oss2} & 0 \\ 0 & 0 & 0 & 0 & -(R_{\rm p}+sL_{\rm p}+sL_{\rm s1}+sL_{\rm s2}) & 0 & -1 \\ 0 & 1 & 0 & 0 & R_{\rm dson\_rv} & 0 & 0 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{U_{\rm DRV}}{s} \\ -L_{\rm cs1}\cdot I_{\rm L} \\ C_{\rm rss2}\cdot U_{\rm DC} - C_{\rm iss2}\cdot U_{\rm th} \\ C_{\rm rss1}\cdot(-I_{\rm L}\cdot R_{\rm dson\_rv} - U_{\rm gd(th)}) \\ -g_{\rm m}\cdot\frac{U_{\rm th}}{s} - C_{\rm oss2}\cdot U_{\rm DC} + C_{\rm rss2}\cdot U_{\rm th} \\ \frac{U_{\rm DC}}{s} - L_{\rm s1}\cdot I_{\rm L} \\ -I_{\rm L}\cdot R_{\rm dson\_rv} - \frac{U_{\rm th}}{s} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} 0 & 0 & -(R_{g2}+sL_{g2}+sL_{cs2}) & 0 & -sL_{cs2} & 0 & 0 \\ 0 & 0 & 0 & -(R_{g1}+sL_{g1}+sL_{cs1}) & -sL_{cs1} & 0 & 0 \\ sC_{iss2} & 0 & 0 & 0 & 0 & -sC_{rss2} & 0 \\ 0 & sC_{iss1} & 0 & 0 & 0 & 0 & -sC_{rss1} \\ g_m - sC_{rss2} & 0 & 0 & 0 & 0 & sC_{oss2} & 0 \\ 0 & 0 & 0 & 0 & -(R_p+sL_p+sL_{s1}+sL_{s2}) & 0 & -1 \\ 0 & \frac{C_{rss1}}{C_{oss1}} & 0 & 0 & \frac{1}{sC_{oss1}} & 0 & 0 \end{bmatrix}$$

$$B_3 = \begin{bmatrix} \frac{U_{DRV}}{s} + L_{cs2} \cdot I_L \\ 0 \\ C_{rss2} \cdot U_{DC} - C_{iss2} \cdot U_{plat} \\ -C_{iss1} \cdot v_{gs1}(t_2) \\ -g_m \cdot \frac{U_{th}}{s} - C_{oss2} \cdot U_{DC} + C_{rss2} \cdot U_{plat} \\ \frac{U_{DC}}{s} + L_{s2} \cdot I_L + L_p \cdot I_L \\ \frac{-I_L}{s^2 C_{oss1}} - \frac{C_{rss1}}{sC_{oss1}} \cdot v_{gs1}(t_2) \end{bmatrix}$$

$$A_4 = \begin{bmatrix} 0 & 0 & -(R_{g2}+sL_{g2}+sL_{cs2}) & 0 & -sL_{cs2} & 0 & 0 \\ 0 & 0 & 0 & -(R_{g1}+sL_{g1}+sL_{cs1}) & -sL_{cs1} & 0 & 0 \\ sC_{iss2} & 0 & 0 & 0 & 0 & -sC_{rss2} & 0 \\ 0 & sC_{iss1} & 0 & 0 & 0 & 0 & -sC_{rss1} \\ -sC_{rss2} & 0 & 0 & 0 & 0 & \frac{1}{R_{dson}} + sC_{oss2} & 0 \\ 0 & 0 & 0 & 0 & -(R_p+sL_p+sL_{s1}+sL_{s2}) & 0 & -1 \\ 0 & \frac{C_{rss1}}{C_{oss1}} & 0 & 0 & \frac{1}{sC_{oss1}} & 0 & 0 \end{bmatrix}$$

$$B_4 = \begin{bmatrix} \frac{U_{DRV}}{s} + L_{cs2} \cdot I_L \\ 0 \\ C_{rss2} \cdot I_L \cdot R_{dson} - C_{iss2} \cdot U_{plat} \\ -C_{iss1} \cdot v_{gs1}(t_3) + C_{rss1} \cdot (U_{DC} - I_L \cdot R_{dson}) \\ -C_{oss2} \cdot I_L \cdot R_{dson} + C_{rss2} \cdot U_{plat} \\ \frac{U_{DC}}{s} + L_{s2} \cdot I_L + L_p \cdot I_L \\ \frac{-I_L}{s^2 C_{oss1}} + \frac{U_{DC} - I_L \cdot R_{dson}}{s} - \frac{C_{rss1}}{sC_{oss1}} \cdot v_{gs1}(t_3) \end{bmatrix}$$

$$A_2^* = \begin{bmatrix} 0 & -(R_{g1} + sL_{g1} + sL_{cs1}) & 0 & -sL_{cs1} \\ sC_{iss1} & 0 & -sC_{rss1} & 0 \\ 1 & 0 & 0 & R_{dson\_rv} \end{bmatrix}$$

$$B_2^* = \begin{bmatrix} -L_{cs1} \cdot I_L \\ C_{rss1} \cdot (-I_L \cdot R_{dson\_rv} - U_{gd(th)}) \\ -U_{gd(th)}/s - I_L \cdot R_{dson\_rv} \end{bmatrix}$$

$$A_3^* = \begin{bmatrix} 0 & -(R_{g1} + sL_{g1} + sL_{cs1}) & 0 & -sL_{cs1} \\ sC_{iss1} & 0 & -sC_{rss1} & 0 \\ C_{rss1}/C_{oss1} & 0 & 0 & 1/sC_{oss1} \end{bmatrix}$$

$$B_3^* = \begin{bmatrix} 0 \\ -C_{iss1} \cdot v_{gs1}(t_2) \\ -C_{rss1} \cdot v_{gs1}(t_2)/sC_{oss1} \end{bmatrix}$$

$$A_4^* = \begin{bmatrix} 0 & -(R_{g1} + sL_{g1} + sL_{cs1}) & 0 & -sL_{cs1} \\ sC_{iss1} & 0 & -sC_{rss1} & 0 \\ C_{rss1}/C_{oss1} & 0 & 0 & 1/sC_{oss1} \end{bmatrix}$$

$$B_4^* = \begin{bmatrix} 0 \\ -C_{iss1} \cdot v_{gs1}(t_3) + C_{rss1} \cdot (U_{DC} - I_L \cdot R_{dson}) \\ -C_{rss1} \cdot v_{gs1}(t_3)/sC_{oss1} + (U_{DC} - I_L \cdot R_{dson})/s \end{bmatrix}$$

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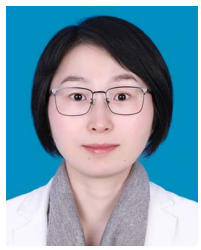

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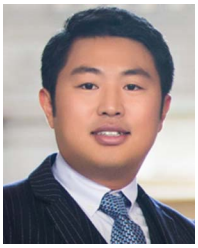

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