An Online Maximum Efficiency Point Tracking Technique for Bidirectional Noninverting Buck–Boost Converter Over Wide Power Range

Fu-Zen Chen, *Member, IEEE*, Hurng-Liahng Jou, *Member, IEEE*, Jinn-Chang Wu, *Member, IEEE*, Hao-Che Hung, and Jun-Yao Luo

***Abstract*—This article presents a novel approach for online tracking of the maximum efficiency point of a bidirectional noninverting buck–boost converter over a wide range of power levels. The proposed technique involves perturbing the phase shift of the gate driver signal and observing the input power and output power to maximize efficiency within both the zero-voltage switching quadrangle mode and the hard switching quadrangle mode. To achieve two modes of operation, a zero-voltage switching detecting circuit is built. This circuit helps detect whether the switching achieves zero voltage switching, sets the phase shift boundary, and adjusts dead time. To evaluate the effectiveness of the proposed approach, a 500 W hardware prototype has been developed.**

***Index Terms*—Bidirectional, maximum efficiency point tracking, noninverting buck–boost, wide power range.**

I. Introduction

A CRITICAL step to slow down global warming is to realize net-zero carbon emission before 2050 [1], [2]. To pursue this goal, most countries pledged to reduce their greenhouse gas emission and make every endeavor to reduce burning fossil fuel in both electricity generation and transportation [3]. One of the effective ways is using sustainable energy sources for electricity generation, such as solar, wind, and hydroelectric power. According to predictions, renewable energy will soon account for a significant portion of grid power usage [4]. However, most sustainable energy sources are intermittent, which makes the grid difficult to maintain the stability. Sustainable energy sources with energy storage systems (ESSs) have become widely endorsed solutions [5]. The installation of energy storage systems has been rapidly increasing in recent years [6]. There will be a greater demand for ESSs as renewable energy sources increase in the future. Another effective way to reduce greenhouse gas emission is to replace internal combustion engine vehicles with electrical vehicles (EVs), which can be powered by sustainable energy sources. Owing to the substantial battery capacitance present in EVs, the incorporation of a vehicle-to-grid framework into the ESSs on the electrical grid has been put forward as a proposition [7]. With the development of ESSs and EVs, there has been a notable increase in battery applications requiring bidirectional converters to work on charging and discharging batteries.

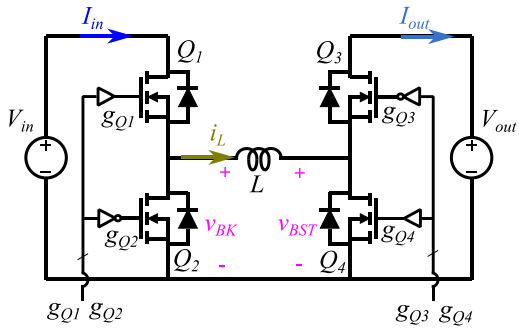

Fig. 1. Topology of NIBB.

Among bidirectional dc–dc converters, noninverting buck–boost (NIBB) converter topology, as shown in Fig. 1, is one of the popular nonisolated topologies, which can achieve both step-up and step-down with low voltage stresses. It has been widely applied on EVs and ESSs [8], [9]. Each arm contains two switches, and the switch node voltages for the buck and boost switching arms, respectively, are v_{BK} and v_{BST}. Based on the inductor voltage second balance, the input voltage (V_{in}) and output voltage (V_{out}) relationship (M) is

$$M = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{D_{BK}}{1 - D_{BST}} \tag{1}$$

where D_{BK} is the duty ratio in control switch Q_1; D_{BST} is the duty ratio in control switch Q_4. Therefore, for a specific operating condition, there are multiple solutions, which means a degree of freedom in controlling the NIBB.

Standard NIBB controller simultaneously modulates D_{BK} to be equal to D_{BST} [10]. Some NIBB controllers switch between

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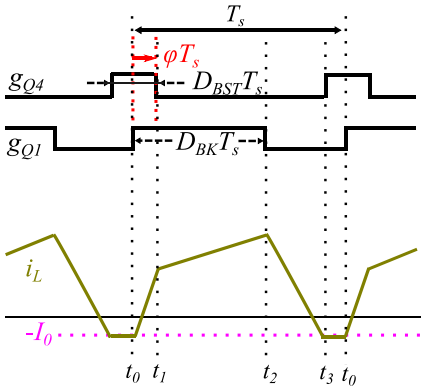

Fig. 2. Illustrated gate drive signals and inductor current waveform in ZVS quadrangle operation mode, an example of $V_{\text{in}} > V_{\text{out}}$.

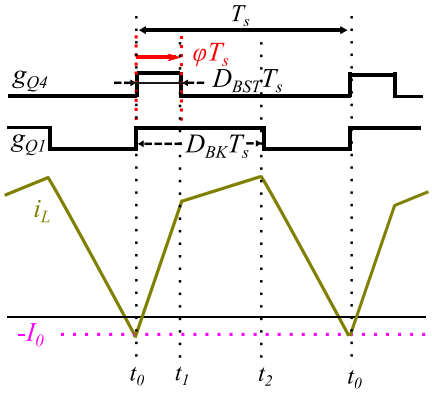

Fig. 3. Illustrated gate drive signals and inductor current waveform in critical regulation mode, an example of $V_{\text{in}} > V_{\text{out}}$.

pure buck mode and pure boost mode to form two-mode operation [11], [12], [13], [14]. Modulation is applied to either D_{BK} or D_{BST}. In two-mode operation, when the input and output voltages closely approximate each other, the presence of a dead-zone can lead to a deterioration of system stability between pure boost mode and pure buck mode, which induces low frequency large ripples [14], [15], [16], [17]. Hence, an extra conventional buck–boost mode operation is added to form a three-mode operation [18], [19]. Selecting the operation range of the buck–boost mode originates from the degree of freedom in (1). Regardless of whether the NIBB is operated in a single-mode, two-mode, or three-mode configuration, the substantial current ripple typically leads to an efficiency drop when the input and output voltages are close to each other.

Without changing the relationship of V_{in} and V_{out}, the phase shift (φ) between two driven signals, D_{BK} and D_{BST}, constitutes an additional degree of freedom for controlling the NIBB, as depicted in Fig. 2. φ is defined as the portion of time interval between the rising edge of the Q_1 gate drive signal (g_{Q1}) and the falling edge of the Q_4 gate drive signal (g_{Q4}) with respect to the switching period (T_s). The waveform of the inductor current (i_L), similar to a quadrangle, is influenced by φ, allowing for adjustments to increase or decrease inductor current ripple. Researchers have leveraged this degree of freedom of the NIBB to enhance the efficiency under this quadrangle operation.

Kolar and Waffler [20] introduced a quadrangle modulation method aiming to achieve zero voltage switching (ZVS) across all switches. By appropriately selecting φ, D_{BK}, and D_{BST}, it is possible to control the polarity of i_L and achieve ZVS during all switching transitions, thereby reducing switching losses, as shown in Fig. 2. However, the presence of a substantial current ripple on i_L leads to an increase in conduction losses. Some researches have worked on reducing i_L root mean square (rms) value or overall conduction loss and also achieving ZVS [21], [22], [23], [24]. Negative current ($-I_0$) is required to achieve ZVS at Q_1, Q_4 turned-ON transitions. For reducing i_L rms value, I_0 has to be precisely controlled with a current zero-crossing detection. The zero-crossing detection has been replaced by the estimated value based on the model [25]. However, studies that achieve ZVS at all switching transitions, are limited by the operation power range. The maximum attainable power is observed when the NIBB operates in critical regulation mode (CRM), wherein Q_1 and Q_4 are simultaneously turned ON, as illustrated in the waveform displayed in Fig. 3.

For most battery applications, the charging and discharging processes of batteries typically occur at distinct power levels. In order to broaden the operational power range, numerous methodologies have been investigated. One approach involves the parallel connection of multiple quadrangle mode operated NIBB modules to expand the power capacity [20]. Paralleling modules leads to a boost in the count of components and introduces complexities in system control. Another strategy incorporates the utilization of multiple inductors that can be switched to enhance power capacity in quadrangle operation mode [26]. An auxiliary switched inductor introduces additional switching elements in series with the inductor, resulting in increased conduction losses. An alternative control utilizes frequency modulation to achieve ZVS in CRM. Frequency-modulated CRM tends to exhibit a propensity for low-frequency switching at high power levels and high-frequency switching at low power levels [27]. Furthermore, an endeavor has been made to maintain consistent quadrangle operation under light loads while employing frequency-modulated CRM operation under heavy loads. Nonetheless, this approach inherits the same limitations as CRM [28]. To achieve high efficiency over wide power range on NIBB, some of them incorporate supplementary power components and some of them change the operation frequency at heavy load, which introduces complexities in the design of electromagnetic interference filters.

To achieve high efficiency over wide power range, the selection of the switching frequency and the inductor value is critical. Switched mode power converters tend to have more conduction losses at high power levels and more switching losses at low power levels [29]. For constant switching frequency operation, the selection of the inductor value affects the inductor current ripple. A large current ripple is positively related to more conduction losses; on the contrary, it is required to have a large inductor current ripple to achieve ZVS at CRM or quadrangle mode. Efficiency is mainly determined by the combination of switching and conduction losses. It is possible to have NIBB be in ZVS quadrangle mode at light load and in hard switching (HS) quadrangle mode at heavy load [30].

Numerous researches are devoted to pursuing the minimum losses in nonisolated dc–dc converters [31]. One approach involves online tracking of the maximum efficiency point to optimize the switching frequency [29]. Besides, applying the switching frequency as an extra degree of freedom in ZVS quadrangle operation is proposed in [32]. Another method suggests the online dead times optimization utilizing the minimum duty cycle as a guiding criterion [33]. Similarly, a concept involving multidimensional optimization, including switching frequency and dead times across both switching legs has been presented; however, its efficiency point tracking relies on a fitting function from the sensed outcomes [34]. In photovoltaic application, a method of online optimization tracks both the maximum power point and the maximum efficiency point by adjusting duty cycle and switching frequency [35].

For a given NIBB hardware, the manipulation of control parameters, such as φ, D_{BK}, and D_{BST}, switching frequency, and dead times between gate drive signals, affect the power losses. The optimum value of those parameters to achieve minimum losses varies depending on the operation conditions, including different $V_{\rm in}$, $V_{\rm out}$, and process power levels. For a constant frequency operated NIBB, a two-dimensional online efficiency optimization technique based on the converter loss model to track maximum efficiency point in φ, D_{BK} vis presented [36]. Among those efficiency optimization methodologies, certain approaches are constrained to operate exclusively within specific modes; some modulate the switching frequency at high power levels; moreover, there exist methods that are executed in real-time but need precise loss parameter information.

A new online maximum efficiency point tracking technique for bidirectional NIBB, operated in constant frequency over wide power range, is proposed in this article. The proposed method is capable of running the NIBB in both ZVS or HS quadrangle modes [30]; furthermore, it adjusts φ while minimizing the power loss of the converter without relying on precise system parameters. The salient features of the proposed approach are shown as follows.

1) The proposed controller is capable of operating in either the ZVS quadrangle mode or the HS quadrangle mode. Utilizing the maximum efficiency point tracker (MEPT) algorithm, it typically functions in the ZVS quadrangle mode at low power levels and in the HS quadrangle mode at high power levels to achieve high efficiency.
2) The proposed controller ensures that the converter operates at a constant switching frequency in both modes.
3) No additional power components are required, and only an extra winding on the inductor is added to the power stage.
4) The system is robust under the condition of parameter variations and can be operated without precise component parameters.

The rest of this article is organized as follows. ZVS and HS combined quadrangle operation of NIBB is discussed in Section II. The adaptive phase shift technique that tracks with maximum efficiency point is introduced in Section III. Experimental results on a 500 W digitally controlled NIBB are given in Section IV. Finally, Section V concludes this article.

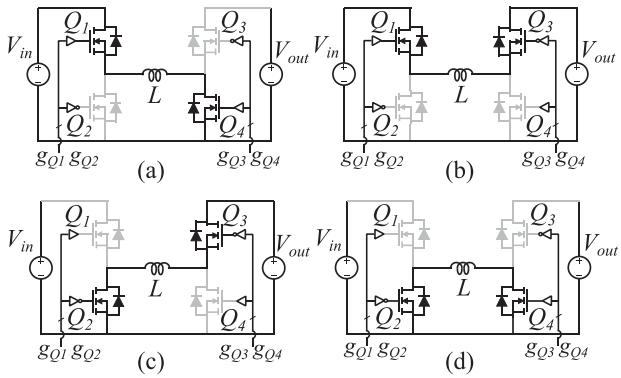

Fig. 4. NIBB main operational stages. (a) Stage A. (b) Stage B. (c) Stage C. (d) Stage D.

II. ZVS and HS Combined Quadrangle Operation

If the switching transitions are ignored, there are mainly four operational stages for NIBB, as shown in Fig. 4. In stage A, Q_1 and Q_4 are turned ON and Q_2 and Q_3 are turned OFF. The voltage difference between v_{BK} and v_{BST} is equal to $V_{\rm in}$. In stage B, Q_1 and Q_3 are turned ON and Q_2 and Q_4 are turned OFF. The voltage difference between v_{BK} and v_{BST} is equal to $V_{\rm in}$-$V_{\rm out}$. In stage C, Q_2 and Q_3 are turned ON and Q_1 and Q_4 are turned OFF. The voltage difference between v_{BK} and v_{BST} is equal to $-V_{\rm out}$. In stage D, Q_2 and Q_4 are turned ON and Q_1 and Q_3 are turned OFF. The voltage difference between v_{BK} and v_{BST} is equal to 0.

If there are four working stages occurring within a single switching period, with all active switches being turned ON and OFF once during this period, there are six possible combinations from stage A, B, C, D to form quadrangle mode operation. Among those combinations, excluding those cannot be realized in buck–boost mode, the sequence of working stages in the order A-B-C-D leads to the lowest achievable value for the inductor current [37]. Using this sequence of operations as a basis, a discussion on the phase shift boundary of the ZVS quadrangle mode is shown in Section II-A. After that, Section II-B explains how the detection mechanism for ZVS works. Then, in Section II-C, the operating principle of the HS/ZVS quadrangle mode is introduced.

A. Phase Shift Boundary of ZVS Quadrangle Mode

Based on the working stages in the A-B-C-D sequence, the inductor current waveform of the NIBB is presented in Fig. 2. In order to achieve ZVS, it is necessary to have the inductor current be positive at t_1 and t_2, when Q_3 and Q_2 are turning ON respectively; and have the inductor current be negative at t_3 and t_0, when Q_4 and Q_1 are turning ON. If the inductor current is nearly zero at the beginning of the switching period (t_0), the output current over one switching period ($I_{\rm out}$), as (2) shown, is affected by D_{BK}, D_{BST}, and φ, which are defined in Section I. For a given $V_{\rm in}$ and $V_{\rm out}$, D_{BK} and D_{BST} have only one constraint, as (1). There are multiple solutions on D_{BK} and φ to achieve a processed power in a given input/output voltage. The relationship between D_{bk} and φ for a given voltage gain and processed current is highly nonlinear [20]. In Fig. 5(a), it is

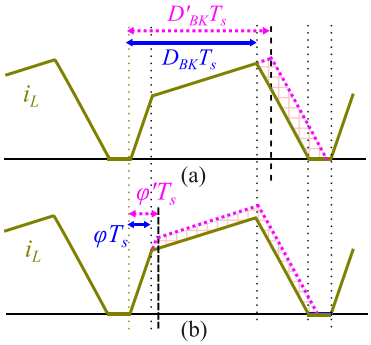

Fig. 5. Illustrated inductor current waveforms in quadrangle operation mode, an example of $V_{\text{in}} > V_{\text{out}}$. (a) Adjusting D_{BK}. (b) Adjusting φ.

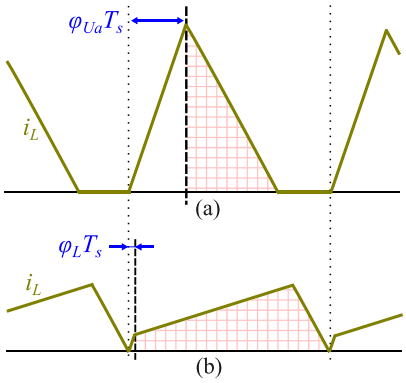

Fig. 6. Illustrated inductor current waveform in quadrangle operation mode, an example of $V_{\text{in}} > V_{\text{out}}$. (a) Upper boundary of φ (φ_{Ua}). (b) Lower boundary of φ (φ_L).

apparent that by increasing the duty ratio on the buck arm from D_{BK} to D'_{BK}, the output current (I_{out}) experiences an increase. Similarly, Fig. 5(b) illustrates that I_{out} rises as φ increases. Adjusting either D_{BK} or φ has the ability to regulate I_{out}

$$I_{\text{out}} = \frac{1}{T_s}\int_{t_1}^{t_3} i_L(t)\,dt. \tag{2}$$

Inherently, under this working stage sequence, there is a bound of D_{BK} and φ is shown as

$$0 \le \varphi \le D_{BK} \le \min[M,\ 1]. \tag{3}$$

For a given processed power, under ZVS operation mode, there is an upper boundary of phase shift (φ_{Ua}), when φ is always equal to D_{BK}, as the inductor current waveform shown in Fig. 6(a); and there is a lower boundary of phase shift (φ_L), when the converter is operated in CRM, as shown in Fig. 6(b).

Based on the ideal inductor waveform, φ_U can be written as

$$\varphi_{Ua} = \sqrt{2M\frac{I_{\text{out}}L}{V_{\text{in}}T_s}} \tag{4}$$

where L is the inductor value. φ_L can be written as

$$\varphi_L = \frac{M^2 - \sqrt{M - 2\left(M^2+M+1\right)\left(\frac{I_{\text{out}}L}{V_{\text{in}}T_s}\right)}}{\left(M^2+M+1\right)}. \tag{5}$$

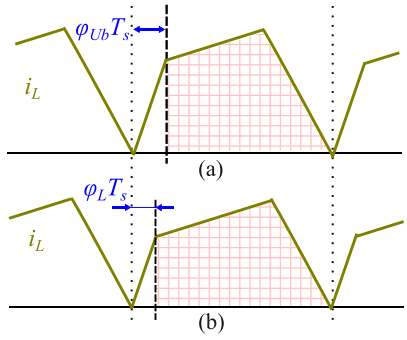

Fig. 7. Illustrated inductor current waveform in quadrangle operation mode, an example of $V_{\text{in}} > V_{\text{out}}$. (a) Upper boundary of φ (φ_{Ub}). (b) Lower boundary of φ (φ_L).

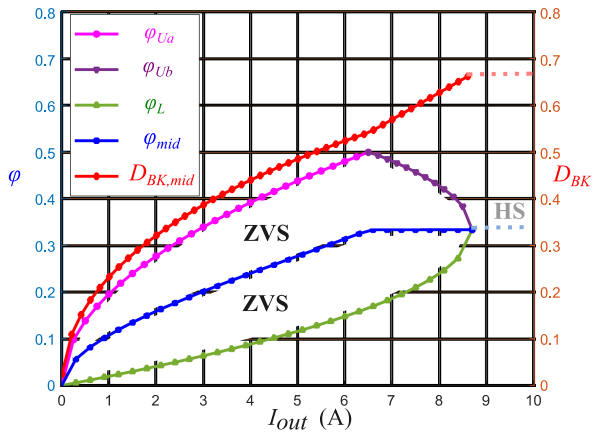

Fig. 8. Boundary of ZVS operation region (φ_U, φ_L), robust phase shift selection (φ_{mid}), and its corresponding duty cycle (D_{BK}) in quadrangle operation mode ($V_{\text{in}} = V_{\text{out}} = 48$ V; $L = 9.2$ μH; $f_s = 100$ kHz).

However, with I_{out} increases, ZVS operation region is limited by CRM mode only. There is a lower boundary of phase shift (φ_L) in CRM, as shown in Fig. 7(b); as the inductor current waveform shown in Fig. 7(a), an upper boundary (φ_{Ub}) is also in CRM mode, φ_{Ub} can be written as

$$\varphi_{Ub} = \frac{M^2 + \sqrt{M - 2\left(M^2+M+1\right)\left(\frac{I_{\text{out}}L}{V_{\text{in}}T_s}\right)}}{\left(M^2+M+1\right)}. \tag{6}$$

Fig. 8 illustrates an example of φ operation region in different I_{out} under ZVS quadrangle mode. As indicated in (4), (5), and (6), φ_U and φ_L are functions of L, which exhibit a certain degree of tolerance in practice. Varied values of L lead to a transformation of the φ operational region within ZVS, and impact the upper limit of I_{out} in ZVS operation.

Due to the variation of L, for a robust operation, a selection of φ_{mid} to be the middle between the upper and the lower boundary is shown in Fig. 8 [30]. The associated duty ratio ($D_{BK,mid}$) is also represented in the same figure. Notably, $D_{BK,mid}$ is monotonically increases with respect to the increase of I_{out}. Therefore, for a given φ_{mid}, I_{out} can be regulated by adjusting D_{BK}.

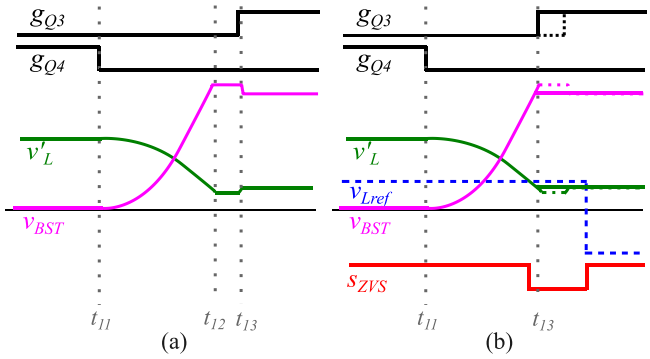

Fig. 9. Illustrated waveforms of switching transition at instant t_1. (a) Transition with fixed long dead time. (b) Transition based on s_{ZVS} signal.

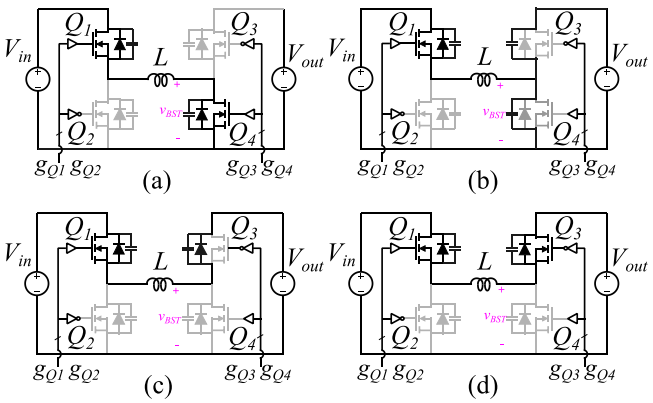

Fig. 10. NIBB operational stages at t_1 transition. (a) Stage A. (b) Stage AB1. (c) Stage AB2. (d) Stage B.

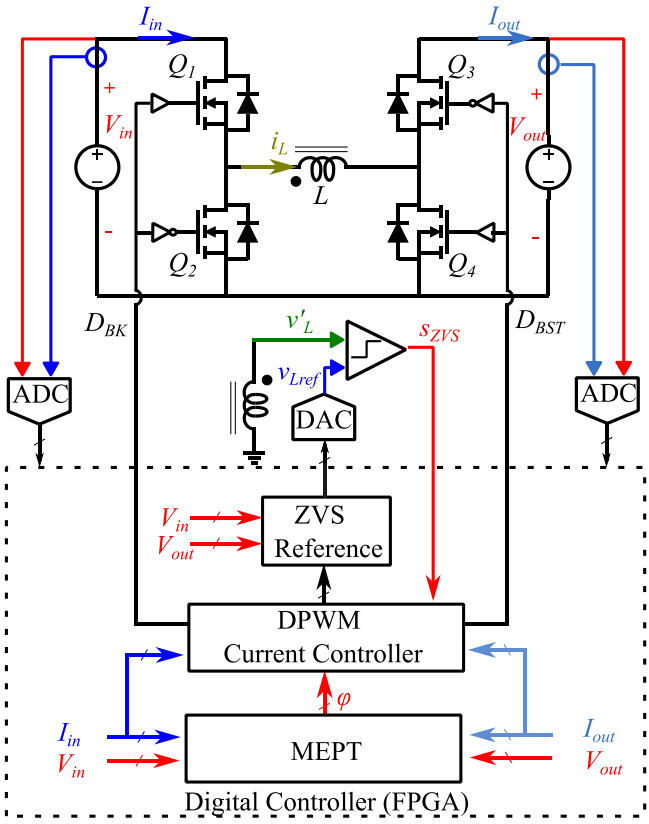

Fig. 11. System block diagram of the proposed approach.

B. ZVS Detection

As described in the previous section, the dead time plays a significant role in power loss [33], [35], [38], [39]. At the instant t_1 in Fig. 2, NIBB is at the switching transition between stage A and stage B. The illustrated waveforms during this transition are shown in Fig. 9(a); while the corresponding stages of operation are shown in Fig. 10. Q_3 is turned OFF at t_{11}, and positive inductor current charges the parasitic capacitance on both Q_3 and Q_4 at stage AB1, as shown in Fig. 10(b). v_{BST} increases until the parallel diode of Q_3 conducts at t_{12}. Starting from t_{12}, the inductor current flows through the parallel diode of Q_3 at stage AB2, as shown in Fig. 10(c). NIBB stays at stage AB2 until Q_3 is turned ON at t_{13}. At t_{13}, the inductor current no longer flows through parallel diode of Q_3, and the voltage drops across Q_3 reduces, which causes v_{BST} to change slightly, as illustrated in Fig. 9(a).

Most NIBBs operated in ZVS quadrangle mode all start the inductor current from a negative value at t_0, as shown in Fig. 2. In order to ensure consistent ZVS operation during steady-state conditions, there is always a mechanism for detecting current zero crossing at instant t_3. However, for the remaining transitions, a detection mechanism is absent. To ensure ZVS switching in these transitions, the dead times associated with transitions t_1, t_2, and t_4 are uniformly set to sufficiently lengthy durations across all operational conditions. Large duration from t_{12} to t_{13} leads to more conduction loss.

In order to reduce the loss from long dead times, for example t_{12} to t_{13}, an adaptively adjustable dead time based on the measurement is proposed [30]. An extra winding on the inductor for inductor voltage information, a ZVS comparator, and a digital to analog converter (DAC) are implemented as the ZVS detection circuits shown in Fig. 11. ZVS comparator compares the secondary voltage of the inductor (v'_L) with ZVS reference voltage (v_{Lref}) from DAC, and generates a digital signal, ZVS comparator signal (s_{ZVS}), and sends it back to the digital controller.

As illustrated in Fig. 9(b), by assigning a proper value to v_{Lref}, s_{ZVS} toggles right before instant t_{12}, which is a timing signal for Q_3 to achieve ZVS switching. Hence, at all working stages, digital controller sends different ZVS reference voltage to achieve ZVS at all switching transitions, as (7). Those reference voltages are functions of V_{in}, V_{out} and a fixed voltage offset on the reference circuits (ΔV_{ref}). The illustrated waveforms of ZVS detection circuits are shown in Fig. 12

$$\begin{array}{ll} V_{\mathrm{in}} - \Delta V_{ref} & @t_0 \\ V_{\mathrm{in}} - V_{\mathrm{out}} + \Delta V_{ref} & @t_1 \\ -V_{\mathrm{out}} + \Delta V_{ref} & @t_2 \\ -\Delta V_{ref} & @t_3 \end{array} . \tag{7}$$

A short dead time can result in current shoot-through, while an extended dead time leads to increased conduction loss on the body diode of the power switch, as shown in Fig. 9(a).

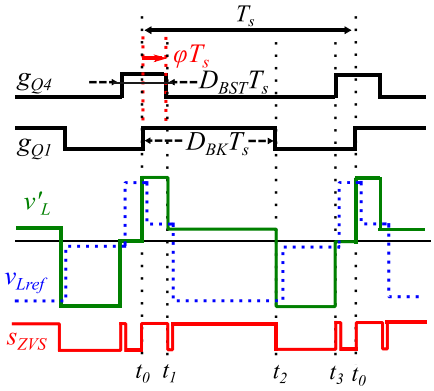

Fig. 12. Illustrated waveforms of ZVS detection circuits.

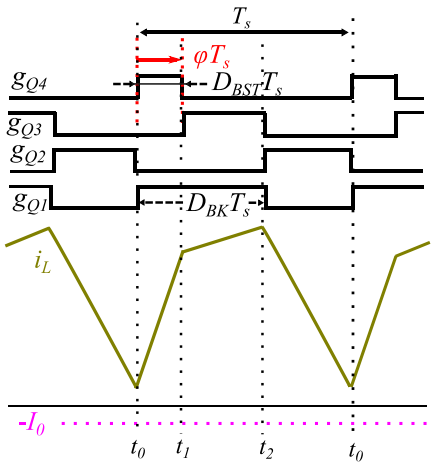

Fig. 13. Illustrated gate drive signals and inductor current waveform of the proposed approach in quadrangle HS operation mode.

Optimizing dead time relies on various factors such as power switch parameters and operating conditions. The proposed ZVS detection circuit does not aim to optimize dead time; rather, it assists in controlling the power switches with an appropriate dead time, which may not necessarily be the optimized value.

C. HS / ZVS Quadrangle Operation Mode

To achieve wide load range operation, NIBB has to work at both HS and ZVS modes. At light load, NIBB can be operated in ZVS quadrangle mode, as shown in Fig. 2. The maximum power level for ZVS quadrangle mode is CRM, as shown in Fig. 3. In order to further increase the power level, if NIBB keeps its phase shift value, it has to work at HS quadrangle mode, as shown in Fig. 13. For the robust selection of phase shift (φ_{mid}), as shown in Fig. 8, its phase shift value is fixed at quadrangle HS mode, and the D_{BK} keeps around the same value [30].

Digital pulsewidth modulation (DPWM) must be able to function in both ZVS and HS quadrangle modes. As the proposed DPWM state machine shown in Fig. 14, the NIBB starts its sequence from stage A, when Q_1 and Q_4 are actively conducting. It stays at stage A until φT_s, at which point Q_4 is turned OFF. Upon receiving a low $s_{\rm ZVS}$ signal, NIBB turns Q_3 ON and moves to stage B. The operation remains within stage B until reaching

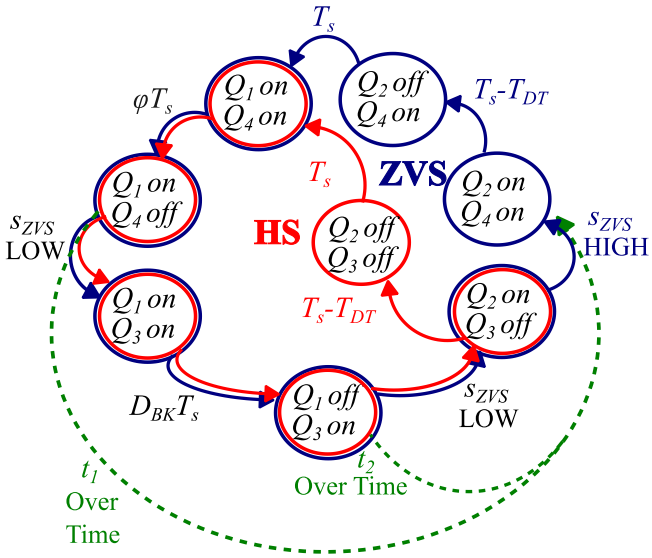

Fig. 14. Proposed DPWM state machine. ZVS quadrangle mode-blue loop; HS quadrangle mode-red loop; over time operation-green dashed line.

$D_{BK}T_s$, where D_{BK} is the output of the current controller. At $D_{BK}T_s$, Q_1 is turned OFF. Once the $s_{\rm ZVS}$ is low, NIBB progresses to stage C, with Q_2 being enabled and Q_3 conducting through the parallel diode, as shown at t_2 in Fig. 13. Parallel diode of Q_3 keeps conducting until i_L reaches zero, while $s_{\rm ZVS}$ pulls high. If $s_{\rm ZVS}$ pulls high before the end of the switching period, NIBB switches to stage D and it is operated in ZVS quadrangle mode, as shown by the blue loop in Fig. 14. On the other hand, if $s_{\rm ZVS}$ keeps low, all switches are turned OFF and it waits for a fixed dead time (T_{DT}) to start another period, as shown by the red loop in Fig. 14.

Based on the $s_{\rm ZVS}$ signal, the DPWM state machine, as illustrated by the blue loop in Fig. 14, can achieve both ZVS quadrangle mode and HS quadrangle mode, as depicted by the red loop in Fig. 14, according to the description above. At instant t_1 and t_2, Q_3 and Q_2 are turned-ON depended on the high to low transition of the $s_{\rm ZVS}$ signal. Nevertheless, $s_{\rm ZVS}$ may stay high if Q_3 and Q_2 cannot achieve ZVS turned-ON at t_1 and t_2. There is a overtime protection mechanism to start over another switching period, as the green dashed line in Fig. 14.

The robust selection on the phase shift (φ_{mid}) at middle of the ZVS boundary (φ_{Ua}/$\varphi_{Ub,}$ φ_L), as illustrated in Fig. 8, increases to enlarge inductor current ripple, when $I_{\rm out}$ increases. With the ability to operate in both ZVS and HS quadrangle mode, NIBB can be operated over wide power range. However, robust selection of the phase shift may not be the maximum efficiency choice. A phase shift based maximum efficiency point tracker technique is proposed in the following section.

The current controller regulates output current by adjusting D_{BK} in both ZVS and HS modes. To design a current controller for both modes, the control-to-output transfer function has to be considered in both scenarios. The small-signal average transfer function from d_{BK} to i_o in ZVS quadrangle mode is a gain [24], as shown in (8); meanwhile, the small-signal average transfer function from d_{BK} to i_o in HS quadrangle mode is an integrator

[40], as shown in (9)

$$\frac{i_o(s)}{d_{bk}(s)} = \frac{T_s V_{\text{in}}}{L}\left[\left(\frac{V_{\text{in}}}{V_{\text{out}}} - 1\right) D_{BK} + \varphi\right] \tag{8}$$

$$\frac{i_o(s)}{d_{bk}(s)} = \frac{V_{\text{in}}}{sL}(1-\varphi). \tag{9}$$

The small-signal gains from d_{BK} to i_o in both ZVS and HS quadrangle modes are monotonic as long as the Q_2 achieves ZVS turn-ON in ZVS quadrangle mode, and the phase shift is less than 100% in HS quadrangle mode. The current controller design is based on the small-signal transfer functions. To further increase the current loop bandwidth, a signal controller with parameter adjustments can be outlined in the two-mode design, as described in [41].

III. Phase Shift Based Maximum Efficiency Point Tracker

For a NIBB, φ, D_{BK}, D_{BST}, dead times are the parameters to be controlled in regulating I_{out} at the operation condition (V_{in} and V_{out}). In the proposed approach, the determination of dead times is guided by the ZVS detection mechanism explained in the previous section. According to the principle of inductor voltage-second balance, there is a constrain in (1). I_{out} can be regulated by adjusting φ or D_{BK}, which ends up having one extra degree of freedom. Given a certain value of φ, the regulation of I_{out} can be achieved by adjusting D_{BK}. For a given input/output voltage, conduction loss dominates during high processed power operation, while switching loss dominates during low processed power operation. With a reduction in φ, overall efficiency increases as conduction loss decreases. Overall loss decreases with φ reduction until the increment of the switching loss surpasses the decrement of the conduction loss. Therefore, φ can serve as a parameter to track maximum efficiency. The fundamental principle of the proposed maximum efficiency point tracker is presented in Section III-A; while its operation limits are presented in Section III-B.

A. Maximum Efficiency Point Tracker

The proposed MEPT is based on the perturb and observe technique. As shown in the system block diagram in Fig. 11, the MEPT in the digital controller acquires voltage and current data from both the input and output terminals. Through the data, the efficiency of the converter (η) can be computed. The operational procedure of the proposed MEPT controller follows the state machine shown in Fig. 15. The MEPT controller perturbs φ and waits for the current to be regulated via adjusting D_{BK}. After the current is well regulated, the MEPT controller computes η. If there is an increase in η, the controller maintains the present direction to perturb φ; however, if η decreases, the controller changes the direction to perturb φ, as the brown loop shown in Fig. 15.

The system block diagram of the proposed MEPT controller is shown in Fig. 16. The corresponding state machines of the DPWM block and MEPT bock are shown in Figs. 14 and 15, respectively. I_{out} is regulated by the current controller via D_{BK} in the current loop, while the slow MEPT loop tracks the maximum efficiency by perturbing φ. Perturbing φ in the MEPT controller affects the boost duty ratio. However, since MEPT loop is a slower loop in the system, the current controller adjusts D_{BK} to maintain the input and output voltage relationship required by (1).

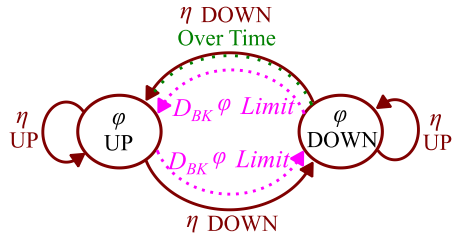

Fig. 15. Proposed MEPT state machine. Normal MEPT- brown loop; D_{BK} and φ limits-pink dashed line; over time limit-green dashed line.

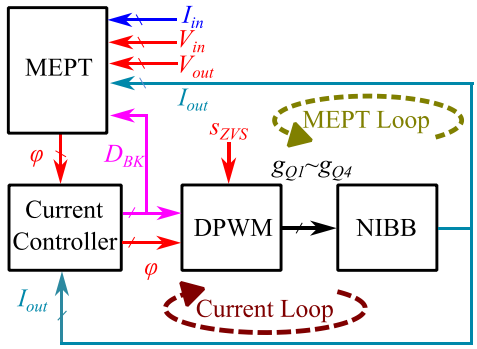

Fig. 16. System block diagram of the proposed MEPT controller.

With some power measurement error, the MEPT controller tracks around the maximum efficiency point. As long as the error is small, the proposed MEPT algorithm still maintains the system at a high-efficiency point.

B. Operation Limits

There are some operation limits in the proposed control strategy of NIBB.

One limitation is the inherent bound of D_{BK} and φ, as (3). When φ reaches its inherent boundary, the MEPT controller adjusts the direction to perturb φ accordingly. Besides, in steady state, when D_{BK} is saturated and I_{out} is not regulated well, the selection of φ is not proper. Hence, the controller changes the direction to perturb φ, as the pink dashed line shown in Fig. 15.

The other constraint arises from the operation involving ZVS. Operated in either ZVS or HS quadrangle, as inductor current waveforms illustrated in Figs. 2 and 13, respectively, inductor current values have to be positive at instant t_1 and t_2. To be more precise, the inductor current limitation to achieve ZVS at instant t_1 and t_2 is listed in

$$i_L(t_1) > V_{\text{out}}\sqrt{\frac{2C_{oss}}{L}} \tag{10}$$

$$i_L(t_2) > V_{\text{in}}\sqrt{\frac{2C_{oss}}{L}} \tag{11}$$

TABLE I
DESIGN PARAMETER OF NIBB CONVERTER

V_{in}	Input voltage	36 V~60 V
V_{out}	Output voltage	36 V~60 V
	Max Power	500 W
f_s	Switching Frequency	100 kHz
L	Inductor Turns Ratio	9.2 μH PQ3230 13:1
Q_1~Q_4	Switches	TK42A12N1
	Comparator	LT1711
	DAC	AD9752
	ADC	AD7492-5
	Current Transducer	ACS730
	Gate Driver	LM5107
	Digital Controller (FPGA)	Cyclone V SE 5CSEBA6U23I7

where C_{oss} is the output capacitance of the switches. Due to variations in both C_{oss} and L, the ZVS operation current changes across different components.

Despite the variation of the components, based on the ZVS detection circuits, ZVS can be distinguished through s_{ZVS} signal. As the green dashed line shown in Fig. 14, when Q_4 is turned OFF, the controller awaits a low s_{ZVS} signal to activate Q_3. If the s_{ZVS} signal remains high beyond a certain duration, this over time indicates that at time t_1, the NIBB cannot achieve ZVS. In response, the controller initiates another switching cycle, as illustrated by the green dashed line in Fig. 14. As long as there is an over time indication, either in t_1 or t_2, the MEPT controller changes the direction of φ, as the green dashed line shown in Fig. 15.

IV. EXPERIMENT RESULTS

A 500 W NIBB converter has been built, as shown in Fig. 11, using a field programmable gate array (FPGA) development platform to implement the digital controller. The design parameters of the hardware configuration are listed in Table I.

The proposed method employs an online MEPT controller capable of adapting to variations in component parameters. Low-cost power switches are employed in the hardware. The selection of capacitor values depends on the input/output voltage ripple, while the inductor value is designed to operate at the boundary of HS and ZVS at 60% of the rated power. The choice of core, wire, and airgap is determined using textbook formulas from [40]. Efficiency measurement is facilitated by voltage and current sensing through ADCs on both sides of the converter. An extra winding on the inductor is added to serve for dead time adjustment and the mode selection between HS and ZVS. The ZVS reference voltage is generated from a 12-bit DAC (AD9752), featuring a 1 ns propagation delay and a 35 ns settling time. This timeframe is less than two main clock periods of the FPGA, which operates with a 50 MHz main clock. Depending on operational conditions, the required dead time may vary from less than 100 ns to over 400 ns. Taking into account the rising and falling transitions of the power switch, as well as gate drive delay, this setup proves effective for most applications. However, for those applications with an ultrahigh switching frequency, a low-resolution DAC with a higher response time may be more suitable.

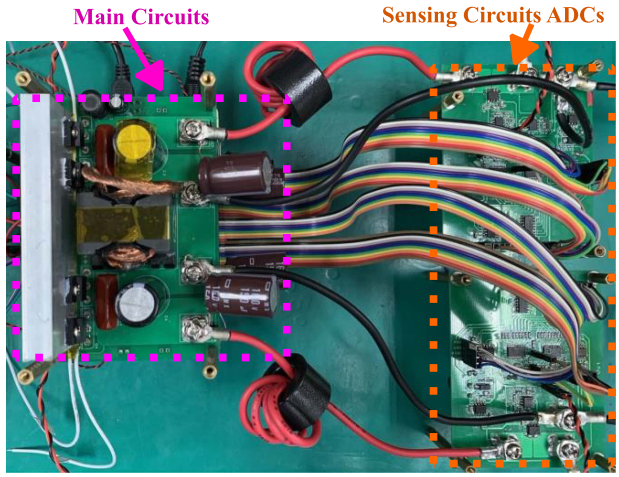

Fig. 17. Photograph of hardware setup.

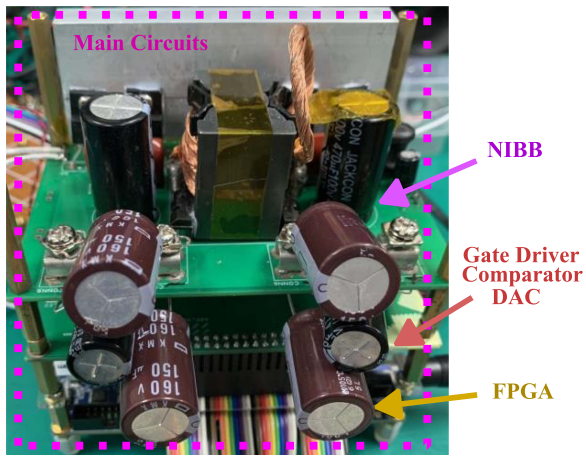

Fig. 18. Photograph of main circuits.

In order to test the NIBB with bidirectional current under different input/output voltages, two sets of dc power supplies (IT6513C) with a decent amount of resistive load are connected to the input and output ports, respectively, serving as the source or the load.

The photograph of the hardware setup is shown in Fig. 17, offering a detailed view of the main circuits, as displayed in Fig. 18.

The experimental results of ZVS detection function and ZVS and HS quadrangle mode operation are presented in Section IV-A, followed by the experimental results on phase shift based MEPT; the final subsection shows the achieved efficiency and efficiency comparison in different approaches.

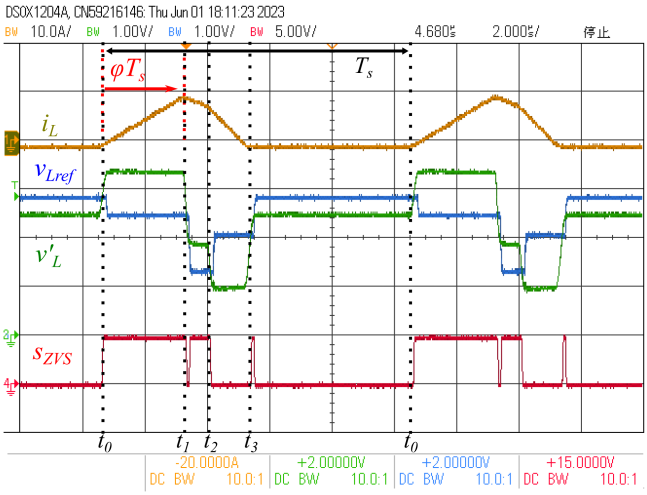

Fig. 19. Experimental waveforms at ZVS quadrangle mode with ZVS detection ($V_{\rm in} = 36$ V; $V_{\rm out} = 60$ V).

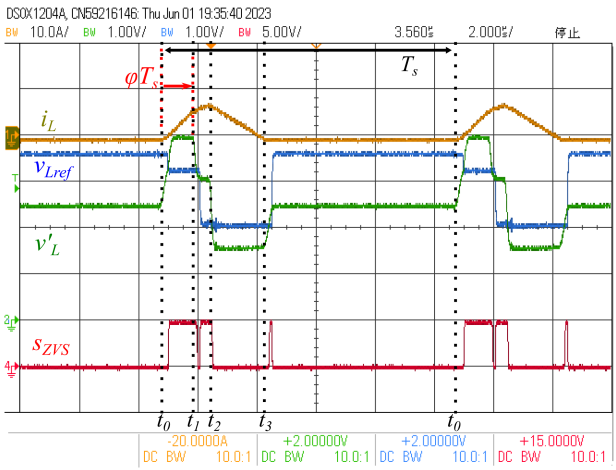

Fig. 20. Experimental waveforms at ZVS quadrangle mode with ZVS detection ($V_{\rm in} = 60$ V; $V_{\rm out} = 36$ V).

A. ZVS and HS Quadrangle Mode Operation

Utilizing the ZVS detection circuits described in Section II-B, the experimental waveforms of the NIBB operated in ZVS quadrangle mode at voltage boost condition, $V_{\rm out} > V_{\rm in}$, are shown in Fig. 19. Based on the $s_{\rm ZVS}$ signal, all four switches, Q_1–Q_4 achieve ZVS turn-ON at instant of t_0, t_2, t_1, t_3, respectively. On the other hand, Fig. 20 shows the experimental waveforms in ZVS quadrangle mode at voltage buck condition, $V_{\rm in} > V_{\rm out}$. Switches, Q_2, Q_3, Q_4 achieve ZVS turn-ON at instant of t_2, t_1, t_3, but Q_1. However, with $s_{\rm ZVS}$ signal, Q_1 achieves low voltage switching at instant t_0.

NIBB can be operated in either ZVS or HS quadrangle modes. During low power processing, the NIBB operates within the ZVS quadrangle mode. However, when handling higher power levels, the NIBB moves to the HS quadrangle mode, as evidenced by the experimental waveforms illustrated in Fig. 21. Switches, Q_2 and Q_3, achieve ZVS turn-ON at instant t_2 and t_1; Q_1 and Q_2 are hard switched at t_0.

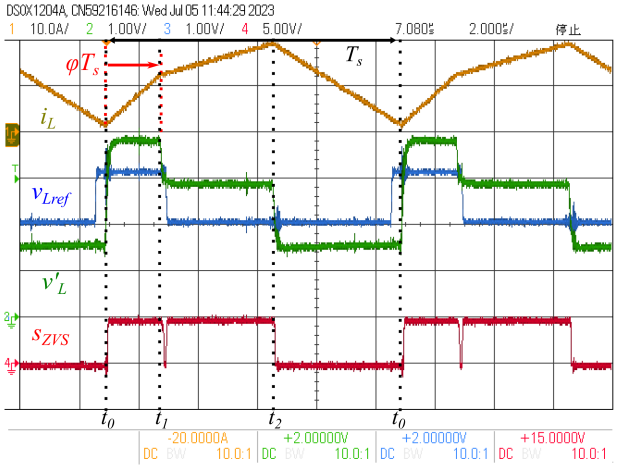

Fig. 21. Experimental waveforms at HS quadrangle mode with ZVS detection ($V_{\rm in} = 60$ V; $V_{\rm out} = 36$ V).

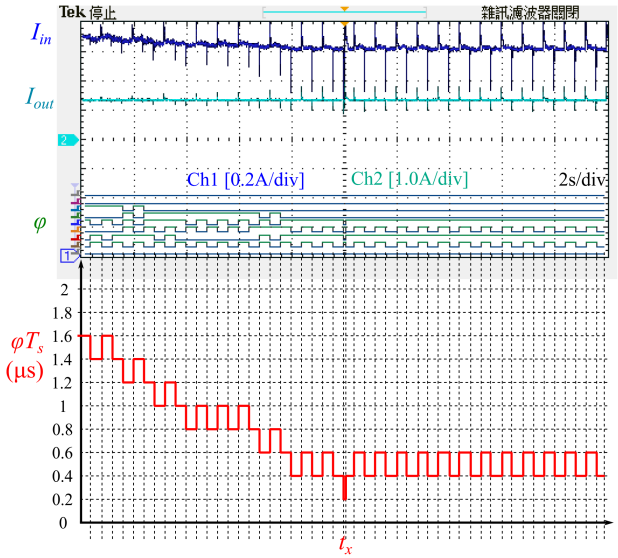

Fig. 22. Experimental waveforms of MEPT at ZVS quadrangle mode ($V_{\rm in} = 48$ V; $V_{\rm out} = 48$ V).

Regarding the ZVS reference voltage waveform shown in Figs. 19–21, the long settling time is caused by an amplification circuit followed by DAC, whose bandwidth is limited by the selected op-amp.

B. Maximum Efficiency Point Tracker

The proposed MEPT maximizes efficiency by iteratively perturbing the phase shift and monitoring converter efficiency through input and output power measurements. For fixed input /output voltages and fixed power level, as the experimental waveforms shown in Fig. 22, the MEPT controller adjusts phase shift and the input current reduces. The controller keeps the perturb and observe until time t_x, when φ is too small to achieve ZVS at t_1 or t_2. When the comparator signal over time happens, the MEPT controller establishes this phase as the operational boundary. This boundary continues to constrain the phase shift until a

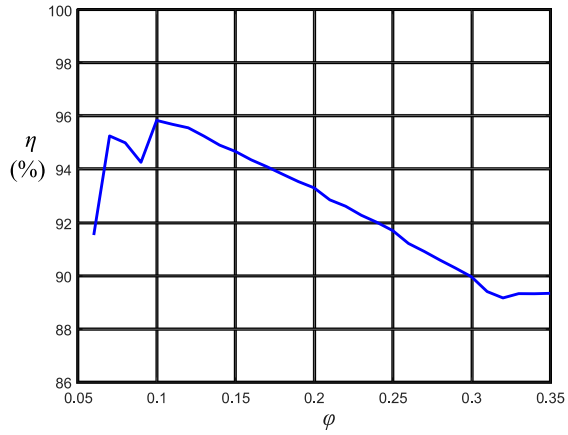

Fig. 23. Experimental efficiency under different φ ($V_{\rm in} = 48$ V; $V_{\rm out} = 60$ V).

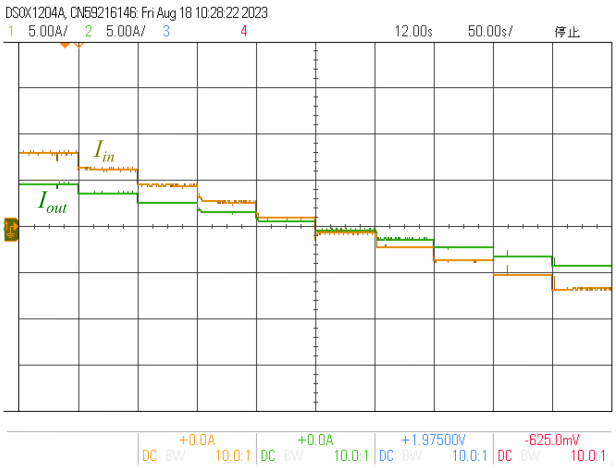

Fig. 24. Experimental waveforms of MEPT ($V_{\rm in} = 36$ V; $V_{\rm out} = 60$ V).

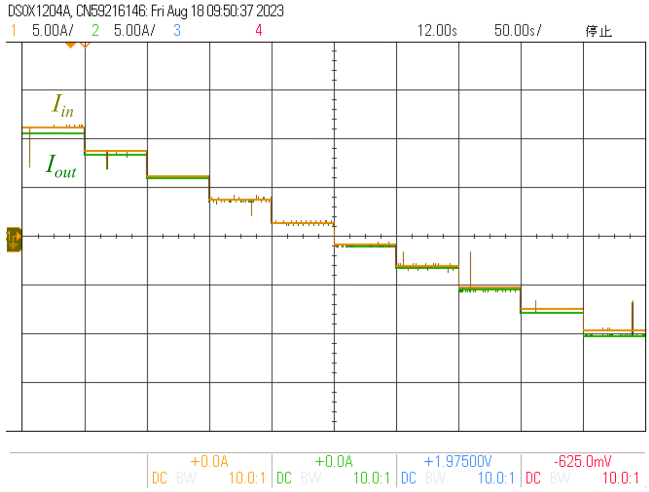

Fig. 25. Experimental waveforms of MEPT ($V_{\rm in} = 48$ V; $V_{\rm out} = 48$ V).

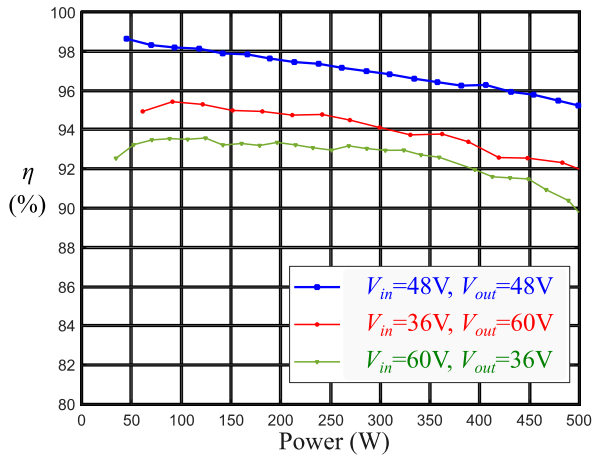

Fig. 26. Efficiency operated in MEPT under different input/output voltages.

change in operational conditions occurs, such as alterations in input/output voltages or power levels.

The maximum efficiency point is highly depended on component selection, inductor design, PCB layout, dead time, and switching frequency. It is possible that there are multiple local maximum efficiency points existing [36]. However, those local maximum efficiency points happened when ZVS turn-ON is not achieved at instant t_2 or t_1, as Fig. 23. When the operation point changes, the proposed MEPT starts from a high initial φ, as the phase shift time shown in Fig. 22.

Fig. 24 shows bidirectional current regulation at voltage buck and voltage boost conditions. It initiates in voltage boost mode when the currents are positive, transitioning to voltage buck mode as the regulation current decreases and becomes negative. Fig. 25 shows the full power range operation when input voltage equals to output voltage. It shows that under light load conditions, the input current closely matches the output current, resulting in high efficiency.

C. Efficiency

The efficiency (η) of the NIBB converter applying proposed MEPT controller at different input/output voltages are shown in Fig. 26. It achieves 95% or higher in efficiency over wide power range when input voltage equals to output voltage ($V_{\rm in} = 48$ V; $V_{\rm out} = 48$ V). The converter efficiency at voltage boost condition ($V_{\rm in} = 36$ V; $V_{\rm out} = 60$ V) is higher than that at voltage buck condition ($V_{\rm in} = 60$ V; $V_{\rm out} = 36$ V) over wide power level.

For the comparison, the operation is tested under three different controllers, including the standard NIBB controller, where φ is always equal to D_{BK} ($\varphi = D_{BK}$) [10]; robust selection of phase shift (φ_{mid}), operated in both ZVS and HS quadrangle mode, as described in Section II-A [30]; the proposed phase shift based MEPT in both ZVS and HS quadrangle mode (MEPT), as described in Section III. The efficiency comparison of conventional single buck–boost mode operation, $\varphi = D_{BK}$, is shown in Fig. 27. Conventional two-mode operations, buck or boost, cannot be well-regulated when the input voltage and output voltage are close to each other. The efficiency of the proposed MEPT controller is always higher than the robust selection (φ_{mid}) and standard NIBB controller ($\varphi = D_{BK}$) all over the wide power range. The corresponding phase shift in this operation condition is shown in Fig. 28. The phase shift of the standard NIBB controller is close to the upper boundary; the

TABLE II
COMPARISON OF STATE-OF-THE-ART ON HIGH EFFICIENCY NIBB

	Modes	HS / ZVS	Max Efficiency	MEPT	Frequency
[11]-[13]	Two modes	HS		N/A	Const.
[14]-[19]	Three modes	HS		N/A	Const.
[20]-[25]	Quadrangle	ZVS		LUT	Const.
[27]	CRM	ZVS	97.38%	LUT -Detection Based	50 kHz-113 kHz
[28]	Quadrangle/ CRM	ZVS	98.5% 48 V-48 V	LUT -Detection Based	700 kHz-800 kHz
[32]	Quadrangle	ZVS	>99%	LUT	0-150 kHz
[36]	Quadrangle	ZVS	90.9%	Online -Model Based	Const.
Proposed	**Quadrangle**	**Both**	**98.6%**	**Online -Detection Based**	**Const.**

LUT: Look Up Table; Const. : constant frequency operation.

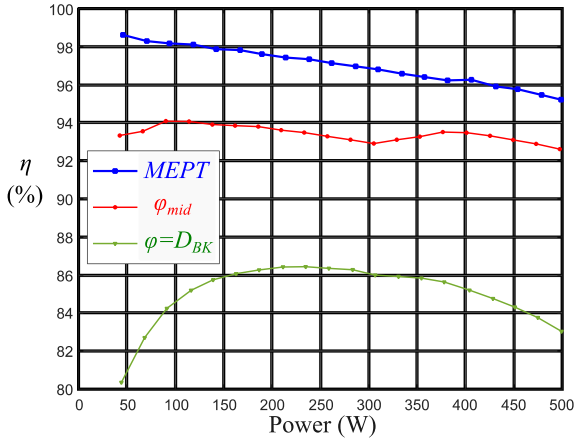

Fig. 27. Efficiency comparison in different controllers ($V_{\rm in} = 48$ V; $V_{\rm out} = 48$ V).

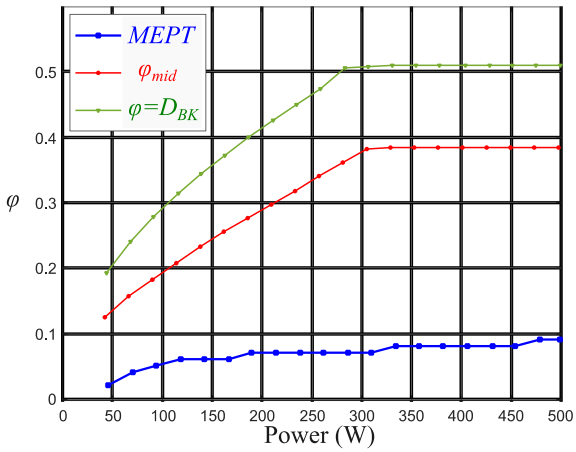

Fig. 28. Phase shift comparison in different controllers ($V_{\rm in} = 48$ V; $V_{\rm out} = 48$ V).

phase shift of the robust selection is at middle of ZVS operation region; the phase shift of MEPT controller is near the lower boundary of ZVS region.

As shown in Figs. 22 and 23, the corresponding current waveforms under different operating conditions mainly demonstrate the capability of bidirectional current drive. For accurate efficiency measurement, power meter-based results are presented in Figs. 24 and 25.

V. CONCLUSION

This article has addressed a maximum efficiency point tracking technique on noninverting buck boost converter. The proposed approach is based on perturbing gate driver signal phase shift and observing input and output power to track maximum efficiency point. The proposed approach applies a comparator and a digital to analog converter as the zero voltage switching detection circuits for selecting dead-time and be able to operate in both ZVS quadrangle mode and HS quadrangle mode. These techniques result in efficiency improvement over all power range without precise component parameters. Experimental results were shown for a 500 W digitally controlled noninverting buck boost converter.

A summarized comparison table between the proposed approach and the references is listed in Table II. The proposed approach can operate at a constant frequency in both HS/ZVS modes and is capable of running online MEPT without requiring an accurate model.

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