Letters

An Alternative-Fed Dual-Active-Bridge DC/DC Converter With Wide Voltage Gains and Low Current Ripples

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***Abstract*—Owing to their distinct principles, voltage-fed dual-active-bridge (DAB) and current-fed DAB converters each exhibit unique strengths and weaknesses, making them appropriate for varying applications. To increase the application flexibility, an alternative-fed dual-active-bridge (AF-DAB) dc/dc converter, with the merits of wide voltage gains and low current ripples, is proposed in this letter. Through the alternative-fed method, the AF-DAB converter can integrate both DABs' merits while eschewing unsuitable areas. Ultimately, the operation schemes and control structure are elaborated, and the experimental results are presented to verify the superior performance of the proposed topology.**

***Index Terms*—Current ripples, dual active bridge (DAB), dc/dc, voltage gains.**

I. Introduction

DUAL-ACTIVE-BRIDGE (DAB) converters were first proposed for high-power-density dc/dc power conversions [1]. Now, they are widely used as interface converters in renewable energy sources, benefitting from bidirectional, soft-switching, and isolation capabilities. Since renewable energy sources, such as fuel cells and photovoltaics, exhibit voltage fluctuation and sensitivity to current ripples, achieving wide voltage gains and low current ripples are of great practical concern for DAB converters [2].

Based on the source-fed types, DAB converters can be mainly classified into two types, voltage-fed (VF) and current-fed (CF) DAB converters, as shown in Fig. 1. Theoretically, the VF-DAB converter has high voltage-boosting capacity; however, the high step-up conversion will result in overlarge circulating current, and advanced modulations can only alleviate but not avoid this problem [3]. In contrast, the CF-DAB converter has an inherent boost characteristic. Its filter inductor not only facilitates high step-up conversion but also ensures low current ripples. Nevertheless, its buck conversion can only depend on the step-down transformers [4].

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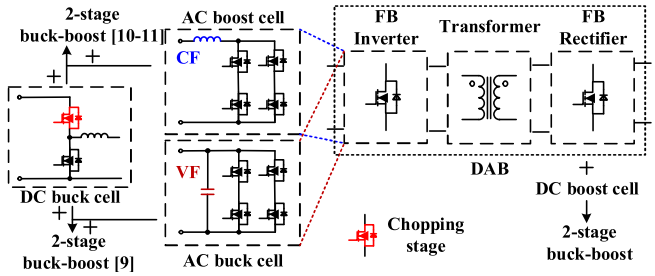

Fig. 1. Two source-fed types and different cascaded DAB structures.

To enhance the step-up conversion capacity, lots of voltage-boosting techniques are developed, including switched capacitor (charge pump), voltage multiplier, switched inductor, magnetic coupling of transformer/inductor, and multilevel technique [5], [6], [7], [8], [9]. The improvements of these voltage boost techniques are based on topological modifications of the basic VF-DAB or CF-DAB converters, with additional active or passive devices required to construct the auxiliary circuits.

Multistage conversion structures (cascaded/interleaved) are also practical solutions to widen the voltage gains of the DAB converters, such as buck-cascaded DAB converters and DAB cascaded boost converters, as shown in Fig. 1. A two-stage buck–boost cell can be formed by the dc buck cell cascading the full-bridge (FB) inverter or the FB rectifier cascading a dc boost cell. Through different combinations, a family of two-stage buck–boost DAB converters can be derived. By coordinating the fronted/cascaded buck/boost/buck–boost cells and DAB, the two-stage DAB structures can provide wider voltage gains [10], [11], [12]. However, such structures will inevitably increase the device number, cost, power losses, and complexity, producing additional barriers to practical implementation.

In [13], the CF-DAB and VF-DAB are systematically studied, and the CF mode is utilized as a fault tolerance solution for VF-DAB's capacitor failures, whose application scenario is a unidirectional and low-probability occurrence. Actually, the mode shifting method can be more fully utilized by bidirectional shifting. Aiming for voltage-fluctuating and current-ripple-sensitive applications, this letter proposes an alternative-fed DAB (AF-DAB) converter with the corresponding control strategy. By bidirectional shifting between VF and CF modes,

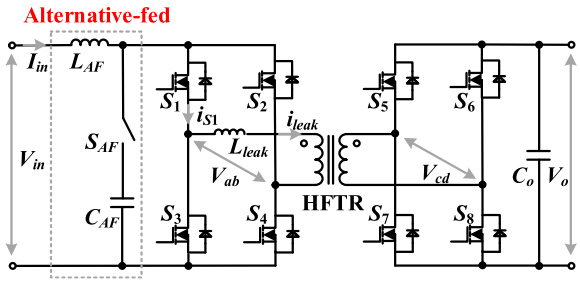

Fig. 2. Schematic of the proposed AF-DAB dc/dc converter.

the AF-DAB converter achieves wide voltage gains by a one-stage structure. Besides, as the fed inductor is directly connected to the source without a chopping stage of switches, low current ripples can always be ensured. In addition, if more extreme step-up conversion is demanded, the existing boost techniques [5], [6], [7], [8], [9] or multistage structures [10], [11], [12] can also be integrated into the proposed AF-DAB converter, further enhancing its application flexibility.

II. Configuration and Operation Scheme

A. Configuration

Fig. 2 shows the schematic of the proposed AF-DAB converter, consisting of fed inductor L_{AF}, fed capacitor C_{AF}, switch S_{AF}, output capacitor C_o, two full bridges (S_1–S_4, S_5–S_8), and a high-frequency transformer (HFTR). The L_{AF}, C_{AF}, and S_{AF} constitute an AF tank. And combining the tank with the full bridge (S_1–S_4), a one-stage buck–boost structure is obtained on the primary side. Moreover, the HFTR is with a turns ratio of n and leakage inductor L_{leak}. V_{ab} and V_{cd} are the voltages across both sides of the HFTR; V_{in} and V_o are the input voltage and the output voltage; and I_{in}, i_{S1}, and i_{leak} are the currents passing through the L_{AF}, S_1, and L_{leak}, respectively. Lastly, the switching frequency and power are defined as f_s and P. ϕ is defined as the normalized phase-shift angle between two full bridges, and α is defined as the normalized inner phase-shift angle on the high-voltage side.

B. Operation Schemes

Fig. 3 shows the theoretical waveforms of VF mode in one cycle and CF mode in half cycle, each including eight states (t_0–t_8). The VF mode works for step-down, voltage following, and low step-up conversions with the extended phase-shift (EPS) control. S_{AF} keeps ON-state. The duty ratios of S_1–S_8 are all fixed at 0.5, and S_2 and S_3 are phase-shifted by half cycle versus S_1 and S_4. ϕ is used to control the output voltage. α is on the primary side for step-down and secondary side for step-up [3].

The CF mode works for high step-up conversions with the pulsewidth-modulation plus dual phase-shifted (PDPS) control. S_{AF} keeps OFF-state. The duty ratios of S_1–S_4 are defined as d_{pri}, and the duty ratios of S_5–S_8 are fixed at 0.5. S_2 and S_3 are phase-shifted by half cycle versus S_1 and S_4. d_{pri} is above 0.5 and used to control the output voltage. ϕ is decided by d_{pri} to realize the synchronous turn-OFF actions of S_5 versus $S_{1\&4}$ and S_7 versus $S_{2\&3}$ [4].

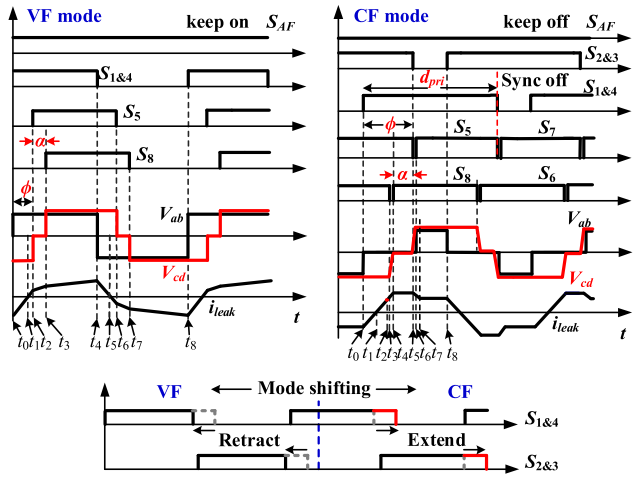

Fig. 3. Theoretical waveforms.

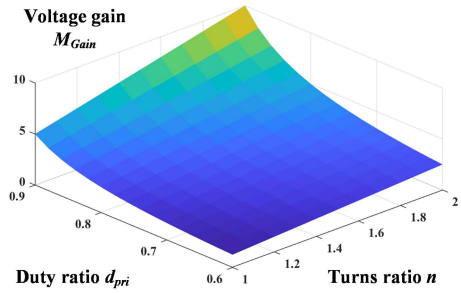

Fig. 4. Voltage gain M_{Gain} variation versus turns ratio n and duty ratio d_{pri}.

III. Mode Analysis

A. AF Mode Analysis

In the CF mode, the voltage gain M_{Gain} can be derived as follows according to the volt–second balance of the inductor L_{AF}:

$$\begin{cases} L_{\mathrm{AF}} \cdot \frac{dI_{\mathrm{in}}}{dt} = V_{\mathrm{in}} & 0 \le t \le d_{\mathrm{pri}} \cdot \frac{1}{f_s} \\ L_{\mathrm{AF}} \cdot \frac{dI_{\mathrm{in}}}{dt} = \frac{V_o}{n} - V_{\mathrm{in}} & d_{\mathrm{pri}} \cdot \frac{1}{f_s} \le t \le \frac{1}{2 \cdot f_s} \end{cases} \quad M_{\mathrm{Gain}} = \frac{n}{2 \cdot (1 - d_{\mathrm{pri}})} \tag{1}$$

$$\phi = d_{\mathrm{pri}} - 0.5. \tag{2}$$

In the VF mode, the relationship between the output voltage and power can be expressed as follows according to the volt-second balance of the leakage inductor:

$$\begin{aligned} P &= f_s \cdot \int_0^{\frac{1}{2 \cdot f_s}} V_{ab}(t) \cdot i_{\mathrm{leak}}(t) \cdot dt \\ &= \frac{n \cdot V_{\mathrm{in}} \cdot V_o}{2 \cdot L_{\mathrm{leak}} \cdot f_s} \cdot \left((1 - \phi) \cdot \phi + \frac{\alpha}{2} \cdot \left(1 - \frac{2 \cdot \phi + \alpha}{\pi} \right) \right) \quad 0 < \phi < 1. \end{aligned} \tag{3}$$

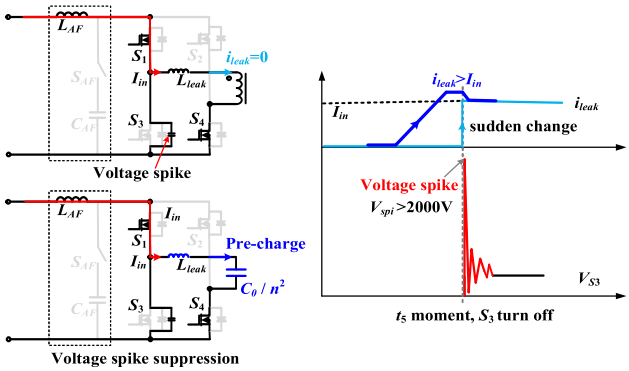

Fig. 5. Principle of voltage spike suppression.

Fig. 4 presents the high step-up voltage gain M_{Gain} of the proposed AF-DAB converter in the CF mode. To ensure enough time for the leakage-inductor current to change direction, the duty ratio d_{pri} should be above 0.6 but not exceeding 0.9 to prevent the saturation of the fed inductor. Hence, the 1:1.25 step-up point is set as the AF critical point between the two modes.

Meanwhile, the voltage stresses across switches S_1–S_4 and S_5–S_8 are expressed as follows:

$$\begin{cases} V_{S1-S4} = V_{\mathrm{in}} & V_{S5-S8} = V_o \quad \mathrm{VF}\cdot\mathrm{Mode} \\ V_{S1-S4} = \frac{V_o}{n} & V_{S5-S8} = V_o \quad \mathrm{CF}\cdot\mathrm{Mode}. \end{cases} \tag{4}$$

In the VF mode, the constraint of zero-voltage switching (ZVS) is that the minimum absolute value of leakage-inductor current should be high enough to charge the parasitic capacitors C_{oss}, expressed as (5). Similarly, in the CF mode, the constraint of soft switching is given as (6). The zero-current-switching (ZCS) OFF action of S_1–S_4 requires that the leakage-inductor current $i_{\mathrm{leak}}(t_5)$ is higher than the input current $I_{\mathrm{in}}(t_5)$ to enable body–diode reverse flow at the off moment t_5. Besides, the ZVS constraint of S_5–S_8 can be obtained by the energy-based method [3].

$$\begin{cases} |i_{\mathrm{leak}}(t_0)| > 2\cdot\sqrt{\frac{C_{\mathrm{oss}}\cdot V_{\mathrm{in}}\cdot V_o}{L_{\mathrm{leak}}}} & S_1 - S_4 \\ |i_{\mathrm{leak}}(t_2)| > 2\cdot\sqrt{\frac{n\cdot C_{\mathrm{oss}}\cdot V_{\mathrm{in}}\cdot V_o}{L_{\mathrm{leak}}}} & S_5 - S_8 \end{cases} \tag{5}$$

$$\begin{cases} i_{\mathrm{leak}}(t_5) > I_{\mathrm{in}}(t_5) & S_1 - S_4 \\ \frac{1}{2}\cdot L_{\mathrm{leak}}\cdot {i_{\mathrm{leak}}}^2 > 2\cdot(\frac{1}{2}\cdot C_{\mathrm{oss}}\cdot {V_o}^2) & S_5 - S_8. \end{cases} \tag{6}$$

B. Voltage Spike Suppression

In VF mode, the fed capacitor C_{AF} plays the role of a snubber between inductors L_{leak} and L_{AF}. By contrast, the latter two devices will be hard connected in CF mode. Then, high voltage spike V_{spi} will occur on switches S_1–S_4 at the turn-OFF moment, as shown in Fig. 5. The amplitude of voltage spikes is expressed as (7), related to the values of parasitic capacitors C_{oss}, inductors L_{leak} and L_{AF}, initial currents ($I_{\mathrm{in}}(t_5)$ and $i_{\mathrm{leak}}(t_5)$), and time constant ω. The instantaneous amplitude of voltage spikes can reach thousands of volts. Thus, a voltage spike suppression approach is integrated into the PDPS control. The principle of the approach is to reduce the mismatching between the input current $I_{\mathrm{in}}(t_5)$ and the leakage-inductor current $i_{\mathrm{leak}}(t_5)$ before the turn-OFF moment t_5, as (6) and Fig. 5 present. The output capacitor is reflected on the primary side (blue part) and used to precharge the leakage inductor [8].

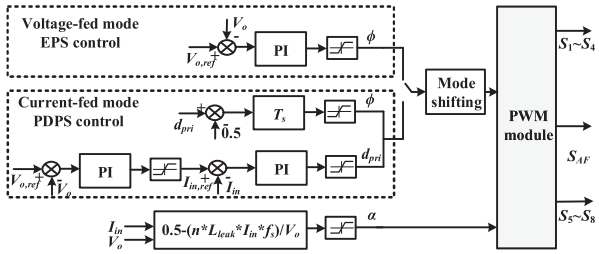

Fig. 6. Control structure.

$$V_{\mathrm{spi}}\big|_{i_{\mathrm{leak}}(t_5)>0}^{I_{\mathrm{in}}(t_5)>0} = (I_{\mathrm{in}}(t_5) - i_{\mathrm{leak}}(t_5))\cdot\frac{\frac{\sqrt{{L_{\mathrm{leak}}}^3\cdot L_{\mathrm{AF}}}+\sqrt{L_{\mathrm{leak}}\cdot {L_{\mathrm{AF}}}^3}}{\sqrt{2\cdot C_{\mathrm{oss}}\cdot(L_{\mathrm{leak}}+L_{\mathrm{AF}})}}}{L_{\mathrm{leak}}+L_{\mathrm{AF}}}\cdot\sin(\omega\cdot t). \tag{7}$$

C. Control Structure

The control structure is illustrated in Fig. 6. The signal of S_{AF} keeps ON state for VF mode and OFF state for CF mode. The inner phase-shift angle α is calculated according to the converter parameters to reduce circulating current, which is the same in both modes. The upper box presents the EPS control of VF mode. The voltage control loop tracks the reference value $V_{o,\mathrm{ref}}$ by ϕ. In contrast, the bottom box explains the PDPS control of CF mode. A dual-loop control is utilized to regulate the output voltage. The outer loop provides the input current reference $I_{\mathrm{in,ref}}$, and the inner loop tracks the reference $I_{\mathrm{in,ref}}$ by d_{pri}. ϕ is calculated according to d_{pri} to realize the synchronous turn-OFF actions of corresponding switches. The controller coordinates the synchronization between mode shifting and updating gate signals. The mode shifting should be away from the moment ($d_{\mathrm{pri}} = 0.5$) to prevent the open circuit of the fed inductor L_{AF}. It is worth mentioning that EPS and PDPS control schemes are used as examples in this letter, and other modulation schemes are also applicable.

IV. Experimental Verification

A scaled-down laboratory prototype is built, as shown in Fig. 7. The switching frequency f_s and power P are 50 kHz and 500 W. All switches are CREE C3M0045065K, driven by CGD15SG00D2. The digital controller is dSPACE DS1202, the voltage/current sensors are LEM LV25/LA25, and the HFTR is an EE55 ferrite core with a turn's ratio n 1:1. The input voltage V_{in} is 80 V, and the output voltage V_o varies from 40 to 320 V (from 2:1 step-down to 1:4 step-up). The leakage inductor L_{leak} and capacitor C_o are 20 and 200 μF. The fed inductor L_{AF} and fed capacitor C_{AF} are 100 and 200 μF.

Fig. 8 presents the wide voltage gains with soft switching, including 2:1 step-down, 1:1 voltage following, 1:2 step-up, and

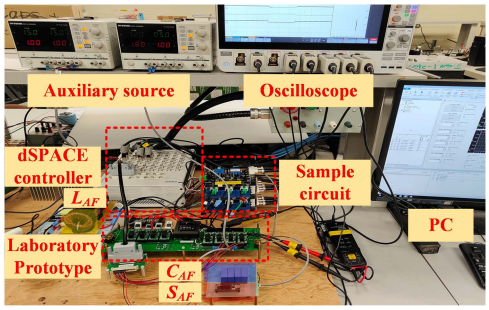

Fig. 7. Laboratory prototype.

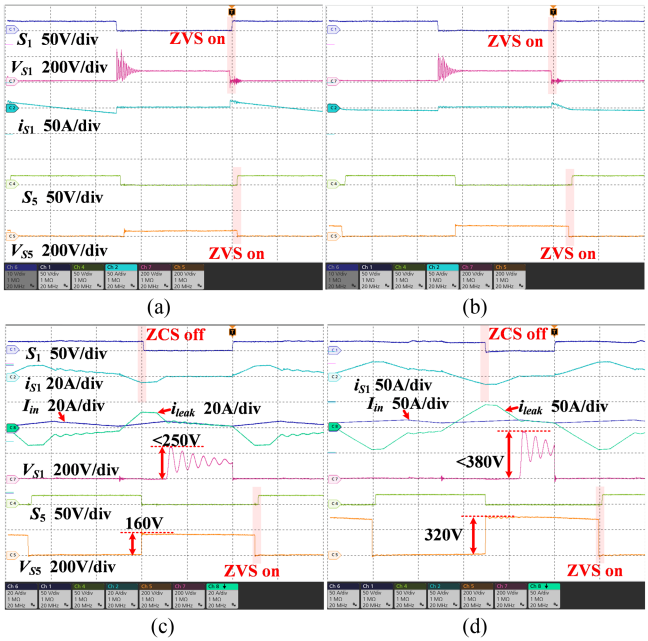

Fig. 8. Experimental waveforms of wide voltage gains with soft switching in full load (4 μs/div): (a) 2:1 step-down, VF mode ($V_{\text{in}} = 80$ V, $V_o = 40$ V); (b) voltage following, VF mode ($V_{\text{in}} = 80$ V, $V_o = 80$ V); (c) 1:2 step-up, CF mode ($V_{\text{in}} = 80$ V, $V_o = 160$ V); (d) 1:4 step-up, CF mode ($V_{\text{in}} = 80$ V, $V_o = 320$ V).

1:4 step-up modes. The soft-switching operations are in the red-shaded area. The voltages upon the switches drop to zero in advance before the rising edge, which introduces ZVS on. In CF mode, the current i_{S1} through the switch S_1 keeps negative at the falling edge of S_1, which introduces ZCS OFF. Moreover, with the voltage spike suppression method, when the output voltage reaches 320 V, the spike voltage is suppressed from thousands of volts to 380 V. Fig. 9 presents the step-up/step-down performance of reverse power flow.

Fig. 10 shows the experimental waveforms of mode shifting between VF mode and CF mode under 1:1.25 step-up point. It can be observed that the AF-DAB converter successfully shifts between the two modes, and the output voltage V_o maintains at the reference value steadily without oscillation.

Fig. 11 verifies the dynamic performance. When the input voltage or load suddenly changes, the output voltage keeps steady. Besides, the output voltage can adjust rapidly when the

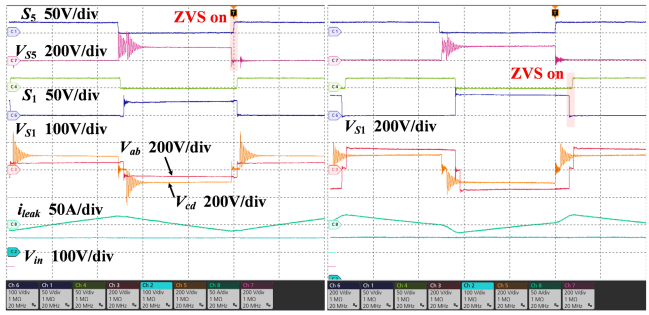

Fig. 9. Experimental waveforms of reverse flow in full load (4 μs/div): (a) 2:1 step-down ($V_{\text{in}} = 100$ V, $V_o = 50$ V); (b) 1:1.5 step-up ($V_{\text{in}} = 100$ V, $V_o = 150$ V).

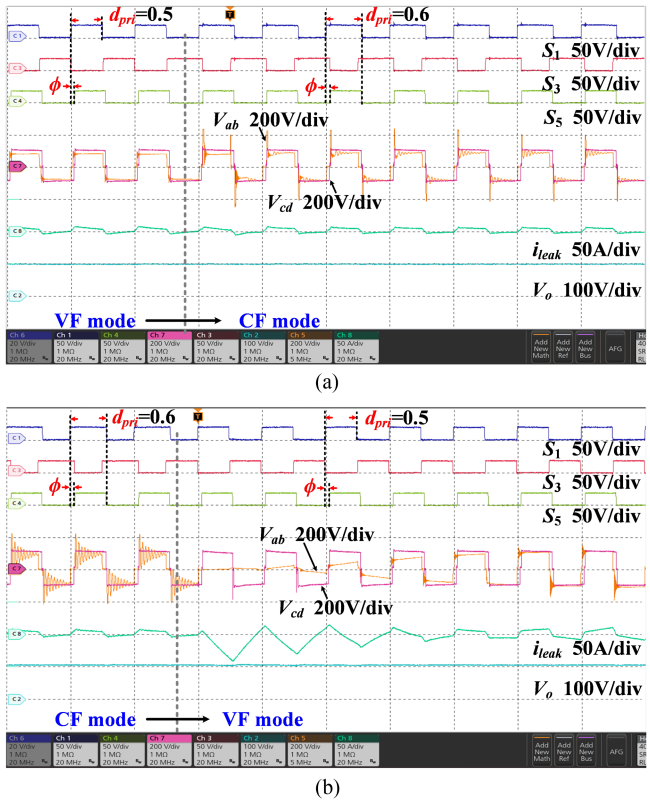

Fig. 10. Experimental waveforms of mode shifting under 1:1.25 step-up point ($V_{\text{in}} = 80$ V, $V_o = 100$ V) in full load (20 μs/div): (a) from VF to CF mode; (b) from CF to VF mode.

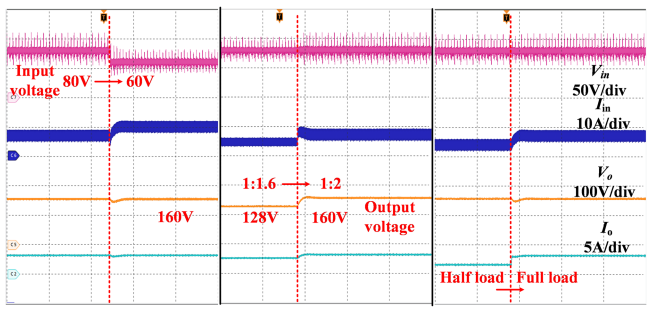

Fig. 11. Experimental waveforms of dynamic performance (200 ms/div).

TABLE I
COMPARISON OF EXISTING ONE-STAGE DABS

Items	VF-DAB	CF-DAB	AF-DAB
Suitable gain range	Narrow	Step-up	Wide
Low current ripples	Need filter	Yes	Yes

TABLE II
EFFICIENCY COMPARISON

Voltage Gains	2:1	1:1	1:1.25	1:2	1:4
VF-DAB with EPS	90.3%	94.8%	92.9%	90.1%	85.2%
CF-DAB with PDPS	N/A	N/A	94.5%	93.6%	90.3%
AF-DAB	90.1%	94.6%	94.5%	93.4%	90.2%

reference changes. Moreover, benefiting from the direct connection between the fed inductor and the source without a chopping stage, the input current I_{in} will not be interrupted. Table I tabulates a brief comparison of the existing one-stage DABs, and the efficiency is equivalent to the combination of VF-DAB and CF-DAB under each suitable area. Table II presents the efficiency comparison at the rated power level.

V. CONCLUSION

In this letter, an AF-DAB dc/dc converter is proposed. The detailed operating principle and experimental results are provided, demonstrating its superior performance. The proposed AF-DAB converter obtains wide voltage gains and low current ripples simultaneously by a one-stage structure, providing a meaningful supplement to the existing DAB family.

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