Active Gate Driver IC Integrating Gate Voltage Sensing Technique for SiC MOSFETs

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***Abstract*—The silicon carbide (SiC) MOSFETs provide superior properties over conventional silicon power devices with a higher switching speed and lower conduction losses. However, high-frequency switching can cause overshoots, oscillations, and electromagnetic interference (EMI) issues. Because of a fixed gate driving strength, the traditional gate driver struggles with the tradeoff between overshoot and switching loss (switching speed). To improve the switching performance of the SiC power devices, an active gate driver (AGD) integrated circuit is proposed using a 0.18-μm CMOS HV BCD process is proposed in this article. Instead of requiring a separate programmable logic board, the controller circuits and driving stage are integrated on a chip. The proposed gate voltage sensing technique detects the slope difference of the gate voltage and generates the appropriate gate driving signals without detecting the SiC MOSFET I_D and V_{DS} information. The area and cost are reduced by removing the high-voltage sensing circuit for I_D and V_{DS} detection. The proposed AGD can also attenuate the oscillations of I_D and V_{DS}, further reduce the EMI noise induced by high switching speed. In addition, the experimental results show that the proposed AGD can be applied to different SiC power MOSFETs.**

***Index Terms*—Gate driver, gate voltage feedback, silicon carbide (SiC) MOSFET.**

I. Introduction

WIDE bandgap power devices, such as silicon carbide (SiC) and gallium nitride (GaN) bring a new milestone to the power industry. These devices outperform silicon MOSFETs and insulated gate bipolar transistors (IGBTs) in terms of physical properties, such as lower intrinsic parasitic, higher thermal conductivity, higher breakdown voltage, and higher operating temperature [1], [2], [3], [4]. By employing wide bandgap power devices, the power conversion systems can achieve higher conversion efficiency and superior performance in areas such as power density, operating voltage, operating temperature, and switching frequency. Compared with the GaN devices, the SiC devices are more suitable for high-voltage applications due to their high current-carrying capabilities. As a result, SiC devices have recently been used in automotive [5], [6], power traction inverters [7], and high power converters.

However, some destructive effects come with increasing the operating frequency due to parasitic elements of device packaging. A large dI/dt interacts with stray inductance and parasitic capacitance of the commutation loop, which results in oscillation and overshoot on the gate of SiC device and leads to a coupling effect and false turn-ON [8], [9], [10]. The large dV/dt causes some noise [11] or leads to voltage overshoot, which may cause the power device to fail. To address these effects, several common approaches have been reported.

1) *RC snubber circuit:* The switching stress and oscillation phenomenon are suppressed by adding an RC snubber circuit. However, the addition of additional components such as inductors and capacitors increases energy loss and reduces efficiency [12], [13], [14].
2) *Driver with gate resistance:* A conventional gate driver (CGD) uses a fixed gate resistance to control the gate driving strength. A high gate resistance effectively reduces the overshoots and suppresses the electromagnetic interference (EMI). However, the switching time and energy loss are increased, which limits the switching frequency [15].
3) *Active gate driver (AGD):* Dynamically controlling the slew rate during switching transient alleviates the tradeoff between the overshoot and the switching speed of CGD. As a result, AGD has emerged as a trend in recent research [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], which can be divided into open-loop and closed-loop types as follows.

Open-loop techniques use predetermined gate currents or voltages to optimize the switching performance of power devices [16], [17], [18], [19]. Open-loop AGDs are simple with no feedbacks, but lack of flexibility to operating condition variations including load current and temperature.

Closed-loop methods identify the switching stages of the power devices and independently control the transient stages by applying different driving currents or voltages in certain stages [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30]. Specific switching characteristics can be optimized with the individual control of power devices dI/dt and dV/dt. In [20], an adaptive multilevel AGD for SiC devices turn-OFF is proposed. Field

Manuscript received 20 November 2023; revised 7 February 2024; accepted 16 March 2024. Date of publication 1 April 2024; date of current version 16 May 2024. This work was supported in part by the National Science and Technology Council (NSTC), Taiwan, under Grant 112-2636-E-A49-006, Grant 112-2221-E-A49-146-MY3 and Grant 112-2218-E-A49-017 and in part by the Higher Education Sprout Project of the National Yang Ming Chiao Tung University and Ministry of Education (MOE), Taiwan. Recommended for publication by Associate Editor B. Shao. *(Corresponding author: Po-Hung Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3383666.

Digital Object Identifier 10.1109/TPEL.2024.3383666

programmable gate array (FPGA) is used to calculate the optimal V_{INT} by sensing V_{BUS} and I_{LOAD} information and inputting SiC datasheet parameters. The topology has the advantages of ease-of-implementation and computational efficiency. However, an FPGA is required for the controller, and datasheet parameters are needed for calculation. Yang et al. [21] introduce a multilevel AGD for SiC MOSFETs which features simple circuit implementation with no negative gate drive voltage. Although the proposed method is simple, a complex programmable logic device (CPLD) for controller and additional detection circuits for I_D and V_{DS} are required. The detection thresholds and optimal delay time of the AGD need to be set when the SiC module and the operating condition are determined. A self-regulating voltage source gate driver for IGBTs is described in [22]. The AGD adopts cycle-by-cycle adjustment to achieve accurate switching characteristics control. Nonetheless, it requires FPGA to receive target values and control objects and produce drive levels for the next switching cycle. Off-chip components are required for V_{CE} and I_C sensing circuits. AGDs in [23], [24], [25], and [26] also use FPGA/CPLD for controller and additional I_D (I_C) and V_{DS} (V_{CE}) sensing circuits. The existing AGD works mentioned earlier are realized on the PCB, which occupy a large area. To achieve miniaturization, an integrated adaptive multilevel gate driver for SiC MOSFET is proposed in [27]. The AGD detects the dV/dt and di/dt noise and adaptively adjusts the driving current in time. However, the ratio of the off-chip capacitive voltage divider needs to be adjusted for different power supply voltage. The values of the capacitive voltage divider should also be selected carefully to prevent them from influencing parasitic drain capacitance of SiC MOSFET. In addition, the proposed di/dt noise detection circuit is available for only four-pin package SiC MOSFETs.

Fig. 1 illustrates the prior arts and proposed approaches for AGD. As the controller, most of the previous works use programmable logic boards such as FPGA or CPLD. I_D and V_{DS} of SiC device must be sensed and fed back to the controller, which necessitates the addition of current and voltage sensing circuits. The sensing circuit and driving stage are made up of commercial discrete components, which expand the area.

In this article, a high integration AGD IC for SiC power MOSFETs with gate voltage sensing technique is proposed. The proposed AGD strategy is to reduce the gate driving voltage during the dI_D/dt and dV_{DS}/dt stages. The proposed AGD can resolve the tradeoff between I_D (V_{DS}) overshoot and energy loss (switching speed). Moreover, the proposed AGD introduces a novel method to detect the change of I_D with a non-Kelvin connection device. The proposed gate voltage sensing technique only senses the V_{GS} of the SiC MOSFET to generate the control signals for AGD. As a result, sensing circuits for I_D and V_{DS} detection are unnecessary in this work. Unlike previous works on SiC MOSFET AGDs that used programmable logic boards to generate control signals; this work integrates the sensing circuit, controller, and driving stage on a single chip.

The rest of this article are organized as follows. In Section II, the proposed AGD and the gate voltage sensing technique are introduced. Section III describes the operation and implementation of the proposed gate driver. In Section IV, the measurement results are shown. Finally, Section V concludes this article.

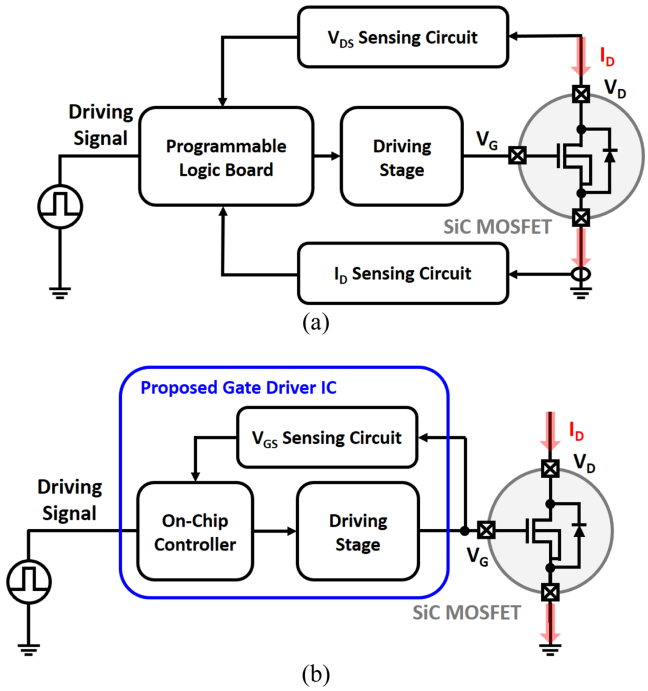


Fig. 1. (a) Previous method. (b) Proposed method.

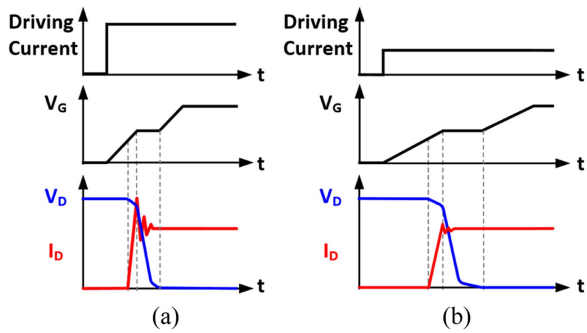


Fig. 2. Turn-ON switching waveform of conventional gate driver with (a) stronger and (b) weaker driving strength.

II. Operating Principle of Proposed Gate Driver

In this section, the operation of the proposed AGD is introduced. The effect of the parasitic inductance in a SiC MOSFET package is concerned. The gate voltage sensing technique is proposed, which makes use of the parasitic inductance effect.

A. Proposed AGD

Fig. 2 shows the turn-ON transient of a SiC power MOSFET with the CGD. A larger gate resistance gives a smaller gate driving current which also means a weaker driving strength, and vice versa. As shown in Fig. 2(a), a stronger driving strength results in a shorter switching transient but a larger overshoot. On the contrary, as shown in Fig. 2(b), a weaker driving strength can reduce overshoot while increasing switching loss. In summary,

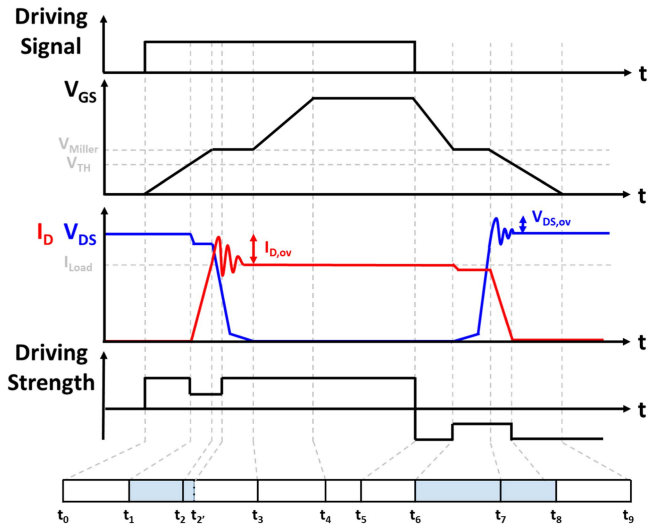


Fig. 3. Switching transient waveform of proposed AGD.

with a fixed gate driving strength, the I_D (V_{DS}) overshoot and the switching loss (switching speed) during switching transient are tradeoffs. The AGD on the other hand dynamically adjusts driving strength during a switching transient to improve overall switching performances.

The switching transient with the proposed AGD is illustrated in Fig. 3. In the turn-ON delay stage (t_0–t_1), the larger PMOS is turned ON to charge the gate capacitance in a short time. After the gate voltage reaches V_{TH}, the SiC turns ON and the drain current I_D starts to rise. During the current rising stage (t_1–t_2), the PMOS is switched to a smaller size to lower the dI_D/dt of the SiC MOSFET (t_1-$t_{2'}$). When the current rising is finished, V_D starts to fall. In the voltage falling stage (t_2–t_3), the larger PMOS is turned ON to achieve fast switching speed, further reduce the switching loss. In the channel enhancement stage (t_3–t_4), the larger PMOS is maintained on to fully turn ON the SiC MOSFET. As a result, the I_D overshoot is suppressed while the switching loss and the rise time are not significantly increased.

In the turn-OFF delay stage (t_5–t_6), the gate capacitance is discharged by a larger NMOS. When the gate voltage is discharged to the Miller plateau region, V_D starts to rise. In the voltage rising stage (t_6–t_7) and current falling stage (t_7–t_8), the smaller NMOS is turned ON to lower the dV_{DS}/dt and the dI_D/dt of the SiC MOSFET. After V_G drops to V_{TH}, the SiC MOSFET enters tail current stage (t_8–t_9). In this stage, the larger NMOS is turned ON until turn-OFF transition is completed.

To achieve the above-mentioned active gate driving strategy, several timings (t_1, $t_{2'}$, t_6, t_8) are required for driving strength adjustment. Details of timing capture will be described in Section II-C.

B. *Effect of Parasitic Source Inductance*

The internal parasitic inductances of a SiC MOSFET package are shown in Fig. 4(a). The L_D, L_G, and L_S are the equivalent

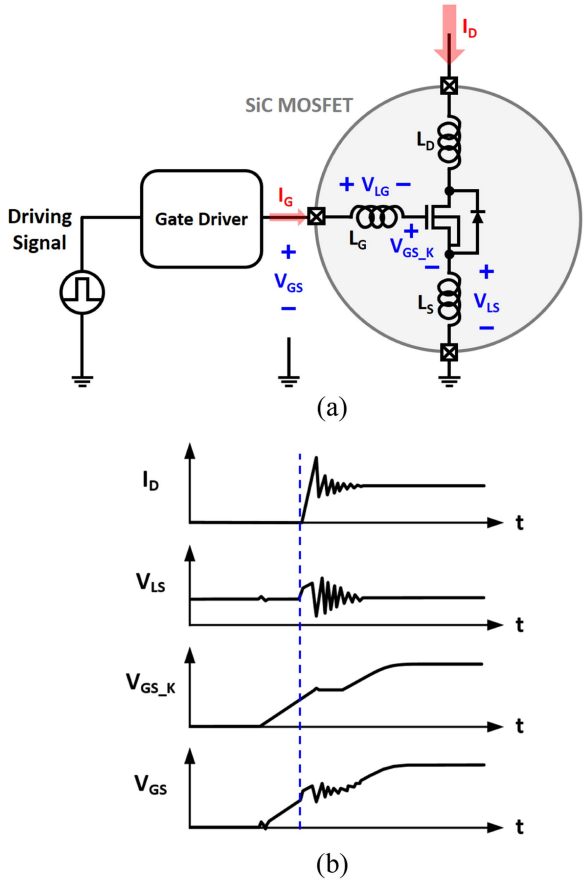


Fig. 4. Parasitic inductance effect of SiC power MOSFET package. (a) Schematic. (b) Waveforms.

parasitic inductances on the drain, gate, and source side, respectively. The values of the L_D, L_G, and L_S are around 6, 15, and 9 nH, introduced in [31]. The external gate-source voltage V_{GS} can be expressed as the sum of the voltage across L_G, the internal gate-source voltage, and the voltage across L_S

$$V_{GS} = V_{LG} + V_{GS\_K} + V_{LS} \tag{1}$$

where the internal gate-source voltage V_{GS_K} is not affected by any parasitic inductance.

The voltage across L_G, V_{LG}, can be expressed as follows:

$$V_{LG} = L_G \cdot \frac{dI_G}{dt}. \tag{2}$$

When the SiC MOSFET starts to conduct, the drain current I_D flows through the parasitic source inductance L_s. The voltage across L_S, V_{LS}, is generated according to the following equation:

$$V_{LS} = L_S \cdot \frac{dI_D}{dt}. \tag{3}$$

Since I_G is small compared to I_D in MOSFETs, the effect of V_{LG} on the V_{GS} is negligible. According to (1)–(3), the effect of the parasitic inductances on the external V_{GS} is illustrated, as shown in Fig. 4(b). The voltage across L_S, V_{LS}, is added to the internal gate-source voltage V_{GS_K}, and further affects the external gate-source voltage V_{GS}.

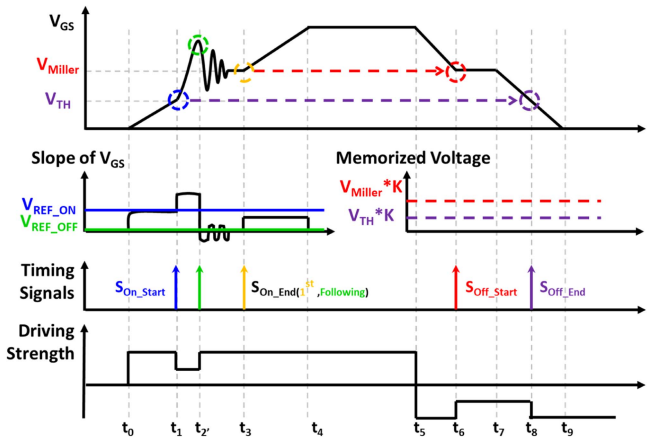


Fig. 5. Proposed gate voltage sensing technique.

C. Gate Voltage Sensing Technique

As mentioned in the previous section, the proposed AGD requires t_1, $t_{2'}$, t_6, and t_8 for driving strength adjustment. In this section, the proposed gate voltage sensing technique for AGD timing is introduced, depicted in Fig. 5. The proposed gate voltage sensing technique makes use of the effect of the parasitic source inductance. During turn-ON transient, when V_{GS} reaches V_{TH} and I_D starts to rise (t_1), a slope difference created by the nonzero V_{LS} occurs on the external gate-source voltage V_{GS}. The AGD timing, denoted as t_1, is determined by detecting the slope difference of V_{GS}. This detection is accomplished by comparing the slope of V_{GS} with the reference voltage V_{REF_ON}, and concurrently, the V_{TH} is recorded. At t_1, the driving strength is adjusted accordingly, reducing it. Throughout the initial switching cycle, the weaker driving strength is maintained until V_{GS} exits the Miller plateau (t_3). Simultaneously, the slope of V_{GS} becomes larger than V_{REF_OFF}, and the value of V_{Miller} is recorded. Subsequently, in the following cycles, the weaker driving strength persists until the occurrence of I_D overshoot ($t_{2'}$). When the I_D overshoot happens, the slope of VGS becomes 0, enabling the determination of $t_{2'}$ by comparing it with the slope of V_{GS} and a 0 V reference, V_{REF_OFF}.

During turn-OFF transient, t_6 and t_8 are found by comparing V_{GS} with memorized voltage V_{Miller} and V_{TH}. As a result, AGD timing can be found by sensing only the SiC MOSFET's gate voltage. The proposed AGD adopts real-time control mechanism, which means that the gate driving strength is adjusted immediately once the timing is detected. Additional sensing circuits and costs are both reduced when sensing I_D and V_{DS} are not used.

III. Circuit Implementation

The block diagram of the proposed integrated gate driver for SiC MOSFET with the gate voltage sensing technique is shown in Fig. 6. It is mainly made up of adaptive slope reference generator, sensing block, controlling block, and driving stage, with an LDO serving as an auxiliary circuit. The driving stage can deliver a maximum driving voltage of 20 V. The propagation delay of the gate driver is approximately 43 ns.

The weak driving signal S_{Weak_ON} (S_{Weak_OFF}) is generated by the weak-ON (OFF) logic using the timing signals S_{ON_Start} (S_{OFF_Start}) and S_{ON_End} (S_{OFF_End}) provided by voltage slope detection circuit. The high-voltage buffer is controlled by the driving pattern generator's control logic and level shifters, and the driving strength is adjusted during the switching transient to improve the switching performance of SiC MOSFET. Hence, the delay from detecting the V_{GS} slope difference to adjusting the driving strength is inevitable.

A. Voltage Slope Detection

The schematic of the voltage slope detection circuit is shown in Fig. 7(a). The voltage slope detection block consists of an RC differentiator, a comparator, a filter, and logic circuit. The comparator consists of transistors M_{P1} to M_{P5} and M_{N1} to M_{N6}. M_{P1} and M_{P2} form the input pair of the comparator, while M_{P3} serves as the current source. M_{N1} to M_{N4} create a positive gain stage, and M_{N5}, M_{P4}, M_{P5}, and M_{N6} contribute to level shifting the output of the gain stage. The hysteresis window is adjustable by the width ratio of M_{N1} to M_{N3} and M_{N2} to M_{N4}. When the input voltage at M_{P1} exceeds that at M_{P2}, the current of M_{P1} is smaller than that of M_{P2}. The current of M_{P1} is then mirrored to M_{P5} through M_{N1}, M_{N5}, and M_{P4}, while the current of M_{P2} is mirrored to M_{N6} through M_{N2}. As the current of M_{P1} is smaller than that of M_{P2}, V_3 is pulled low, causing the output of the inverter to go high.

The operation waveforms are shown in Fig. 7(b). The feedback gate-source voltage V_{GS_FB} of the SiC MOSFET is differentiated by the RC differentiator. The differentiated V_{GS_FB}, $V_{GS\_Diff.}$, can be expressed as follows:

$$V_{GS\_Diff.} = R \cdot C \cdot \frac{dV_{GS\_FB}}{dt}. \tag{4}$$

The relationship between the gate driving current (I_{dr}) and the V_{GS} between t_0 and t_1 in Fig. 7(b) can be written as follows:

$$\Delta V_{GS\_FB} = \frac{I_{dr}}{C_{iss}} \cdot \Delta t. \tag{5}$$

When the drain current (I_D) begins to conduct, the V_{DS} remains significantly greater than V_{GS} - V_{TH}, the I_D can be expressed in (6), where β represents the transconductance coefficient of the SiC MOSFET.

$$\begin{aligned} I_D\left(t = t_1 + \Delta t\right) &= \beta \cdot \left[V_{GS}\left(t = t_1 + \Delta t\right) - V_{TH}\right]^2 \\ &= \beta \cdot \left[V_{GS}\left(t = t_1\right) + V_{GS}\left(t = \Delta t\right) - V_{TH}\right]^2. \end{aligned} \tag{6}$$

As illustrated in Fig. 7(b), the V_{GS} is equal to V_{TH} at t_1.

Therefore, the V_{TH} term is eliminated and (6) can be written as follows:

$$I_D\left(t = t_1 + \Delta t\right) = \beta \cdot \left[V_{GS}\left(t = \Delta t\right)\right]^2. \tag{7}$$

Combine (3), (4), and (7), the change in differentiated V_{GS}, denoted as $\Delta V_{LS\_Diff.}$, can be derived as follows:

$$\Delta V_{LS\_Diff.} = R \cdot C \cdot L_s \frac{d^2\left[\left(\beta \cdot \frac{I_{dr}}{C_{iss}} \cdot \Delta t\right)^2\right]}{dt^2}. \tag{8}$$

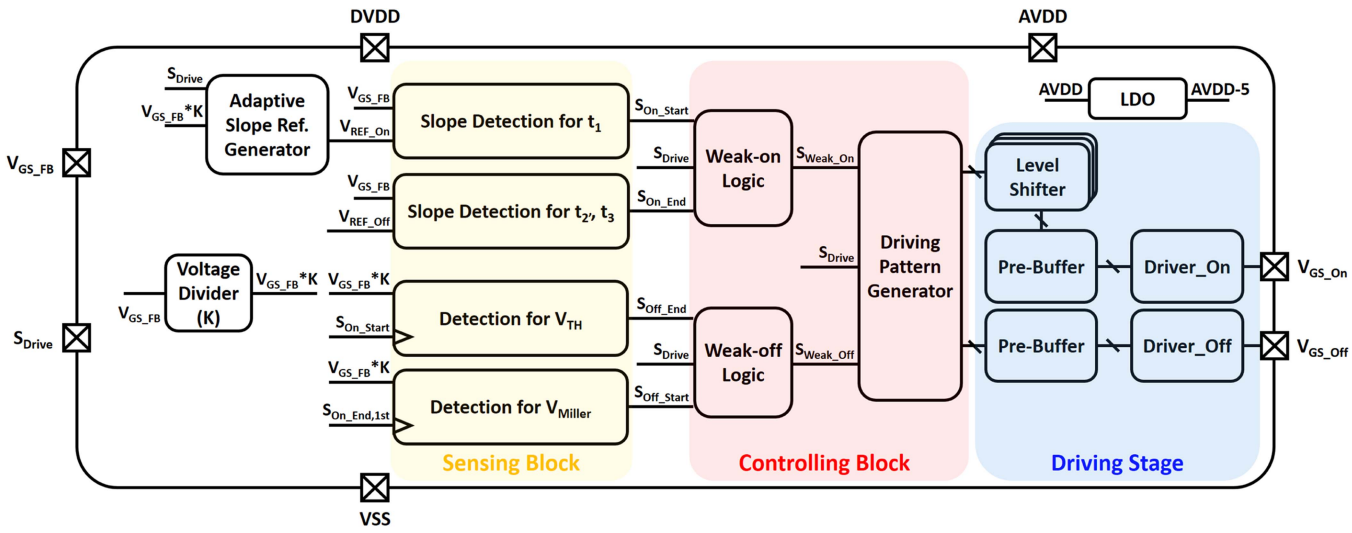


Fig. 6. System architecture.

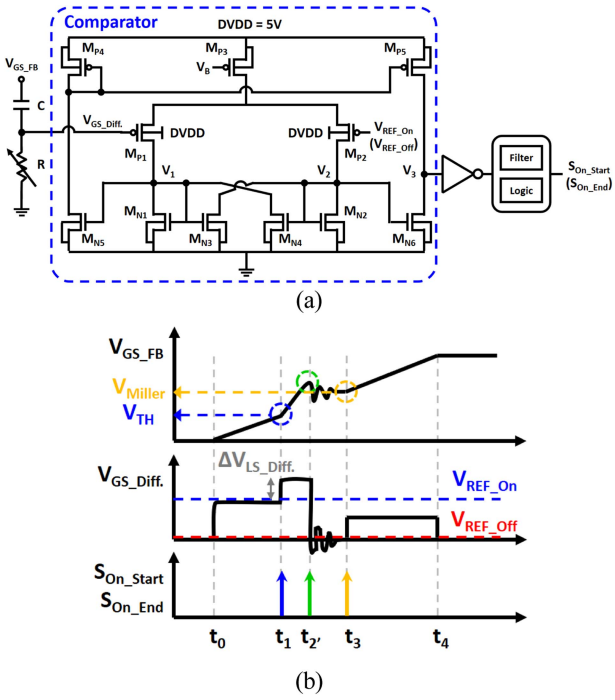


Fig. 7. Voltage slope detection. (a) Schematic. (b) Waveforms.

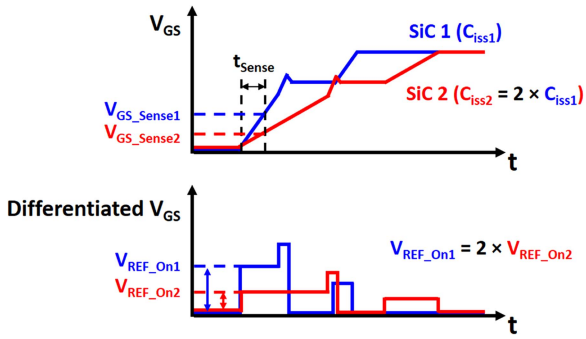


Fig. 8. Waveforms of SiC MOSFETs' gate voltage with different gate capacitance, differentiated V_{GS}, and proper V_{REF_ON} for different SiC MOSFETs.

Therefore, the value of V_{REF_ON} is set to match with this voltage difference $\Delta V_{LS\_Diff.}$, which aids in detecting the t_1 time point. The differentiated V_{GS} is then compared with a reference voltage. When the $V_{GS\_Diff.}$ is larger than V_{REF_ON}, the signal S_{ON_Start} turns high and the slope difference of V_{GS} is detected. The signal S_{ON_Start} then triggers the weak-ON logic and the signal S_{Weak_ON} is generated.

The $t_{2'}$ is acquired from a comparison between the $V_{GS\_Diff.}$ and V_{REF_OFF}, facilitated by the second set of slope detectors. In addition, in the initial cycle, a filter is employed to attenuate high-frequency noise during the early phase of entering the Miller plateau region. When V_{GS} leaves the Miller plateau region, the slope difference is detected in a similar way and thus determining the timing of t_3. Given that V_{GS} ringing occurs during the Miller plateau interval, a filter is essential to eliminate noise and sense the timing of t_3.

A trimmable resistance is required for inaccurate on-chip capacitor and resistor values because proper resistance and capacitance values in the RC differentiator are required. If the parasitic inductance varies for different PCBs or SiC MOSFETs, the value of differentiated V_{GS} can be adjusted through tunable resistance in RC differentiator.

B. Adaptive Slope Reference Generator for Different SiC

Since the value of gate capacitance between different SiC MOSFET products is not the same, the V_{REF_ON} should be different. Fig. 8 shows the waveforms of SiC MOSFETs' gate voltage with different gate capacitance, differentiated V_{GS}, and proper V_{REF_ON} for different SiC MOSFETs. A proper V_{REF_ON} should be slightly larger than the differentiated V_{GS} to catch the timing when V_{GS} reaches V_{TH}. A SiC MOSFET with larger gate capacitance requires a smaller V_{REF_ON} due to smaller slope of V_{GS}. The charging behavior of SiC MOSFET gate capacitance

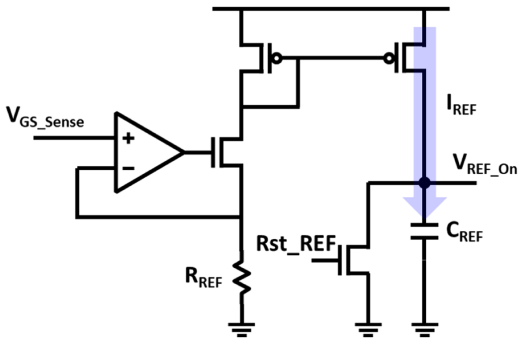


Fig. 9. Schematic of adaptive slope reference generator.

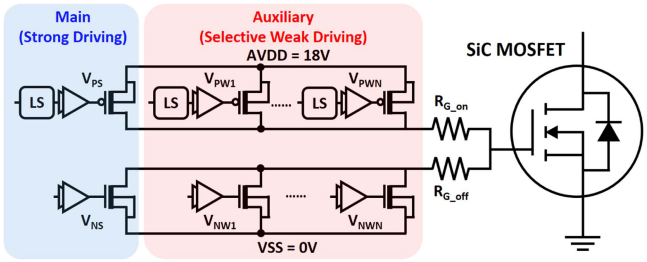


Fig. 10. Schematic of high voltage buffer.

can be written as follows:

$$I_{dr} = C_{iss} \cdot \frac{dV_{GS}}{dt}. \tag{9}$$

Substitute the dV_G/dt term in (9).

$$I_{dr} = C_{iss1} \cdot \frac{V_{GS\_sense1}}{t_{sense}} = C_{iss2} \cdot \frac{V_{GS\_sense2}}{t_{sense}}. \tag{10}$$

Therefore, with a same t_{sense}

$$\frac{C_{iss2}}{C_{iss1}} = \frac{V_{GS\_sense1}}{V_{GS\_sense2}}. \tag{11}$$

The schematic of the adaptive V_{REF} generator is depicted in Fig. 9. The V_{GS_sense} is converted to a current I_{REF} through a V-to-I circuit. The current I_{REF} is proportional to the V_{GS_sense}. Then, I_{REF} charges C_{REF} to generate V_{REF_ON}.

$$V_{REF\_On} = \frac{I_{REF} \cdot \Delta t}{C_{REF}} = \frac{V_{GS\_sense} \cdot \Delta t}{R_{REF} C_{REF}}. \tag{12}$$

By (11) and (12)

$$V_{REF\_On} \propto V_{GS\_sense} \propto \frac{1}{C_{iss}}. \tag{13}$$

As a result, a slope reference V_{REF_ON} which is inversely proportional to the gate capacitance is generated.

C. High-Voltage Buffer

To achieve gate resistance adjustment, the driving stage is composed of parallel PMOSs and NMOSs with different size, drawn in Fig. 10. The weak-ON (OFF) logic controls the selection between main PMOS (NMOS) and auxiliary PMOSs (NMOSs).

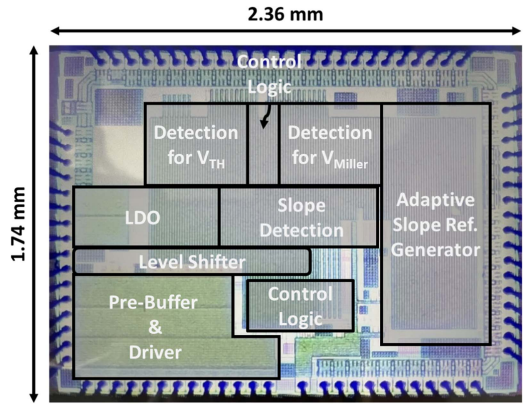


Fig. 11. Chip micrograph.

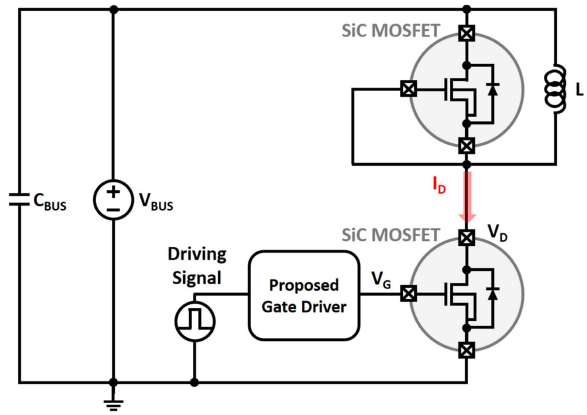


Fig. 12. Schematic of multiple pulse test.

The SiC power MOSFET models used in this article are IMW65R048M1H and IMW65R027M1H. The datasheets [32], [33] recommend a high driving voltage of 18 V and a low driving voltage of 0 V.

IV. Measurement Result

The chip was designed and fabricated using the 0.18-μm HV BCD process. Fig. 11 shows the chip micrograph of the proposed AGD IC for SiC MOSFET with the gate voltage sensing technique. The total chip area was 2.36×1.74 mm^2.

As shown in Fig. 12, a multiple pulse test is used to measure the switching transient. It consists of an inductive load, a clamped diode, a gate driver IC, and a SiC power MOSFET. The Infineon IMW65R048M1H and IMW65R027M1H SiC power MOSFETs are selected as the device under test (DUT) in this article. The photograph of the test setup is shown in Fig. 13.

The measurement results of CGD are also provided for comparison. To realize a CGD, the same chip is used and the function of AGD is disabled. The driving strength of CGD can be adjusted by changing the external gate resistance. The external gate resistance for turn-ON/OFF is set as 125/20 Ω in AGD measurement.

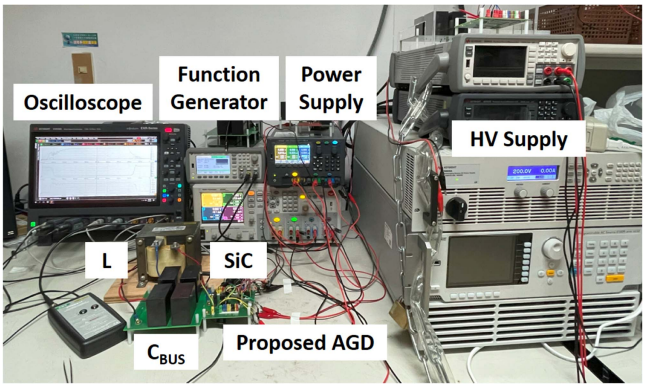


Fig. 13. Photograph of multiple pulse test.

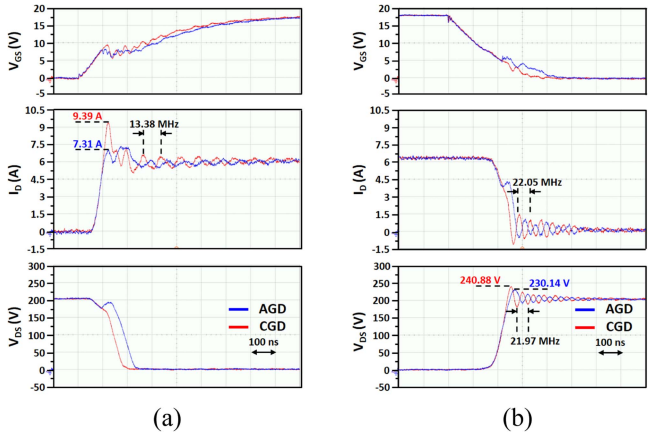


Fig. 14. Waveforms of CGD and proposed AGD under $V_{BUS} = 200$ V and $I_{LOAD} = 6$ A with DUT of IMW65R027M1H. (a) Turn-ON. (b) Turn-OFF.

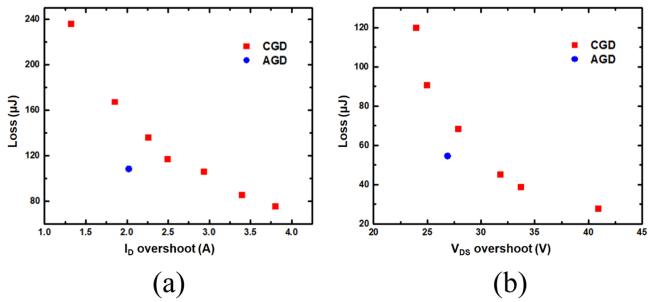


Fig. 15. Tradeoff curves of CGD and proposed AGD under $V_{BUS} = 200$ V and $I_{LOAD} = 6$ A with DUT of IMW65R027M1H. (a) Turn-ON. (b) Turn-OFF.

A. Proposed AGD Versus CGD

Fig. 14 illustrates the measured turn-ON and turn-OFF waveforms of the proposed AGD and CGD under $V_{BUS} = 200$ V and $I_{LOAD} = 6$ A. The DUT is the IMW65R027M1H SiC power MOSFET with an input capacitance of 2131 pF. The AGD exhibits lower I_D and V_{DS} overshoots compared to CGD. Additionally, the oscillation magnitudes of I_D, V_{DS}, and V_{GS} in AGD are smaller than those in CGD with the same gate resistance. In Fig. 15, a tradeoff curve is presented, depicting the relationship between energy loss and I_D (V_{DS}) overshoot for CGD. The

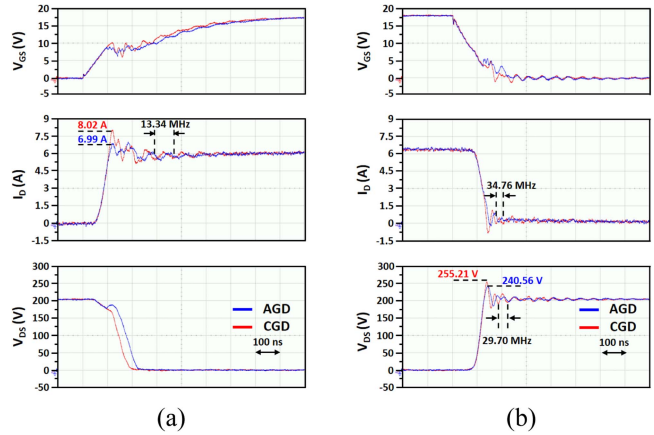


Fig. 16. Waveforms of CGD and proposed AGD under $V_{BUS} = 200$ V and $I_{LOAD} = 6$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

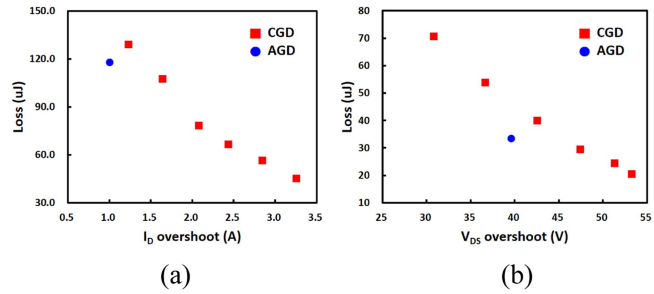


Fig. 17. Tradeoff curves of CGD and proposed AGD under $V_{BUS} = 200$ V and $I_{LOAD} = 6$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

results of AGD fall below these tradeoff curves, highlighting the advantages of AGD. The proposed AGD demonstrates the capability to achieve lower energy loss while maintaining the same overshoot, and vice versa.

B. Proposed AGD With Different SiC Power MOSFETs

To validate the adaptability of the proposed AGD in generating V_{REF_ON} for various SiC power MOSFETs, a different SiC model is chosen as the DUT in this section. The selected model for the DUT is IMW65R048M1H, with an input capacitance of 1118 pF.

In Fig. 16, the measured waveforms of the proposed AGD and CGD are presented under $V_{BUS} = 200$ V and $I_{LOAD} = 6$ A, utilizing a different DUT compared to Fig. 14. The I_D and V_{DS} overshoots in AGD are observed to be lower than those in CGD. Fig. 17 illustrates the tradeoff curve between energy loss and I_D (V_{DS}) overshoot for CGD. The results obtained with AGD lie below the tradeoff curves, highlighting the advantageous performance of AGD.

C. Proposed AGD Under Different V_{BUS}

Figs. 18 and 20 present the measured waveforms under varying VBUS while maintaining a fixed I_{LOAD} of 40 A, utilizing the IMW65R048M1H SiC power MOSFET as the DUT. The V_{BUS} values are set at 400 V and 200 V, respectively. As depicted

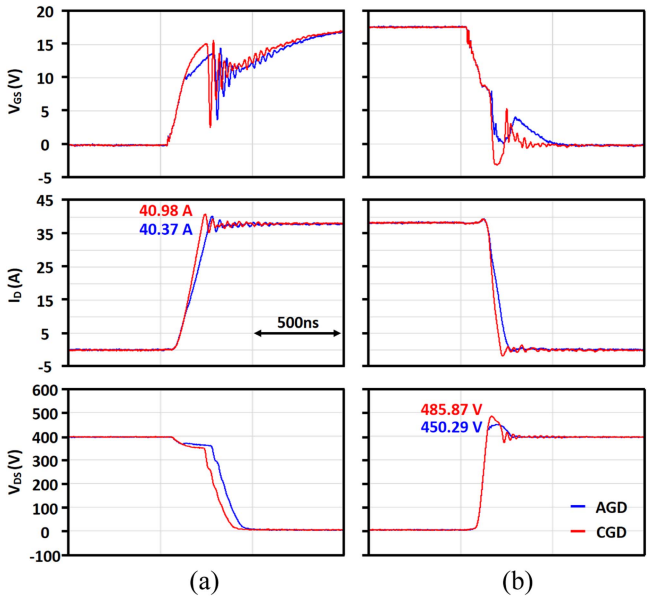


Fig. 18. Waveforms of CGD and proposed AGD under $V_{BUS} = 400$ V and $I_{LOAD} = 40$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

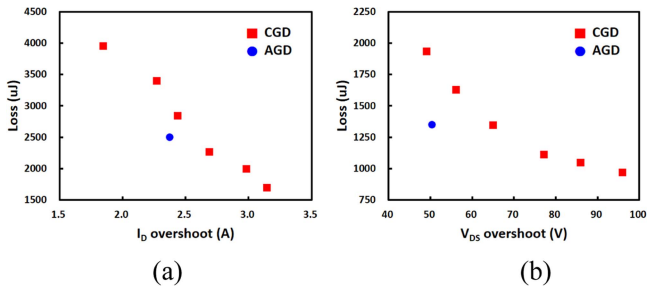


Fig. 19. Tradeoff curves of CGD and proposed AGD under $V_{BUS} = 400$ V and $I_{LOAD} = 40$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

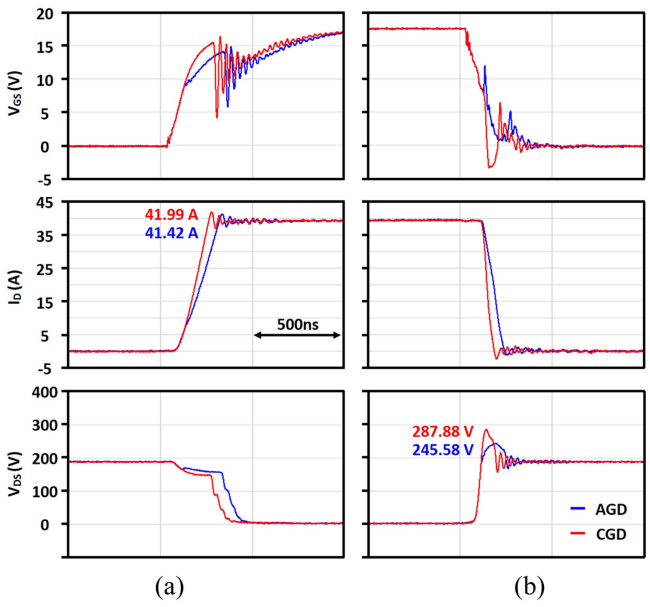


Fig. 20. Waveforms of CGD and proposed AGD under $V_{BUS} = 200$ V and $I_{LOAD} = 40$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

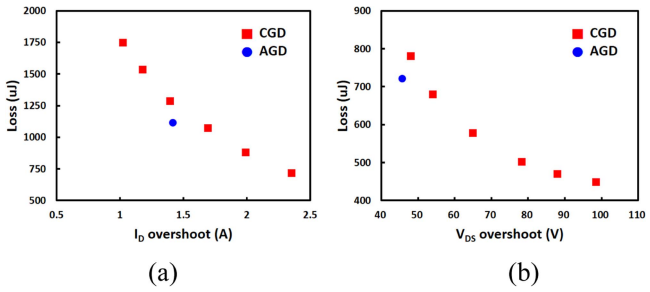


Fig. 21. Tradeoff curves of CGD and proposed AGD under $V_{BUS} = 200$ V and $I_{LOAD} = 40$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

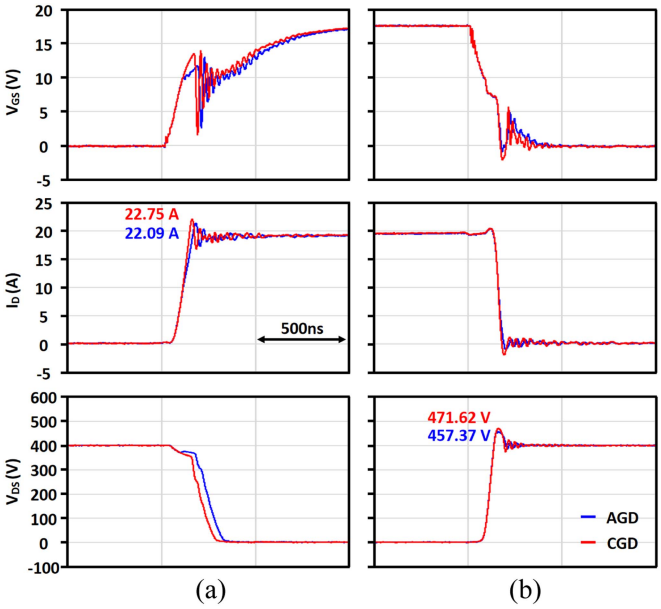


Fig. 22. Waveforms of CGD and proposed AGD under $V_{BUS} = 400$ V and $I_{LOAD} = 20$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

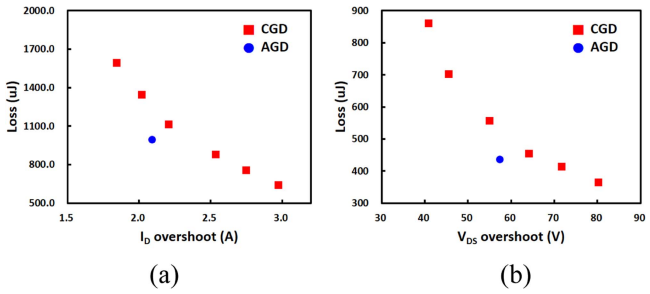
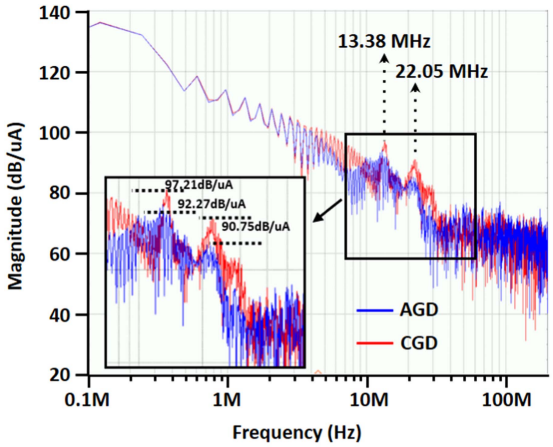
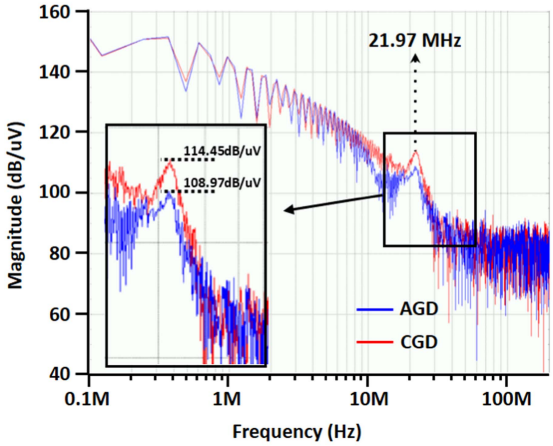


Fig. 23. Tradeoff curves of CGD and proposed AGD under $V_{BUS} = 400$ V and $I_{LOAD} = 20$ A with DUT of IMW65R048M1H. (a) Turn-ON. (b) Turn-OFF.

in Figs. 19 and 21, the proposed AGD successfully mitigates the tradeoff issues observed in CGD. The measurement results under different V_{BUS} conditions suggest the adaptability of the proposed AGD to varying V_{BUS} settings. The large voltage drop and oscillation observed on V_{GS} during the turn-ON process result from the voltage across the parasitic inductance in the package, specifically on the source terminal.



(a)



(b)

Fig. 24. Spectrum comparison between CGD and AGD for (a) I_D and (b) V_{DS}.

D. Proposed AGD Under Different I_{LOAD}

Figs. 18 and 22 present the observed waveforms under different ILOAD conditions while keeping V_{BUS} constant at 400 V, using the IMW65R048M1H SiC power MOSFET as the DUT. The I_{LOAD} values are set at 40 A and 20 A, respectively. As shown in Figs. 19 and 23, the proposed AGD effectively addresses the tradeoff challenges observed in CGD. The measurement results under different I_{LOAD} conditions suggest the capability of the proposed AGD to operate across various I_{LOAD} settings.

E. EMI Analysis

The proposed AGD has the capability of reducing the slope and oscillation in both I_D and V_{DS}. Generally, the EMI noise is mainly caused by the dI/dt, dV/dt, and oscillations in I_D and V_{DS} during the switching transients of power devices. The effect of oscillations can be characterized considering the current or voltage source as a periodic trapezoidal pulse and fast Fourier transform (FFT) analysis.

The approximation of the spectrum for I_D and V_{DS} with DUT of IMW65R027M1H is shown in Fig. 24(a) and (b), respectively. These results were obtained from experimental measurement and the spectrum was obtained applying the FFT function by the oscilloscope. The results show that the proposed AGD can reduce the EMI noise in I_D and V_{DS}, especially at the resonant frequencies.

V. Conclusion

In this study, we proposed a high integration AGD IC for SiC MOSFETs in the TSMC 0.18-μm HV BCD process. The high-voltage buffer and the controller are built into the chip. The proposed gate voltage sensing technique can provide the timing for AGD through the slope difference of the V_{GS}. Because it is not necessary to directly sense the I_D and V_{DS} information, the additional sensing circuit and cost can be reduced. The performance of the proposed AGD was verified in a multiple pulse test under different V_{BUS} and I_{LOAD} conditions. The experimental results demonstrate that the proposed AGD can solve the tradeoff between the I_D (V_{DS}) overshoot and the switching loss (switching speed) in CGD. Benefit from the proposed gate voltage sensing technique, the proposed AGD does not need any adjustment when the operating V_{BUS} or I_{LOAD} condition changes. The proposed AGD can also attenuate the slope and oscillation of I_D and V_{DS}, further reduce the EMI noise induced by high switching speed. In addition, the experimental results show that the proposed AGD can be applied to different SiC power MOSFETs.

Acknowledgment

The authors would like to thank the Taiwan Semiconductor Research Institute (TSRI) for chip fabrication.

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