A Single-Switch Trans-Inverse High Step-Up Semiquadratic DC–DC Converter Based on Three-Winding Coupled Inductor

Yuegang Hu, Weishu Zhan, Shunlei Li, and Muhammad Adeel Azam

***Abstract*—This article introduces a new nonisolated single-switch trans-inverse high step-up semiquadratic dc–dc converter with low input current ripple for renewable energy generation systems. In the presented topology, a three-winding coupled inductor combined with a quadratic boost converter to achieve high voltage gains. The advanced features of the suggested structure are its ultrahigh voltage conversion ratio, low voltage stress ratio across the switching components, low input current ripple, zero current switching of the semiconductors and also common ground between the input and output sides. Due to the trans-inverse feature in the proposed circuit, higher voltage gains can be achieved without needing large turns' ratios of the coupled inductor in comparison to the other typical quadratic converters, which decreases the conduction power loss. Furthermore, in this topology, the maximum voltage stress across the power switch is mitigated with the help of a regenerative passive clamp cell. The operating principle, steady-state analysis, theoretical efficiency analysis of the suggested circuit, along with performance comparison with other similar converters are discussed in detail. Finally, to verify the theoretical analysis, a 200 W with 25 V input voltage and 400 V output dc voltage sample prototype is established.**

***Index Terms*—Renewable energy, step-up dc–dc converter, three-winding coupled-inductor, trans-inverse.**

I. Introduction

In the last decades, as the electrical energy demand is rapidly growing, renewable energy sources (RES), such as photovoltaic (PV) and fuel cells (FC), and wind energy, are the best options to decrease fossil fuels and have been widely used. However, these resources suffer from low output voltage. That is why high step-up (high voltage gain) dc–dc converters are widely employed as an interface circuit in many industrial applications to provide the desired high output dc voltage from low input voltage sources [1], [2]. Since continuous input current with low ripple leads to improve RES performance, current-fed structures of high step-up dc–dc converters are more preferred to achieve extract the maximum power from the RES [3]. Also, high voltage gain ratio, low voltage and current stress rates, enough high efficiency, and low cost are the other main key indicators of these circuits. Besides, nonisolated structures with simple structures, and cheaper implementation are often preferred for low-power applications [4].

Today, due to some issues such as a very low voltage gain ratio, and very high voltage stresses on the switching components, conventional step-up structures such as Boost, and SEPIC are not suitable for realizing high step-up voltage gain together with high efficiency [5]. Therefore, in recent years, many efforts have been made to provide improved step-up dc–dc structures.

So far, many modified dc–dc converters with high voltage gain have been presented. In these topologies, to obtain higher voltage conversion ratios, some effective voltage boosting methods including switched capacitor, switched inductor, voltage lift, cascading /interleaving methods, and voltage multiplier cells have been applied [1], [2], [6], [7], [8]. Nonetheless, for very high voltage applications, such structures often suffer from a large number of components, which prevents the proper performance of converters [9], [10]. Accordingly, the magnetic devices consisting coupled-inductor (CI) and transformer (isolated/nonisolated) as valuable voltage boosting techniques are able to provide higher voltage gains in a wider range through turns' ratio [11]. However, in CI-based circuits, the high voltage spikes across the power switch caused by the leakage inductance should be restricted by considering an active or a passive clamp circuit [12], [13].

Until now, many nonisolated dc–dc structures based on magnetic devices and other boosting methods with ultrahigh voltage gain have been presented. In [14] and [15], two new ultrahigh step-up CI-based dc–dc topologies with quadratic voltage gain and low voltage stress are proposed. However, high input current ripple limits the applications of the mentioned converters for RES. To solve this problem, in [16], [17], [18], and [19], some new single-switch two-winding CI-based step-up dc–dc converters with low input current ripple are suggested. However,

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in these mentioned circuits, to achieve large voltage gains, the turns' ratio of the CI must be set very high, which leads to high voltage and current stress rates and more power loss. Besides, ultrahigh voltage gain quadratic structures using a three-winding CI (TWCI) with more freedom of degrees are presented in [20], [21], and [22]. Although providing ultrahigh voltage gains at low-duty cycles, input current with high ripple is considered the main demerit of the mentioned converters. Also, in [23], [24], [25], and [26], using a TWCI, some modified quadratic single-switch circuits with low input current ripple are also proposed. Nevertheless, in these structures, high voltage gains with quadratic form need high turns' ratio of the CI. In addition, a new ultrahigh step-up soft-switched quadratic dc–dc topology with continuous input current and low switch voltage stress is introduced in [27]. However, in this topology, soft-switching performance is obtained using two active switches along with a CI with four windings. Furthermore, two new quadratic-based single-switch high step-up dc–dc converters using TWCI with low input current and reduced voltage stress are suggested in [28], [29], and [30]. However, these converters suffer from the lack of common ground between the input voltage and output load.

Recently, high voltage gain CI-based structures with trans-inverse properties have been paid more attention. In such converters, ultrahigh voltage gains can be obtained under a low number of turns' ratios of the magnetic components, which improves the converter efficiency more. In [31], a new ultra-high voltage gain with partial trans-inverse characteristics has been introduced with low input current ripple and low voltage stress. However, this converter does not have a clamp circuit, which can be considered the main disadvantage of this topology. Moreover, a new single-switch ultrahigh step-up converter based on quadratic y-sources techniques is presented in [32]. In this circuit, the power switch has to withstand high voltage stress (close to output dc voltage) at high voltage gains. A new nonisolated double-switch TWCI-based trans-inverse high voltage gain dc–dc converter is presented in [33]. Nevertheless, in this circuit, ultrahigh voltage gain is achieved with the help of two power switches. Besides, a new type of cascaded couple inductor-reverse converter using a TWCI along with diode-capacitor method is suggested in [34]. However, in the mentioned topology, a greater than unity ratio of the turns' ratios of the TWCI is needed to obtain high output dc voltages. Integration of TWCIs with SEPIC converter [35], [38], with Y-source converter [36] also yields high voltage gains. However, in [36], the common ground between load and source is lost and this converter also does not support trans-inverse operation. In [37], a two-winding CI is merged in a VMC and through two units of VMCs, the introduced converter achieves high voltage gains.

Motivated by above discussions, this article proposes a new TWCI-based structure of quadratic high step-up dc–dc converter with low input current ripple. The features of the proposed converter are listed as follows.

1) Ability to provide ultrahigh voltage gains at small turns' ratios of the TWCI.
2) Trans-inverse properties.
3) Three different design freedom degrees to enhance the voltage gain ratio.
4) Low component count.
5) Low input current ripple.
6) Low voltage stress across the switching components.
7) Zero current switching (ZCS) turn-ON of the MOSFET.
8) Leakage inductance energy is recycled to the output.
9) The falling current rate of the diodes are controlled by the leakage inductances, which alleviates reverse recovery problems and minimizes switching losses.
10) Common ground between the input dc source and output load.

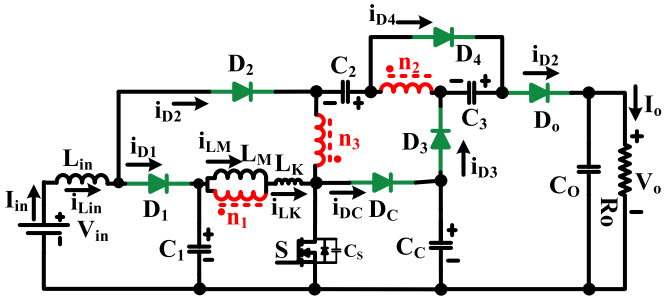

Fig. 1. Power circuit of the proposed converter.

The rest of this article is organized as follows. In Sections II and III, the operating principles of the proposed topology and mathematical derivations are provided in detail. Subsequently, the performance of the suggested topology is compared with some other similar converters in Section IV. Sections V and VI provide the parameters design considerations and experimental results of a laboratory prototype. Finally, Section VII concludes this article.

II. Proposed Converter and Operating Principle

The power circuit of the proposed converter is shown in Fig. 1. It consists of a power switch S; six diodes D_1, D_2, D_3, D_4, D_C, D_O; five capacitors C_1, C_2, C_3, C_C, C_o; input inductor L_{in} and a three-winding CI with n_1, n_2, and n_3 turns at the primary, secondary, and tertiary windings, respectively. L_M and L_K symbolize the magnetizing inductor and equivalent leakage inductance at the primary of the CI, respectively. The turns' ratios of the CI are defined as $n_{21} = n_2/n_1$ and $n_{31} = n_3/n_1$. V_{in} and V_O are the input and the output voltages; I_{in} and I_O are the input and the output currents and R_O is the resistance of the output load. The clamp circuit consists of the clamp diode D_C and the clamp capacitor C_C not only absorbs the energy of the leakage inductance and prevents the high spikes across the switch S, but also clamps the voltage stress of the switch to a low value in comparison with the high output voltage. To simplify the operating principal analysis of the proposed converter, the following assumptions are made.

1) L_{in} is sufficiently large so that i_{Lin} is considered continuous; the capacitors are large enough and their associated voltage ripple in one switching cycle is neglected.

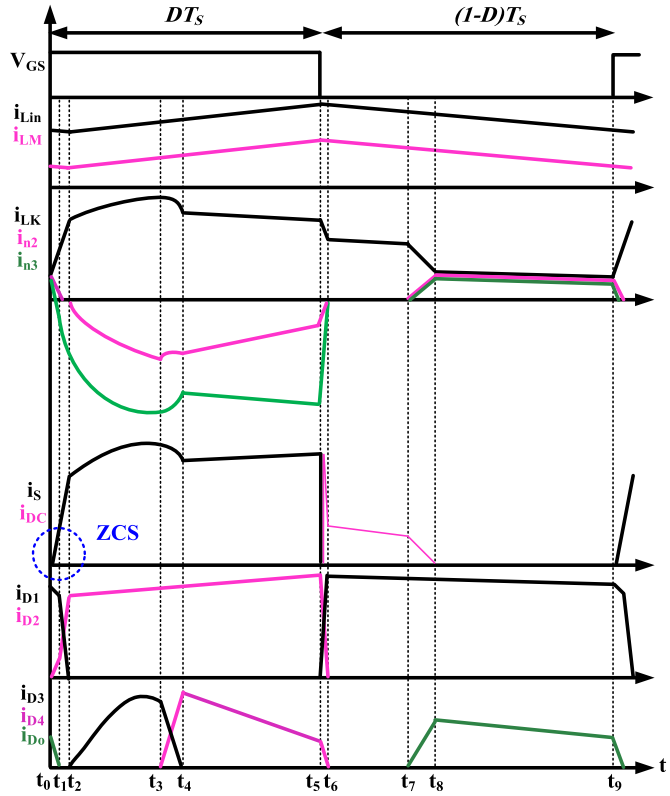

Fig. 2. Key waveforms of the proposed converter under CCM operation.

2) i_{LM} is continuous and discontinuous respectively in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Moreover, boundary conduction mode (BCM) is the boundary between CCM and DCM.
3) Except the leakage inductance of the CI, all other parasitic elements of the components are neglected.

A. CCM Operation

The key waveforms of the proposed converter in CCM are shown in Fig. 2. Also, Fig. 3 illustrates the equivalent circuits of the proposed converter in a switching cycle. There are nine modes of operation in CCM that are demonstrated as follows.

Mode I $[t_0 \sim t_1]$: The equivalent circuit of this mode is shown in Fig. 3(a). At t_0, the gate-source pulse is applied to S and the switch is turned ON with ZCS. The passing currents through the secondary ($i_{n2} = i_{Do}$) and tertiary ($i_{n3} = i_{Do} - i_{D2}$) windings of the CI start to decrease. D_1 and D_2 are connected to inductive nodes; therefore, i_{D2} should be increased gradually from zero. Since, $i_{D1} + i_{D2}$ is I_{in}, i_{D1} is decreasing, during this mode. The current falling rate of D_o is controlled by the leakage inductance and this mode ends at t_1 when D_o is turns OFF.

Mode II $[t_1 \sim t_2]$: The equivalent circuit of this mode is shown in Fig. 3(b). D_1 and D_2 along with switch S are conducting. During this interval, i_{D1} and i_{D2} are decreasing and increasing, respectively. This mode ends at t_2 when i_{D1} reaches zero and D_1 turns OFF.

Mode III $[t_2 \sim t_3]$: The equivalent circuit of this mode is shown in Fig. 3(c). At the beginning of this mode, D_3 turns ON. $V_{in} + n_{31}V_{C1}$ and V_{C1} to the input inductor and the magnetizing inductor, respectively, and both of i_{Lin} and i_{LM} start charging. Moreover, D_2 is handling the input current during this mode of operation. A resonance circuit is made between C_1, C_2, C_C, and L_K. The capacitor C_1, delivers part of its energy to the CI and through the transformer effect discharges and charges C_C and C_2, respectively. The output load is supplied by the stored energy in the output capacitor C_O

$$\omega_R^{III} = \frac{1}{\sqrt{L_K\left(\frac{C_1 C_X}{C_1+C_X}\right)}}; C_X = (n_2+n_3)^2 \frac{C_2 C_C}{C_2+C_C} \quad (1)$$

$$i_S = i_{LM} + (n_{31}+1)\, I_{in} + (n_{31}+n_{21}+1)\, i_{D3}. \quad (2)$$

Mode IV $[t_3 \sim t_4]$: The equivalent circuit of this mode is shown in Fig. 3(d). At the beginning of this mode, D_4 is forward biased. Capacitor C_3 starts to be charged through the secondary winding of the CI, which is i_{D3} plus i_{D4}. During this mode, $i_{D3}$and i_{D4} are decreasing and increasing, respectively. This mode ends at the time t_4 when i_{D3} reaches to zero and D_3 is turns OFF

$$i_S = i_{LM} + (n_{31}+1)\, I_{in} + (n_{31}+n_{21}+1)\, i_{D3} + n_{21} i_{D4}. \quad (3)$$

Mode V $[t_4 \sim t_5]$: The equivalent circuit of this mode is shown in Fig. 3(e). During this mode, C_3 is still charging the secondary winding of the CI and the third winding of the CI transfers the input current I_{in} through D_2. This mode ends at the time t_5 when the switch S is turned OFF

$$i_S = i_{LM} + (n_{31}+1)\, I_{in} + n_{21} i_{D4}. \quad (4)$$

Mode VI $[t_5 \sim t_6]$: The equivalent circuit of this mode is shown in Fig. 3(f). At the beginning of this mode, switch S is turned OFF and the clamp diode D_C is forward biased to handle the passing current through the switch S at time t_5 to the clamp capacitor C_C. As a result, it successfully recycles the leakage energy and avoids high voltage spikes across the power switch. Moreover, the voltage of the switch is clamped to V_{CC} and the clamp capacitor starts to be charged by the leakage current. On the other hand, similar to the analysis in mode I, D_2 is not turned OFF at t_5, because it is connected to inductive nodes in both sides and the passing current of the third winding of the CI forces it to continue conduction. In such a case, D_1 turns ON, at the beginning of this mode. D_1 and D_2 are simultaneously handling the input current in a way that i_{D1} is increasing and i_{D2} is decreasing. This mode ends at t_6 when i_{D2} reaches to zero and D_2 turns OFF.

Mode VII $[t_6 \sim t_7]$: The equivalent circuit of this mode is shown in Fig. 3(f). C_C and C_1 are being charged by i_{LM} and i_{Lin}. The output load is still being supplied by the energy of the output capacitor C_O. This mode ends at t_7 when C_C is charged sufficiently and the D_O is forward biased.

Mode VIII $[t_7 \sim t_8]$: The equivalent circuit of this mode is shown in Fig. 3(g). At the beginning of this mode, D_O turns ON and transfers the energy of the magnetizing inductor L_M to the output load through the secondary and tertiary windings of the CI and capacitors C_2 and C_3. This mode ends at t_8 when

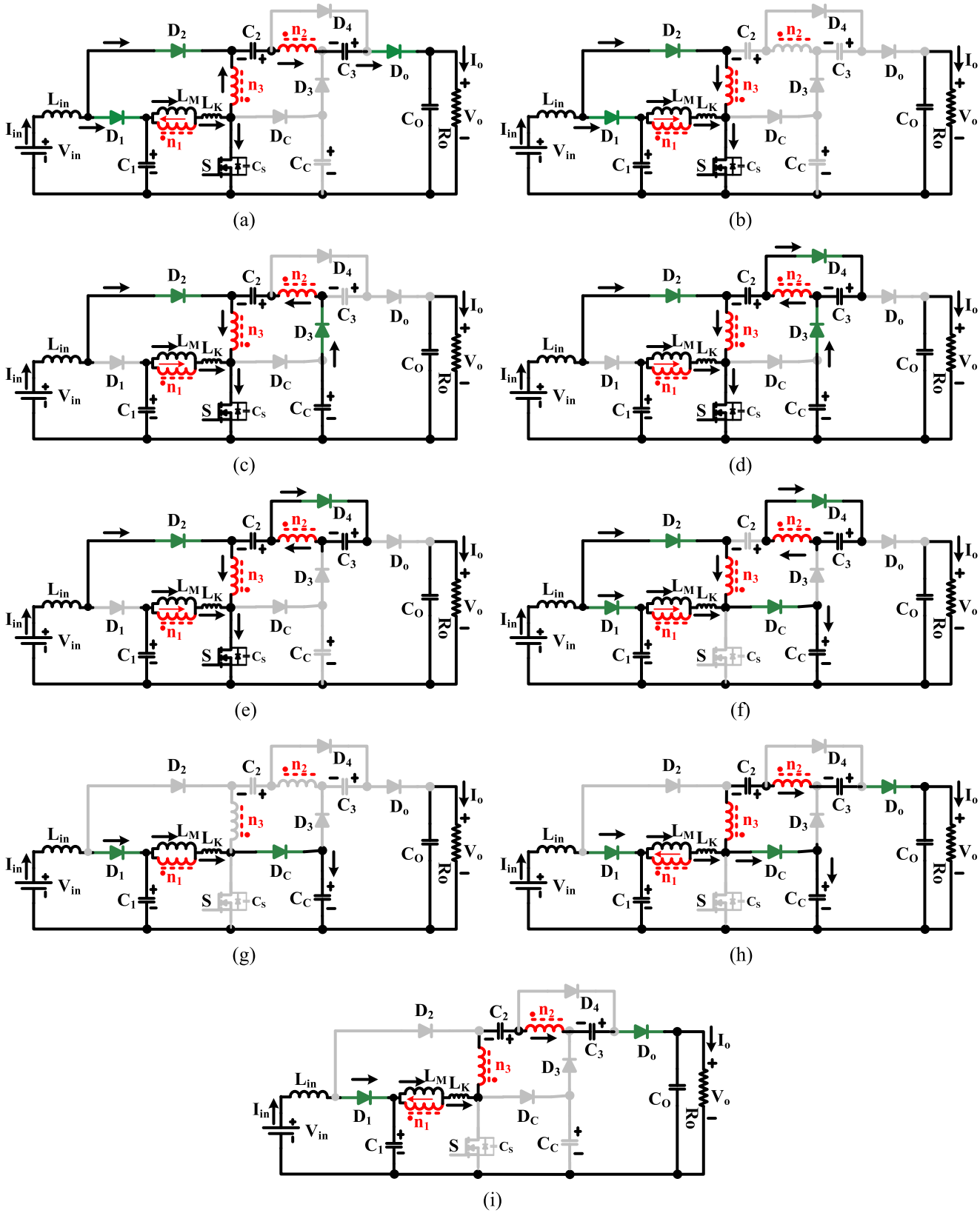

Fig. 3. Equivalent circuits of the proposed converter at CCM. (a) Mode I [$t_0 \sim t_1$]. (b) Mode II [$t_1 \sim t_2$]. (c) Mode III [$t_2 \sim t_3$]. (d) Mode IV [$t_3 \sim t_4$]. (e) Mode V [$t_4 \sim t_5$]. (f) Mode VI [$t_5 \sim t_6$]. (g) Mode VII [$t_6 \sim t_7$]. (h) Mode VIII [$t_7 \sim t_8$]. (i) Mode IX [$t_8 \sim t_9$].

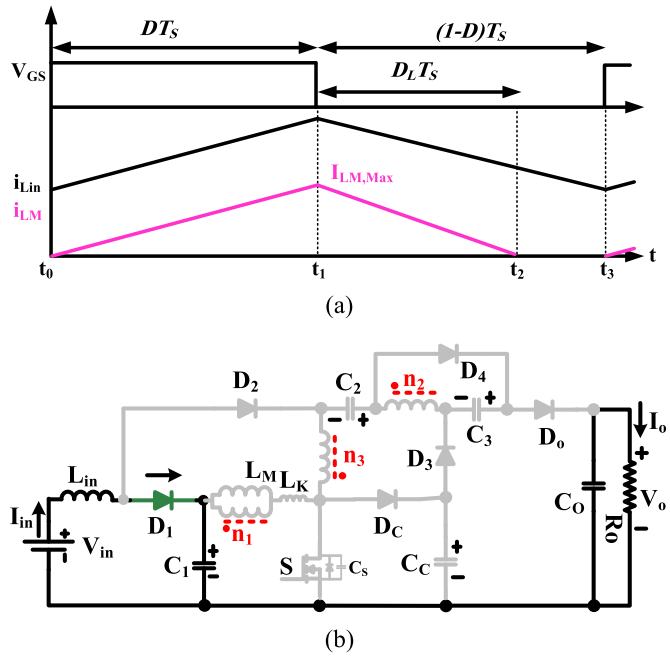

Fig. 4. DCM operation. (a) Waveforms of i_{Lin} and i_{LM}. (b) Equivalent circuit.

the passing current through the clamp diode reaches to zero and turns OFF.

Mode IX $[t_7 \sim t_8]$: The equivalent circuit of this mode is shown in Fig. 3(h). The stored energy in the magnetizing inductor L_M continuous transferring to the load. This mode ends at t_8 when the gate-source pulse comes and the next switching cycle begins.

B. DCM Operation

Following to the mode IX in CCM operation, if the stored energy of the magnetizing inductor L_M reaches to zero before switching pulses comes, the converter will enter to DCM operation. It is worth mentioning that the input inductor L_{in} should be designed in such a way that its current does not reach to DCM region. Because discontinuous input current due to high amount of ripple is not suitable while PV or FC power sources are being implemented. At this condition, the MPPT performance and life span of these sources are deteriorated. As a result, the DCM condition is decided by the passing current of L_M. The waveforms of i_{Lin} and i_{LM} along with the equivalent circuit of the proposed converter in DCM are shown in Fig. 4. Capacitor C_1 and output load are continuously being charged by the i_{Lin} and stored energy in C_O, respectively.

III. Steady-State Analysis

A. CCM Operation

The time durations of modes I, II, and VI are very short. As a result, these modes are neglected in voltage gain analysis. The coupling coefficient is considered $K = L_M/(L_M + L_K)$. During ON state of the switch S, the following equations could be written:

$$V_{LM}^{\text{on}} = KV_{C1}. \tag{5}$$

The proof of (5) is presented in appendix

$$V_{Lin}^{\text{on}} = V_{in} + Kn_{31}V_{C1} \tag{6}$$

$$V_{C3} = n_{21}\, KV_{C1} \tag{7}$$

$$V_{C2} = (n_{21} + n_{31})\, KV_{C1} + V_{CC}. \tag{8}$$

During OFF state of the switch S, we have

$$V_{LM}^{\text{off}} = K(V_{C1} - V_{CC}) \tag{9}$$

$$V_{Lin}^{\text{off}} = V_{in} - V_{C1} \tag{10}$$

$$V_O = K\,(n_{21} + n_{31})\,(V_{CC} - V_{C1}) + V_{CC} + V_{C2} + V_{C3}. \tag{11}$$

By applying the volt-second balance principle to V_{Lin} and V_{LM}, the voltages of capacitors C_1 and C_C are derived as

$$V_{C1} = \frac{V_{in}}{1 - (1 + Kn_{31})\,D} \tag{12}$$

$$V_{CC} = \frac{V_{C1}}{1 - D} = \frac{V_{in}}{(1 - D)\,[1 - (1 + Kn_{31})\,D]}. \tag{13}$$

Substituting (12) into (7), yields V_{C3} as

$$V_{C3} = \frac{Kn_{21}V_{in}}{1 - (1 + Kn_{31})\,D}. \tag{14}$$

From (8), (12), and (13), V_{C2} is derived as follows:

$$V_{C2} = \left[K(n_{21} + n_{31}) + \frac{1}{1 - D}\right] \frac{V_{in}}{1 - (1 + Kn_{31})\,D}. \tag{15}$$

Finally, by substituting (12)–(15) into (11), the voltage gain of the proposed converter at CCM operation is obtained as

$$M_{\text{CCM}} = \frac{V_O}{V_{in}} = \frac{2 + n_{21}K\,(2 - D) + Kn_{31}}{[1 - (1 + Kn_{31})\,D]\,(1 - D)}. \tag{16}$$

By neglecting the effect of the leakage inductance, the ideal voltage gain of the proposed converter is derived as

$$M_{\text{CCM}} = \frac{V_O}{V_{in}} = \frac{2 + n_{21}(2 - D) + n_{31}}{[1 - (1 + n_{31})\,D]\,(1 - D)}. \tag{17}$$

Moreover, the voltages of the capacitors are given by

$$V_{C1} = \frac{V_{in}}{1 - (1 + n_{31})\,D} \tag{18}$$

$$V_{C2} = \left[n_{21} + n_{31} + \frac{1}{1 - D}\right] \frac{V_{in}}{1 - (1 + n_{31})\,D} \tag{19}$$

$$V_{C3} = \frac{n_{21}V_{in}}{1 - (1 + n_{31})\,D} \tag{20}$$

$$V_{CC} = \frac{V_{C1}}{1 - D} = \frac{V_{in}}{(1 - D)\,[1 - (1 + n_{31})\,D]}. \tag{21}$$

Fig. 5, shows the voltage gain of the proposed converter versus duty cycle for $n_{31} = 0.25$ and different values of n_{21}. It is clear that the voltage gain of the proposed converter increases by increasing of the turn's ratios of the CI and duty cycle. Moreover,

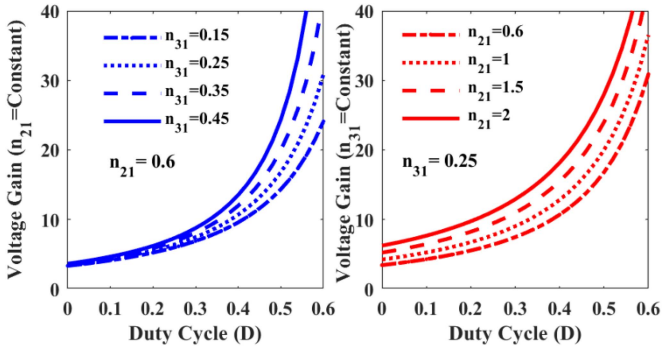

Fig. 5. Voltage gain of the proposed converter under CCM operation versus duty cycle.

due to trans-inverse and semiquadratic operation of the proposed converter, with low values of turns' ratios and duty cycles, high voltage gains are achieved. It should be noticed that by selecting the proper duty cycle, the value of n_{31} is limited as

$$n_{31} < \left(\frac{1-D}{D}\right). \tag{22}$$

According to equivalent circuit of Fig. 3(h), the voltage stress across the power switch is expressed as

$$V_S = V_{CC} = \frac{V_{in}}{(1-D)\left[1-(1+n_{31})\,D\right]} = \frac{V_O}{2+n_{21}(2-D)+n_{31}}. \tag{23}$$

It is seen from (23) that the voltage stress across switch S is much lower than the output voltage. As a result, switches with low ON-state resistances can be used to reduce conduction losses and cost.

The voltage stresses across the diodes are obtained as

$$V_{\rm dc} = V_{CC} = \frac{V_{in}}{(1-D)\left[1-(1+n_{31})\,D\right]} = \frac{V_O}{2+n_{21}(2-D)+n_{31}} \tag{24}$$

$$V_{D1} = \frac{(1+n_{31})\,V_{in}}{1-(1+n_{31})\,D} = \frac{(1+n_{31})\,(1-D)\,V_O}{2+n_{21}(2-D)+n_{31}} \tag{25}$$

$$V_{D2} = \frac{(1+n_{31})\,DV_{in}}{(1-D)\left[1-(1+n_{31})\,D\right]} = \frac{(1+n_{31})\,DV_O}{2+n_{21}(2-D)+n_{31}} \tag{26}$$

$$V_{D3} = V_{DO} = \left(\frac{1+n_{21}+n_{31}}{1-D}\right)\frac{V_{in}}{\left[1-(1+n_{31})\,D\right]} = \frac{(1+n_{21}+n_{31})\,V_O}{2+n_{21}(2-D)+n_{31}} \tag{27}$$

$$V_{D4} = \frac{n_{21}V_{in}}{(1-D)\left[1-(1+n_{31})\,D\right]} = \frac{n_{21}V_O}{2+n_{21}(2-D)+n_{31}}. \tag{28}$$

It is clear from (24)–(28) that the voltages across the diodes are substantially lower than the output voltage. Therefore, diodes with low forward voltage drops could be implemented to improve the performance of the proposed converter.

Keeping in mind that the average current passing from the capacitors is zero, the average currents of the diodes are derived as

$$I_{D3,\rm Ave} = I_{D4,\rm Ave} = I_{DO,\rm Ave} = I_{\rm dc,Ave} = I_O \tag{29}$$

$$I_{D1,\rm Ave} = (1-D)\,I_{in} = (1-D)\,M_{\rm CCM}I_O \tag{30}$$

$$I_{D1,\rm Ave} = DI_{in} = DM_{\rm CCM}I_O. \tag{31}$$

Moreover, by writhing the KCL law for the average currents at the node in which the cathode of D_1 is connected, we have

$$I_{D1,\rm Ave} = I_{LM} + n_{21}I_{D1,\rm Ave} + n_{31}I_{D2,\rm Ave}. \tag{32}$$

Considering (17) and substituting (29)–(31) into (32), the average current of the magnetizing inductor is obtained as

$$I_{LM} = \frac{2+n_{21}+n_{31}}{1-D}I_O. \tag{33}$$

The maximum currents of the diodes can be written as

$$I_{D1,\rm Max} = I_{D1,\rm Max} = i_{Lin,\rm Max} = M_{\rm CCM}I_O + \frac{D\,(V_{in}+n_{31}V_{C1})}{2L_{in}f_S} \tag{34}$$

$$I_{D3,\rm Max} \cong I_{D4,\rm Max} \cong \frac{4I_O}{D} \tag{35}$$

$$I_{DO,\rm Max} = i_{Do}(t_8) = \frac{i_{LM}(t_8)}{1+n_{21}+n_{31}} \cong \frac{I_{LM}}{1+n_{21}+n_{31}} \tag{36}$$

$$I_{\rm dc,Max} = i_{\rm dc}(t_5) = i_S(t_5) = I_{LM} + (1+n_{31})\,I_{D2,\rm Max}. \tag{37}$$

The maximum current of the power switch is derived as

$$I_{S,\rm Max} = i_S(t_3) = I_{LM} + (1+n_{31})\,M_{\rm CCM}I_O + \frac{4\,(1+n_{21}+n_{31})\,I_O}{D}. \tag{38}$$

The rms current of the components are obtained as follows:

$$I_{D1,\rm rms} = M_{\rm CCM}I_O\sqrt{1-D} \tag{39}$$

$$I_{D2,\rm rms} = M_{\rm CCM}I_O\sqrt{D} \tag{40}$$

$$I_{D3,\rm rms} \cong I_{D4,\rm rms} \cong I_{D3,\rm Max}\sqrt{\frac{D}{6}} \tag{41}$$

$$I_{\rm dc,rms} \cong I_{LM}\sqrt{\frac{1-D}{2+n_{21}+n_{31}}} \tag{42}$$

$$I_{DO,\rm rms} \cong I_{LM}\sqrt{\frac{1-D}{(2+n_{21}+n_{31})\,(1+n_{21}+n_{31})}} \tag{43}$$

$$I_{S,\rm rms} \cong (M_{\rm CCM}-1)\,I_O\sqrt{\frac{1}{D}} \tag{44}$$

$$I_{n2,\rm rms} = \sqrt{2{I_{D3,\rm rms}}^2 + {I_{DO,\rm rms}}^2} \tag{45}$$

$$I_{n3,\rm rms} = \sqrt{{I_{D2,\rm rms}}^2 + {I_{D3,\rm rms}}^2 + {I_{DO,\rm rms}}^2 + 2M_{\rm CCM}{I_O}^2} \tag{46}$$

$$I_{LK,\text{rms}} = \sqrt{\begin{matrix} {I_{LM}}^2 + 2I_{LM}I_O\left(n_{21}+n_{31}DM_{\text{CCM}}\right) + \left(n_{21}I_{n2,\text{rms}}\right)^2 \\ +\left(n_{31}I_{n3,\text{rms}}\right)^2 + 2n_{21}n_{31}\left({I_{D3,\text{rms}}}^2 + {I_{DO,\text{rms}}}^2\right. \\ \left. + 2M_{\text{CCM}}{I_O}^2\right) \end{matrix}} \tag{47}$$

$$I_{C1,\text{rms}} = \sqrt{{I_{D3,\text{rms}}}^2 + {I_{LK,\text{rms}}}^2 - 4M_{\text{CCM}}{I_O}^2} \tag{48}$$

$$I_{C2,\text{rms}} = \sqrt{{I_{D3,\text{rms}}}^2 + {I_{DO,\text{rms}}}^2} \tag{49}$$

$$I_{C3,\text{rms}} = \sqrt{{I_{DO,\text{rms}}}^2 + {I_{D4,\text{rms}}}^2} \tag{50}$$

$$I_{CC,\text{rms}} = \sqrt{{I_{\text{dc,rms}}}^2 + {I_{D3,\text{rms}}}^2} \tag{51}$$

$$I_{CO,\text{rms}} = \sqrt{{I_{DO,\text{rms}}}^2 - {I_O}^2}. \tag{52}$$

B. DCM Operation

The effect of the leakage inductance is ignored in DCM analysis and as a result $K = 1$. The derived equations of (5)–(11) are valid for DCM operation. Moreover, since I_{Lin} is still continuous and the voltages of V_{C1} and V_{C3} are obtained based on the volt-second balance principle for L_{in}; as a result, (12) is also valid, here. Referring to Fig. 4(a), by applying the volt-second principle to the V_{LM}, we have

$$V_{CC} = \left(1 + \frac{D}{D_L}\right) V_{C1}. \tag{53}$$

From (8) and (53), V_{C2} can be written as

$$V_{C2} = \left(1 + n_{21} + n_{31} + \frac{D}{D_L}\right) V_{C1}. \tag{54}$$

By substituting (6), (12), (53), and (54) into (11), the following relationship is derived:

$$V_O = \left[n_{31} + \left(1 + \frac{D}{D_L}\right)(2 + n_{21} + n_{31})\right] \frac{V_{in}}{1 - (1 + n_{31})\,D}. \tag{55}$$

Moreover, from (33) and the current waveform of i_{LM} in Fig. 4(a), we have

$$I_{LM} = \frac{2 + n_{21} + n_{31}}{1 - D} I_O = \frac{1}{2}(D + D_L)\, I_{LM,Max} \tag{56}$$

$$I_{LM,Max} = \frac{DV_{C1}}{L_M f_S} = \frac{DV_{in}}{L_M f_S\left[1 - (1 + n_{31})\,D\right]}. \tag{57}$$

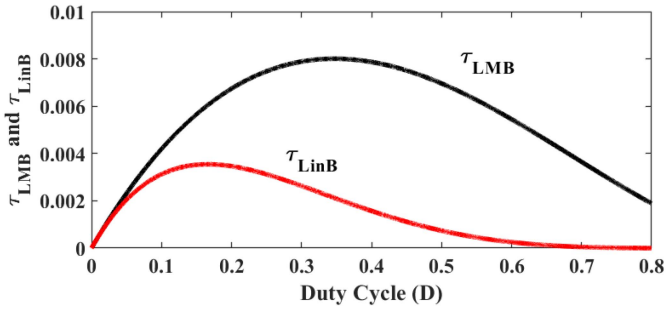

Fig. 6. BCM condition of the proposed converter.

By substituting (57) in (56) and considering $I_O = V_O/R_O$, $M_{\text{DCM}} = V_O/V_{in}$, and $\tau_{LM} = L_M f_S/R_O$, D_L is obtained as

$$D_L = \frac{2\,(2 + n_{21} + n_{31})\left[1 - (1 + n_{31})\,D\right]}{D\,(1 - D)} \tau_{LM} M_{\text{DCM}} - D. \tag{58}$$

By applying (58) into (55), the voltage gain of the proposed converter at DCM can be expressed as (59) shown at the bottom of this page, where

$$\alpha_1 = \frac{2\,(2 + n_{21} + n_{31})\left[1 - (1 + n_{31})\,D\right]}{D\,(1 - D)}$$

$$\alpha_2 = 2 + n_{21} + n_{31};\ \alpha_3 = 1 - (1 + n_{31})\,D.$$

C. BCM Operation

At BCM, the following relationship can be written:

$$I_{LM} = \frac{2 + n_{21} + n_{31}}{1 - D} I_O = \frac{1}{2} I_{LM,\max}. \tag{60}$$

From (57) and (60), the boundary value of τ_{LM} (τ_{LMB}) is obtained as

$$\tau_{LMB} = \frac{L_{MB} f_S}{R_O} = \frac{D(1 - D)^2}{2\,(2 + n_{21} + n_{31})\left[2 + (2 - D)n_{21} + n_{31}\right]} \tag{61}$$

where L_{MB} is the boundary value of L_M. Similarly, for inductor L_{in}, we have

$$\tau_{LinB} = \frac{L_{inB} f_S}{R_O} = \frac{D\,(1 - D)\,(1 + n_{31})}{2{M_{CCM}}^2\left[1 - (1 + n_{31})\,D\right]} \tag{62}$$

where L_{inB} is the boundary value of L_{in}.

Fig. 6 shows the boundary curves for the magnetizing inductor and input inductor considering $n_{21} = 0.5$ and $n_{31} = 0.25$. It can be seen that at a given power L_{inB} is much lower than L_{inB} and as a result, L_{MB} determines the converter to work in CCM or DCM.

$$M_{\text{DCM}} = \frac{\alpha_1\alpha_2\tau_{LM} + D\alpha_3 + \alpha_1 n_{31}\tau_{LM} + \sqrt{\left(\alpha_1\alpha_2\tau_{LM} + D\alpha_3 + \alpha_1 n_{31}\tau_{LM}\right)^2 - 4\alpha_1\alpha_3\tau_{LM}n_{31}D}}{2\left(\alpha_1\alpha_2\tau_{LM} + D\alpha_3 + \alpha_1 n_{31}\tau_{LM}\right)}. \tag{59}$$

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH OTHER COUNTERPARTS

Converter Topology	No. of Components S/D/C/CI+L/T	Voltage Gain	L.I.C.R	Voltage Stress on Main Switch	Maximum Voltage Stress on Diodes	M.S.S	D.R.R	C.G
Quadratic Topologies								
[10]	1/7/5/0 +3/16	$\frac{4}{(1-D)^2}$	No	$\frac{V_o}{2}$	$\frac{V_o}{2}$	-	High	Yes
[17]	1/5/4/1^{2w} +1/12	$\frac{2+n}{(1-D)^2}$	Yes	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	-	High	Yes
[19]	1/6/5/1^{2w} +1/14	$\frac{2+n(2-D)}{(1-D)^2}$	Yes	$\frac{V_o}{2+n(2-D)}$	$\frac{(1+n)V_o}{2+n(2-D)}$	-	High	Yes
[22]	3/1/2/2^{2w} +0/10	$\frac{(2-D)(n_2+n_3(1-D))+(1-D)}{(1-D)^2}$	No	$\frac{DV_o}{(2-D)(n_2+n_3(1-D))+(1-D)}$	$\frac{(n_3+n_2(1-D))V_o}{(2-D)(n_2+n_3(1-D))+(1-D)}$	ZVS	Very Low	Yes
[24]	1/5/4/1^{3w} +1/12	$\frac{1+n_{21}+n_{31}D}{(1-D)^2}$	Yes	$\frac{V_o}{1+n_{21}+n_{31}D}$	$\frac{(1+n_2)V_o}{1+n_{21}+n_{31}D}$	-	High	Yes
[25]	1/5/4/1^{3w}+1/12	$\frac{n_{21}+n_{31}(1-D)+2-D}{(1-D)^2}$	Yes	$\frac{V_o}{n_{21}+n_{31}(1-D)+2-D}$	$\frac{(n_{21}+2-D)V_o}{n_{21}+n_{31}(1-D)+2-D}$	-	High	Yes
[27]	2/4/5/1^{4w} +1/13	$\frac{1+n_{21}+n_{31}}{(1-D)^2}$	Yes	$\frac{V_o}{1+n_{21}+n_{31}}$	$\frac{(n_{21}+n_{31})V_o}{1+n_{21}+n_{31}}$	ZVZCS	Very Low	Yes
[28]	1/4/3/1^{3w} +1/10	$\frac{(2+n_{21}+n_{31})-(n_{31}+1)D}{(1-D)^2}$	Yes	$\frac{V_o}{(2+n_{21}+n_{31})-(n_{31}+1)D}$	$\frac{(1+n_{21}+n_{31})V_o}{(2+n_{21}+n_{31})-(n_{31}+1)D}$	-	High	No
[29]	1/6/5/1^{3w}+1/14	$\frac{2+n_{21}+n_{31}-n_{31}D}{(1-D)^2}$	Yes	$\frac{V_o}{2+n_{21}+n_{31}-n_{31}D}$	$\frac{(1+n_{21}+n_{31})V_o}{2+n_{21}+n_{31}-n_{31}D}$	-	High	No
Non-Quadratic Topologies								
[11]	1/5/6/1^{3W} +1/14	$\frac{2+D+n_{31}(2-D)-n_{21}}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+D+n_{31}(2-D)-n_{21}}$	$\frac{(1+n_{31})V_o}{2+D+n_{31}(2-D)-n_{21}}$	ZVS	-	Yes
[33]	2/5/5/1^{3w} +1/14	$\frac{1+(3-2D)n_{21}+(4-2D)n_{31}}{[1-n_{21}].(1-2D)}$	Yes	$\frac{(1-n_{21})V_o}{1+(3-2D)n_{21}+(4-2D)n_{31}}$	$\frac{(2+2n_{31})V_o}{1+(3-2D)n_{21}+(4-2D)n_{31}}$	-	-	Yes
[35]	1/4/5/1^{3W} +1/12	$\frac{1+n_{21}+n_{31}+D}{n_{21}(1-D)}$	Yes	$\frac{n_{21}V_o}{1+n_{21}+n_{31}+D}$	$\frac{(1+n_{31})V_o}{1+n_{21}+n_{31}+D}$	ZCS	-	Yes
[36]	1/3/4/1^{3W} +1/10	$\frac{2+n_{21}-n_{31}}{(1-n_{31})(1-D)}$	Yes	$\frac{(1-n_{31})V_o}{2+n_{21}-n_{31}}$	$\frac{(1+n_{21})(1-n_{31})V_o}{2+n_{21}-n_{31}}$	ZCS	-	No
[37]	1/6/7/1^{2W} +1/16	$\frac{3+n(3-D)}{(1-D)}$	Yes	$\frac{V_o}{3+n(3-D)}$	$\frac{(1+n)V_o}{3+n(3-D)}$	ZCS	-	Yes
[38]	1/4/5/1^{3W} +1/12	$\frac{2+n_{21}.(2-D)-n_{31}(1+D)}{(1-n_{31})(1-D)}$	Yes	$\frac{(1-n_{31})V_o}{2+n_{21}.(2-D)-n_{31}(1+D)}$	$\frac{(1+n_{21}-n_{31})V_o}{2+n_{21}.(2-D)-n_{31}(1+D)}$	ZCS+QR	-	Yes
Semi-quadratic								
Proposed Converter	1/6/5/1^{3w} +1/14	$\frac{2+n_{21}(2-D)+n_{31}}{[1-D(1+n_{31})].(1-D)}$	Yes	$\frac{V_o}{2+n_{21}(2-D)+n_{31}}$	$\frac{1+n_{21}+n_{31}}{2+n_{21}(2-D)+n_{31}}V_o$	ZCS	Very Low	Yes

S = Switch, **D** = Diode, **C** = Capacitor, **CI** = Coupled-Inductor, **L** = Inductor, **T** = Total Device Count, **L.I.C.R** =Low Input Current Ripple, **M.S.S**=Soft Switching for Main Power Switch, **D.R.R**= Reverse Recovery for Input Diodes, **C.G**=Common Ground.

IV. PERFORMANCE COMPARISON

The advantages of the proposed converter are demonstrated by a comprehensive performance comparison with different quadratic based and nonquadratic topologies presented in Table I. Some results are presented graphically in Fig. 7. The turns' ratios of the three-winding CIs are considered to be $n_{21} = 0.5$ and $n_{31} = 0.25$. In order to have a fair comparison, for the converters with two-winding CIs, $n = 0.75$ is selected.

To clearly illustrate the impact of the total number of the components on the voltage gain, Fig. 7(a) shows the voltage conversion ratio per total count of the components. It is seen that the proposed converter and [33], have better performance than all other competitors. However, it should be fairly stated that topologies like [22], have wider range of duty cycle rather that trans-inverse topologies like the proposed converter. Moreover, according to Fig. 7(b) and (c), the normalized voltage stress across MOSFET and the normalized maximum imposed voltage across the diode in the proposed converter is in the middle rank in comparison with other topologies. Therefore, low voltage stresses switches can be implemented to reduce conduction losses and to improve performance operation of the converter.

An important issue in quadratic dc–dc step-up converters is the power losses of switch S and the input diodes D_1 and D_2 passing high input current. In the proposed converter, due to the third winding with n_3 turns included in the power circuit of the converter, according to detailed operating principle presented in Section II, all of the diodes as well as the power switch are operated with ZCS performance, which alleviates the reverse recovery problem. The reverse recovery of the input diodes and the soft switching of the MOSFETS are compared in Table I. It is clear that between the mentioned quadratic-based topologies and the proposed semiquadratic proposed converter, only in the proposed converter and the ones introduced in [22] and [27], soft switching performance of the input diodes are provided. However, the nonquadratic based converters sorted in the Table I usually do not have any diode at the high current side and the

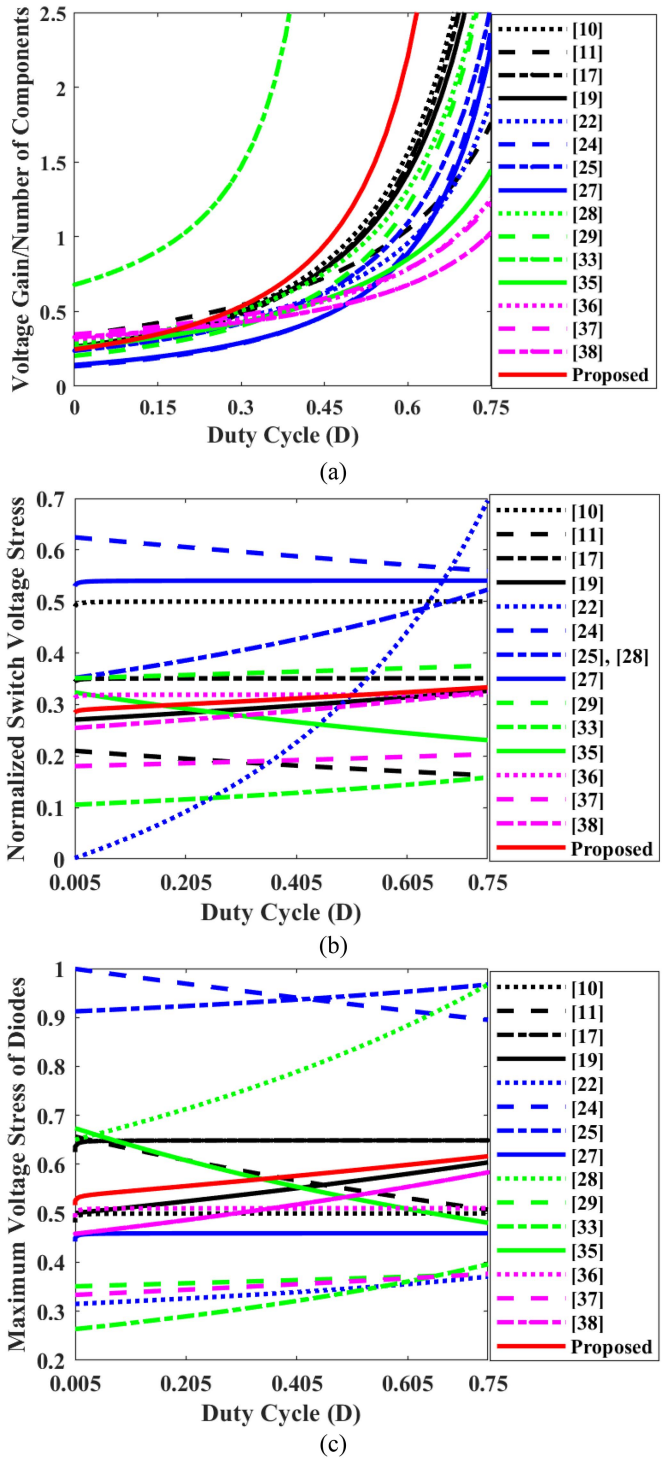

Fig. 7. Performance comparison of the proposed converter. (a) Voltage gain per total number of the components. (b) Normalized voltages stress across switch. (c) Normalized maximum voltage stress across the diodes.

diodes pass low currents. The diodes are operating with ZCS performance due to the presence of the leakage inductance. As a result, the mentioned issue is not a challenge in these kinds of converters.

Another comparison has been made between the efficiency of the competitors and the result are summarized in Table II. It is seen that the proposed converter has relatively a medium cost in the given costs of the converters.

The reported efficiencies of the competitors in Table I along with the operating conditions such as input/output voltages, switching frequency, and output power are provided in Table III. It is seen that the efficiency of the proposed converter is acceptable in comparison with its counterparts.

As a result, the proposed trans-inverse soft switching semi-quadratic high step-up dc–dc converter with low input current ripple and low voltage stresses could be considered as a suitable candidate for renewable energy systems.

V. Design Guidelines

A. Selection of Input Inductor L_{in}

For RES such as PV and FC, low input current ripple of the converter is an important issue. As a result, the input inductor L_{in} is designed to ensure the input current ripple to be limited within the predetermined range

$$L_{in} = \frac{D\,(1-D)\,(1+n_{31})}{\Delta i_{Lin} f_S\,[1-(1+n_{31})\,D]} V_{in}. \tag{63}$$

Considering 95% conversion efficiency of the proposed converter, the input current is obtained to be $200\,\mathrm{W}/(25\,\mathrm{V}\times 0.95) = 8.42\,\mathrm{A}$. If the input current ripple is about 0.25% of the average input current, by substituting of the given specifications of the experimental prototype from Table IV in (63), the value of the input inductor L_{in} is derived 211 μH. It is worth to mention that the fabricated input inductor has the inductance of 210 μH that is very close to the designed value.

B. Selection of Turns Ratio and Magnetizing Inductor of the CI

The boundary magnetizing inductor L_{MB} is designed from (61) in such a way that the proposed converter operates in CCM at about 25–35% of full load. The mentioned consideration results the value of 290 μH for L_{MB}. The value of the magnetizing inductor of the fabricated TWCI is about 300 μH.

From (17), the value of n_{21} is extracted as follows:

$$n_{21} = \frac{\frac{V_O}{V_{in}}\,[1-(1+n_{31})\,D]\,(1-D) - 2 - n_{31}}{2-D}. \tag{64}$$

Due to the trans-inverse operation of the proposed converter in which n_{31} appears at the denominator of the voltage gain expression as a coefficient of the duty cycle, by selecting of a low value of $n_{31} = 0.25$ high voltage gain could be ensured. It is worth to mention that increasing of n_{31} will increases the input current ripple according to (58), which is not reasonable. As a result, from the given input–output voltages of the experimental prototype in Table III, $n_{21} = 0.4$ is obtained. However, the leakage inductor and the parasitic elements of the components affect the voltage gain according to discussions in Sections III-A and VI. As a result, n_{31} is chosen 0.5.

C. Selection of the Semiconductors

The switch S and the diodes are selected based on the voltage and current stresses obtained in Section III, (23)–(44) that are

TABLE II
COST COMPARISON OF THE PROPOSED CONVERTER WITH OTHER COUNTERPARTS IN TABLE I

Conv.	Prop.	[10]	[11]	[17]	[19]	[22]	[24]	[25]	[27]	[28]	[29]	[33]	[35]	[36]	[37]	[38]
Cost ($)	25.36	27.93	23.76	25.46	25.78	44.27	27.35	25.75	34.56	25	27.68	31.59	20.35	24.6	22.44	24.95

TABLE III
COMPARISON OF OUTPUT/INPUT VOLTAGES, SWITCHING FREQUENCY, FULL LOAD POWER, AND EFFICIENCY

References	Proposed	[11]	[17]	[19]	[22]	[24]	[25]	[27]	[28]	[29]	[33]	[35]	[36]	[37]	[38]
V_O/V_{in} (V)	25/400	25/400	10/100	30/200	60/400	30/770	40/312	48/380	20/240	30/400	25/380	48/400	24/200	30/380	25/400
f_S (kHz)	50	60	108	50	100	50	30	100	50	100	50	50	50	50	55
P_{out} (W)	200	400	45	160	200	400	200	200	240	300	200	200	150	200	200
η(%)	95.1	93.5	92.1	94.7	96.0	94.0	95.3	96	94.4	94.7	95.2	94.1	95.3	94.2	94.4

TABLE IV
SPECIFICATIONS OF THE PROTOTYPE

Output Power (P_O)	200 W
Input Voltage (V_{in})	25 V
Output Voltage (V_o)	400 V
Switching Frequency (f_S)/Nominal D	50 kHz-50%
Capacitor C_1-*MKF*	2×15 μF / 100 V
Capacitor C_C-*MPX*	2.2 μF / 250 V
Capacitor C_2-*MPX*	2×8.2 μF / 250 V
Capacitor C_3- *Aluminum Electrolytic*	47 μF / 100 V
Capacitor C_o- *Aluminum Electrolytic*	220 μF / 450 V
Power Switch S	IPP076N15N5/ $R_{DS(on)}$=7.6 mΩ
Input Inductor L_{in} / Core	210 μH / EE42/21/15
Magnetizing Inductor of the CI (L_M)	300 μH
Turns Ratios of the TWCI / Core	(1:0.5:0.25) / EE42/21/20
Diodes D_3, D_O	MUR440
Diodes D_4	SR410
Diode D_C	MBR820
Diodes D_1 and D_2	MBR10100

given by

$$\begin{aligned} V_S &= V_{\rm dc} = 127\,{\rm V}; V_{D1} = V_{D2} = 80\,{\rm V}; V_{D3} \\ &= V_{DO} = 235\,{\rm V}; V_{D4} = 77\,{\rm V} \\ I_{S,{\rm rms}} &= 10.7\,{\rm A}; I_{{\rm dc},{\rm rms}} = 1.1\,{\rm A}; I_{D1,{\rm rms}} = 5.7\,{\rm A}; \\ I_{D2,{\rm rms}} &= 5.6\,{\rm A}; \\ I_{D3,{\rm rms}} &= 0.87\,{\rm A}; I_{D4,{\rm rms}} = 0.8\,{\rm A}; I_{DO,{\rm rms}} = 0.7\,{\rm A}. \end{aligned}$$

Accordingly, IPP076N15N5 and MBR820 are chosen for MOSFET and clamp diode; MBR10100 is selected for diodes D_1 and D_2; MUR440 is implemented for D_3 and D_O; and SR40 is utilized for D_4.

D. Selection of the Capacitors

The capacitors are chosen based on limiting their voltage ripple ΔV_C. Therefore

$$C_1 \geq \frac{[M_{\rm CCM}(1-D)-2]\,P_O}{V_O \Delta V_{C1} f_S} \tag{65}$$

$$C_{2,3,C} \geq \frac{P_O}{V_O \Delta V_{C2,3,C} f_S} \tag{66}$$

$$C_O \geq \frac{DP_O}{V_O \Delta V_{CO} f_S}. \tag{67}$$

From the steady-state analysis in Section III, the voltages of the capacitors are obtained to be

$$V_{CC} = 132\,{\rm V}; V_{C1} = 66\,{\rm V}; V_{C2} = 188V; V_{C3} = 39.6\,{\rm V}.$$

Assuming 3% voltage ripple for the capacitors the criterion of the capacitors' selection is derived as

$$\begin{aligned} C_1 \geq 30\,\mu{\rm F}; C_2 \geq 1.8\,\mu{\rm F}; C_3 \geq 8.4\,\mu{\rm F}; C_C \geq 2.25\,\mu{\rm F}; C_O \\ \geq 0.4\,\mu{\rm F}. \end{aligned}$$

Finally, considering the rated voltage of each capacitor, the following capacitors are implemented:

$$\begin{aligned} C_1 &= MKS - 2 \times 15\,\mu{\rm F}/100\,V; C_2 \\ &= {\rm MEF} - 2 \times 8.2\,\mu{\rm F}/250\,V \\ C_3 &= {\rm Aluminum\ Electrolitic} - 47\,\mu{\rm F}/100\,V \\ C_C &= 2.2\mu{\rm F}/250V; C_O = {\rm Aluminum\ Electrolitic} \\ &\quad - 220\mu{\rm F}/400V. \end{aligned}$$

The passing current of the output capacitor is low and, therefore, available electrolytic capacitor has been implemented.

VI. EXPERIMENTAL VERIFICATIONS

To illustrate the effectiveness of the proposed converter a 25–400 V 200 W prototype has been developed and tested in the laboratory. The developed control circuit along with the fabricated prototype is presented in Fig. 8. A simple PI controller has been used to control the proposed converter. The dynamic performance of the converter can be adjusted by tuning of the resistor and the capacitor connected to TL082. The components specifications are provided in Table IV.

Fig. 9 shows the experimental result of the V_{GS}, V_O, i_{Lin}, and i_{LK}. The high output voltage of 400 V is obtained with small duty cycle of about 0.5. The input current ripple is about 1.6 A.

Fig. 10 shows the voltage and current of the power switch *S*. The voltage stress of the switch is about 125 V, which is much smaller than the output voltage. Moreover, the MOSFET is turned ON with ZCS, which minimizes the switching losses.

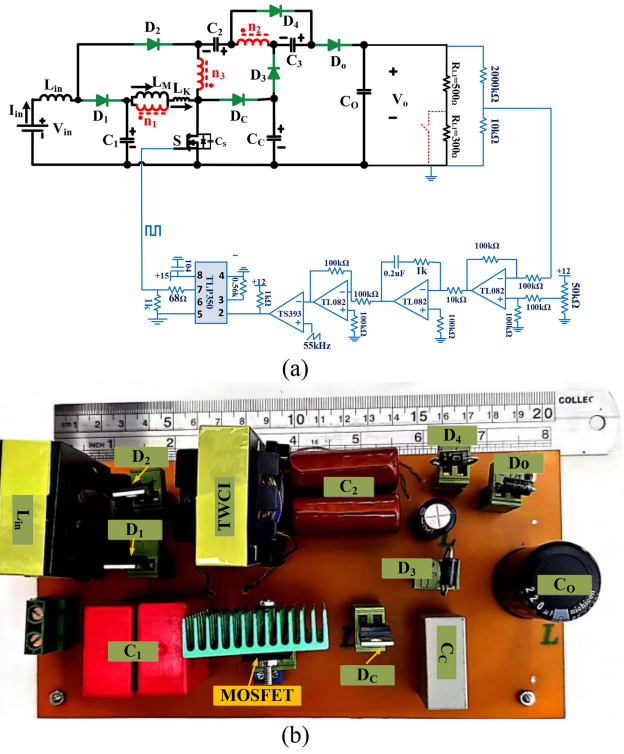

Fig. 8. Photographs of the (a) developed control and (b) fabricated prototype.

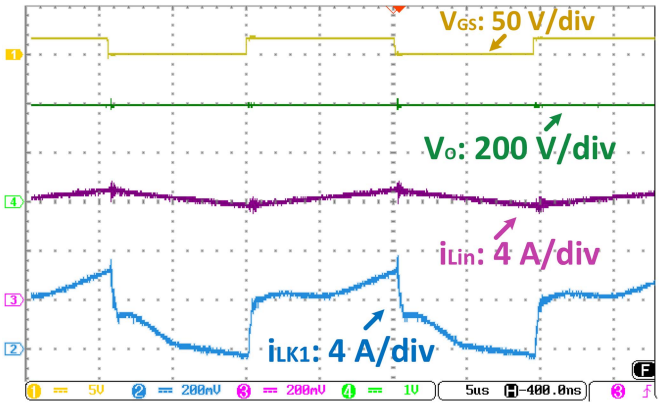

Fig. 9. Experimental result of V_{GS}, V_O, i_{Lin}, and i_{LK}.

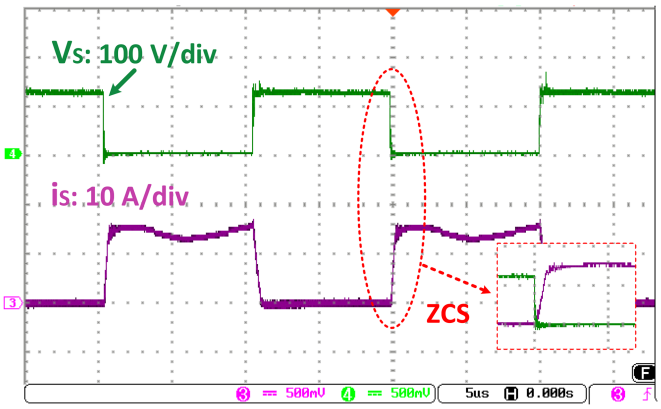

Fig. 10. Experimental results of the voltage and current of the power switch *S*.

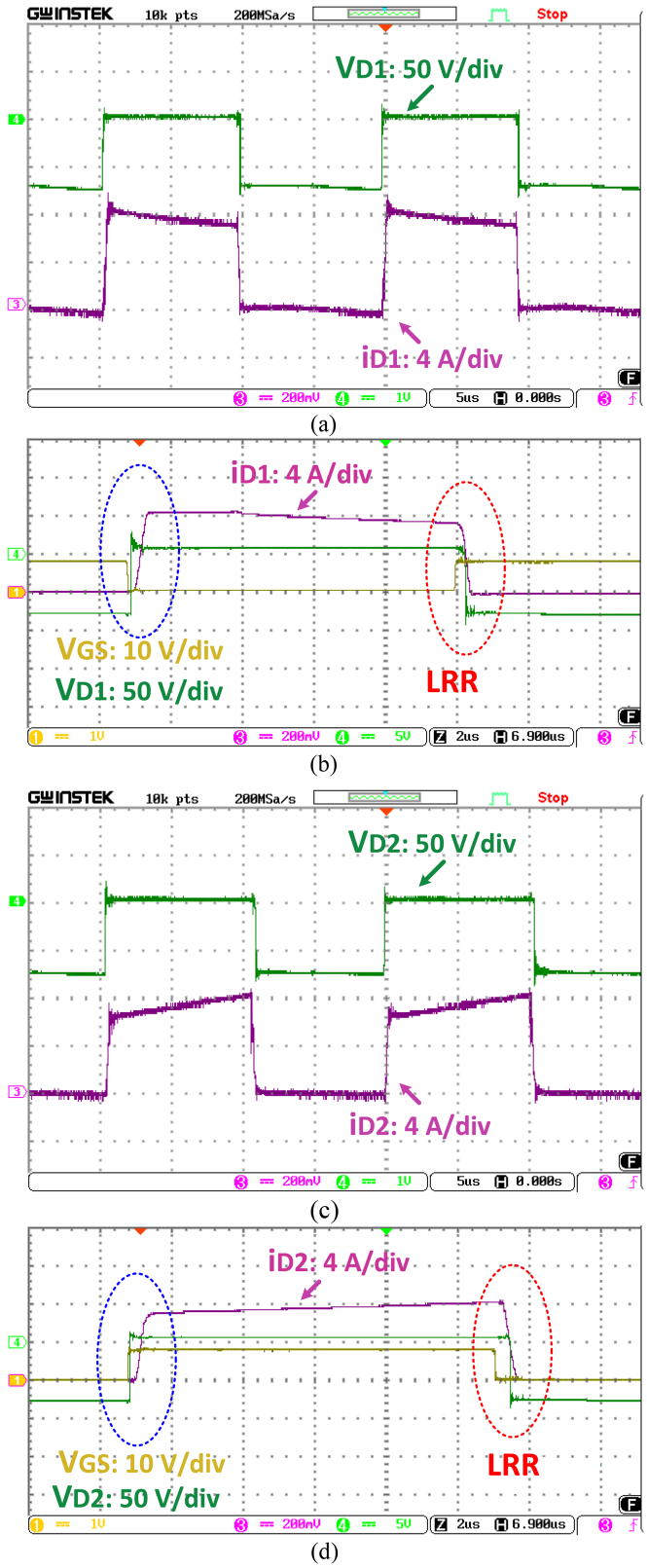

Fig. 11. Experimental results of (a) V_{D1}, i_{D1}, (b) Zoom view of V_{D1}, i_{D1}, (c) V_{D2}, i_{D2}, and (d) Zoom view of V_{D2}, i_{D2}.

Fig. 11. shows the experimental result of the voltage and currents of input diodes D_1 and D_2. The voltage stresses of the diodes are about $V_{D1} = V_{D1} \cong 75$ V that are consistent with the carried steady-state analysis. Moreover, Fig. 9(b) and (d) shows the zoomed view of the waveforms, which clearly demonstrates the currents are softly passing from zero during ON and OFF states without any ringing and reverse recovery phenomenon.

Fig. 12 shows the experimental results of the voltage and current of the diodes D_3, D_4, D_C, and D_O. The voltages stresses across these diodes are about $V_{D3} \cong 225$ V, $V_{D4} \cong 75$ V, $V_{\rm dc} \cong 125$ V, and $V_{DO} \cong 230$ V. Meanwhile, the currents cross from zero during ON and OFF softly and there are no ringing and reverse recovery.

Fig. 13 shows the dynamic response of the proposed converter versus load variations. It is seen that the output voltage is well regulated around the 400 V while the output load resistance fluctuates between 500 Ω and 800 Ω. The responses times of the proposed converter with load fluctuation from 800 to 500 Ω and vice versa are about 20 ms and 40 ms, respectively.

Fig. 14. shows the measured efficiency of the proposed converter along with some other converter operating in relatively similar conditions. The maximum efficiency is about 95.8% at around 120 W up to 140 W output power and the full load efficiency is about 95.1%. Moreover, it is seen that in comparison with the counterparts, the proposed converter achieves satisfying conversion efficiencies from light load to full load.

The power dissipations of the proposed converter is related to the ON-state resistance ($R_{S-\rm ON}$) of the MOSFET, turn-OFF switching losses of the MOSFET, forward voltages of the diode (V_{FD}), ON-state resistance of the diodes (R_D), winding resistance of the input inductor (R_{Lin}), winding resistances of the CI (R_{n1}, R_{n2}, R_{n3}), core losses of the magnetic devices ($P_{\rm Cores}$), and the equivalent series resistance of the capacitors. To calculate the losses of each component, the carried average and rms analysis in Section III, as (29)–(52) are numerically evaluated at first and then the results are utilized in the following analysis. The parasitic elements of the components are listed as follows:

$R_{S-\rm ON} = 6.7\,\text{m}\Omega$, $R_D = 10\,\text{m}\Omega$, $V_{FD1} = V_{FD2} = 0.5$ V, $V_{FD3} = 0.58$ V, $V_{FD4} = V_{FDC} = 0.52$ V, $V_{FDO} = 0.63$ V, $R_{C1} = 2.6\,\text{m}\Omega$, $R_{C2} = 4.45\,\text{m}\Omega$, $R_{C3} = 54\,\text{m}\Omega$, $R_{CC} = 7.7\,\text{m}\Omega$, $R_{Co} = 132.5\,\text{m}\Omega$, $R_{Lin} = 14\,\text{m}\Omega$, $R_{n1} = 12\,\text{m}\Omega$, $R_{n2} = 7\,\text{m}\Omega$, $R_{n3} = 8\,\text{m}\Omega$, $P_{\rm Cores} = 0.6$ W, $C_{OSS} = 900$ pF.

The power MOSFETS is turned ON with ZCS performance and, therefore, the turn ON switching losses is zero. The associated power dissipation of the power switch is calculated as

$$P_{\rm MOSFET} = R_{S-\rm ON}{I_{S,\rm rms}}^2 + \frac{1}{2}V_S i_S(t_5) f_S t_{\rm OFF} + \frac{f_S}{2}C_{OSS}{V_S}^2 = 1.25\,\text{W}. \quad (68)$$

The power losses of the diodes, capacitors, and magnetic devices are obtained by

$$P_{\rm Diodes} = \sum \left(R_D {I_{D,\rm rms}}^2 + V_{FD} I_{D,Ave}\right) = 5.24\,\text{W} \quad (69)$$

$$P_{\rm Capacitors} = \sum R_C {I_{C,\rm rms}}^2 = 0.24\,\text{W} \quad (70)$$

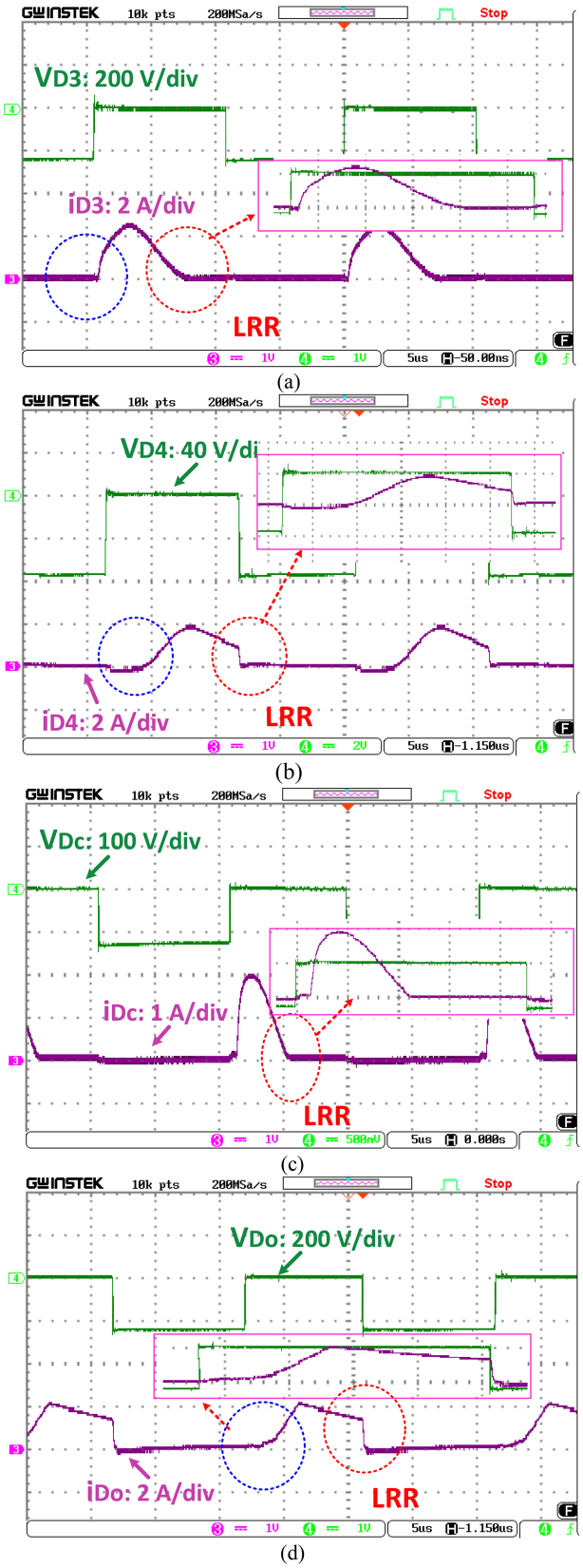

Fig. 12. Experimental results of (a) V_{D3}, i_{D3}, (b) V_{D4}, i_{D4}, (c) $V_{\rm dc}, i_{\rm dc}$, and (d) V_{DO}, i_{DO}.

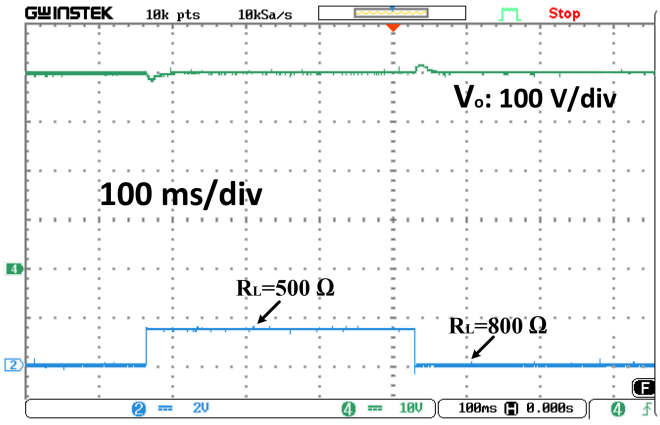

Fig. 13. Dynamic response of the proposed converter.

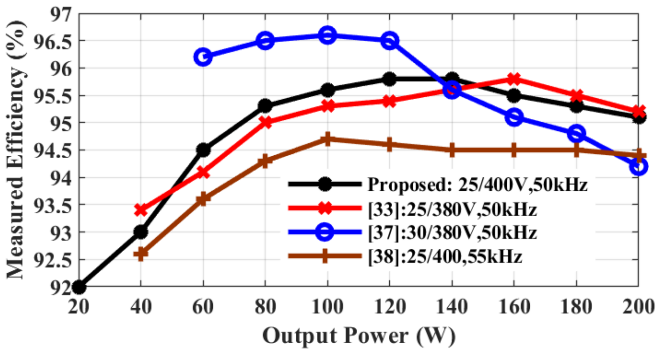

Fig. 14. Measured efficiency of the proposed converter.

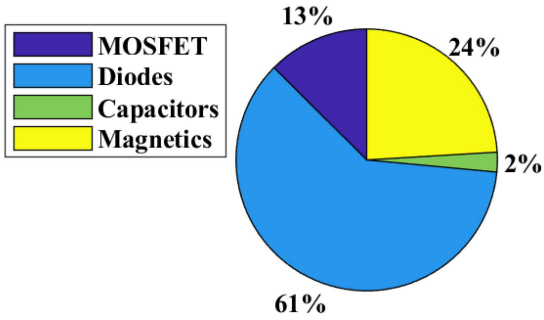

Fig. 15. Losses break-down of the proposed converter at full load.

$$P_{\text{Magnetics}} = R_{Lin} {I_{in,\text{RMS}}}^2 + \sum_{j=1}^{3} R_{nj} {I_{nj,\text{rms}}}^2 + \rho_C V_C K_C f^{\alpha} \Delta B^{\beta} = 2.32\,\text{W} \tag{71}$$

where ρ_C, α, and β are constant and are dependent on the core material and ΔB is the swing of the magnetic flux density. Fig. 15 shows the losses break-down of the proposed converter at full load. The total losses at full load is about 9.04 W and the theoretical conversion efficiency is about 95.7%.

VII. Conclusion

A high step-up trans-inverse semiquadratic dc–dc converter has been proposed in this article. The voltage gain is increased by the three degrees of freedom that are duty cycle and the turns' ratios of the three-winding CI n_{21} and n_{31}. The MOSFET is operating with ZCS performance, which minimizes the switching losses. Moreover, the falling current rates of the diodes are controlled by the leakage inductances, which diminish the reverse recovery problem. Due to the specific structure of the proposed converter, the passing currents of the diodes at the ON and OFF instants are zero that is missed in similar converters. Through comprehensive performance comparison, the superiority of the proposed converter over its counterparts in the terms of voltage gain and voltage stresses across the semiconductor have been illustrated. Moreover, the input current has very low content that is a necessity for RES such as PV and FC. Finally, a 200 W 25–400 V laboratory prototype has been developed to prove the effectiveness of the proposed converter.

Appendix

When switch S is ON, the following equations are valid:

$$V_{C1} = V_{LK} + V_{LM} \tag{A.1}$$

$$\begin{aligned} V_{LK} &= L_K \frac{di_{LK}}{dt} = L_K \frac{d}{dt}(i_{LM} + i_{n1}) \\ &= \frac{L_K}{L_M}\left(L_M \frac{di_{LM}}{dt}\right) + L_K \frac{di_{n1}}{dt} \\ &= \frac{L_K}{L_M} V_{LM} + L_K \frac{di_{n1}}{dt}. \end{aligned} \tag{A.2}$$

By substituting of (A.2) in to (A.1), we have

$$V_{C1}\left(\frac{L_M}{L_M + L_K}\right) = V_{LM} + L_K L_M \frac{di_{n1}}{dt}. \tag{A.3}$$

The second term in the right hand of (A.3) is negligible due to the fact that it consists of the multiplication of L_K and L_M (pH). As a result

$$V_{LM} \simeq V_{C1}\left(\frac{L_M}{L_M + L_K}\right) = K V_{C1}. \tag{A.4}$$

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