A Novel Modulation Method to Decouple Output Power and Suppress Current Zero-Crossing Distortion for Vienna Rectifiers in Bipolar Output Mode

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***Abstract*—In practical applications, Vienna rectifier often operates in a bipolar output mode to improve efficiency and reduce cost. In this case, the output voltage and power of the upper and lower dc buses are no longer equal, and the vector synthesis becomes very complex. In this article, the analysis is conducted from the perspective of the carrier, and the zero-sequence voltage (ZSV) is injected to decouple the output power of the upper and lower dc buses and control the neutral point voltage, which simplified the calculation. Based on the constraints of output level and maximum limit of modulation voltage, the constraints of ZSV are provided. Then, the maximum output power of the upper and lower dc buses relative to the entire dc bus under different operating conditions is calculated, which can provide reference for parameter design. In addition, the current zero-crossing distortion (CZCD) for Vienna rectifier in bipolar output mode is analyzed, and a novel method for suppressing CZCD is proposed and the modulation voltage are directly provided. Finally, an experimental platform is built to verify the feasibility and superiority of the proposed method.**

***Index Terms*—Bipolar output, current zero-crossing distortion (CZCD), output power decoupling, unbalanced dc bus, Vienna rectifier.**

I. Introduction

VIENNA rectifier was proposed in [1] in 1996. As a three-level rectifier, Vienna rectifiers have the advantages of high efficiency and low current harmonics [2], which have been widely used in situations where energy flows unidirectionally, such as the front-end of electric vehicle (EV) charging [3], [4], wind power generation, and the low-voltage dc microgrid [5], [6].

The characteristics of Vienna rectifier determine that it can operate in unipolar or bipolar output modes, as shown in Fig. 1.

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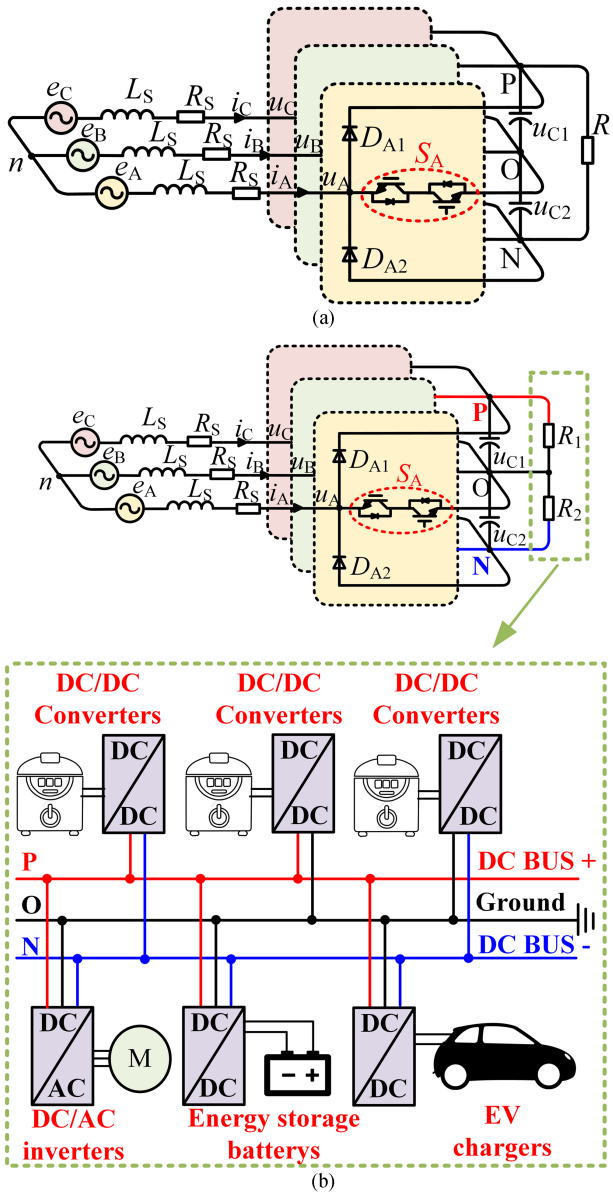

Fig. 1. Topology and output mode of Vienna rectifiers. (a) Unipolar output mode. (b) Bipolar output mode.

Compared to unipolar output, bipolar output has more flexible output voltage levels, including two positive and negative polarity voltages, offering paramount flexibility and interface with various voltage-ranged loads [7], [8], [9]. In existing papers, there have been studies on three-level rectifiers in bipolar output mode. In [10], the limit of unbalanced operation was exceeded, and an additional NPC leg was used to control the capacitor voltage. To overcome the identified limitations without an additional NPC leg, an improved three-level neutral point clamped (3L-NPC) converter system with a zigzag transformer and a neutral line was proposed in [11]. However, the operating characteristics of Vienna rectifier are not exactly the same as those of three-level rectifiers. For Vienna rectifiers, there are more restrictions, and it is necessary to study the distribution relationship and active control method of the output power.

In fact, in existing studies on the unbalanced operation of the dc bus for Vienna rectifiers, it is generally assumed that the entire dc-bus voltage remains unchanged [12], [13], [14], that is, the module length of the large vector in the space vector diagram remains unchanged, but the reference voltage of the upper and lower dc buses is no longer equal. Generally, regulating the NP current and ZSV injection are used to control the NP voltage [15], [16], [17], [18], [19], [20]. In fact, these two methods are essentially the same in existing papers. For example, in [15], the reference value of NP current was calculated by the difference in voltage between the upper and lower dc busbars, and the ZSV that can generate the reference value of NP current was solved. In [16], based on the voltage difference between the upper and lower dc buses and the sign of the current, the vector that is more conducive to NP voltage balance was selected as the candidate vector in the redundant vector. A simple PI regulator was added in [17]. The inputs of the PI regulator are the sampled value and reference value of the difference between the upper and lower dc-bus voltages, respectively. The output of the PI regulator was the ZSV used to regulate the NP current. In [18], reactive current was injected to control the voltage and current of the rectifier to be in phase and eliminate CZCD. Then, the clamping method that generates NP current closest to the reference NP was selected among all available clamping methods. In [19], two ZSV injection methods based on CBPWM were proposed, which can improve the quality of input current and reduce switching losses. In [20], an optimized carrier-based discontinuous pulsewidth modulation strategy adopting self-adjusted redundant clamping modes was proposed to minimize the NP voltage fluctuation under balanced and unbalanced dc bus. In fact, there are two essential control objectives in existing papers. One is to control the entire dc-bus voltage through the voltage closed loop, and the other is to control the difference between the upper and lower dc-bus voltages by adjusting the NP current. The upper and lower dc buses are not treated as two independent control objectives, that is, there is still a coupling relationship between the upper and lower dc buses.

The sings of input voltage and current for Vienna rectifier must not be opposite, otherwise it will cause CZCD [21]. To suppress CZCD, a CBPWM method suitable for Vienna rectifier was proposed in [22], which injected compensation voltage into the three-phase input voltage to improve the quality of input current. But when the modulation index is high, it will cause over modulation, which will also cause current distortion. Discontinuous pulsewidth modulation was used to suppress CZCD and reduce switching losses [23], [24]. But the above methods are still ineffective when the modulation index is high. In [25], the angle between the input voltage and current in the rectifier side was calculated and the reactive power was injected to ensure that the current and voltage were in phase. In [17], the minimum reactive current that can eliminate CZCD was calculated. However, the power factor in the grid side and the conversion efficiency of the rectifier were reduced. When the Vienna rectifier operates in bipolar output mode, imbalance on the dc buses can easily lead to high modulation index of the upper or lower dc buses. Therefore, the suppression method of CZCD at high modulation index is more valuable when Vienna rectifier operates in bipolar output mode.

Based on the above analysis, a novel modulation method for Vienna rectifier in bipolar output mode is proposed in this article, and the main contributions are as follows.

1) There are also two control objectives for the proposed method. One is to control the power flowing into the upper dc bus to be equal to the demand for the equivalent load of the upper dc bus, and the other is to control the power flowing into the lower dc bus to be equal to the demand for the equivalent load of the lower dc bus. And the output decoupling is essentially achieved, which cannot be achieved through existing methods of adjusting NP current.
2) The maximum output power of the upper and lower dc buses relative to the entire dc bus for Vienna rectifiers under different operating conditions is calculated, which can provide reference for parameter design.
3) CZCD in bipolar output mode is analyzed, and a modulation method is proposed to suppress CZCD even under high modulation index conditions while ensuring the unit power factor in the grid side.

The rest of this article as follows. In Section II, the basic principle of Vienna rectifier is introduced. In Section III, the modulation method of Vienna rectifier is analyzed. In Section IV, the principle of instantaneous power exchange, the method to decouple output power and the impact of ZSV on the distribution relationship of output power are introduced, respectively. In Section V, the method of CZCD suppression and the implementation of proposed method are provided. In Section VI, three methods are compared in terms of current THDs and fluctuations on output voltage. Experimental results verify the feasibility and superiority of the method proposed in this article. Finally, Section VII concludes this article.

II. Basic Theory of Vienna Rectifiers

The topology of Vienna rectifier is shown in Fig. 1, where e_X (X = A, B, C) is the phase voltage of grid; i_X is the input phase current, and its positive direction is flowing into Vienna rectifiers. u_X is the input phase voltage of the rectifier; L_S and R_S are the inductance and resistance of grid-side filters, respectively. R, R_1, and R_2 are the equivalent resistances of the dc bus output.

D_{X1} and D_{X2} are freewheeling diodes. The upper and lower dc-bus voltages are u_{C1} and u_{C2}, and the dc-bus voltage is $u_{dc} = u_{C1}+u_{C2}$.

The switching function S_X ($X = $ A, B, C) represents the state of the switching devices of phase X. $S_X = 1$ means that the switches are on, whether the current is positive or negative, this phase is connected to neutral point (NP), and the state is defined as level 0. $S_X = 0$ means that the switches are OFF, if the current is positive, the phase is connected to the positive bus through D_{X1}, and the state is defined as level 1; if the current is negative, the phase is connected to the negative bus through D_{X2}, and the state is defined as level -1. It can be obtained that the sign of the output level cannot be opposite to the sign of the current, which constrains the operation state of Vienna rectifiers.

There two output modes for Vienna rectifier shown in Fig. 1. One mode is that there is only one output with an equivalent resistance of R on the dc bus, which is called the unipolar output mode, as shown in Fig. 1(a). The other is that the upper and lower capacitors of the dc bus are connected with equivalent resistors, R_1 and R_2, respectively. This mode is called the bipolar output mode, as shown in Fig. 1(b). In practical applications, the equivalent resistance corresponds to the instantaneous power output from the Vienna rectifier to the secondary circuit. The secondary circuit usually includes dc/dc converters, dc/ac inverters, energy storage batteries, and EV changers etc.

When the Vienna rectifier operates in unipolar output mode, the NP of the dc-bus capacitor is not connected to the load, and the output voltage and power of the entire dc-bus depend on the demand of R. Therefore, the reference output voltage and power of the upper and lower dc-buses are the same. When the Vienna rectifier operates in bipolar output mode, the NP of the dc-bus capacitor is connected to the load, and the reference output voltage and power of the upper and lower dc buses depend on the requirements of R_1 and R_2, which may be not the same. This means that the control and modulation methods of the upper and lower dc buses need to be further analyzed.

In order to simplify the analysis of the control and modulation methods for Vienna rectifier in bipolar output mode, the upper and lower modulation indexes m_{up} and m_{low} are defined as follows

$$\begin{cases} m_{up} = \frac{u_m}{u_{C1}} \\ m_{low} = \frac{u_m}{u_{C2}} \end{cases} \tag{1}$$

where u_m is the peak value of each phase modulation voltage, and $m_{up}, m_{low} \in [0, 1]$.

III. Modulation Method for Vienna Rectifiers

To simplify the analysis, u_A, u_B, and u_C are rearranged according to the instantaneous value, which can be expressed as

$$\begin{cases} u_{MAX} = \max(u_A, u_B, u_C) \\ u_{MID} = \mathrm{mid}(u_A, u_B, u_C) \\ u_{MIN} = \min(u_A, u_B, u_C) \end{cases} \tag{2}$$

where i_{MAX}, i_{MID}, and i_{MIN} correspond to the phase of u_{MAX}, u_{MID}, and u_{MIN}, respectively.

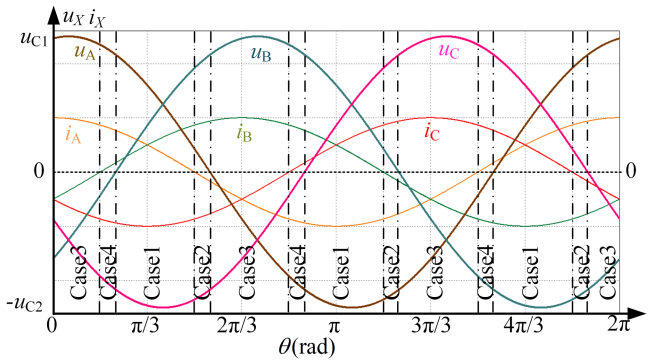

Fig. 2. Cases of ZSV in a fundamental period.

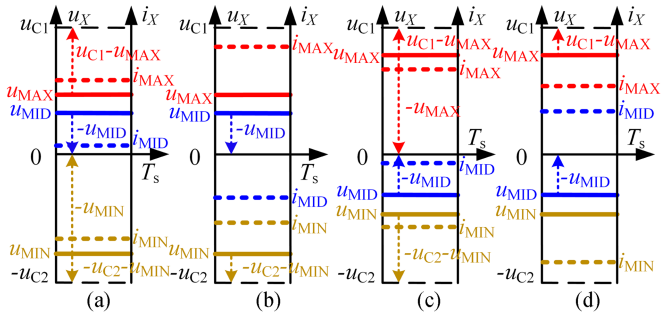

Fig. 3. Range of ZSV under different cases. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

ZSV injection is a commonly modulation method for Vienna rectifiers. The principles of ZSV injection are used to suppress CZCD and to avoid over modulation. Define the injected ZSV as u_{ZSV}. Define the modulation voltage after injecting u_{ZSV} as u'_X, and they are rearranged according to the instantaneous value as u'_{MAX}, u'_{MID}, and u'_{MIN}. The duty cycles corresponding to the levels 1, 0, and -1 are d'_{X1}, d'_{X0}, and d'_{X-1}, respectively, which can be expressed as

$$\begin{cases} u'_X \geq 0 : d'_{X1} = \frac{u'_X}{u_{C1}},\ \ d'_{X0} = 1 - \frac{u'_X}{u_{C1}},\ d'_{X-1} = 0 \\ u'_X < 0 : d'_{X1} = 0,\ \ d'_{X0} = 1 + \frac{u'_X}{u_{C2}},\ d'_{X-1} = -\frac{u'_X}{u_{C2}} \end{cases} . \tag{3}$$

The line-to-line voltage of the modulation voltage can be expressed as

$$\begin{cases} [d'_{A1}u_{C1} + d'_{A0}0 + \ d'_{A-1}(-u_{C2})] \\ \quad -[d'_{B1}u_{C1} + d'_{B0}0 + \ d'_{B-1}(-u_{C2})] = u_A - u_B \\ [d'_{B1}u_{C1} + d'_{B0}0 + \ d'_{B-1}(-u_{C2})] \\ \quad -[d'_{C1}u_{C1} + d'_{C0}0 + \ d'_{C-1}(-u_{C2})] = u_B - \ u_C \end{cases} . \tag{4}$$

This indicates that when the voltage of the upper and lower dc buses is unbalanced, the line-to-line voltage will not be changed by injecting u_{ZSV} to calculate u'_X.

As shown in Fig. 2, the injected ZSV in a fundamental period can be classified into four cases, denoted as case 1, case 2, case 3, and case 4, with their ranges shown in Fig. 3. The specific analysis is as follows.

1) Case 1: $u_{MID} > 0$ and $i_{MID} > 0$

In this case, the signs of u_X and i_X are the same. The constraints of ZSV are to avoid changing the sign of the modulation voltage and avoid over modulation for each phase. As shown in Fig. 3(a), u_{ZSV} satisfies with

$$\begin{aligned}&\max(-u_{\mathrm{MID}}, -u_{C2} - u_{\mathrm{MIN}}) \le u_{\mathrm{ZSV}}\\ &\le \min(u_{C1} - u_{\mathrm{MAX}}, -u_{\mathrm{MIN}}).\end{aligned} \tag{5}$$

2) Case 2: $u_{\mathrm{MID}} > 0$ and $i_{\mathrm{MID}} < 0$

In this case, the signs of u_{MID} and i_{MID} are opposite. There two constraints for ZSV. One is to avoid changing the sign and over modulation for the phase corresponding to u_{MAX} and u_{MIN}. The other is to suppress CZCD for the phase corresponding to u_{MID}. As shown in Fig. 3(b), u_{ZSV} satisfies with

$$-u_{C2} - u_{\mathrm{MIN}} \le u_{\mathrm{ZSV}} \le -u_{\mathrm{MID}}. \tag{6}$$

3) Case 3: $u_{\mathrm{MID}} < 0$ and $i_{\mathrm{MID}} < 0$

In this case, the constraints of ZSV are similar to those of case 1. As shown in Fig. 3(c), u_{ZSV} satisfies with

$$\begin{aligned}&\max(-u_{\mathrm{MAX}}, -u_{C2} - u_{\mathrm{MIN}}) \le u_{\mathrm{ZSV}}\\ &\le \min(u_{C1} - u_{\mathrm{MAX}}, -u_{\mathrm{MID}}).\end{aligned} \tag{7}$$

4) Case 4: $u_{\mathrm{MID}} < 0$ and $i_{\mathrm{MID}} > 0$

In this case, the constraints of ZSV are similar to those of case 2. As shown in Fig. 3(d), u_{ZSV} satisfies with

$$-u_{\mathrm{MID}} \le u_{\mathrm{ZSV}} \le u_{C1} - u_{\mathrm{MAX}}. \tag{8}$$

Based on the above analysis and the definition of modulation index, the maximum and minimum values of u_{ZSV} in a fundamental period are shown as follows:

$$u_{\mathrm{ZSV,MAX}} = \begin{cases}\min\left(\frac{U_m}{m_{\mathrm{up}}} - u_{\mathrm{MAX}}, -u_{\mathrm{MIN}}\right) & \mathrm{Case1}\\ \min\left(\frac{U_m}{m_{\mathrm{up}}} - u_{\mathrm{MAX}}, -u_{\mathrm{MID}}\right) & \mathrm{Case3}\\ -u_{\mathrm{MID}} & \mathrm{Case2\ or\ Case4}\end{cases} \tag{9}$$

$$u_{\mathrm{ZSV,MIN}} = \begin{cases}\max\left(-u_{\mathrm{MID}}, -\frac{U_m}{m_{\mathrm{low}}} - u_{\mathrm{MIN}}\right) & \mathrm{Case1}\\ \max\left(-u_{\mathrm{MAX}}, -\frac{U_m}{m_{\mathrm{low}}} - u_{\mathrm{MIN}}\right) & \mathrm{Case3}\\ -u_{\mathrm{MID}} & \mathrm{Case2\ or\ Case4}\end{cases}. \tag{10}$$

where $u_{\mathrm{ZSV,MAX}}$ and $u_{\mathrm{ZSV,MIN}}$ are the maximum and minimum values of u_{ZSV} within a fundamental period, respectively. It can be concluded that the range of u_{ZSV} depends on m_{up} and m_{low}. The waves of $u_{\mathrm{ZSV,MAX}}$ and $u_{\mathrm{ZSV,MIN}}$ within a fundamental period under different modulation indexes are shown in Fig. 4. Specifically, the situation where $u_{\mathrm{ZSV,MAX}} < u_{\mathrm{ZSV,MIN}}$ occurs in Fig. 4(d). It indicates that in this case, there is no suitable u_{ZSV} that can simultaneously suppress CZCD and avoid over modulation. This is consistent with the conclusion that the Vienna rectifier cannot avoid CZCD when the modulation index is very high [5].

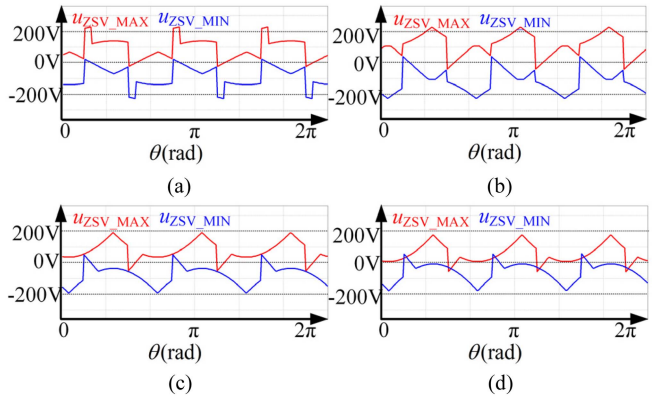

Fig. 4. Waves of $u_{\mathrm{ZSV,MAX}}$ and $u_{\mathrm{ZSV,MIN}}$ within a fundamental period under different modulation index. (a) $m_{\mathrm{up}} = m_{\mathrm{low}} = 0.4$. (b) $m_{\mathrm{up}} = m_{\mathrm{low}} = 0.7$. (c) $m_{\mathrm{up}} = m_{\mathrm{low}} = 0.9$. (d) $m_{\mathrm{up}} = m_{\mathrm{low}} = 0.98$.

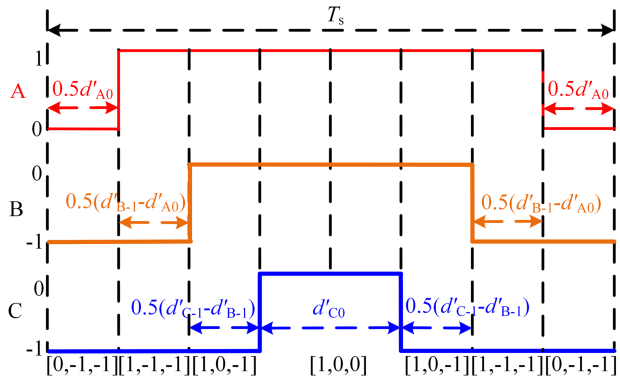

Fig. 5. Switching sequences after injection of u_{ZSV} in case 3.

IV. Output Power Exchange Relationship for Vienna Rectifiers in Bipolar Output Mode

A. Principle of Instantaneous Power Exchange

Taking case 3 shown in Fig. 2 as an example, the power exchange relationship for the Vienna rectifier in bipolar output mode will be analyzed as follows. In case3, $u_A > 0$, $u_B < 0$, $u_C < 0$ $i_A > 0$, $i_B < 0$, and $i_C < 0$. Assuming that the switching sequence after the injection of u_{ZSV} within a control cycle (i.e., T_s) is shown in Fig. 5. Phase A is modulated between level 1 and 0, while phases B and C are modulated between level -1 and 0. Within a control cycle, there are four different switching states, namely $[0, -1, -1]$, $[1, -1, -1]$, $[1, 0, -1]$, and $[1, 0, 0]$.

When the switching sequence is $[0, -1, -1]$, the current path is shown in Fig. 6(a). In this case, the lower dc bus is charged by phases B and C, and the charging power is as follows:

$$\begin{cases}p_{\mathrm{UP},[0,-1,-1]} = 0\\ p_{\mathrm{LOW},[0,-1,-1]} = -u_{C2}(i_B + i_C)d'_{A0}\end{cases} \tag{11}$$

where $p_{\mathrm{UP},[0,\ -1,\ -1]}$ and $p_{\mathrm{LOW},[0,\ -1,\ -1]}$ represent the power from the ac side to the upper and lower dc buses, respectively. When the switching sequences are $[1, -1, -1]$, $[1, 0, -1]$, and $[1, 0, 0]$, the current paths are shown in Fig. 6(b), (c) and (d), respectively. Similarly, the charging power to the dc buses is as

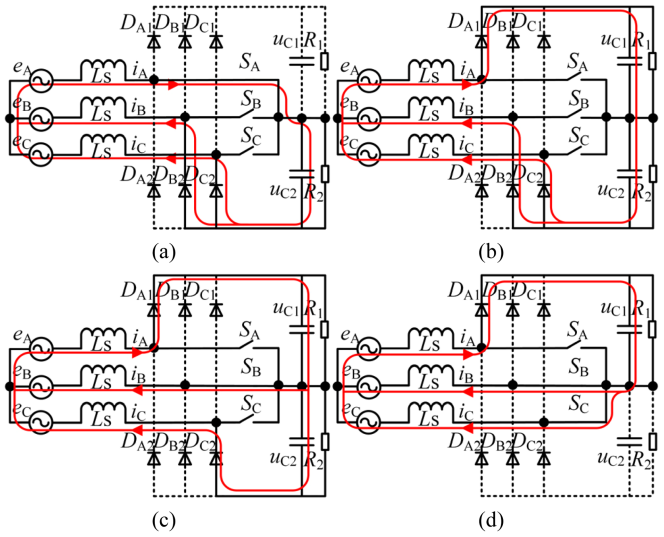

Fig. 6. Current paths of diffident switching sequences in case 3 for Vienna rectifiers. (a) [0, −1, −1]. (b) [1, −1, −1]. (c) [1, 0, −1]. (d) [1, 0, 0].

follows:

$$\begin{cases} p_{\mathrm{UP},[1,-1,-1]} = u_{C1} i_A (d'_{B-1} - d'_{A0}) \\ p_{\mathrm{LOW},[1,-1,-1]} = -u_{C2}(i_B + i_C)(d'_{B-1} - d'_{A0}) \end{cases} \tag{12}$$

$$\begin{cases} p_{\mathrm{UP},[1,0,-1]} = u_{C1} i_A (d'_{C-1} - d'_{B-1}) \\ p_{\mathrm{LOW},[1,0,-1]} = -u_{C2} i_C (d'_{C-1} - d'_{B-1}) \end{cases} \tag{13}$$

$$\begin{cases} p_{\mathrm{UP},[1,0,0]} = u_{C1} i_A d'_{C0} \\ p_{\mathrm{LOW},[1,0,0]} = 0 \end{cases}. \tag{14}$$

In summary, the total power from the ac side to the upper and lower dc buses within a control cycle is as follows

$$\begin{cases} p_{\mathrm{UP}} = p_{\mathrm{UP},[0,-1,-1]} + p_{\mathrm{UP},[1,-1,-1]} \\ \quad + p_{\mathrm{UP},[1,0,-1]} + p_{\mathrm{UP},[1,0,0]} \\ \quad = u_{C1} i_A (-d'_{A0} + d'_{C-1} + d'_{C0}) \\ p_{\mathrm{LOW}} = p_{\mathrm{LOW},[0,-1,-1]} + p_{\mathrm{LOW},[1,-1,-1]} \\ \quad + p_{\mathrm{LOW},[1,0,-1]} + p_{\mathrm{LOW},[1,0,0]} \\ \quad = -u_{C2} i_B d'_{B-1} - u_{C2} i_C d'_{C-1} \end{cases}. \tag{15}$$

Substituting (3) into (15), it yields

$$\begin{cases} p_{\mathrm{UP}} = u_A i_A + u_{\mathrm{ZSV}} i_A \\ p_{\mathrm{LOW}} = u_B i_B + u_C i_C - u_{\mathrm{ZSV}} i_A \end{cases}. \tag{16}$$

It can be concluded that the power from the ac side to the upper and lower dc buses can be changed by injecting appropriate u_{ZSV}.

B. Method to Decouple Output Power

Ignoring the loss of the rectifier, the instantaneous power input from the ac side before and after injecting u_{ZSV} is defined as

$$\begin{cases} p_{\mathrm{in}} = u_A i_A + u_B i_B + u_C i_C \\ p'_{\mathrm{in}} = p_{\mathrm{UP}} + p_{\mathrm{LOW}} = u_A i_A + u_B i_B + u_C i_C = p_{\mathrm{in}} \end{cases} \tag{17}$$

where p_{in} and p'_{in} represent the instantaneous power input from the ac side before and after injecting u_{ZSV}, respectively. It can be seen that the injection of u_{ZSV} does not affect the power input from the ac side to the entire dc bus, but it does change the power distribution between the upper and lower dc buses.

By converting the voltage and current in (16) into the form sorted by (2), the instantaneous power of the dc buses in Case 3 can be obtained as

$$\begin{cases} p_{\mathrm{UP,Case3}} = u_{\mathrm{MAX}} i_{\mathrm{MAX}} + u_{\mathrm{ZSV}} i_{\mathrm{MAX}} \\ p_{\mathrm{LOW,Case3}} = u_{\mathrm{MID}} i_{\mathrm{MID}} + u_{\mathrm{MIN}} i_{\mathrm{MIN}} - u_{\mathrm{ZSV}} i_{\mathrm{MAX}} \end{cases}. \tag{18}$$

Similarly, the instantaneous power of the DC buses in case 1, case 2, and case 4 can be obtained as

$$\begin{cases} p_{\mathrm{UP,Case1}} = u_{\mathrm{MAX}} i_{\mathrm{MAX}} + u_{\mathrm{MID}} i_{\mathrm{MID}} - u_{\mathrm{ZSV}} i_{\mathrm{MIN}} \\ p_{\mathrm{LOW,Case1}} = u_{\mathrm{MIN}} i_{\mathrm{MIN}} + u_{\mathrm{ZSV}} i_{\mathrm{MIN}} \end{cases} \tag{19}$$

$$\begin{cases} p_{\mathrm{UP,Case2}} = u_{\mathrm{MAX}} i_{\mathrm{MAX}} + u_{\mathrm{MID}} i_{\mathrm{MID}} + u_{\mathrm{ZSV}} i_{\mathrm{MIN}} \\ p_{\mathrm{LOW,Case2}} = u_{\mathrm{MIN}} i_{\mathrm{MIN}} - u_{\mathrm{ZSV}} i_{\mathrm{MIN}} \end{cases} \tag{20}$$

$$\begin{cases} p_{\mathrm{UP,Case4}} = u_{\mathrm{MAX}} i_{\mathrm{MAX}} - u_{\mathrm{ZSV}} i_{\mathrm{MAX}} \\ p_{\mathrm{LOW,Case4}} = u_{\mathrm{MID}} i_{\mathrm{MID}} + u_{\mathrm{MIN}} i_{\mathrm{MIN}} + u_{\mathrm{ZSV}} i_{\mathrm{MAX}} \end{cases}. \tag{21}$$

The reference powers for the upper and lower dc buses are defined as $p_{\mathrm{UP,ref}}$ and $p_{\mathrm{LOW,ref}}$. In order to maintain the instantaneous power balance for the upper and lower dc buses, it is necessary to meet $p_{\mathrm{UP,ref}} = p_{\mathrm{UP}}$ and $p_{\mathrm{LOW,ref}} = p_{\mathrm{LOW}}$.

If $u'_{\mathrm{MID}} > 0$ (corresponding to case 1 and case 2), the lower dc bus only exchanges power with the phase corresponding to minimum voltage, and the required u_{ZSV} for decoupling the output power of the upper and lower dc buses is obtained as

$$u_{\mathrm{ZSV,Case1}} = \frac{p_{\mathrm{LOW,ref}}}{i_{\mathrm{MIN}}} - u_{\mathrm{MIN}}. \tag{22}$$

Similarly, if $u'_{\mathrm{MID}} < 0$ (corresponding to case 3 and case 4), the upper dc bus only exchanges power with the phase corresponding to maximum voltage, and the required u_{ZSV} for decoupling the output power of the upper and lower dc buses is obtained as

$$u_{\mathrm{ZSV,Case3}} = \frac{p_{\mathrm{UP,ref}}}{i_{\mathrm{MAX}}} - u_{\mathrm{MAX}}. \tag{23}$$

Based on above analysis, the following conclusions can be drawn as follows.

1) Before and after injecting u_{ZSV}, the power input from the ac side to the entire dc bus will not be changed.
2) The instantaneous power input from the ac side to the upper and lower dc buses can be controlled by adjusting u_{ZSV}.
3) The power input from the ac side to the upper and lower dc buses is independent of the dc-bus voltage, and the range of u_{ZSV} is determined by the upper and lower dc-bus voltage.

C. Limit Value of Output Power Distribution

According to (18) to (21), the average power of the dc bus after the injecting u_{ZSV} within one fundamental period can be obtained as

$$\begin{cases} \overline{p_{\mathrm{UP}}} = \int_0^{2\pi} \left(\begin{matrix} p_{\mathrm{UP,Case1}} + p_{\mathrm{UP,Case2}} \\ + p_{\mathrm{UP,Case3}} + p_{\mathrm{UP,Case4}} \end{matrix} \right) d\omega t \\ \overline{p_{\mathrm{LOW}}} = \int_0^{2\pi} \left(\begin{matrix} p_{\mathrm{LOW,Case1}} + p_{\mathrm{LOW,Case2}} \\ + p_{\mathrm{LOW,Case3}} + p_{\mathrm{LOW,Case4}} \end{matrix} \right) d\omega t \end{cases} \tag{24}$$

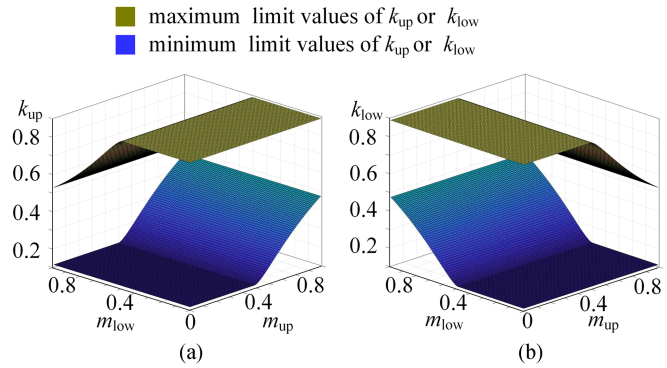

Fig. 7. Range of k_{up} and k_{low} under different m_{up} and m_{low} within a fundamental period. (a) Range of k_{up}. (b) Range of k_{low}.

where $\overline{p_{UP}}$ and $\overline{p_{LOW}}$ are the average power of the upper and lower dc buses after the injecting u_{ZSV} within one fundamental period, respectively.

Under different m_{up} and m_{low}, if the u_{ZSV} during each switching cycle is $u_{ZSV,MAX}$, the proportion of power input from the ac side to the upper dc bus is the highest in one fundamental period. If the u_{ZSV} during each switching cycle is $u_{ZSV,MIN}$, the proportion of power input from the ac side to the upper dc bus is the lowest in one fundamental period. The proportions of $\overline{p_{UP}}$ and $\overline{p_{LOW}}$ relative to the average power exchanged to the entire dc bus are defined as

$$\begin{cases} k_{up} = \dfrac{\overline{p_{UP}}}{\overline{p_{UP}}+\overline{p_{LOW}}} \\ k_{low} = \dfrac{\overline{p_{LOW}}}{\overline{p_{UP}}+\overline{p_{LOW}}} \end{cases} \tag{25}$$

where k_{up} and k_{low} represent the proportion of the average power of the upper and lower dc buses relative to the average power of the entire dc bus, respectively. Based on (18) to (21), (24), and (25), the range of k_{up} and k_{low} under different m_{up} and m_{low} within a fundamental period can be calculated as shown in Fig. 7. Taking the upper dc bus as an example. As shown in Fig. 7(a), the surface for the maximum value of k_{up} corresponding to u_{ZSV} is always $u_{ZSV,MAX}$. It can be seen that the maximum value of k_{up} is related to m_{low} and independent of m_{up}. When $m_{low} > 0.5$, as m_{low} gradually increases, the maximum value of k_{up} gradually decreases, and the relationship is approximately linear. Similarly, the surface for the minimum value of k_{up} corresponding to u_{ZSV} is always $u_{ZSV,MIN}$, and the analysis is similar.

Specifically, when $m_{up} = m_{low}$, the voltage of the upper and lower dc buses is equal, and the maximum and minimum values of k_{up} are shown in Fig. 8. When $m_{up} = m_{low} < 0.5$, the maximum and minimum limit value of k_{up} remain constant, approximately 0.89 and 0.11, respectively. When $m_{up} = m_{low} > 0.5$, the maximum value of k_{up} gradually decreases and the minimum value of k_{low} gradually increases. When $m_{up} = m_{low} = 1$, the maximum and minimum values of k_{up} are approximately 0.52 and 0.48, respectively.

The analysis of the maximum and minimum values of k_{low} shown in Fig. 7(b) is very similar and will not be repeated here. To clarify the above relationship more clearly, the specific

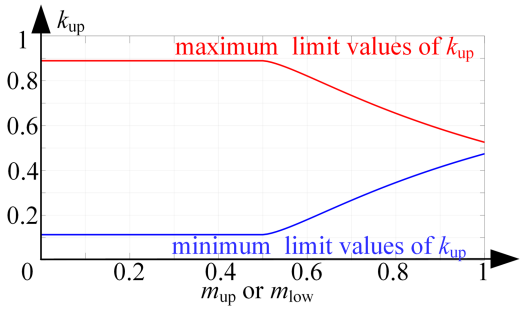

Fig. 8. Maximum and minimum values of k_{up} when $m_{up} = m_{low}$.

TABLE I
SPECIFIC VALUES OF K_{UP} AND K_{LOW} UNDER SPECIFIC M_{UP} AND M_{LOW}

	u_{ZSV}	m_{up}=0.2 m_{low}=0.2	m_{up}=0.4 m_{low}=0.7	m_{up}=0.7 m_{low}=0.4	m_{up}=1 m_{low}=1
k_{up}	$u_{ZSV,MAX}$	0.89	0.74	0.89	0.53
	$u_{ZSV,MIN}$	0.11	0.11	0.26	0.47
k_{low}	$u_{ZSV,MAX}$	0.11	0.26	0.11	0.47
	$u_{ZSV,MIN}$	0.89	0.89	0.74	0.53

values of k_{up} and k_{low} under specific m_{up} and m_{low} are given in Table I. Taking $m_{up} = 0.4$ and $m_{low} = 0.7$ as an example. Within a fundamental period, if the injected u_{ZSV} is $u_{ZSV,MAX}$, the maximum value of k_{up} is 74%; if the injected u_{ZSV} is $u_{ZSV,MIN}$, the minimum value of k_{up} is 11%.

V. CZCD Suppression and Implementation Method

A. CZCD Suppression Method

The topology of the Vienna rectifier determines that input current distortion will occur when $u_{MID}i_{MID} < 0$, such as case 2 and case 4. In [15], CZCD is suppressed by making the phase corresponding to u_{MID} always output level 0 when $u_{MID}i_{MID} < 0$. In fact, the method proposed in [15] will not be effective when the modulation index is high because of over modulation. For example, in case 2, u_{ZSV} needs to satisfy (6), but when the maximum value of u_{ZSV} is less than the minimum value in (6), i.e., $u_{C2} < u_{MID}$-u_{MIN}. There is no available u_{ZSV}. If the phase corresponding to u_{MID} is forcibly clamped to level 0, i.e., $u_{ZSV} = -u_{MID}$, then $u'_{MIN} = u_{MIN}$-$u_{MID} < -u_{C2}$. In this case, the phase corresponding to u_{MIN} will be overmodulated, also resulting in CZCD. If $u_{ZSV} = -u_{C2}$-u_{MIN}, that is, $u'_{MID} = u_{MID}$-u_{MIN}-u_{C2}, it is not possible to keep the phase corresponding to u_{MID} always output level 0, and CZCD on the phase corresponding to u_{MID} will not be completely eliminated. When the above situation occurs, CZCD cannot be avoided. Therefore, it is necessary to find a method to minimize CZCD. The approximate synthesis method proposed in [5] is adopted in this article to minimize CZCD, and the three-phase modulation voltage is directly given in Table II.

B. Implementation of the Proposed Method

The control block diagram of the method proposed in this article is shown in Fig. 9. The reference and sampling values

TABLE II
THREE-PHASE MODULATION VOLTAGE OF VIENNA RECTIFIER IN BIPOLAR OUTPUT MODE

Condition I	Condition II	Range of u_{ZSV}	Function of u_{ZSV}	Three-phase modulation voltage
$u_{MID}>0$, $i_{MID}>0$	/	(5)	Output power distribution	$u'_X=u_X+(e_d i_{d\_low\_ref})/i_{MIN}-u_{MIN}$
$u_{MID}>0$, $i_{MID}<0$	$u_{MID}-u_{MIN}\le u_{C2}$	(6)	Output power distribution and CZCD elimination	$u'_X=u_X+(e_d i_{d\_low\_ref})/i_{MIN}-u_{MIN}$
	$u_{MID}-u_{MIN}>u_{C2}$	/	CZCD suppression	$u''_{MAX}=1.5u_{MAX}-0.5u_{C2}$,$u''_{MID}=0$,$u''_{MIN}=-u_{C2}$
$u_{MID}<0$, $i_{MID}<0$	/	(7)	Output power distribution	$u'_X=u_X+(e_d i_{d\_up\_ref})/i_{MAX}-u_{MAX}$
$u_{MID}<0$, $i_{MID}>0$	$u_{MAX}-u_{MID}\le u_{C1}$	(8)	Output power distribution and CZCD elimination	$u'_X=u_X+(e_d i_{d\_up\_ref})/i_{MAX}-u_{MAX}$
	$u_{MAX}-u_{MID}>u_{C1}$	/	CZCD suppression	$u''_{MAX}=u_{C1}$,$u''_{MID}=0$,$u''_{MIN}=1.5u_{MIN}+0.5u_{C1}$

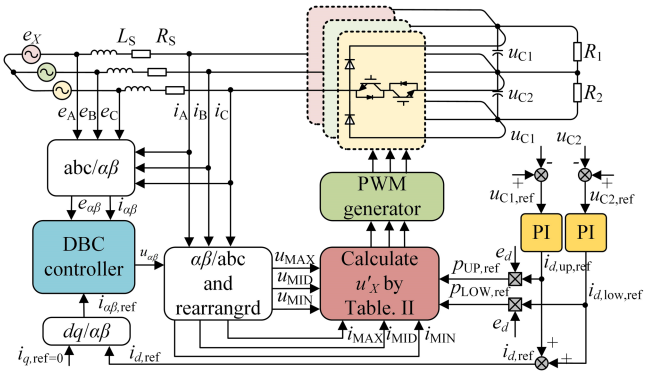

Fig. 9. Control block diagram of proposed method.

TABLE III
MAIN PARAMETERS OF THE EXPERIMENTAL PLATFORM

Parameter	Value
upper and lower dc-link capacitor	1000 μF
grid line-to-line voltage (rms)	120 V
input filter inductor	3 mH
carrier frequency	10 kHz

for the voltage of the upper and lower dc buses are $u_{C1,\mathrm{ref}}$, $u_{C2,\mathrm{ref}}$, u_{C1}, and u_{C2}, respectively. By using a proportional integral regulator, the reference currents of the upper and lower dc buses, i.e., $i_{d,\mathrm{up,ref}}$ and $i_{d,\mathrm{low,ref}}$, can be obtained. The sum of $i_{d,\mathrm{up,ref}}$ and $i_{d,\mathrm{low,ref}}$ is the d-axis component of the total reference current, that is $i_{d,\mathrm{ref}}$.

Deadbeat control proposed in [26] is selected as current controller, the output of the current controller is the modulated voltage in the $\alpha\beta$ coordinate. Through coordinate system transformation, i.e., $\alpha\beta$/abc transformation, the three-phase modulation voltage without ZSV injection can be obtained. Finally, according to Table II, the final modulation voltage that can be used for output power distribution and CZCD suppression can be directly obtained.

VI. EXPERIMENTAL RESULTS

The experimental platform is shown in Fig. 10, and the experimental parameters are given in Table III. The oscilloscope is DLM3024 of YOKOGAWA company. TMSF320F28374S of

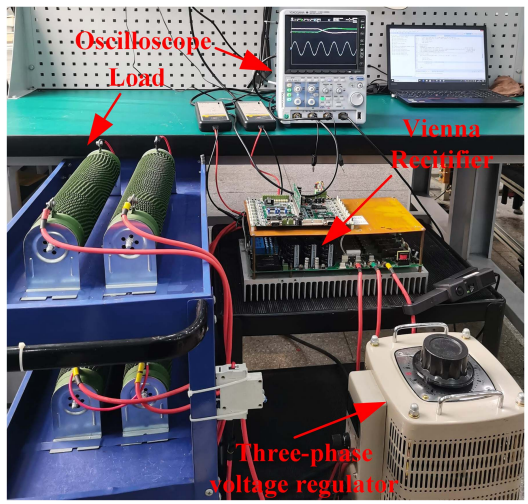

Fig. 10. Experimental platform of the Vienna rectifier.

TI company is selected as the control chip, while the inner and outer tubes of the Vienna rectifier are FGH25N120FTDS and ISL9R30120G2 produced by ONSEMI company.

To show the benefits of the proposed scheme, the experimental results of the three methods were compared under different steady-state and dynamic operating conditions. When method 1 is adopted, the dc-bus voltage is controlled by output power decoupling, and CZCD is suppressed by the proposed modulation method, which is the same as the method proposed in this article. When method 2 is adopted, the dc-bus voltage is controlled by adjusting the NP current, and the CZCD is suppressed by the proposed modulation method. When method 3 is adopted, the dc-bus voltage is controlled by adjusting the NP current, and CZCD is suppressed by clamping in the current zero crossing region, which is the same as the method proposed in [15].

It is worth noting that when the modulation index is low, the clamping method proposed in [15] can also eliminate CZCD. And in this case, methods 2 and 3 are the same.

A. Comparison of Steady-State Performance in Balanced Bipolar Output Mode

When the output power of the upper and lower dc buses is balanced, the steady-state experimental results under different

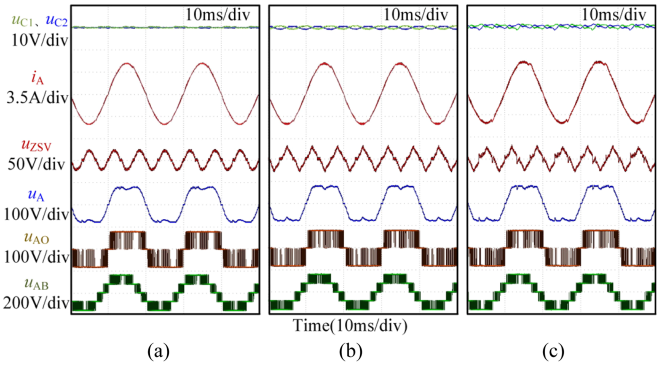

Fig. 11. Steady-state experimental results under $m_{\rm up} = m_{\rm low} = 0.98$, $k_{\rm up} = 0.5$. $u_{C1} = u_{C2} = 85$ V, and $R_1 = R_2 = 20\,\Omega$. (a) Method 1. (b) Method 2. (c) Method 3.

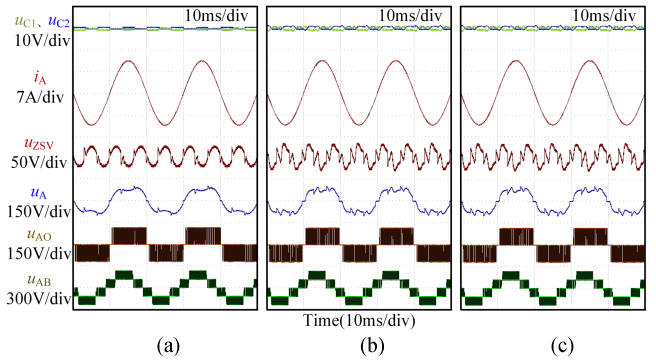

Fig. 12. Steady-state experimental results under $m_{\rm up} = m_{\rm low} = 0.67$, $k_{\rm up} = 0.5$. $u_{C1} = u_{C2} = 125$V, and $R_1 = R_2 = 20\ \Omega$. (a) Method 1. (b) Method 2. (c) Method 3.

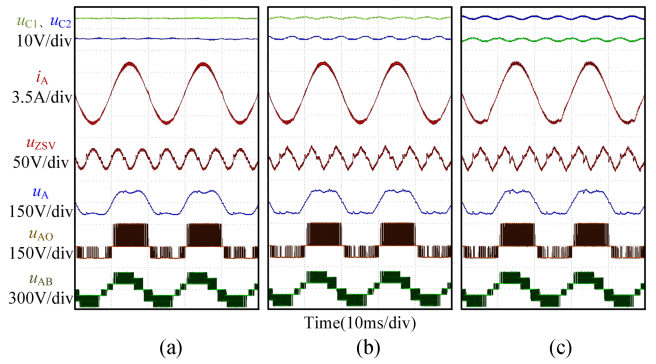

Fig. 13. Steady-state experimental results under $m_{\rm up} = 0.49$, $m_{\rm low} = 0.98$, $k_{\rm up} = 0.5$. $u_{C1} = 170$V, $u_{C2} = 85$V, $R_1 = 80\ \Omega$, and $R_2 = 20\ \Omega$. (a) Method 1. (b) Method 2. (c) Method 3.

modulation indexes are shown in Figs. 11–13, respectively. The current THD under different operation states are given in Table IV.

From Figs. 11–13, it can be seen that all three methods can control the stability of dc-bus voltage. While the ripple of the dc-bus voltage with method 1 is smaller than that with methods 2 and 3. It indicates that output power decoupling is more effective than adjusting the NP current in terms of dc-bus output power distribution.

TABLE IV
CURRENT THD OF DIFFERENT METHODS IN DIFFERENT OPERATION STATES

Operation states	Methods	Current THD
$m_{\rm up}$=$m_{\rm low}$=0.98 and $k_{\rm up}$=0.5 (see Fig. 11)	Method 1	2.11%
	Method 2	2.39%
	Method 3	3.03%
$m_{\rm up}$=$m_{\rm low}$=0.67 and $k_{\rm up}$=0.5 (see Fig. 12)	Method 1	0.88%
	Method 2	0.92%
	Method 3	0.92%
$m_{\rm up}$=0.49, $m_{\rm low}$=0.9 $k_{\rm up}$=0.5 (see Fig. 13)	Method 1	3.81%
	Method 2	3.84%
	Method 3	4.42%
$m_{\rm up}$=0.98, $m_{\rm low}$=0.67, and $k_{\rm up}$=0.32 (see Fig.14)	Method 1	2.32%
	Method 2	2.34%
	Method 3	3.26%
$m_{\rm up}$=$m_{\rm low}$=0.67, and $k_{\rm up}$=0.67 (see Fig.15)	Method 1	1.39%
	Method 2	1.43%
	Method 3	1.43%
$m_{\rm up}$=0.98, $m_{\rm low}$=0.67, and $k_{\rm up}$=0.48 (see Fig.16)	Method 1	2.52%
	Method 2	2.60%
	Method 3	3.23%

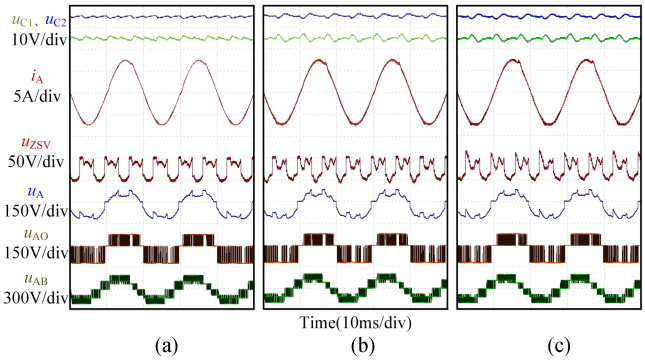

Fig. 14. Steady-state experimental results under $m_{\rm up} = 0.98$, $m_{\rm low} = 0.67$, and $k_{\rm up} = 0.32$. $u_{C1} = 85$ V, $u_{C2} = 125$ V, and $R_1 = R_2 = 20\ \Omega$. (a) Method 1. (b) Method 2. (c) Method 3.

From Table IV, it can be seen that the current THD with methods 1 and 2 is smaller than that with method 3, especially in situations where the modulation index is high. It indicates that the proposed modulation method is more effective than the method proposed method in [15] in terms of the CZCD suppression.

B. Comparison of Steady-State Performance in Unbalanced Bipolar Output Mode

The steady-state experimental results under unbalanced output voltage and power conditions are shown in Figs. 14–16. The results are consistent with the experimental results under balanced output voltage and power conditions. This validates the feasibility and superiority of the proposed method under unbalanced output voltage and power conditions.

C. Verification of the Limit Value of Output Power Distribution

Taking the maximum limit value of $k_{\rm up}$ as an example, this section will use experimental results to verify the limit value of output power distribution analyzed in Section IV. As shown in Fig. 8, when $m_{\rm up} = m_{\rm low} = 0.98$, the theoretical maximum

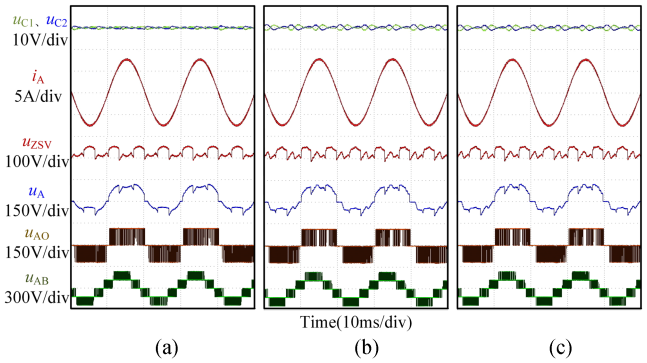

Fig. 15. Steady-state experimental results under $m_{up} = m_{low} = 0.67$ and $k_{up} = 0.67$. $u_{C1} = u_{C2} = 125$ V, $R_1 = 20\ \Omega$, and $R_2 = 40\ \Omega$. (a) Method 1. (b) Method 2. (c) Method 3.

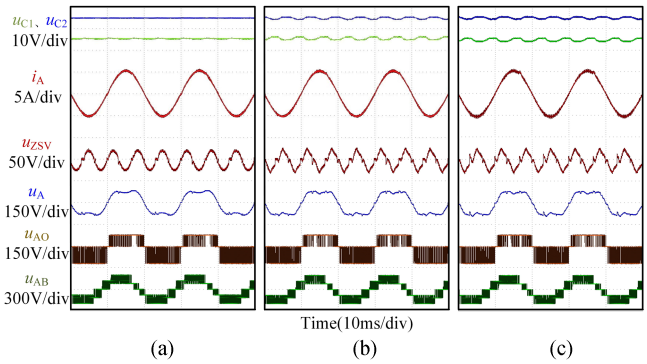

Fig. 16. Steady-state experimental results under $m_{up} = 0.98$, $m_{low} = 0.67$, and $k_{up} = 0.48$. $u_{C1} = 85$ V, $u_{C2} = 125$ V, $R_1 = 20\ \Omega$, and $R_2 = 40\ \Omega$. (a) Method 1. (b) Method 2. (c) Method 3.

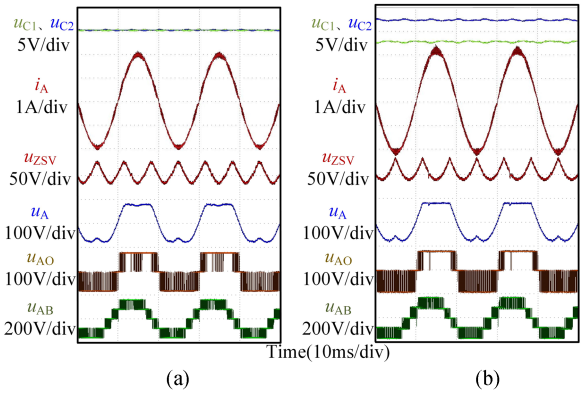

Fig. 17. Limit value of output power distribution verification experiment I. $m_{up} = m_{low} = 0.98$. (a) $k_{up} = 0.52$. (b) $k_{up} = 0.60$.

limit value of k_{up} is 0.52. In Fig. 17(a), both the upper and lower dc-bus voltages can stably track the reference voltage of 85 V. It indicates that the Vienna rectifier can operate stably under the experimental conditions of $m_{up} = m_{low} = 0.98$ and $k_{up} = 0.52$. As shown in Fig. 17(b), the k_{up} is 0.60, and there is a significant separation between the upper and lower dc-bus voltages, which cannot be traced to 85 V. Therefore, when $k_{up} > 0.52$, the

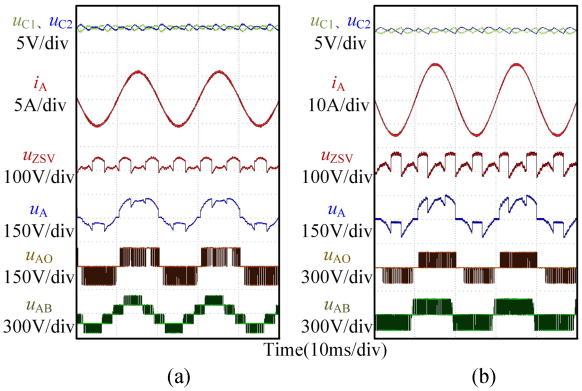

Fig. 18. Limit value of output power distribution verification experiment II. (a) $m_{up} = m_{low} = 0.67$ and $k_{up} = 0.70$. (b) $m_{up} = m_{low} = 0.40$ and $k_{up} = 0.80$.

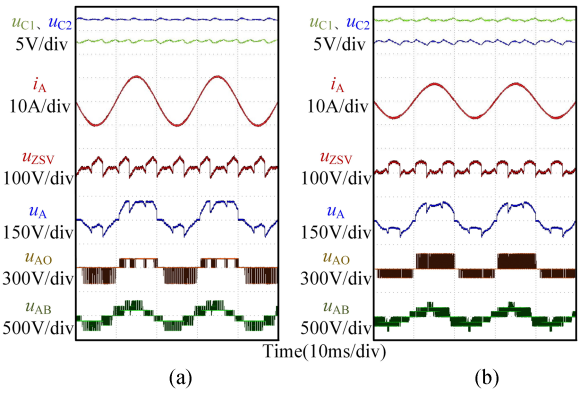

Fig. 19. Limit value of output power distribution verification experiment II. (a) $m_{up} = 0.70$, $m_{low} = 0.40$, and $k_{up} = 0.87$. (b) $m_{up} = 0.40$, $m_{low} = 0.70$, and $k_{up} = 0.65$.

Vienna rectifier cannot operate as expected, which is consistent with the theoretical analysis. Similarly, when $m_{up} = m_{low} = 0.67$, the theoretical maximum limit value of k_{up} is 0.75. The experimental results with $k_{up} = 0.70$ are shown in Fig. 18(a). When $m_{up} = m_{low} = 0.40$, the theoretical maximum limit value of k_{up} is 0.88. The experimental results with $k_{up} = 0.80$ are shown in Fig. 18(b).

When $m_{up} = 0.7$ and $m_{low} = 0.4$, the theoretical maximum limit value of k_{up} is 0.89, while in the experiment, the maximum value of k_{up} can reach around 0.87. When $m_{up} = 0.4$ and $m_{low} = 0.7$, the theoretical maximum limit value of k_{up} is 0.68, while in the experiment, the maximum value of k_{up} can reach around 0.65. The experimental results are shown in Fig. 19. Considering measurement and calculation deviation in practice, the above experimental results are consistent with the theoretical analysis.

D. Comparison of Dynamic Experimental Results

When R_1 remains unchanged and R_2 step-down from 20 to 40 Ω or step-up from 40 to 20 Ω, the dynamic experimental results with methods 1 and 2 are shown in Fig. 20. If method 1 is adopted, shown in Fig. 20(a) and (b), the maximum voltage

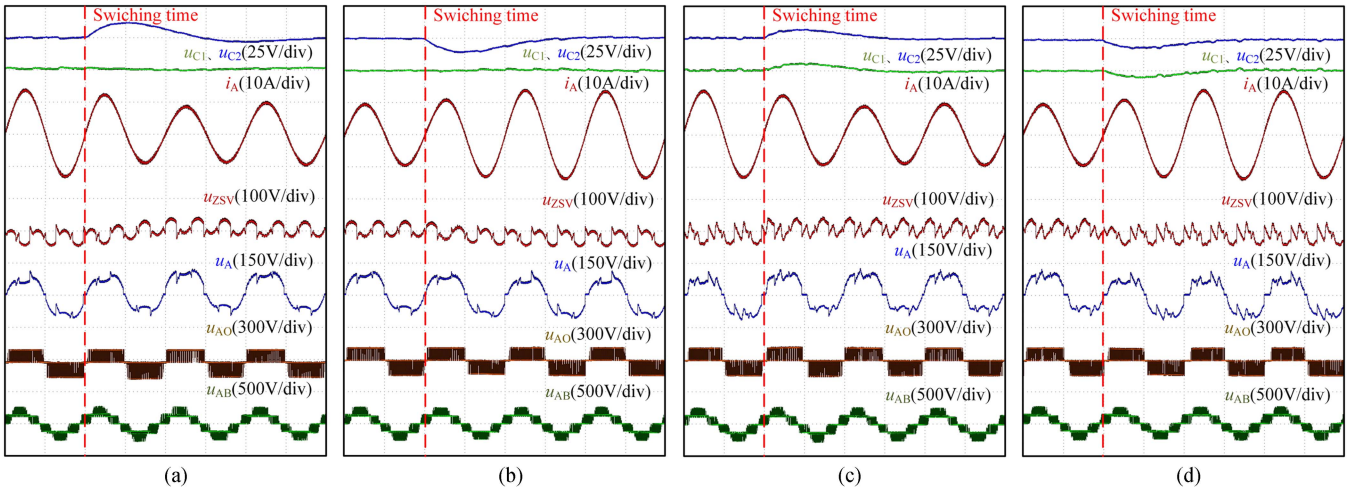

Fig. 20. Dynamic experimental results with methods 1 and 2 under load step-up and step-down conditions. (a) $R2$ step-down from 20 to 40 Ω with method 1. (b) $R2$ step-down from 40 to 20 Ω with method 1. (c) $R2$ step-down from 20 to 40 Ω with method 2. (d) $R2$ step-down from 40 to 20 Ω with method 2.

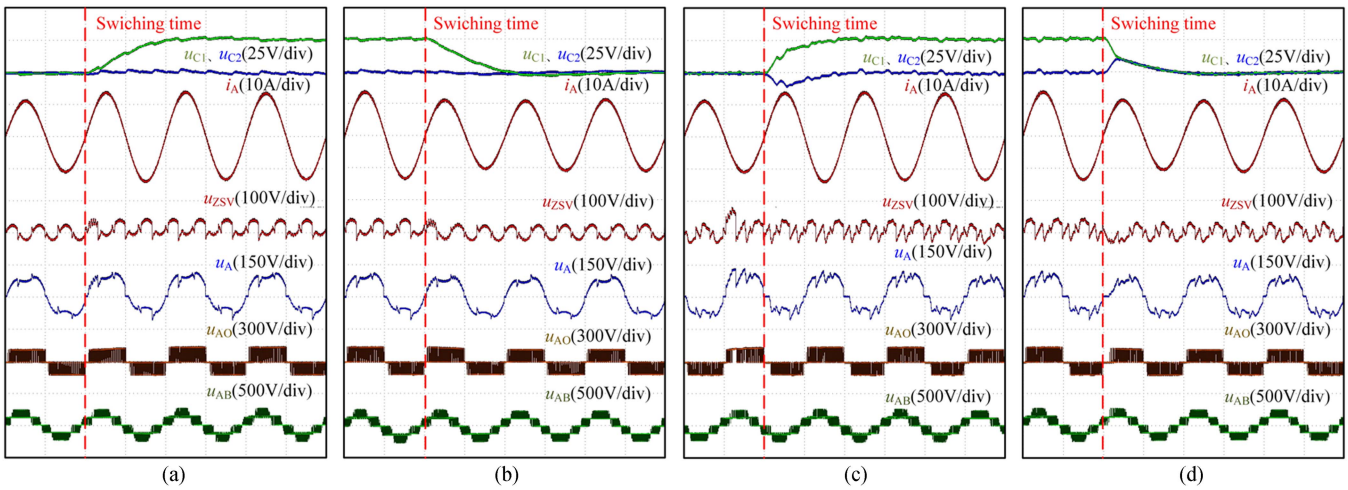

Fig. 21. Dynamic experimental results with method 1 and 2 under DC-bus voltage step-up and step-down conditions. (a) $u_{C2,\mathrm{ref}} = 125$ V, $u_{C1,\mathrm{ref}}$ step-up from 125 to 150 V with method 1. (b) $u_{C2,\mathrm{ref}} = 125$ V, $u_{C1,\mathrm{ref}}$ step-down from 150 to 125 V with method 1. (c) $u_{\mathrm{C2,ref}} = 125$V, $u_{\mathrm{C1,ref}}$ step-up from 125 to 150 V with method 2. (d) $u_{C2,\mathrm{ref}} = 125$ V, $u_{C1,\mathrm{ref}}$ step-down from 150 to 125 V with method 2.

fluctuation on the lower dc bus is about 18 V, while the voltage fluctuation on the upper dc bus is very small. It means that the output fluctuation of one dc bus will not affect the other dc bus, that is, output decoupling has been completely achieved. If method 2 is adopted, shown in Fig. 20(c) and (d), the maximum voltage fluctuation both on the upper and lower dc bus is about 9 V. This means that output decoupling has not been fully achieved by adjusting the NP current.

When $u_{C2,\mathrm{ref}}$ remains unchanged and $u_{C1,\mathrm{ref}}$ step-down from 150 to 125 V or step-up from 125 to 150 V, the dynamic experimental results with methods 1 and 2 are shown in Fig. 21. If method 1 is adopted, shown in Fig. 21(a) and (b), u_{C1} quickly tracks to $u_{C1,\mathrm{ref}}$, while u_{C2} remains almost unchanged. If method 2 is adopted, shown in Fig. 21(c) and (d), While u_{C1} tracks $u_{C1,\mathrm{ref}}$, u_{C2} also fluctuates. This can also indicate that output decoupling can be achieved by the proposed method rather than by adjusting the NP current.

VII. Conclusion

In this article, the basic principle of Vienna rectifier operating in bipolar output mode is introduced, and the range of ZSV is analyzed. By deriving the power distribution principle of the upper and lower dc buses, it is revealed that the power flowing into the upper and lower dc buses can be adjusted by adjusting ZSV. The output decoupling is essentially achieved, which cannot be achieved through existing methods of adjusting NP current. In addition, this article introduces the constraint relationship between the limit value of ZSV and the power distribution between the upper and lower dc buses. Finally,

three-phase modulation voltages that can decouple output and suppress CZCD are directly provided based on the operating status in Table IV.

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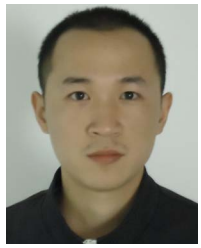

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