A Bidirectional Current-Fed Isolated MMC With Partial Soft-Switching for High Step Ratio DC–DC Applications

Philippe A. Gray, *Member, IEEE*, Noah J. B. Hosein, *Student Member, IEEE*, Xi Lan, *Member, IEEE*, and Peter W. Lehn, *Senior Member, IEEE*

***Abstract*—Medium-voltage direct current (MVDC) systems offer many advantages in a future of renewables and dc loads including reducing the number of required power conversion stages. An enabling technology for MVDC distribution systems will be high step ratio dc-dc converters with bidirectional power transfer capability, performing a role similar to ac distribution transformers. The current shaping modular multilevel converter (CS-MMC) has been proposed for this type of application. This converter family operates at high effective frequencies, enabled by the elimination of internal string inductors. While foundational work on the CS-MMC focused on unidirectional, voltage-fed operation, recent work has demonstrated the bidirectional capabilities of the CS-MMC when operated as a current-fed converter driven by the low-voltage side. This article proposes an improved modulation for the bidirectional CS-MMC that: 1) ensures zero-voltage switching of the secondary-side switches in forward operation; and 2) minimizes the reverse body diode conduction time to improve efficiency. This article is also the first to detail a balancing mechanism between the VSM strings and between the dc-blocking capacitors of the bidirectional CS-MMC. Peak measured efficiencies of 97.0% in forward operation and 96.3% in reverse operation are achieved for a 6 module, 3 kW, 1 kV/100 V prototype.**

***Index Terms*—Current-fed, dc–dc power conversion, modular multilevel converter, soft switching, solid-state transformer (SST).**

I. Introduction

With the expansion of clean energy technologies throughout the electrical grid, dc-based distribution is becoming increasingly competitive with respect to its ac counterpart. Using dc-based distribution offers the potential to improve transmission efficiency and power quality, as well as to reduce the total number of power conversion stages [2]. To exchange power between dc networks, a key enabling technology is the dc solid-state transformer (SST) [3], [4]. The focus of this article is on dc SSTs for high step ratio applications such as interfacing a medium voltage dc (MVDC) network and a low voltage dc (LVDC) system. Examples of LVDC systems include fuel cell stacks, electric vehicles, and battery energy storage systems (BESS), many of which require bidirectional power transfer capabilities.

A state-of-the-art dc SST for high step ratio applications involves cascading power electronic modules in series on the higher-voltage side and in parallel on the lower-voltage side. This arrangement is often termed input-series output-parallel (ISOP) [5], [6]. Many different topologies can be employed for the power electronic modules including the dual-active bridge (DAB), CLLC resonant converter [7], as well as many other less common topologies [8]. While ISOP structures are well suited to this application, there are drawbacks including a high number of switches and magnetics, high control and operational complexity, and high isolation requirements imposed on some of the power electronic modules.

The current shaping modular multilevel converter (CS-MMC) is a recently proposed class of modular multilevel converter (MMC) which addresses many of the aforementioned challenges [9], [10], [11]. The CS-MMC has a low switch count as it scales to high voltages by only adding half-bridges and requires just a single secondary-side switch stage. In addition, the isolated CS-MMC in [11] requires just one low-voltage, high-frequency, three-winding transformer. The control complexity is also greatly simplified with self-balancing of the voltage source submodule (VSM) capacitors, eliminating the need for voltage sensors on the individual VSMs. Similar to the flying capacitor converter, the CS-MMC leverages a frequency multiplication effect whereby the effective frequency experienced by the transformer and VSM capacitors is greater than the individual VSM switching frequency. This enables a reduction in converter volume and cost without leading to increased switching losses [11].

While some bidirectional dc SSTs with MMC structures have been proposed based on voltage-fed DAB operating principles [12], [13], the CS-MMC uniquely employs a current source module (CSM) on the lower-voltage side which naturally

Manuscript received 31 October 2023; revised 16 January 2024; accepted 17 March 2024. Date of publication 2 April 2024; date of current version 16 May 2024. This work was supported by the Natural Sciences and Engineering Research Council of Canada under the Discovery Grants program under Grant RGPIN-2019-06453. An earlier version of this paper was presented at the 2023 IEEE 11th International Conference on Power Electronics and ECCE Asia, Jeju Island, Republic of Korea [DOI: 10.23919/ICPE2023-ECCEAsia54778.2023.10213540]. Recommended for publication by Associate Editor A. Yazdani. *(Corresponding author: Noah J. B. Hosein.)*

Philippe A. Gray was with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada. He is now with the Department of Electrical and Software Engineering, University of Calgary, Calgary, AB T2N 4V8, Canada (e-mail: philippe.gray@ucalgary.ca).

Noah J. B. Hosein, Xi Lan, and Peter W. Lehn are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: noah.hosein@mail.utoronto.ca; xi.lan@mail.utoronto.ca; lehn@ece.utoronto.ca).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3383651.

Digital Object Identifier 10.1109/TPEL.2024.3383651

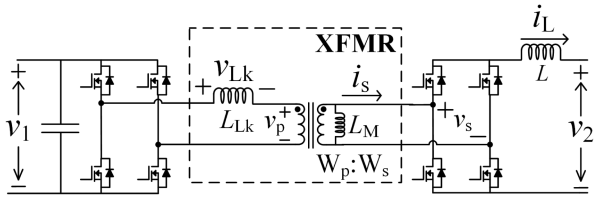

Fig. 1. Circuit topology of the current-fed dual-active bridge.

bounds the transformer current. This allows for the removal of arm inductors to enable rapid reversal of string currents for high-frequency operation. A limitation with foundational work on the CS-MMC, however, has been that it has only considered voltage-fed, unidirectional operation.

The challenge of implementing bidirectional operation for the CS-MMC is similar to that of other current-fed topologies like the current-fed dual-active bridge (CF-DAB), shown in Fig. 1. Although current-fed converters offer advantages such as improved fault handling [14] and the ability to generate pulsed currents for fuel cell applications [15], the presence of two current sources–the full-bridge inductor L and the transformer leakage inductance L_{lk}–complicates the transition between switching states during reverse operation (from v_2 to v_1). In reverse operation, when a secondary-side switch pair is gated OFF, the difference between the transformer leakage inductance current and the full-bridge inductor current is forced to flow through the stray capacitance of the switches, generating a potentially damaging voltage stress.

Several methods for handling this challenge have been proposed in prior literature. The simplest solution is to utilize a snubber to limit the stress experienced by the switches [16]. However, the lossy nature of this method makes it generally impractical, motivating the development of other hardware-based approaches such as active-clamps [17], [18], [19] or advanced topological modifications [20]. While these approaches do offer improvements, they also introduce additional complexity, increased component stress, and higher costs.

In [21], a novel modulation based approach was proposed to resolve the voltage spike issue. The approach leverages a technique to ensure zero-current switching (ZCS) and natural commutation of the leakage inductance current. When performed correctly, this eliminates the risk of high voltage stress on the switches all without additional components or losses.

Building on this fundamental concept, several variations of the modulation in [21] have been presented for a variety of current-fed topologies [22], [23], [24], [25]. In [26], the modulation is generalized to full-bridge based converters such as the CF-DAB. In addition, modifications to the original technique was developed in [27], [28], and [29] which reduce circulating current for improved efficiency.

In [1], bidirectional power transfer was first demonstrated in the CS-MMC by employing the ZCS natural commutation technique in a new current-fed modulation scheme. However, [1] experiences high body diode conduction losses in forward operation as a result of the gating design of the standard ZCS technique. Furthermore, [1] does not detail a control mechanism

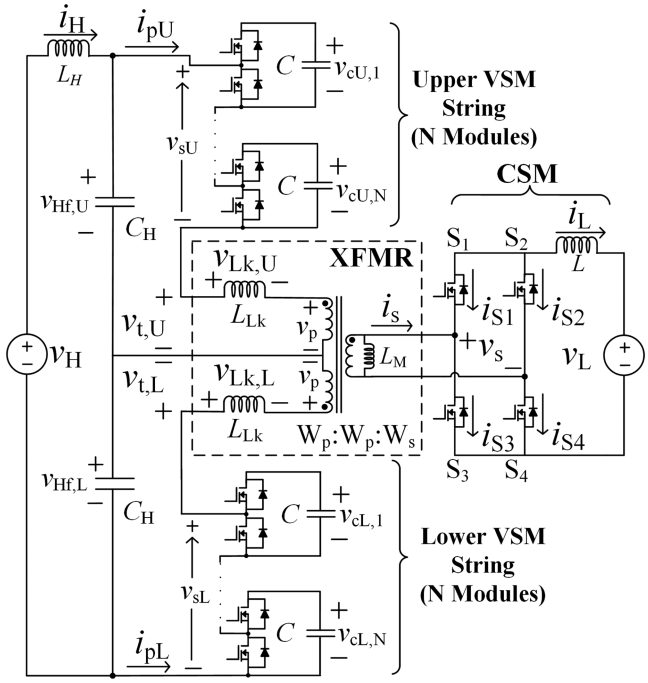

Fig. 2. Circuit topology of the bidirectional CS-MMC.

to prevent voltage imbalance between the VSM strings and between the dc-blocking capacitors which can develop as a result of leakage inductance asymmetry in the three-winding transformer.

In this article, an improved modulation scheme of the bidirectional CS-MMC is presented which is optimized over the entire converter operating range. This new modulation modifies the CSM gating to minimize body diode conduction time while not interfering with ZCS, mitigating a major loss mechanism in [1]. Further efficiency improvements are achieved with the introduction of zero-voltage switching (ZVS) of CSM switches during forward operation. In addition, a new active balancing scheme is implemented which ensures voltage balance between the VSM strings and between the dc-blocking capacitors while still ensuring ZCS conditions.

This article first presents the topology and fundamental operating concepts underlying the converter. Next the equivalent circuit model for the converter is described. Afterward, the article discusses the approach to balancing the voltages of the VSM capacitors within and between strings, as well as balancing the voltages of the dc-blocking capacitors. A circuit analysis is then presented to derive the time-averaged large and small-signal model, which informs control design in the subsequent section. Finally, the experimental results are presented followed by the conclusion.

II. Circuit Topology and Structure

The topology of the bidirectional CS-MMC is presented in Fig. 2. The converter interfaces between an MVDC and LVDC network represented by v_H and v_L, respectively. It is assumed

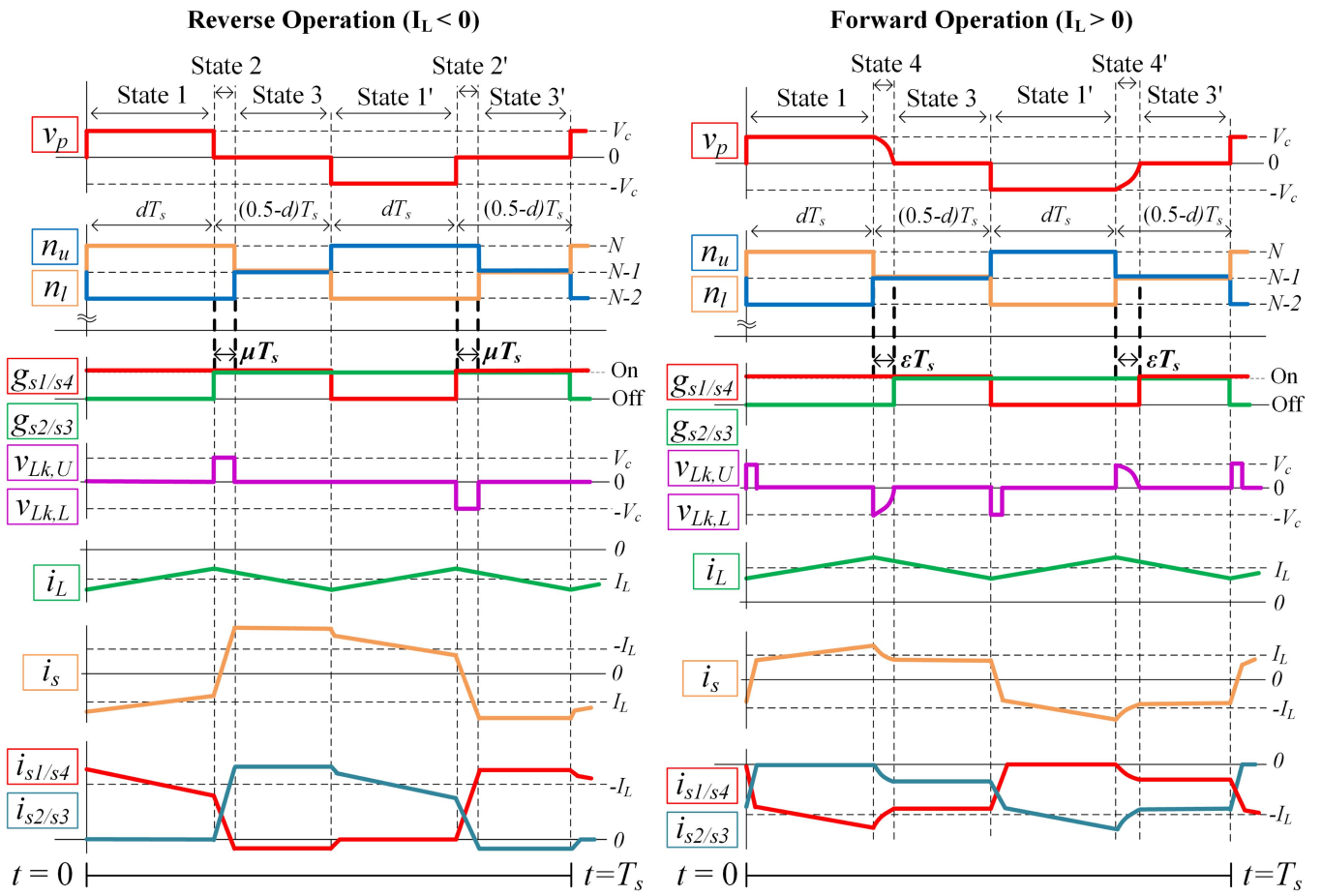

Fig. 3. Waveforms of important quantities in reverse and forward operation over one operating cycle.

that the connection between v_H and the converter possesses some nonnegligible inductance L_H.

Similar to the CS-M2IC in [10], the topology features an upper and lower string of half-bridge VSMs, each connected to the oppositely wound primary terminals on a three-winding transformer with turns ratio $r_t = \frac{W_s}{W_p}$. The transformer midpoint is connected to the common node of two dc-blocking capacitors C_H which connect across the medium voltage converter input. The secondary side of the transformer connects to the full-bridge of the CSM, and the CSM inductor L directly feeds the low voltage network.

As described in [10], this arrangement provides galvanic isolation with flux cancellation of the dc current common to the upper and lower VSM strings. This feature combined with the design of the high frequency modulation, allows for excellent transformer and VSM power density and utilization.

III. Bidirectional Operating Principles

Operation of the bidirectional CS-MMC is designed to achieve: 1) regulation of power transfer between the MVDC and LVDC networks; 2) ZCS of CSM switches in reverse operation; and 3) ZVS of CSM switches in forward operation. This section will describe the concepts utilized to meet these objectives.

Fig. 3 presents the waveforms of key quantities over one operating cycle in both reverse and forward operation. The period of an operating cycle is defined as T_s in Fig. 3. The reciprocal of T_s represents the frequency seen by the transformer. In Fig. 3, the variables n_u and n_l represent the number of inserted VSMs in the upper and lower VSM strings, respectively. The variable $g_{s1/s4}$ represents the gating signal that is common to CSM switches S1 and S4, and $g_{s2/s3}$ represents the gating signal that is common to S2 and S3.

It is clear that the waveforms of Fig. 3 (except the CSM inductor current) are antisymmetric between the first and second half of the operating cycle, mitigating flux accumulation in the transformer. By virtue of this antisymmetry, only the first half of an operating cycle is studied in the following sections. Thus, converter states in Fig. 3 are only defined in the first half with their latter half complementary states denoted by an apostrophe (e.g. 1' is complementary to 1).

A. Power Regulation

Coordinated modulation of both the primary-side VSMs and the secondary-side CSM defines power flow in the bidirectional CS-MMC. Gating of the CSM determines the direction the CSM inductor current is fed into the transformer, thus defining the

transformer secondary current i_s. Gating of the VSMs defines the voltage across the primary winding of the transformer v_p, which can be a positive, negative, or zero voltage. These two quantities, v_p and i_s, completely determine power flow through the transformer.

When the converter is in State 1, CSM switches S_1 and S_4 are conducting and the transformer secondary current equals i_L. There are $N-2$ VSMs inserted in the upper string and N VSMs in the lower string. Assuming each VSM capacitor is balanced with voltage $V_c = V_H/(2N-2)$, the transformer primary voltage equals V_c. This is the power transfer state.

In State 3, all four CSM switches are conducting and $N-1$ VSMs are inserted in both the upper and lower VSM strings. Consequently, there is approximately zero voltage applied across the primary winding of the transformer making State 3 the zero-power transfer state. Furthermore, with zero voltage applied to the transformer leakage inductances, the transformer secondary current i_s is maintained at its value from the end of the previous state as illustrated in Fig. 3. It should also be noted that in contrast to [1], the modulation approach proposed in this article ensures that all four CSM switches are actively gated ON in State 3. This is critical for minimizing body diode conduction losses.

To regulate power transfer, the dc value of the CSM inductor current I_L is controlled. In State 1, the CSM inductor voltage is $r_t V_c - v_L$ (positive) and in State 3 it is $-v_L$ (negative). Thus, by adjustment of each state's duration, control of I_L is achieved through volt-second balance. The duty variable d, which takes on a value between 0 and 0.5, is used to implement this relative duration as shown in Fig. 3.

It is clear the converter must transition between State 1 and State 3. However, in the next two subsections it will be shown that interactions with parasitic elements in the circuit generate high switching stress if direct transitions are attempted. The solution will be to insert intermediate states (State 2 and State 4) at the transition to achieve soft-switching which mitigates switch stress in both reverse and forward operation.

B. Zero-Current CSM Switching for $I_L < 0$

In reverse operation, directly transitioning from State 1 to State 3 without any intermediate state will result in the transformer secondary current i_s being conducted by the same CSM switches in State 3 as in State 1. However, these switches open at the end of State 3 in which case the transformer leakage inductances will force i_s through their drain-to-source capacitances. This generates a high voltage stress which can lead to device failure.

To mitigate high switch stress in reverse operation, it is required that transitions from State 1 to State 3 ensure: 1) commutation of the CSM switch currents; and 2) reversal of the transformer secondary current i_s as shown in Fig. 3.

In [1], CS-MMC modulation was redesigned to always meet these conditions to enable reverse operation. This new current-fed approach inserts a new interval, State 2, at the transition between State 1 and State 3. In State 2, which is also called the overlap interval, all CSM switches are gated ON, decoupling the CSM inductor current i_L and transformer secondary current i_s. In addition, with all CSM switches ON, the VSM gating defines the voltage across the leakage inductances, enabling control of i_s. By adjusting the duration of State 2 (μT_s), the transformer secondary current i_s can be reversed so that CSM switch currents are brought to negative values in State 3 prior to their turn-OFF events. This permits commutation of any residual switch current to the body diodes at turn-OFF transitions, thus achieving ZCS.

At the top of Fig. 4, simplified circuit diagrams are shown depicting the transition process. Current paths are shown in dashed lines with red indicating a decreasing, green indicating an increasing, and purple indicating a steady current.

In State 1, CSM switches S_1 and S_4 conduct and since $I_L < 0$, the transformer secondary current i_s is negative. During State 2, all CSM switches are gated ON so that the VSMs apply a voltage of V_c to the leakage inductances of the transformer. This causes the current in S_1 and S_4 to decrease (red dashed line) and the current in S_2 and S_3 to increase (green dashed line). Once i_L has fully commutated to S_2 and S_3, the converter can enter State 3 where the VSMs are gated to apply zero voltage to the transformer stopping i_s from changing any further.

As illustrated in Fig. 3, there is a minimum duration of μT_s required to ensure ZCS. More specifically, μT_s must be long enough to completely reverse the polarity of i_s resulting in a change of magnitude $2|I_L|$. To calculate this minimum duration, the rate of change of the transformer primary currents can be written in terms of the applied voltage divided by the leakage inductance. This can be referred to the secondary side of the transformer to yield

$$\frac{di_s}{dt} = \frac{1}{r_t}\left(\frac{v_{t,U}(t)}{L_{lk}} + \frac{v_{t,L}(t)}{L_{lk}}\right). \tag{1}$$

As illustrated in Fig. 4, in State 2 the magnitude of the voltage across the leakage inductances is V_c.

Using these voltages and integrating (1) yields

$$\Delta t = \frac{r_t|\Delta i_s|L_{Lk}}{2V_c}. \tag{2}$$

As described previously, the magnitude of the change in transformer secondary current $|\Delta i_s|$ during the overlap must be at least $2|I_L|$. Substituting the duration of the overlap μT_s for Δt, provides a minimum constraint on the overlap variable

$$\mu > \frac{r_t|I_L|L_{Lk}}{V_c T_s}. \tag{3}$$

The condition expressed in (3) provides the basis for computing the required duration of State 2 for ZCS to be achieved. If the duration of State 2 does not meet this condition, current will still be flowing through the switches when they open, generating a high voltage stress.

Overestimating the required overlap causes additional current to circulate in the CSM and VSM strings, leading to higher conduction losses. Thus, in practical implementation of this technique, the overlap variable should be chosen to be as small as possible but with margin to account for parameter estimation error. Fig. 3 depicts this optimal choice where there is a small secondary current overshoot at the end of State 2.

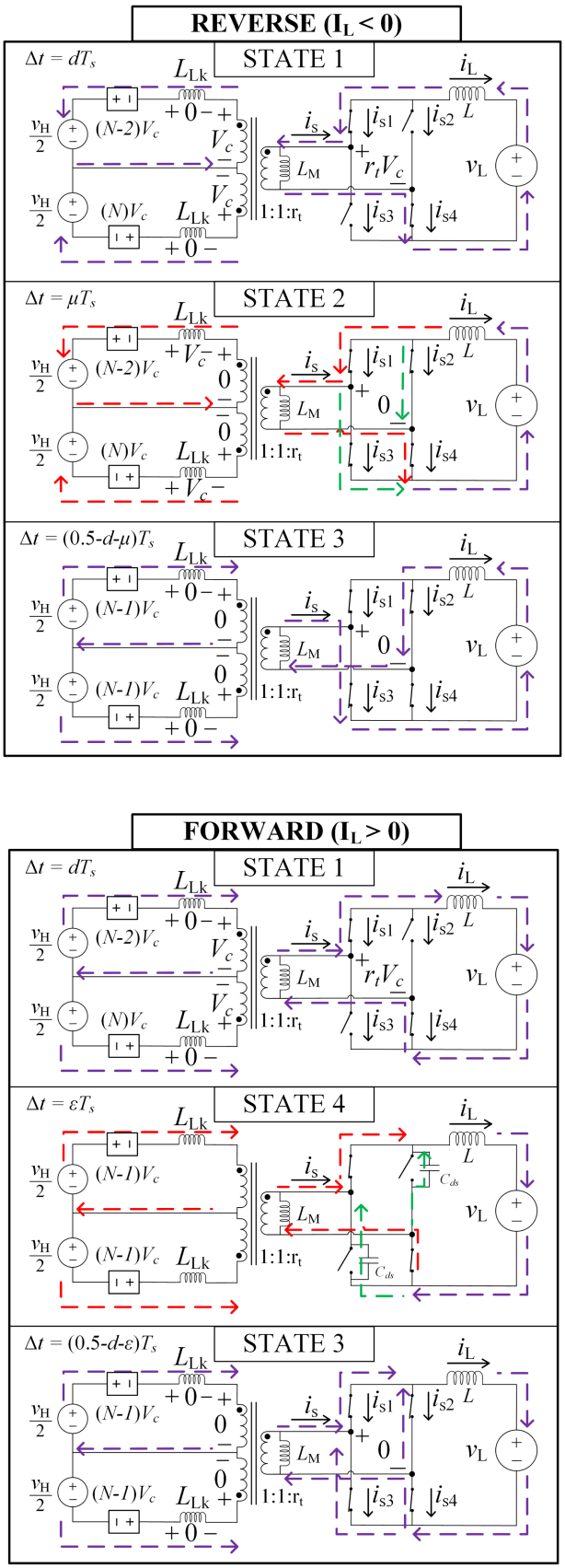

Fig. 4. Simplified diagrams of each converter state.

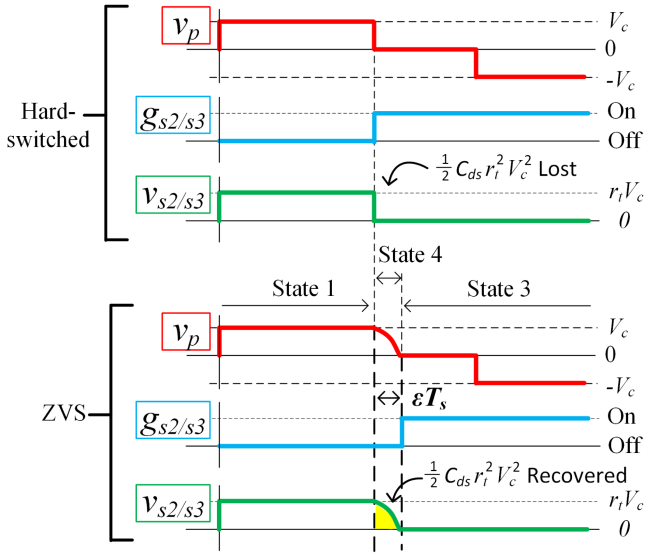

Fig. 5. Waveforms of switch voltages in hard-switched versus ZVS operation.

C. Zero-Voltage CSM Switching for $I_L > 0$

When operating in the forward direction, the duration of State 2 is reduced to zero as ZCS conditions are always ensured by the body diodes. However, if State 2 is simply eliminated, the CSM switches will be turned ON at the same instant the voltage applied to the transformer terminals is removed. As depicted in Fig. 5, this does not provide time for the switch drain-to-source capacitances to discharge, so gating on the switches at this instant dissipates the energy stored in the CSM drain-to-source capacitances.

To avoid these losses in forward operation, the proposed modulation inserts State 4 at the transition from State 1 to State 3 as shown in Fig. 4. In State 4, the turn-ON timing of the CSM switches is delayed by a small amount ϵT_s. As Fig. 5 shows, this allows the drain-to-source capacitances to naturally decay to zero voltage before the switch turns on, thus achieving ZVS and recovering the CSM capacitive energy.

The minimum duration of State 4 (ϵT_s) needed to achieve ZVS can be found by studying how the drain-to-source capacitances discharge in Fig. 5. At the end of State 1, the VSMs apply zero voltage across the transformer terminals. However, the drain-to-source capacitances will initially retain their blocking state voltage. This generates a voltage difference which will appear across the transformer leakage inductances causing a negative current to flow through the drain-to-source capacitances. As a result, the drain-to-source capacitance voltage will fall at an increasing rate until it reaches zero. This process is equivalent to one quarter of the resonant period T_r of the drain-to-source capacitances and transformer leakage inductances, enabling the following calculation:

$$\epsilon T_s > \frac{T_r}{4} = \frac{\pi}{2}\sqrt{r_t^2 L_{\text{lk}} C_{\text{ds}}}. \tag{4}$$

Relative to VSM gating, the converter must delay CSM switch turn-ON events by an amount greater than this minimum threshold for ZVS to be achieved in forward operation.

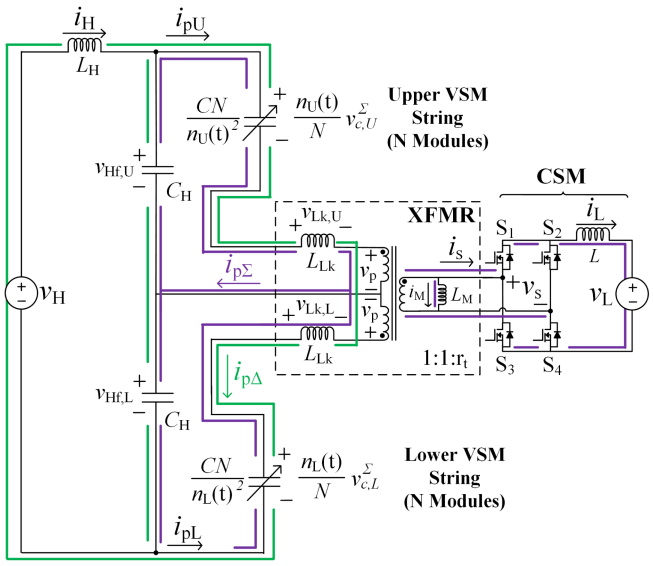

Fig. 6. Equivalent circuit model of bidirectional CS-MMC with principal currents highlighted and VSM strings modeled as variable capacitors.

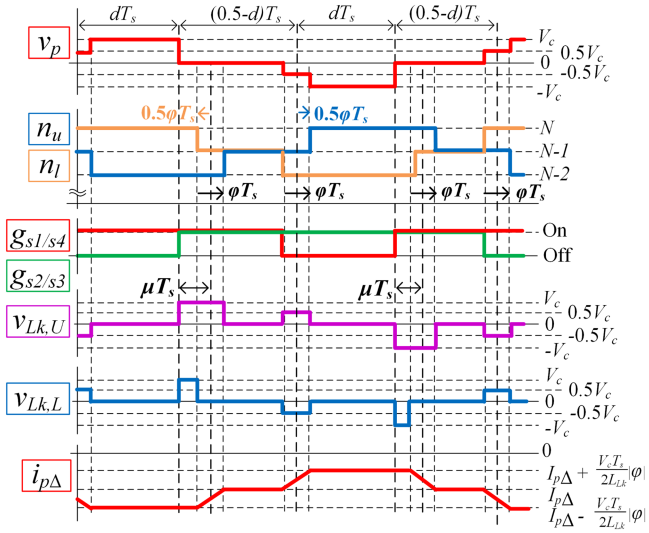

Fig. 7. Converter waveforms with phase-shift balancing in reverse operation.

IV. Equivalent Circuit Representation

In Fig. 6, an equivalent circuit representation of the bidirectional CS-MMC is shown. In this representation it is assumed that the VSMs in a string remain balanced, allowing both strings to be modelled as variable capacitors. Furthermore, the quantities v_{cU}^{Σ} and v_{cL}^{Σ} represent the sum of the VSM capacitor voltages in the upper and lower strings, respectively.

Using this representation, sum and difference quantities of the converter can be defined

$$v_{Hf,\Sigma}(t) = \frac{v_{Hf,U}(t) + v_{Hf,L}(t)}{2} \tag{5}$$

$$v_{Hf,\Delta}(t) = v_{Hf,U}(t) - v_{Hf,L}(t) \tag{6}$$

$$v_{c\Sigma}^{\Sigma}(t) = \frac{v_{cU}^{\Sigma}(t) + v_{cL}^{\Sigma}(t)}{2} \tag{7}$$

$$v_{c\Delta}^{\Sigma}(t) = v_{cU}^{\Sigma}(t) - v_{cL}^{\Sigma}(t) \tag{8}$$

$$i_{p\Sigma}(t) = i_{pU}(t) + i_{pL}(t) \tag{9}$$

$$i_{p\Delta}(t) = \frac{i_{pU}(t) - i_{pL}(t)}{2}. \tag{10}$$

These definitions enable intuitive interpretations for concepts such as balancing since it is easy to see that if $v_{c\Delta}^{\Sigma}(t) = v_{Hf,\Delta}(t) = 0$ the upper and lower VSM strings and dc-blocking capacitors are balanced.

In addition, the principal currents $i_{p\Sigma}$ and $i_{p\Delta}$ have very meaningful interpretations. As shown in Fig. 6, the sum current $i_{p\Sigma}$ is the current which circulates within the converter on the MV side and is directly proportional to the transformer secondary current. Conversely, the difference current $i_{p\Delta}$ experiences flux cancellation in the transformer and flows common to both the upper and lower strings.

V. Capacitor Balancing and State Machine

Voltage balancing of the dc-blocking capacitors and VSMs is essential for proper operation. More specifically, the converter requires voltage balance of the VSM capacitors within and between the upper and lower strings, as well as between the upper and lower dc-blocking capacitors. The following subsections will describe how balancing is achieved.

A. Balancing Between Upper and Lower VSM Strings and Between Upper and Lower DC-Blocking Capacitors

In an ideal CS-MMC, charge balance of both the dc blocking and VSM capacitors is passively achieved as a result of the symmetric topology and operation. However, asymmetries between the upper and lower halves of the converter will always exist due to practical effects such as manufacturing tolerances. These asymmetries result in imbalances between the upper and lower half which can negatively impact operation.

To compensate for practical asymmetries, active balancing is implemented by adding an adjustable phase-shift φT_s between the upper and lower VSM gating patterns as shown in Fig. 7. In an ideal converter, the upper and lower VSM gating patterns are 180° out of phase so that no active power is exchanged between them. However, by adding an additional phase-shift, an ac component is created in $i_{p\Delta}$ which can be used to control power flow between the strings.

For example, if $v_{c\Delta}^{\Sigma}(t) < 0$ the controller can add a phase-shift of φT_s as shown in Fig. 7. This generates an ac component in $i_{p\Delta}$ which is in phase with n_u and out of phase with n_l. This delivers power from the lower string to the upper string causing $v_{c\Delta}^{\Sigma}$ to increase and restore balance. Note that the phase-shift is implemented by delaying n_u by $0.5\varphi T_s$ and advancing n_l by $0.5\varphi T_s$ so that it does not interfere with ZCS.

As shown later in (25) of Section VI-B, the steady-state dc-blocking capacitor voltage imbalance $V_{Hf,\Delta}$ is directly proportional to the voltage imbalance between the upper and

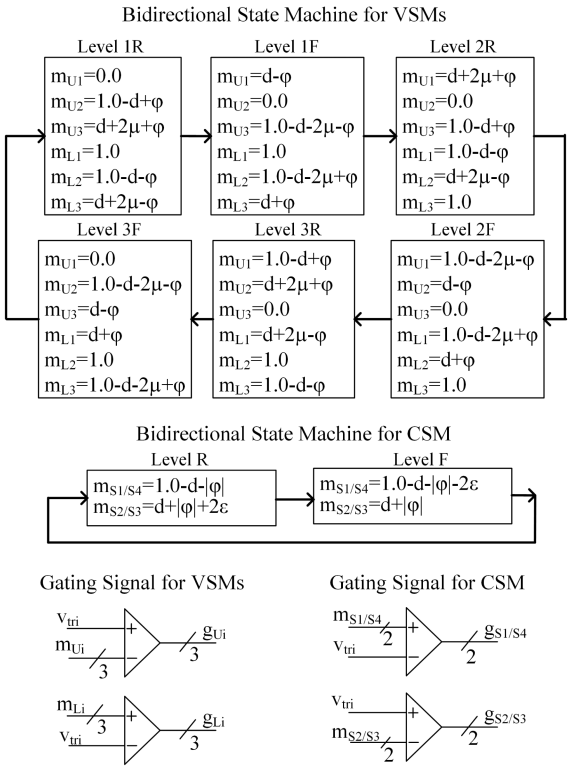

Fig. 8. State machine modulation scheme with phase-shift balancing for bidirectional CS-MMC with $N = 3$ VSMs in each string.

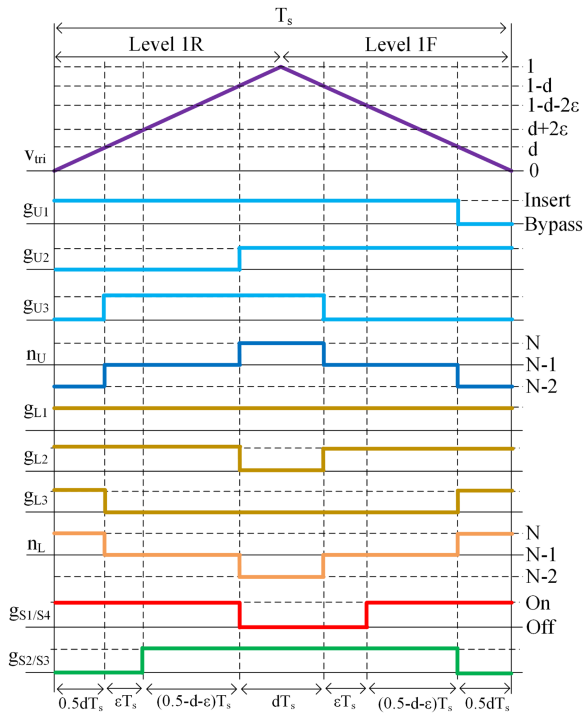

Fig. 9. Visualization of gating pattern generation for one operating period in forward operation with $\varphi = 0$. Duration of ϵT_s exaggerated for visibility.

lower strings $V_{c\Delta}^{\Sigma}$. Thus, as a consequence of balancing the VSM strings with φT_s, the dc-blocking capacitors will also balance.

B. Balancing Within VSM Strings

To create the desired n_u and n_l waveforms, each VSM in a string must be gated with a certain pattern. As some of these patterns are different, the charge accumulated by VSM capacitors over an operating cycle will be different, leading to imbalance. To achieve balancing, a state machine is used to rotate the gating pattern between VSMs in a string over consecutive operating cycles. Thus, over N operating cycles, each VSM in a string will have the same gating pattern (with shifted phases) resulting in net charge balance.

Fig. 8 shows a state machine for a converter with $N = 3$ modules. This state machine has $2N = 6$ levels in total with each level comprising a number and the letter R or F. A single symmetric triangular carrier v_{tri} is used with the state machine where levels containing R coincide with the rising edge of v_{tri}, and levels containing F coincide with the falling edge.

In each level, all of the VSMs are assigned a modulation index m, which is compared with v_{tri} according to Fig. 8. This generates the gating pattern g shown in Fig. 9. The number in each level designates a rotation of the modulation indices given to the VSMs in a string. For example, in Fig. 8 notice that the lower VSM assigned 1.0 as its modulation index is rotated for levels with different numbers (i.e., Level 1R, Level 2R, and Level 3R).

Gating of the CSM also utilizes a state machine (Fig. 8) and the same carrier v_{tri} (Fig. 9). This enables coordinated gating of the CSM and VSMs required for bidirectional operation. However, as there is no rotation of the gating pattern, the CSM state machine consists of only a Level R and Level F.

An advantage with the state machine approach is that measurements of VSM voltages are not needed, minimizing system cost and complexity. Also notice that not all VSMs are switched over an operating period in Fig. 9. This is the frequency multiplication effect mentioned earlier.

VI. Circuit Analysis

To inform the design of controllers for power regulation and phase-shift balancing, time-averaged dynamic models of the converter must be developed. The first step in the derivation of these models is to utilize Figs. 3 and 6 to express the instantaneous state equation of every circuit element during each interval of an operating cycle. As the relative duration of State 2 and 4 are negligible compared to State 1 and State 3, these intervals can be neglected. Furthermore, by using (5)–(10) the state equations can be expressed in terms of the sum and difference variables. Finally, by applying state-space averaging with the small-ripple approximation, the time averaged large signal model of the converter can be developed as discussed in the following section. Note that the small-ripple approximation cannot be applied to $i_{p\Delta}$ as this will fail to capture the effect of the phase-shift balancing.

A. Time-Averaged Large Signal Model

The following set of equations form the time-averaged large signal model of the converter. The operator $\langle\cdot\rangle_{T_s}$ is used to denote the average value over an operating cycle.

$$L_H\frac{d\langle i_H(t)\rangle_{T_s}}{dt} = \langle v_H(t)\rangle_{T_s} - 2\langle v_{Hf,\Sigma}(t)\rangle_{T_s} \tag{11}$$

$$C_H\frac{d\langle v_{Hf,\Sigma}(t)\rangle_{T_s}}{dt} = \langle i_H(t)\rangle_{T_s} - \langle i_{p\Delta}(t)\rangle_{T_s} \tag{12}$$

$$C_H\frac{d\langle v_{Hf,\Delta}(t)\rangle_{T_s}}{dt} = -r_t\langle i_M(t)\rangle_{T_s} \tag{13}$$

$$C\frac{d\langle v^{\Sigma}_{c,\Sigma}(t)\rangle_{T_s}}{dt} = -r_t d(t)\langle i_L(t)\rangle_{T_s} + (N-1)\langle i_{p\Delta}(t)\rangle_{T_s} \tag{14}$$

$$C\frac{d\langle v^{\Sigma}_{c,\Delta}(t)\rangle_{T_s}}{dt} = r_t(N-1)\langle i_M(t)\rangle_{T_s} + \frac{2T_sV_c}{L_{lk}}d(t)\varphi(t) \tag{15}$$

$$L_{lk}\frac{d\langle i_{p\Delta}(t)\rangle_{T_s}}{dt} = \langle v_{Hf,\Sigma}(t)\rangle_{T_s} - \frac{N-1}{N}\langle v^{\Sigma}_{c,\Sigma}(t)\rangle_{T_s} \tag{16}$$

$$L_M\frac{d\langle i_M(t)\rangle_{T_s}}{dt} = \frac{r_t}{2}\langle v_{Hf,\Delta}(t)\rangle_{T_s} - \frac{r_t(N-1)}{2N}\langle v^{\Sigma}_{c,\Delta}(t)\rangle_{T_s} \tag{17}$$

$$L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = \frac{2r_td(t)}{N}\langle v^{\Sigma}_{c,\Sigma}(t)\rangle_{T_s} - \langle v_L(t)\rangle_{T_s}. \tag{18}$$

B. Steady State Relations

By setting the time derivatives of (11)–(18) to zero and replacing the time-averaged quantities with their dc values, the following steady state relationships can be found:

$$V_{Hf,\Sigma} = \frac{1}{2}V_H \tag{19}$$

$$I_{p\Delta} = I_H \tag{20}$$

$$I_M = 0 \tag{21}$$

$$I_H = \frac{r_tD}{N-1}I_L \tag{22}$$

$$\Phi = 0 \tag{23}$$

$$V_c = \frac{V^{\Sigma}_{c,\Sigma}}{N} = \frac{V_H}{2N-2} \tag{24}$$

$$V_{Hf,\Delta} = \frac{N-1}{N}V^{\Sigma}_{c,\Delta} \tag{25}$$

$$D = \frac{(N-1)V_L}{r_tV_H} \tag{26}$$

where (23) is valid only for a perfectly symmetric converter.

C. Linearized Small Signal Model

To derive transfer functions for each control variable, the time-averaged large signal model (11)–(18) must be linearized. Replacing each time-averaged quantity $\langle x\rangle_{T_s}$ with its dc value plus a small-signal component $X+\hat{x}(t)$ and retaining only first-order terms yields the linearized small-signal model

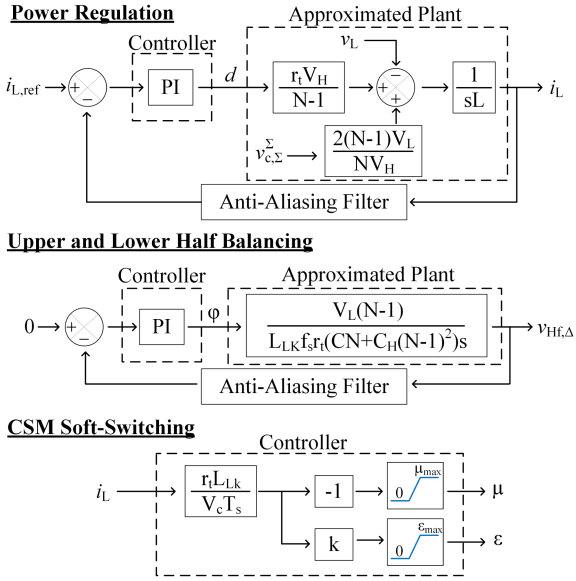

Fig. 10. Control block diagrams for each control variable.

$$L_H\frac{d\hat{i}_H(t)}{dt} = \hat{v}_H(t) - 2\hat{v}_{Hf,\Sigma}(t) \tag{27}$$

$$C_H\frac{d\hat{v}_{Hf,\Sigma}(t)}{dt} = \hat{i}_H(t) - \hat{i}_{p\Delta}(t) \tag{28}$$

$$C_H\frac{d\hat{v}_{Hf,\Delta}(t)}{dt} = -r_t\hat{i}_M(t) \tag{29}$$

$$C\frac{d\hat{v}^{\Sigma}_{c,\Sigma}(t)}{dt} = (N-1)\hat{i}_{p\Delta}(t) - \frac{(N-1)V_L}{V_H}\hat{i}_L(t) - r_tI_L\hat{d}(t) \tag{30}$$

$$C\frac{d\hat{v}^{\Sigma}_{c,\Delta}(t)}{dt} = r_t(N-1)\hat{i}_M(t) + \frac{V_L}{r_tL_{lk}f_s}\hat{\varphi}(t) \tag{31}$$

$$L_{lk}\frac{d\hat{i}_{p\Delta}(t)}{dt} = \hat{v}_{Hf,\Sigma}(t) - \frac{N-1}{N}\hat{v}^{\Sigma}_{c,\Sigma}(t) \tag{32}$$

$$L_M\frac{d\hat{i}_M(t)}{dt} = \frac{r_t}{2}\hat{v}_{Hf,\Delta}(t) - \frac{r_t(N-1)}{2N}\hat{v}^{\Sigma}_{c,\Delta}(t) \tag{33}$$

$$L\frac{d\hat{i}_L(t)}{dt} = \frac{2(N-1)V_L}{NV_H}\hat{v}^{\Sigma}_{c,\Sigma}(t) + \frac{r_tV_H}{N-1}\hat{d}(t) - \hat{v}_L(t). \tag{34}$$

VII. Control Design

Utilizing the Laplace transformation with (27)–(33), the approximate transfer functions for the duty and phase-shift control variables can be found as shown in Fig. 10. Properly tuned PI controllers can effectively stabilize both closed-loop systems with zero-error tracking.

It should be noted that the phase-shift transfer function is technically third order. However, it can be shown that the two

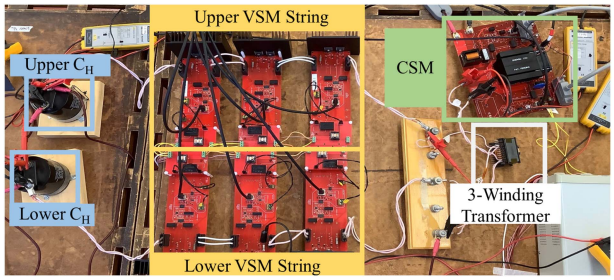

Fig. 11. Photograph of laboratory-scale experimental setup.

TABLE I
CIRCUIT PARAMETERS OF EXPERIMENTAL SETUP

Symbol	Parameter	Value
V_H	MVDC network voltage, EA-PSB 12000-40 4U	1 kV
V_L	LVDC network voltage, Regatron TC.GSS.32.400.100	100 V
P_o	Rated output power	3 kW
N	Number of VSMs per string	3
T_s	Operating cycle duration	20 µs
f_{ac}	Transformer ac frequency $(1/T_s)$	50 kHz
$f_{\text{sw},VSM}$	VSM switching frequency $(2f_{\text{ac}}/N)^*$	33.3 kHz
V_c	Nominal VSM capacitor voltage	250 V
C	VSM capacitance	5 µF
–	Ratio of VSM energy storage to rated power $(\frac{1}{2}CV_c^2 2N/P_o)$	0.3 J/kW
r_t	Transformer turns ratio	0.5
L_{lk}	Transformer leakage inductance	16 µH
L_M	Transformer magnetizing inductance	167 µH
–	Transformer core material ETD 45959EC	-
L	CSM inductance	33 µH
C_H	DC-blocking capacitance	160 µF
L_H	MVDC input inductance	26 µH
–	CSM RCD snubber capacitance	0.1 µF
–	CSM RCD snubber resistance	330 Ω
–	VSM MOSFET C3M0021120K	–
$S_1 - S_4$	CSM MOSFET C3M0015065K	–

*This represents the VSM switching frequency averaged over NT_s.

high-frequency poles are sufficiently damped by parasitic resistances provided they are not excited by controller action. This is ensured by the antialiasing filters, allowing them to be neglected in the transfer function of Fig. 10.

Control variables μ and ϵ are calculated by an open-loop controller designed to meet the conditions for ZCS and ZVS developed in Section III. As shown in Fig. 10, both μ and ϵ are simply equal to a constant multiplied by i_L.

VIII. EXPERIMENTAL RESULTS

The experimental setup used for testing of the bidirectional CS-MMC is shown in Fig. 11. The laboratory-scale prototype has a rated power of 3 kW and interfaces between a 1 kV and a 100 V dc network (10:1 step ratio). Additional circuit parameters of this setup are listed in Table I. For sizing and component selection, the guidelines found in [10] were used.

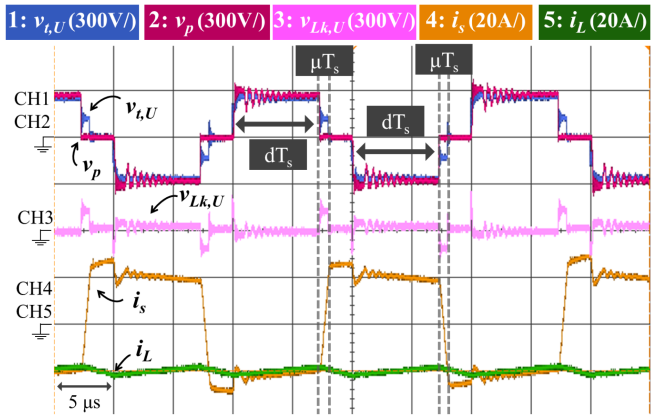

Fig. 12. Reverse operation oscilloscope waveform capture with overlap and duty intervals labelled.

A. Steady State Reverse Operation Results

Fig. 12 shows regulation of the CSM inductor current $I_L = -20$ A in reverse operation without any high switch stress present. The duty and overlap interval μT_s can clearly be seen in Fig. 12 with the waveforms closely matching the behavior predicted in theory (Fig. 3). The overlap is most clearly visible in the leakage inductance voltage waveform (CH3). During the overlap it can be seen that the secondary current (CH4) reverses its polarity to reach a magnitude slightly greater than the CSM inductor current (CH5). The small overshoot of the secondary current during the overlap is due to the conservative calculation of μ by the controller as discussed earlier.

Note the small ringing present in the transformer terminal voltage (CH1) and primary voltage (CH2) waveforms. This is caused by parasitic resonance between the transformer leakage inductances and the CSM MOSFET drain-to-source capacitances. The resonance is excited by step changes in the transformer terminal voltage applied by VSM gating. Note that this phenomenon is distinct from ringing caused by interruption of an inductor conduction path. An RCD snubber (parameters listed in Table I) is installed on the CSM to mitigate the ringing. Further details regarding snubber design and this phenomenon can be found in [30].

In Fig. 13, the current of CSM switch S_3 (CH3) can be seen along with its gate-to-source voltage (CH1) during reverse operation. Notice that the switch current (CH3) is negative whenever the gate-to-source voltage (CH1) transitions to its OFF-state voltage. As the small negative current can commutate to the switch body diode, this confirms ZCS is achieved.

B. Steady State Forward Operation Results

Fig. 14 shows regulation of the CSM inductor current $I_L = 20$ A in forward operation. The transformer terminal (CH1) and primary (CH2) voltages are shown along with the transformer secondary current (CH4) and CSM inductor current (CH5). The duty interval can be seen labeled with the waveforms again closely matching theory (Fig. 3).

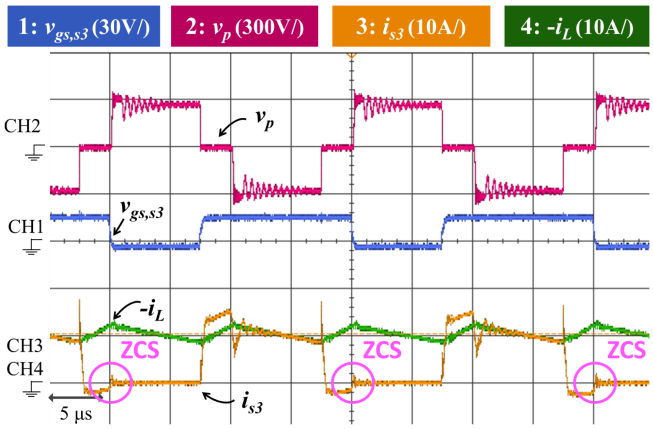

Fig. 13. Reverse operation oscilloscope waveform capture showing ZCS.

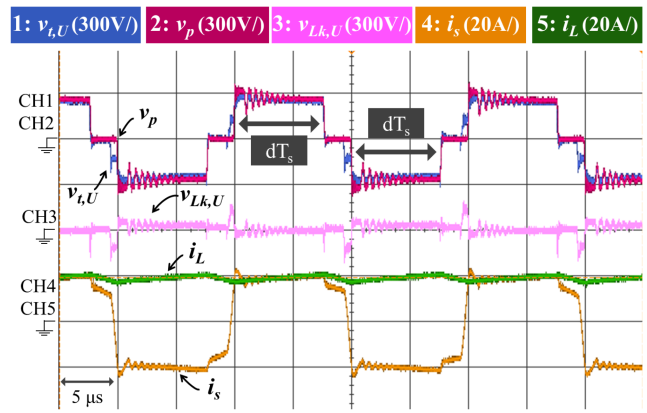

Fig. 14. Forward operation oscilloscope capture with duty interval labeled.

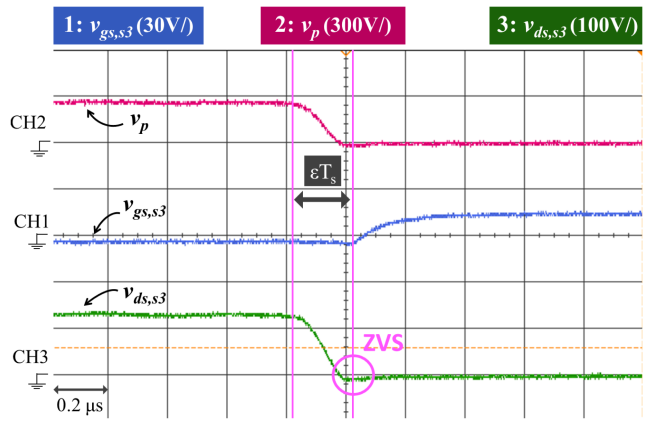

Fig. 15. Forward operation oscilloscope capture showing ZVS.

In Fig. 15, the drain-to-source voltage (CH3) of CSM switch S_3 along with its gate-to-source voltage (CH1) can be seen with the transformer primary voltage (CH2) during forward operation. It can be seen that the drain-to-source voltage reaches zero before the gate-to-source voltage transitions to its ON-state value, confirming that ZVS is achieved.

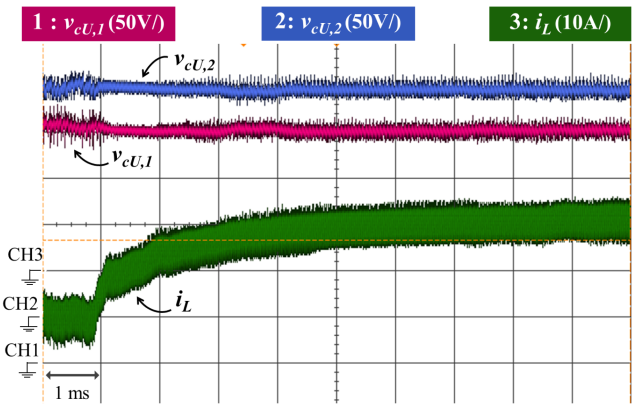

Fig. 16. Transient oscilloscope capture showing a transition from reverse to forward power transfer (−10 A to 10 A) with VSM balancing.

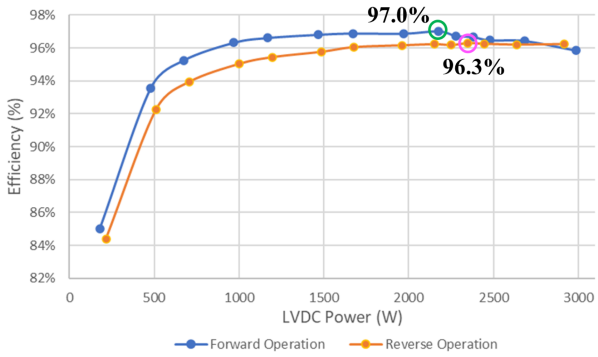

Fig. 17. Experimentally measured efficiencies for various power levels.

C. Transient Results

Fig. 16 shows a –10 A (reverse) to 10 A (forward) transient, with the CSM inductor current i_L (CH3) displayed. Two upper string VSM capacitor voltages (CH1 and CH2) are also shown. The CSM inductor current experiences a smooth transition between the reference setpoints. The VSM waveforms show that the VSM capacitor voltages always remain close to their nominal value V_c, demonstrating that the state machine and phase-shift active balancing are operating effectively.

D. Efficiency

The measured efficiency of the bidirectional CS-MMC in both forward and reverse operation can be seen in Fig. 17. The converter achieves peak efficiencies of 97.0% at 2.2 kW and 96.3% at 2.3 kW in forward and reverse operation, respectively. Similar efficiencies are also maintained over a wide operating range. It should be noted that the peak reverse efficiency in Fig. 17 is higher than that found previously in [1]. This is a result of the new modulation minimizing the body diode conduction time as described earlier.

IX. Conclusion

This article proposes a new variant of the CS-MMC with bidirectional power transfer capability, making it a fully featured

candidate for interfacing LVDC and MVDC networks. The proposed current-fed modulation leverages partial soft-switching, self-balancing of VSMs, and frequency multiplication effects to enable highly efficient operation in a power dense, cost-effective structure. Furthermore, the proposed active-balancing between the converter upper and lower VSM strings and dc-blocking capacitors successfully prevents imbalance while not interfering with soft-switching conditions. Experimental results are presented displaying transient and steady state results obtained from a prototype operating between 1 kV and 100 V dc networks. Recorded maximum efficiencies of 97.0% and 96.3% are demonstrated in forward and reverse operation, respectively.

REFERENCES

[1] P. A. Gray, N. J. B. Hosein, X. Lan, and P. W. Lehn, "A bidirectional current-fed isolated MMC with zero-current switching for high step ratio DC-DC applications," in *Proc. 11th Int. Conf. Power Electron. ECCE Asia*, 2023, pp. 629–635.

[2] WG C6.31, "Medium voltage direct current (MVDC) grid feasibility study," CIGRE, Technical brochure TB793, 2020.

[3] WG C6/B4.37, "Medium voltage DC distribution systems," CIGRE, Technical brochure TB875, 2022.

[4] M. A. Shamshuddin, F. Rojas, R. Cardenas, J. Pereda, M. Diaz, and R. Kennel, "Solid state transformers: Concepts, classification, and control," *Energies*, vol. 13, no. 9, May 2020, Art. no. 2319.

[5] J. Yao, W. Chen, C. Xue, Y. Yuan, and T. Wang, "An ISOP hybrid DC transformer combining multiple SRCs and DAB converters to interconnect MVDC and LVDC distribution networks," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11442–11452, Nov. 2020.

[6] B. Zhao, Q. Song, J. Li, W. Liu, G. Liu, and Y. Zhao, "High-frequency-link DC transformer based on switched capacitor for medium-voltage DC power distribution application," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4766–4777, Jul. 2016.

[7] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC–DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[8] L. Zheng et al., "SiC-based 5-kV universal modular soft-switching solid-state transformer (M-S4T) for medium-voltage DC microgrids and distribution grids," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11326–11343, Oct. 2021.

[9] P. A. Gray and P. W. Lehn, "The current shaping modular multilevel DC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10050–10063, Oct. 2020.

[10] P. A. Gray, Z. C. Ma, and P. W. Lehn, "A high-frequency MMC for DC–DC applications using a three-winding transformer with DC flux cancellation," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 3, pp. 647–657, Jul. 2022.

[11] P. A. Gray, P. W. Lehn, and N. Yakop, "A modular multilevel DC–DC converter with flying capacitor converter like properties," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6774–6783, Jul. 2022.

[12] H. Saeedifard and A. Yazdani, "Modeling and soft-switching operation of an isolated modular-multilevel-converter-based DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–8.

[13] S. Bazyar, J.-H. Jung, R. Li, H. Beiranvand, and M. Liserre, "Losses analysis of MMC in medium frequency medium voltage DAB converter for charging station," in *Proc. 25th Eur. Conf. Power Electron. Appl.*, 2023, pp. 1–9.

[14] I. Pitel, "Current-fed power processing-ride through robustness [expert view]," *IEEE Power Electron. Mag.*, vol. 6, no. 1, pp. 58–62, Mar. 2019.

[15] M. Iurich et al., "Bidirectional DC-DC converter supplying pulsed current for solid oxide fuel-cell," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2023, pp. 2189–2196.

[16] A. K. Rathore, "Current-fed DC/DC converters for high voltage gain and low voltage high current applications: An overview of topologies and modulation techniques," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst.*, 2016, pp. 1–6.

[17] S.-K. Chung, J.-G. Lim, and Y. Song, "Active clamped three-phase isolated boost converter with series output connection for high step-up applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 1090–1097.

[18] R. Watson and F. Lee, "A soft-switched, full-bridge boost converter employing an active-clamp circuit," in *Proc. 27th Annu. IEEE Power Electron. Specialists Conf.*, 1996, pp. 1948–1954.

[19] V. Yakushev, V. Meleshin, and S. Fraidlin, "Full-bridge isolated current fed converter with active clamp," in *Proc. APEC Fourteenth Annu. Appl. Power Electron. Conf. Expo. Conf. Proc.*, 1999, pp. 560–566.

[20] W. Song and B. Lehman, "Current-fed dual-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 461–469, Mar. 2007.

[21] A. K. Rathore and U.R. Prasanna, "Analysis, design, and experimental results of novel snubberless bidirectional naturally clamped ZCS/ZVS current-fed half-bridge DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4482–4491, Oct. 2013.

[22] D. Sha, X. Wang, K. Liu, and C. Chen, "A current-fed dual-active-bridge DC–DC converter using extended duty cycle control and magnetic-integrated inductors with optimized voltage mismatching control," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 462–473, Jan. 2019.

[23] X. Sun, X. Wu, Y. Shen, X. Li, and Z. Lu, "A current-fed isolated bidirectional DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6882–6895, Sep. 2017.

[24] F. Wu, S. Fan, and S. Luo, "Elimination of transient current mutation and voltage spike for buck–boost current-fed isolated DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10928–10937, Nov. 2021.

[25] V. Rathore, K. Rajashekara, A. Ray, L. A. G. Rodriguez, and J. Mueller, "A current-fed high gain multilevel DC-DC converter for BESS grid integration applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1964–1970.

[26] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[27] Y. Zhang, Z. Wang, Y. W. Li, N. Hou, and M. Cheng, "Decoupled dual-PWM control for naturally commutated current-fed dual-active-bridge DC/DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4246–4259, Dec. 2020.

[28] X. Pan, F. Yang, L. Li, R. Zhang, and C. Wang, "An improved modulation scheme of active commutated current-fed bidirectional DC/DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1375–1388, Apr. 2021.

[29] A. Blinov, R. Kosenko, D. Vinnikov, and L. Parsa, "Bidirectional isolated current-source DAB converter with extended ZVS/ZCS range and reduced energy circulation for storage applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10552–10563, Dec. 2020.

[30] S.-Y. Lin and C.-L. Chen, "Analysis and design for RCD clamped snubber used in output rectifier of phase-shift full-bridge ZVS converters," *IEEE Trans. Ind. Electron.*, vol. 45, no. 2, pp. 358–359, Apr. 1998.

Philippe A. Gray (Member, IEEE) received the B.A.Sc. (Hons.) degree in engineering science, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, ON, Canada, in 2010, 2013, and 2022, respectively.

From 2012 to 2013, he was a Visiting Researcher with ABB Corporate Research, Västerås, Sweden. From 2014 to 2017, he was a System Design Engineer with General Electric, Stafford, U.K. From 2022 to 2023, he was a Senior Power Electronics Engineer with Lucid Motors, California, USA. From 2023, he has been an Assistant Professor with the University of Calgary, Calgary, AB, Canada. His current research interests include multilevel converters, power electronics for electric vehicle applications, and the grid integration of distributed resources.

Noah J. B. Hosein (Student Member, IEEE) received the B.A.Sc. degree in engineering science, in 2023, from the University of Toronto, Toronto, ON, Canada, where he is currently working toward the M.A.Sc. degree in electrical engineering.

His research interests include solid-state transformer design and optimization, advanced modeling techniques for power electronic circuits, and grid integration of clean energy technologies.

Xi Lan (Member, IEEE) received the B.A.Sc (Hons.) degree in engineering science and the M.A.Sc degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2021 and 2024, respectively.

Her research interests include high-frequency and high-density power converter design and control, with a particular emphasis on emerging applications of modular multilevel converters.

Peter W. Lehn (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees from the University of Manitoba, Winnipeg, MB, Canada, and the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, all in electrical engineering.

In 1999, he joined the Faculty of the University of Toronto. In 2005, he was a Visiting Professor with the University of Erlangen, Nuremberg, Erlangen, Germany. His current research interests include HVDC technologies, grid integration of storage and renewables, power electronics for electric vehicles, and theoretical analysis of power electronic systems.

Dr. Lehn was recipient of the 2022 IEEE Canada P.D. Ziogas Electric Power Award. He served as an Editor for IEEE TRANSACTIONS ON ENERGY CONVERSION from 2013 to 2019, and co-chaired IEEE COMPEL in 2019.