Small-Signal Modeling and Loss Analysis of Capacitor-Current Dynamic Freewheeling Controlled PCCM SIDO Buck Converter

Shuhan Zhou, *Member, IEEE*, Xiaomeng Zhang, and Guohua Zhou, *Senior Member, IEEE*

***Abstract*—The pseudocontinuous-conduction mode (PCCM) can be used in the single-inductor multiple-output (SIMO) dc–dc converter to achieve minimized cross-regulation, which will suffer the restrictions of limited load-range and low light-load efficiency. In this article, a capacitor-current dynamic-freewheeling control scheme for PCCM SIMO dc-dc converter is proposed to overcome these restrictions. Taking PCCM single-inductor dual-output (SIDO) buck converter as an example, a complete and accurate small-signal model is established to guide the error amplifier design. Then, the cross-regulation and transient response are explored via impedance transfer functions. With the employment of DF controller, the freewheeling current and the freewheeling period are updated in real-time via load current and capacitor current, which can improve the light-loading efficiency and broaden the load-range. Finally, the effectiveness of the theoretical analysis is verified by experimental results. These results show that the proposed control scheme is more suitable for the PCCM SIDO dc–dc converter to improve efficiency, broaden load range, suppress cross-regulation and enhance transient performance.**

***Index Terms*—Cross-regulation, efficiency, load range, pseudocontinuous-conduction mode (PCCM), single-inductor dual-output (SIDO) dc–dc converter.**

I. Introduction

NOWADAYS, multioutput dc–dc converters are commonly used in electric vehicle auxiliary power supplies [1], renewable energy systems [2], [3], portable power electronic devices [4], etc. Among these multioutput dc–dc converters, the single-inductor multiple-output (SIMO) dc–dc converters have attracted much attention and become more and more popular due to their low cost and high-power density [5], [6], [7], [8], [9], [10], [11].

There are mainly three types of operation mode for the SIMO dc–dc converter, the continuous conduction mode (CCM) [2], [7], [8], [9], the discontinuous conduction mode (DCM) [10], [11], and the pseudocontinuous-conduction mode (PCCM) [12], [13], [14], [15]. In CCM, the power flow coupling among different outputs is inevitable, which leads to deterioration in the accuracy and stability of the output. This phenomenon is called cross-regulation [7], [8], [9]. Time-multiplexing method has been developed to control the SIMO dc–dc converter to operate in DCM, which successfully suppresses cross-regulation [10], [11]. However, the large amplitude of the inductor current ripple under heavy load conditions impacts output voltages ripple, switching noise and dynamic response. In PCCM, the freewheeling period between different outputs is introduced to isolate the outputs [12], [13], [14], [15]. As long as this freewheeling period does not disappear during load change, the outputs are regulated independently and there is no cross-regulation. The main drawbacks are limited load-range and extra power loss during the freewheeling period.

Various control schemes have been proposed to suppress the cross-regulation in the CCM SIMO dc–dc converter [7], [8], [9] and improve the efficiency in the PCCM SIMO dc–dc converter [12], [13], [14], [15]. In [7] and [9], the current-mode control was introduced to obtain the fast transient response and low cross-regulation. Zhang et al. [8] developed a deadbeat-based control for the SIMO converter to solve the cross-regulation problem. Although the advanced control schemes can partly suppress cross-regulation, they cannot absolutely eliminate it. To improve the efficiency and maintain the minimized cross-regulation in PCCM SIMO dc–dc converter, a lot of researchers study dynamic freewheeling (DF) control techniques [13], [14], [15]. A hybrid mode control for PCCM single-inductor dual-output (SIDO) buck converter is presented in [13], [14], and [15]. It operates in PCCM with a single freewheel phase to reduce switching loss and minimize cross regulation. In [13], by employing an on-line charge meter, the freewheel switching current of the converter is instantaneously adjusted based on load conditions so that conduction loss in the freewheel switch is minimized. For this type of method, the cross-regulation still exists when the load-step occurs in non-PCCM phase. Thus, it is of great significance to develop an effective and practical control scheme for PCCM SIMO dc–dc converter with high efficiency, wide load range and minimized cross-regulation.

Up to now, many modeling methods have been developed in the literature to predict the transient response of CCM SIDO dc–dc converters. However, little report was involved with the

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Shuhan Zhou is with the College of Electrical Engineering, Sichuan University, Chengdu 610065, China (e-mail: shzhou@scu.edu.cn).

Xiaomeng Zhang and Guohua Zhou are with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 611756, China (e-mail: yj2017112354@my.swjtu.edu.cn; eeghzhou@swjtu.edu.cn).

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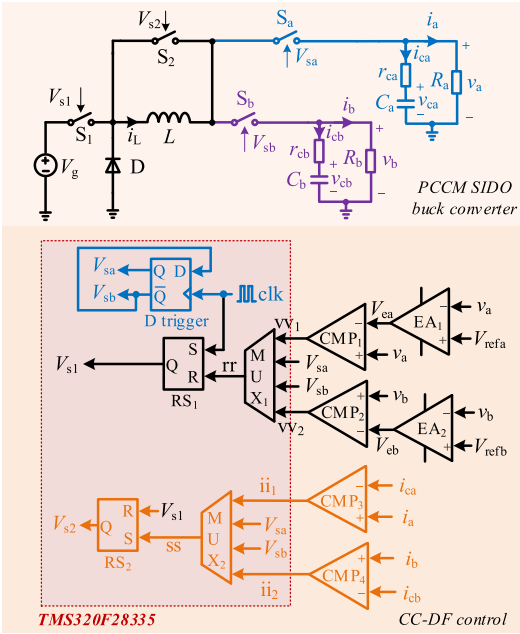

Fig. 1. CC-DF controlled PCCM SIDO buck converter.

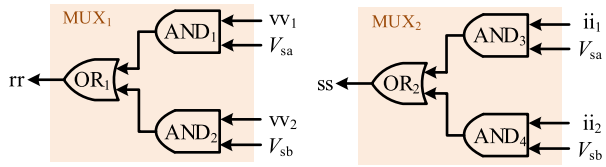

Fig. 2. Schematic of multiplexer MUX_1 and MUX_2.

PCCM SIDO dc–dc converter, especially considering the DF control. Only one literature presents the modeling of constant-freewheeling (CF) controlled PCCM SIDO dc–dc converter [16], while the light-load efficiency is poor. Compared to CCM SIDO dc–dc converters and PCCM SIDO dc–dc converter with CF control, developing a small-signal model for PCCM with DF control is challenging due to the presence of four duty-ratios in one switching period. Moreover, these four duty-ratios are coupled resulting in complex transfer functions. However, it is a useful tool for deriving the loop gain transfer functions and closed-loop transfer functions for studying transient response and designing controller.

In this article, a capacitor-current dynamic-freewheeling (CC-DF) control is proposed for the PCCM SIMO dc–dc converter to improve the efficiency, widen the load range and guarantee that the converter maintains minimized cross-regulation and fast transient response. The main contributions of this article are as follows.

1) A CC-DF control scheme for PCCM SIMO dc–dc converter is first proposed. In this scheme, the freewheeling current value and freewheel switching duration are adaptively and continuously adjusted according to the instantaneous load condition, which can achieve low conduction loss. Moreover, different outputs are isolated, and the freewheeling current value is only related to the corresponding load current and capacitor current. Thus, the cross-regulation is minimized. The proposed controller also accelerates the duty ratio adjustment process during the load transient periods.
2) A complete and accurate small-signal model for CC-DF controlled PCCM SIMO dc–dc converter is established. The small-signal model of PCCM converter is practical because it consists of four duty-ratios in one switching period. Similarly, the small-signal model of CC-DF controller is also challenging due to the presence of DF control. Moreover, the four duty-ratios and the controller are coupled, resulting in complex transfer functions. The proposed unified small-signal model is validated through the circuit simulation software SIMPLES.
3) The theoretical analysis of transient performance, cross-regulation, efficiency and load range under CC-DF control and traditional voltage-mode/voltage-ripple constant-freewheeling (VM/VR-CF) control is derived. All of these are verified by the experimental results.

Taking CC-DF controlled PCCM SIDO buck converter as the research object, the rest of this article is organized as follows. The operating principles are presented in Section II. In Section III, the small-signal model, the error amplifier (EA) design, and the theoretical analysis of cross-regulation and transient response are emphatically investigated. Section IV illustrates the load range and the power loss of the proposed CC-DF control and VM/VR-CF control. Section V presents the experimental waveforms to verify the effectiveness of the proposed control scheme. Finally, Section VI concludes this article.

II. CC-DF Control Scheme for PCCM SIDO Buck Converter

A. Operation Principle of CC-DF Controlled PCCM SIDO Buck Converter

Fig. 1 shows a PCCM SIDO buck converter under CC-DF control, where V_g is the input voltage, L is the inductor, C_a and C_b are the output capacitors, r_{ca} and r_{cb} are the equivalent series resistances (ESRs) of the output capacitors, R_a and R_b are the load resistances, i_L is the inductor current, i_{ca} and i_{cb} are the output capacitor currents, i_a and i_b are the load currents, v_a and v_b are the output voltages, $V_{si(i\,=\,1,\,2,\,a,\,b)}$ are the duty cycle signals of $S_{i(i\,=\,1,\,2,\,a,\,b)}$, respectively. Its control circuit consists of one time-multiplexing control loop, two voltage-ripple control loops, and two CC-DF control loops, includes two error amplifiers EA_1 and EA_2, four comparators $\mathrm{CMP}_{i\ (i\,=\,1,\,2,\,3,\,4)}$, two multiplexers MUX_1 and MUX_2, two RS triggers RS_1 and RS_2, a D trigger, and a clock signal clk. The multiplexers are shown in Fig. 2, which consists of two AND gates, and a OR gate.

In the hardware circuit, the control circuit, including two multiplexers MUX_1 and MUX_2, two RS triggers RS_1 and RS_2, a D trigger, and a clock signal clk, is realized using the DSP TMS320F28335, which means DSP mainly implements the logical calculation.

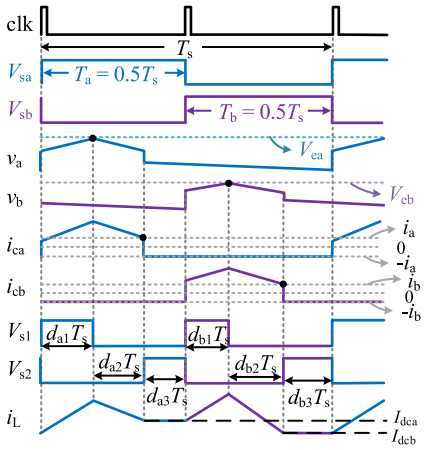

Fig. 3. Key waveforms of PCCM SIDO buck converter under CC-DF control.

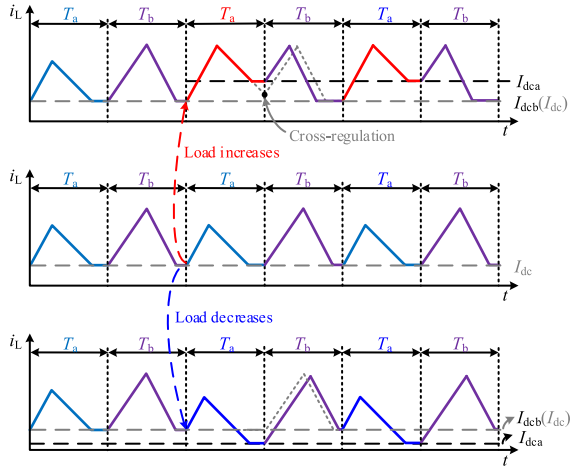

Fig. 4. Inductor current waveforms with load variations.

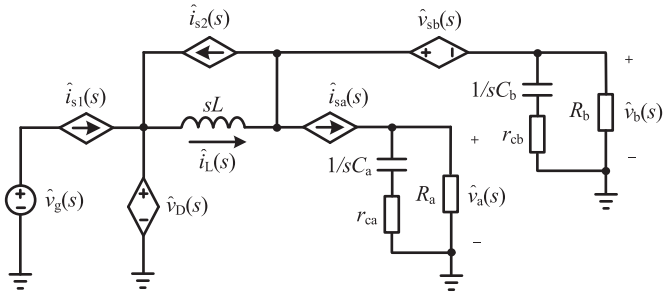

Fig. 5. Small signal equivalent circuit of PCCM SIDO buck converter.

Fig. 3 illustrates the operating principles of CC-DF controlled PCCM SIDO buck converter. The steady-state switching period is denoted by T_s and the corresponding switching frequency is denoted by f_s. The operating principle can be briefly described as follows: At the beginning of the nth switching period, the clock signal clk sets the trigger RS$_1$ and D to output high level (i.e., V_{s1} and V_{sa} are high level), thus, charging the inductor and the output capacitor, both i_L and v_a increase. When the output voltage v_a reaches the peak value V_{ea}, determined by the EA of output A, S_1 is turned OFF. i_L decreases and discharges to v_a. Considering the inductor current ripple flows in the output capacitor, the capacitor current i_{ca} is in the same phase as i_L. Therefore, as soon as i_{ca} reaches the freewheeling current value i_a, the freewheeling switch S_2 is turned ON, and the freewheeling period is activated until the next clock signal arrives, the power delivery path is turned from output A to B. Similar charging, discharging and freewheeling switching actions are repeated during T_b.

B. Control Characteristics of CC-DF Control

With the proposed CC-DF control technique, the freewheeling current and the freewheeling period can be adaptively and continuously adjusted based on the instantaneous load conditions. Fig. 4 shows the inductor current waveforms with load variations. As the load increases, the circuit automatically increases the freewheeling current to prevent the converter from entering CCM operation. This ensures low cross regulation. Moreover, by adjusting the freewheeling current according to the load condition, the PCCM load range of the outputs is extended. When the load drops to a low value, the efficiency is improved by reducing the freewheeling current, which can also shorten the freewheeling period.

III. Small-Signal Model and Frequency-Domain Analysis of CC-DF Controlled PCCM SIDO Buck Converter

A. Small-Signal Modeling of PCCM SIDO Buck Converter

Based on the time-averaged equivalent circuit approach [17], the small signal equivalent circuit of the PCCM SIDO buck converter can be obtained, as shown in Fig. 5. Here, the switches S_1, S_2, and S_a are replaced by the controlled-current sources $\hat{i}_{s1}(s)$, $\hat{i}_{s2}(s)$, and $\hat{i}_{sa}(s)$, respectively, the switch S_b and diode D are replaced by the controlled-voltage source $\hat{v}_{sb}(s)$ and $\hat{v}_D(s)$. The value of $\hat{i}_{s1}(s)$, $\hat{i}_{s2}(s)$, $\hat{i}_{sa}(s)$, $\hat{v}_{sb}(s)$, and $\hat{v}_D(s)$ can be determined as follows:

$$\hat{i}_{s1}(s) = \left(\hat{d}_{a1}(s) + \hat{d}_{b1}(s)\right) I_L + (D_{a1} + D_{b1})\,\hat{i}_L(s) \quad (1)$$

$$\hat{i}_{s2}(s) = \left(\hat{d}_{a3}(s) + \hat{d}_{b3}(s)\right) I_L + (D_{a3} + D_{b3})\,\hat{i}_L(s) \quad (2)$$

$$\hat{i}_{sa}(s) = \left(\hat{d}_{a1}(s) + \hat{d}_{a2}(s)\right) I_L + (D_{a1} + D_{a2})\,\hat{i}_L(s) \quad (3)$$

$$\hat{v}_D(s) = \frac{R_a\left(D_{a3}\hat{v}_{ca}(s) + V_{ca}\hat{d}_{a3}(s)\right)}{R_a + r_{ca}} + \frac{R_b\left(D_{b3}\hat{v}_{cb}(s) + V_{cb}\hat{d}_{b3}(s)\right)}{R_b + r_{cb}} + (D_{a1} + D_{b1})\,\hat{v}_g(s) + \left(\hat{d}_{a1}(s) + \hat{d}_{b1}(s)\right) V_g \quad (4)$$

$$\hat{v}_{sb}(s) = \frac{0.5R_a}{R_a + r_{ca}}\hat{v}_{ca}(s) - \frac{0.5R_b}{R_b + r_{cb}}\hat{v}_{cb}(s) + \frac{R_a r_{ca} I_L}{R_a + r_{ca}}\left(\hat{d}_{a1}(s) + \hat{d}_{a2}(s)\right)$$

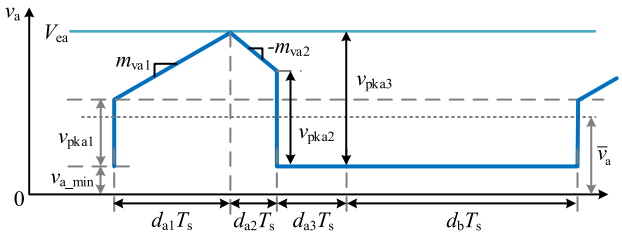

Fig. 6. Steady-state waveforms of output voltage v_a.

$$+\frac{R_a r_{ca}}{R_a+r_{ca}}(D_{a1}+D_{a2})\,\hat{i}_L(s). \tag{5}$$

For the circuit shown in Fig. 5, according to the Kirchhoff's current law and Kirchhoff's voltage law laws, the following expressions can be obtained:

$$\hat{i}_L(s)=\hat{i}_{s2}(s)+\hat{i}_{sa}(s)+\hat{v}_b(s)/R_{eqb}(s) \tag{6}$$

$$\hat{i}_{sa}(s)=\hat{v}_a(s)/R_{eqa}(s)=\hat{v}_a(s)/R_a+s\hat{v}_{ca}(s)/C_a \tag{7}$$

$$\hat{v}_b(s)/R_{eqb}(s)=\hat{v}_b(s)/R_b+s\hat{v}_{cb}(s)/C_b \tag{8}$$

$$\hat{v}_D(s)=sL\hat{i}_L(s)+\hat{v}_{sb}(s)+\hat{v}_b(s) \tag{9}$$

where $R_{eqa}(s)=\frac{(sC_ar_{ca}+1)R_a}{s(C_ar_{ca}+C_aR_a)+1}$, $R_{eqb}(s)=\frac{(sC_br_{cb}+1)R_b}{s(C_br_{cb}+C_bR_b)+1}$.

Based on (1)–(9), all the transfer functions of PCCM SIDO buck converter can be calculated, as given in Table I.

B. Small-Signal Modeling of Voltage-ripple Control

Fig. 6 shows the steady state waveforms of output voltage v_a. According to the geometric relationship, the average of output voltage v_a during one switching cycle can be derived as

$$\begin{aligned}\bar{v}_a=&(0.5+d_{a3})\,v_{a\_min}+\frac{1}{T_s}\int_0^{d_{a1}T_s}(v_{a\_min}+v_{pka1}+m_{va1}t)\,dt\\&+\frac{1}{T_s}\int_0^{d_{a2}T_s}(v_{ea}-m_{va2}t)\,dt\\=&(0.5+d_{a3})\,v_{a\_min}+(v_{a\_min}+v_{pka1})\,d_{a1}+0.5m_{va1}d_{a1}^2T_s\\&+v_{ea}d_{a2}-0.5m_{va2}d_{a2}^2T_s\end{aligned} \tag{10}$$

where v_{a_min} is the valley value of v_a, v_{pka1} is the voltage jump of v_a in the transition moment of output B to A, and it can be expressed as $v_{pka1}=2v_ar_{ca}/R_a$, $m_{vai\ (i=1,2)}$ is the absolute value of increasing and decreasing slopes for output voltage v_a, which can be denoted as

$$\begin{cases}m_{va1}=(V_g-v_a)\,r_{ca}/L\\ m_{va2}=v_ar_{ca}/L\end{cases}. \tag{11}$$

Based on the geometric relationship between output voltage v_a and corresponding inner loop control signal V_{ea} shown in Fig. 6, the V_{ea} can be described as

$$\begin{aligned}V_{ea}&=v_{a\_min}+v_{pka1}+m_{va1}d_{a1}T_s\\&=v_{a\_min}+v_{pka2}+m_{va2}d_{a2}T_s.\end{aligned} \tag{12}$$

TABLE I
TRANSFER FUNCTIONS OF PCCM SIDO BUCK CONVERTER

Control-to-inductor current transfer functions:

$$G_{i\text{-}da1}(s)=\frac{\hat{i}_L(s)}{\hat{d}_{a1}(s)}=\frac{V_g}{sL+R_{xa}(s)+R_{xb}(s)}=G_{i\text{-}db1}(s)$$

$$G_{i\text{-}da3}(s)=\frac{\hat{i}_L(s)}{\hat{d}_{a3}(s)}=\frac{R_a\left((V_a+r_{ca}I_L)(1+sC_ar_{ca})+(0.5-D_{a3})I_LR_{eqa}(s)\right)}{\left(sL+R_{xa}(s)+R_{xb}(s)\right)\left(R_a+r_{ca}\right)\left(1+sC_ar_{ca}\right)}$$

$$G_{i\text{-}db3}(s)=\frac{\hat{i}_L(s)}{\hat{d}_{b3}(s)}=\frac{R_b\left(V_b+r_{cb}I_L\right)(1+sC_br_{cb})+(0.5-D_{b3})R_bI_LR_{eqb}(s)}{\left(sL+R_{xa}(s)+R_{xb}(s)\right)\left(R_b+r_{cb}\right)(1+sC_br_{cb})}$$

Control-to-output transfer functions:

$$G_{va\text{-}da1}(s)=\frac{\hat{v}_a(s)}{\hat{d}_{a1}(s)}=(0.5-D_{a3})R_{eqa}(s)G_{i\text{-}da1}(s)=G_{va\text{-}db1}(s)$$

$$G_{vb\text{-}da1}(s)=\frac{\hat{v}_b(s)}{\hat{d}_{a1}(s)}=(0.5-D_{b3})R_{eqb}(s)G_{i\text{-}da1}(s)=G_{vb\text{-}db1}(s)$$

$$G_{va\text{-}da3}(s)=\frac{\hat{v}_a(s)}{\hat{d}_{a3}(s)}=(0.5-D_{a3})R_{eqa}(s)G_{i\text{-}da3}(s)-I_LR_{eqa}(s)$$

$$G_{vb\text{-}da3}(s)=\frac{\hat{v}_b(s)}{\hat{d}_{a3}(s)}=(0.5-D_{b3})R_{eqb}(s)G_{i\text{-}da3}(s)$$

$$G_{va\text{-}db3}(s)=\frac{\hat{v}_a(s)}{\hat{d}_{b3}(s)}=(0.5-D_{a3})R_{eqa}(s)G_{i\text{-}db3}(s)$$

$$G_{vb\text{-}db3}(s)=\frac{\hat{v}_b(s)}{\hat{d}_{b3}(s)}=(0.5-D_{b3})R_{eqb}(s)G_{i\text{-}db3}(s)-I_LR_{eqb}(s)$$

Input-to-inductor current transfer functions:

$$G_{i\text{-}vg}(s)=\frac{\hat{i}_L(s)}{\hat{v}_g(s)}=\frac{D_{a1}+D_{b1}}{sL+R_{xa}(s)+R_{xb}(s)}$$

Input-to-output transfer functions:

$$G_{va\text{-}vg}(s)=\frac{\hat{v}_a(s)}{\hat{v}_g(s)}=(0.5-D_{a3})R_{eqa}(s)G_{i\text{-}vg}(s)$$

$$G_{vb\text{-}vg}(s)=\frac{\hat{v}_b(s)}{\hat{v}_g(s)}=(0.5-D_{b3})R_{eqb}(s)G_{i\text{-}vg}(s)$$

Load-to-inductor current transfer functions:

$$G_{iaz}(s)=\frac{\hat{i}_L(s)}{\hat{i}_a(s)}=\frac{(D_{a3}-0.5)R_aR_{eqa}(s)}{\left(sL+R_{xa}(s)+R_{xb}(s)\right)\left(R_a+r_{ca}\right)\left(1+sC_ar_{ca}\right)}$$

$$G_{ibz}(s)=\frac{\hat{i}_L(s)}{\hat{i}_b(s)}=\frac{(0.5+D_{b3})R_b-\left(R_b+r_{cb}\right)\left(1+sC_br_{cb}\right)}{\left(sL+R_{xa}(s)+R_{xb}(s)\right)\left(R_b+r_{cb}\right)\left(1+sC_br_{cb}\right)}R_{eqb}(s)$$

Impedance transfer functions:

$$Z_{aa}(s)=\frac{\hat{v}_a(s)}{\hat{i}_a(s)}=(0.5-D_{a3})R_{eqa}(s)G_{iaz}(s)+R_{eqa}(s)$$

$$Z_{ba}(s)=\frac{\hat{v}_b(s)}{\hat{i}_a(s)}=(0.5-D_{b3})R_{eqb}(s)G_{iaz}(s)$$

$$Z_{ab}(s)=\frac{\hat{v}_a(s)}{\hat{i}_b(s)}=(0.5-D_{a3})R_{eqa}(s)G_{ibz}(s)$$

$$Z_{bb}(s)=\frac{\hat{v}_b(s)}{\hat{i}_b(s)}=(0.5-D_{b3})R_{eqb}(s)G_{iaz}(s)+R_{eqb}(s)$$

From (1)–(3), the average of output voltage v_a can be rearranged as

$$\begin{aligned}\bar{v}_a=&V_{ea}-(0.5+d_{a3})\frac{2v_b}{R_b}r_{ca}-\frac{(v_g-v_a)\,r_{ca}}{L}d_{a1}\,(0.5+d_{a3})\,T_s\\&-\frac{(V_g-v_a)\,r_{ca}}{2L}d_{1a}^2T_s-\frac{v_ar_{ca}}{2L}d_{a2}^2T_s.\end{aligned} \tag{13}$$

Adding small disturbance into (4), and ignoring the dc and high-order perturbations, the small-signal expression of the duty

ratio d_{a1} can be obtained as

$$\hat{d}_{a1}(s) = F_{a1}\hat{v}_g(s) + F_{a2}\hat{v}_a(s) + F_{a3}\hat{v}_{ea}(s) + F_{a4}\hat{v}_b(s) + F_{a5}\hat{d}_{a3}(s) \tag{14}$$

where F_{a1}, F_{a2}, F_{a3}, F_{a4}, and F_{a5} denote the input feedforward gain, output feedback gain, modulator gain, cross feedback gain and duty-ratio gain, respectively, which can be further expressed as

$$F_{a1} = \frac{-2D_{a1}(0.5+D_{a3}) - D_{a1}^2}{2(V_g(0.5+D_{a1}+D_{a3}) - V_a)},$$

$$F_{a2} = \frac{2D_{a1}(0.5+D_{a3})r_{ca}T_s + D_{a1}^2 r_{ca}T_s - (0.5-D_{a1}-D_{a3})^2 r_{ca}T_s - 2L}{2(V_g(0.5+D_{a1}+D_{a3}) - V_a)r_{ca}T_s}$$

$$F_{a3} = \frac{L}{(V_g(0.5+D_{a1}+D_{a3}) - V_a)r_{ca}T_s}$$

$$F_{a4} = \frac{-2L(0.5+D_{a3})}{(V_g(0.5+D_{a1}+D_{a3}) - V_a)R_bT_s}$$

$$F_{a5} = \frac{V_a(0.5-D_{a3})R_bT_s - V_gD_{a1}R_bT_s - 2LV_b}{(V_g(0.5+D_{a1}+D_{a3}) - V_a)R_bT_s}$$

where D_{a1}, D_{a3}, V_a, and V_b are the steady state of d_{a1}, d_{a3}, v_a, and v_b, respectively.

Similarly, the small-signal expression of the duty ratio d_{b1} can be given as follows:

$$\hat{d}_{b1}(s) = F_{b1}\hat{v}_g(s) + F_{b2}\hat{v}_b(s) + F_{b3}\hat{v}_{eb}(s) + F_{b4}\hat{v}_a(s) + F_{b5}\hat{d}_{b3}(s) \tag{15}$$

where

$$F_{b1} = \frac{-2D_{b1}(0.5+D_{b3}) - D_{b1}^2}{2(V_g(0.5+D_{b1}+D_{b3}) - V_b)},$$

$$F_{b2} = \frac{2D_{b1}(0.5+D_{b3})r_{cb}T_s + D_{b1}^2 r_{cb}T_s - (0.5-D_{b1}-D_{b3})^2 r_{cb}T_s - 2L}{2(V_g(0.5+D_{b1}+D_{b3}) - V_b)r_{cb}T_s}$$

$$F_{b3} = \frac{L}{(V_g(0.5+D_{b1}+D_{b3}) - V_b)r_{cb}T_s}$$

$$F_{b4} = \frac{-2L(0.5+D_{b3})}{(V_g(0.5+D_{b1}+D_{b3}) - V_b)R_aT_s}$$

$$F_{b5} = \frac{V_b(0.5-D_{b3})R_aT_s - V_gD_{b1}R_aT_s - 2LV_a}{(V_g(0.5+D_{b1}+D_{b3}) - V_b)R_aT_s}.$$

C. Small-Signal Modeling of Dynamical Freewheeling Control

The inductor current i_L of CC-DF controlled PCCM SIDO buck converter is shown in Fig. 7, and the average of inductor current during one switching cycle can be derived as follows:

$$\bar{i}_L = \left(I_{dcb} + \frac{T_s}{2L}(V_g - v_a)d_{a1}\right)d_{a1} + \left(I_{dca} + \frac{T_s}{2L}v_a d_{a2}\right)d_{a2} + I_{dca}d_{a3} + \left(I_{dca} + \frac{T_s}{2L}(V_g - v_b)d_{b1}\right)d_{b1} + \left(I_{dcb} + \frac{T_s}{2L}v_b d_{b2}\right)d_{b2} + I_{dcb}d_{b3} \tag{16}$$

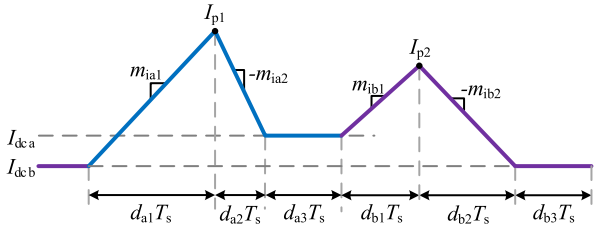

Fig. 7. Steady-state waveforms of inductor current i_L.

where $I_{dca} = 2v_a/R_a$, $I_{dcb} = 2v_b/R_b$.

Adding a small disturbance into (7), and ignoring the dc and high-order perturbations, the small-signal expression of the duty ratio d_{a3} can be obtained as

$$\hat{d}_{a3}(s) = G_{a1}\hat{v}_g(s) + G_{a2}\hat{d}_{a1}(s) + G_{a3}\hat{v}_a(s) + G_{a4}\hat{d}_{b1}(s) + G_{a5}\hat{v}_b(s) + G_{a6}\hat{i}_L(s) \tag{17}$$

where

$$G_{a1} = -\left(\left(D_{a1}^2 + D_{b1}^2\right)/2 + (0.5 - D_{b1} - D_{b3})D_{b1}\right)T_sG_{a6}$$

$$G_{a2} = -(T_s(D_{a1}V_g - (0.5-D_{a3})V_a)/L + (2R_aV_b - 2R_bV_a)/(R_aR_b))G_{a6}$$

$$G_{a3} = -\left(T_s\left((0.5-D_{a1}-D_{a3})^2 - D_{a1}^2\right)\Big/(2L) + 2(1-D_{a1}-D_{b3})/R_b\right)G_{a6}$$

$$G_{a4} = -(T_s(0.5-D_{b3})(V_g - V_b)/L + (2R_bV_a - 2R_aV_b)/(R_aR_b))G_{a6}$$

$$G_{a5} = -\left(2(D_{a1}+D_{b3})/R_b - T_s(0.5-D_{b3})^2\Big/2L\right)G_{a6}$$

$$G_{a6} = -L/(T_s(0.5-D_{a1}-D_{a3})V_a)..$$

Similarly, the small-signal expression of the duty ratio d_{b3} can be written as

$$\hat{d}_{b3}(s) = G_{b1}\hat{v}_g(s) + G_{b2}\hat{d}_{b1}(s) + G_{b3}\hat{v}_b(s) + G_{b4}\hat{d}_{a1}(s) + G_{b5}\hat{v}_a(s) + G_{b6}\hat{i}_L(s) \tag{18}$$

where

$$G_{b1} = -\left(\left(D_{b1}^2 + D_{a1}^2\right)/2 + (0.5 - D_{a1} - D_{a3})D_{a1}\right)T_sG_{b6}$$

$$G_{b2} = -((T_s(D_{b1}V_g - (0.5-D_{b3})V_b))/L + 2(R_bV_a - R_aV_b)/(R_aR_b))G_{b6}$$

$$G_{b3} = -\left(T_s\left((0.5-D_{b1}-D_{b3})^2 - D_{b1}^2\right)\Big/(2L) + 2(1-D_{b1}-D_{a3})/R_b\right)G_{b6}$$

$$G_{b4} = -(T_s(0.5-D_{a3})(V_g - V_a)/L$$

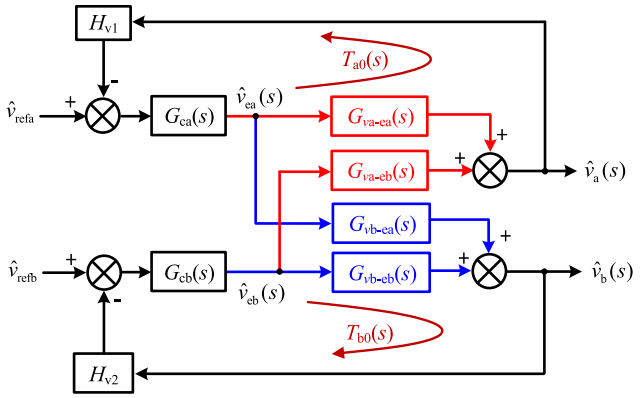

Fig. 8. Simplified small-signal diagram of CC-DF controlled PCCM SIDO buck converter.

$$+2(R_aV_b - R_bV_a)/R_aR_b)\,G_{b6}$$

$$G_{b5} = -\left(2\,(D_{b1}+D_{a3})/R_a - T_s(0.5-D_{a3})^2\Big/(2L)\right)G_{b6}$$

$$G_{b6} = -L/(T_s\,(0.5-D_{b1}-D_{b3})\,V_b).$$

D. Error Amplifier Design

Based on the above analysis, the small-signal model of CC-DF controlled PCCM SIDO buck converter is established, and the simplified small-signal diagram can be obtained, as shown in Fig. 8. It includes the small signal model of the control loop and the transfer functions of the power stage, where $H_{va}(s)$ and $H_{vb}(s)$ are the sampling coefficients of output voltages, $G_{ca}(s)$ and $G_{cb}(s)$ are the transfer functions of EA, $G_{va\text{-}ea}(s)$ and $G_{vb\text{-}eb}(s)$ are the transfer functions of control to output, $G_{va\text{-}eb}(s)$ and $G_{vb\text{-}ea}(s)$ are the transfer functions of control coupling.

The loop-gain transfer functions $T_{a0}(s)$ and $T_{b0}(s)$ shown in Fig. 8, are as follows:

$$T_{a0}(s) = H_{va}(s)G_{ca}(s) \times \left(G_{va-ea}(s) - \frac{G_{vb-ea}(s)G_{va-eb}(s)H_{vb}(s)G_{cb}(s)}{1+G_{vb-eb}(s)H_{vb}(s)G_{cb}(s)}\right) \tag{19}$$

$$T_{b0}(s) = H_{vb}(s)G_{cb}(s) \times \left(G_{vb-eb}(s) - \frac{G_{va-eb}(s)G_{vb-ea}(s)H_{va}(s)G_{ca}(s)}{1+G_{va-ea}(s)H_{va}(s)G_{ca}(s)}\right). \tag{20}$$

Assuming $G_{ca}(s) = G_{cb}(s) = 1$ for CC-DF controlled PCCM SIDO buck converter without EA, the Bode plots of $T_{a0}(s)$ and $T_{b0}(s)$ with/without EA are depicted, as shown in Fig. 9, the long-dashed lines represent the theoretical results obtainable from Mathcad, and the solid lines represent the SIMPLIS simulation results. Both results are in excellent agreement up to half of the switching frequency, which means that the theoretical model presented in this article is accurate. The circuit parameters of PCCM SIDO buck converter in Fig. 9 are listed in Table II. In this article, the proposed CC-DF control is a ripple-based control, which uses the output voltage ripple to implement the

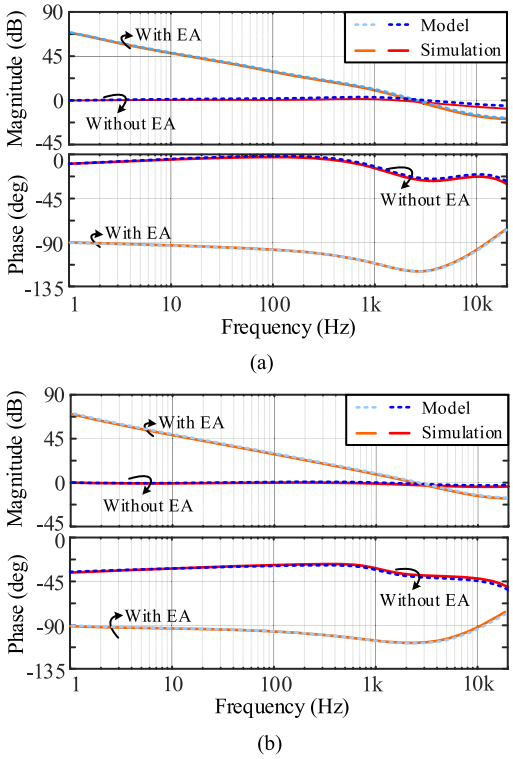

Fig. 9. Bode plots of loop-gain transfer functions with/without EA. (a) $T_{a0}(s)$. (b) $T_{b0}(s)$.

TABLE II
MAIN CIRCUIT PARAMETERS OF PCCM SIDO BUCK CONVERTER

Symbol	Parameter	Value
V_g	Input voltage	20V
L	Inductor	30μH
C_a, C_b	Output capacitors	470μF
r_{ca}, r_{cb}	equivalent series resistance of output capacitor	75mΩ
V_{refa}	reference voltage of va	12V
V_{refa}	reference voltage of vb	5V
i_a, i_b	Load current	1A
clk	Clock signal frequency	50kHz
f_s	Switching frequency	25kHz

control. So, a relatively large ESR of the output capacitor is used to ensure stable operation.

From the Bode plots without EA for $T_{a0}(s)$ and $T_{b0}(s)$, it is clearly that the low frequency magnitudes are small, about 0 dB for $T_{a0}(s)$ and $T_{b0}(s)$, which would cause too large steady-state error. Moreover, the crossover frequencies of $T_{a0}(s)$ and $T_{b0}(s)$ are low, resulting in poor dynamic performance.

Considering the system bandwidth and the high-frequency noise, the crossover frequency $f_c = 3$ kHz (one-eighth of the switching frequency) is designed with an EA. In addition, it is necessary to increase the low-frequency gain for stability and smaller steady-state error. Combining the above analysis, the proportional-integral type EA is selected to increase an open-loop pole, which can reduce the steady-state error and improve the steady-state performance. $G_{ca}(s)$ and $G_{cb}(s)$ can

be calculated as

$$G_{ca}(s) = 0.003 + 24000/s;\ G_{cb}(s) = 0.003 + 24000/s. \tag{21}$$

Based on (21), the Bode plots of $T_{a0}(s)$ and $T_{b0}(s)$ with EA are shown in Fig. 9, where the solid lines represent the results with EA. The crossover frequencies of both $T_{a0}(s)$ and $T_{b0}(s)$ are 3 kHz. The phase margin of $T_{a0}(s)$ and $T_{b0}(s)$ is about 80° and 95°, respectively. The low-frequency margin of $T_{a0}(s)$ and $T_{b0}(s)$ is about 70.6 and 70.3 dB, respectively. The system has the desired crossover frequency and phase margin. Therefore, the control loop will be featured in stable and fast response with a wide bandwidth and sufficient phase margin.

E. Cross-Regulation and Transient Performance Analysis

The Bode plots of the closed-loop impedance transfer functions are presented in Fig. 10, comparing the cross-regulation and the load transient performance of the proposed control scheme with the VM/VR-CF control, where both theoretical results and SIMPLIS simulation, where both theoretical results and SIMPLIS simulation results are in excellent agreement up to half of the switching frequency, which means that the theoretical model presented in this article is accurate.

From Fig. 10(a) and (b), it is obvious that the low-frequency magnitudes of output impedance ${Z_{aa}}^*(s)$and ${Z_{bb}}^*(s)$ under CC-DF control are lower than those under traditional VM-CF control. This indicates that the load transient performance of the PCCM SIDO buck converter is greatly improved by the proposed CC-DF control. Comparing the low-frequency gain of CC-DF control and VR-CF control in Fig. 10(a) and (b), the magnitudes of ${Z_{aa}}^*(s)$and ${Z_{bb}}^*(s)$ for these two controls are the same with each other, which indicates that CC-DF control and VR-CF control have similar load transient performance.

From Fig. 10(c) and (d), it can be seen that the low-frequency magnitudes of the cross-regulation impedance ${Z_{ba}}^*(s)$and ${Z_{ab}}^*(s)$ of the CC-DF control are similar to those of the VM/VR-CF control with small cross-regulation, which is reported in [17]; this means that the CC-DF control also has small cross-regulation compared to the VM-CF control and VR-CF control.

F. Transient Simulation Results

Fig. 11 show transient simulation waveforms of the output voltages, the EA outputs and the output currents of CC-DF controlled PCCM SIDO buck converter.

In Fig. 11(a), it is obviously that the cross-regulation from output a to output b is about zero, and the transient response time of output a is about two switching periods, when i_a step decrease from 1 to 0.5 A and $i_b = 1$ A. In Fig. 11(b), the cross-regulation from output b to output a is about zero, and the transient response time of output b is about two switching periods, when i_b step decrease from 1 to 0.5A and $i_a = 1$A. Simulation results show that the EA output can quickly follow the output voltages during transient, which verify that the CC-DF controlled PCCM SIDO buck converter has excellent transient performance and it is able to suppress its cross regulation.

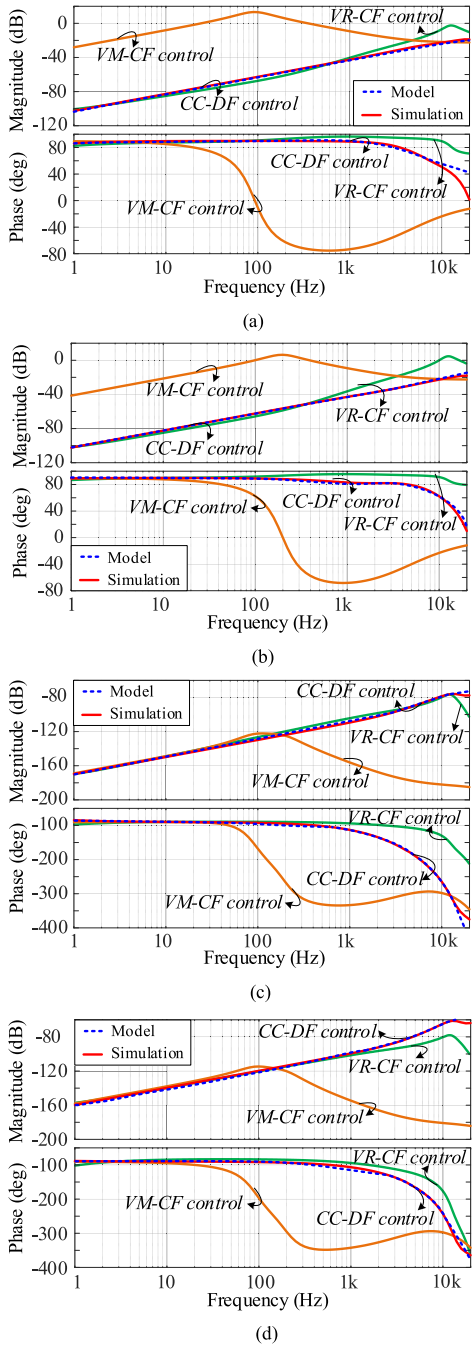

Fig. 10. Bode plots of closed-loop impedance transfer functions under CC-DF control and VM/VR-CF control for PCCM SIDO buck converter. (a) ${Z_{aa}}^*(s)$. (b) ${Z_{bb}}^*(s)$. (c)${Z_{ba}}^*(s)$. (d)${Z_{ab}}^*(s)$.

IV. Load Range and Loss Analysis

A. Load Range Analysis

Analyzing the load range is useful for optimizing the parameters which are used to ensure that each output is operating in PCCM. If the load resistances R_a and R_b are lower than the minimum load resistances $R_{a(\min)}$ and $R_{b(\min)}$, the converter will transition from PCCM to CCM, i.e., the different outputs will be coupled and cross-regulation will occur.

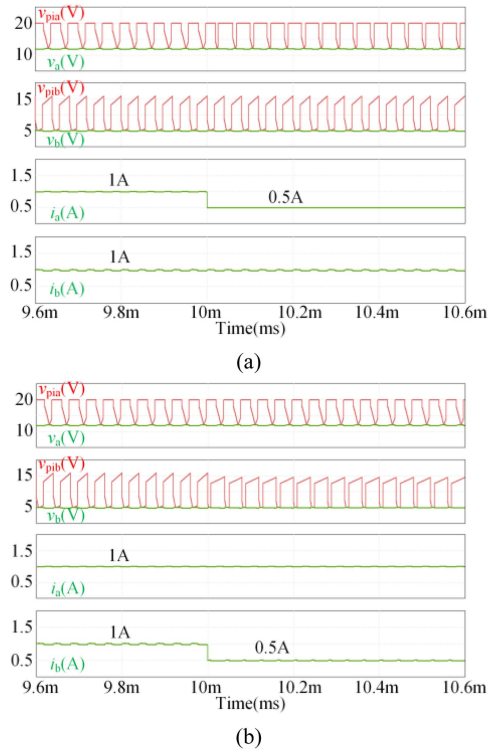

Fig. 11. Transient simulation waveforms of output voltages, the EA outputs and the output currents of CC-DF controlled PCCM SIDO buck converter. (a) i_a step change. (b) i_b step change.

Based on the steady-state waveforms of i_{L} shown in Fig. 7, the freewheeling duty-ratio d_{a3} and d_{b3} can be expressed as

$$\begin{cases} d_{a3} = \left(-b_a \pm \sqrt{b_a^2 - 4a_a c_a}\right) \Big/ (2a_a) \\ d_{b3} = \left(-b_b \pm \sqrt{b_b^2 - 4a_b c_b}\right) \Big/ (2a_b) \end{cases} \tag{22}$$

where $a_a = (V_g - V_a)V_a T_s$, $b_a = LV_a(I_{dca} - I_{dcb}) - LV_g(I_{dca} + I_{dcb}) - a_a$

$$\begin{aligned} c_a &= L^2(I_{dca} - I_{dcb})^2 (2V_g - V_a) + LV_a (I_{dcb} - I_{dca}) \\ &\quad + LV_g (I_{dca} - 2I_a) + a_a/4 \\ a_b &= (V_g - V_b) V_b T_s, b_b = LV_b (I_{dcb} - I_{dca}) \\ &\quad - LV_g (I_{dca} + I_{dcb}) - a_b \\ c_b &= L^2(I_{dcb} - I_{dca})^2 (2V_g - V_b) + LV_b (I_{dca} - I_{dcb}) \\ &\quad + LV_g (I_{dcb} - 2I_b) + a_b/4. \end{aligned}$$

It is clear that the converter would operate in PCCM when the freewheeling duty-ratios d_{a3} and d_{b3} are above zero. From (22), the load resistance range for PCCM can be calculated as

$$\begin{cases} R_a > \frac{2V_a^2 V_g L T_s}{a_a(LI_{dca} + V_a T_s/4) + L^2(I_{dca} - I_{dcb})^2(2V_g - V_a) + V_a^2 T_s L I_{dcb}} \\ R_b > \frac{2V_b^2 V_g L T_s}{a_b(LI_{dcb} + V_b T_s/4) + L^2(I_{dcb} - I_{dca})^2(2V_g - V_b) + V_b^2 T_s L I_{dca}} \end{cases}. \tag{23}$$

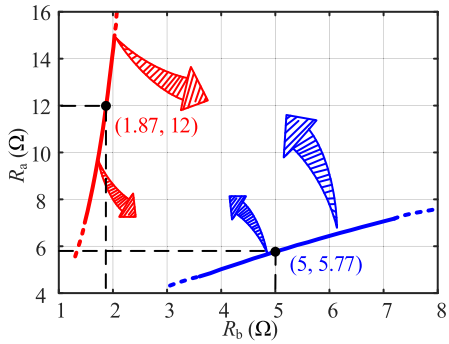

Fig. 12. Load range of CC-DF controlled PCCM SIDO buck converter.

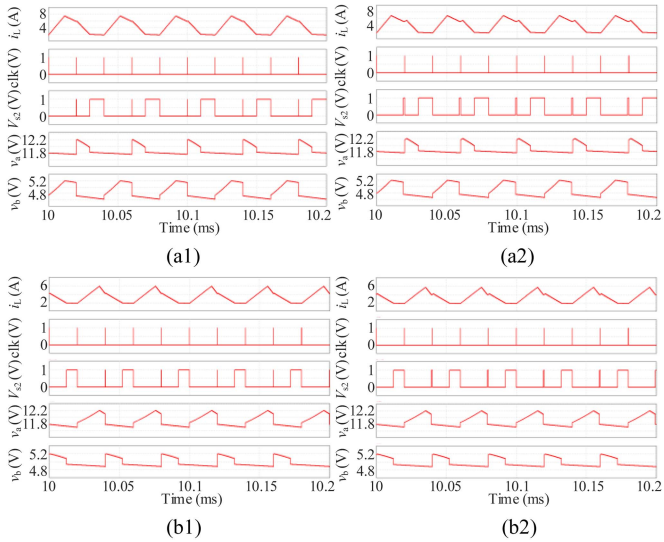

Fig. 13. Simulation waveforms of CC-DF controlled PCCM SIDO buck converter under different load resistances. (a1) $R_a = 12\ \Omega$ and $R_b = 1.7\ \Omega$. (a2) $R_a = 12\ \Omega$ and $R_b = 1.9\ \Omega$. (b1) $R_a = 5.7\ \Omega$ and $R_b = 5\ \Omega$. (b2) $R_a = 6\ \Omega$ and $R_b = 5\ \Omega$.

In (22), the freewheel values I_{dca} and I_{dcb} are highly related to I_a and I_b. Therefore, to deeply investigate the load range of CC-DF controlled PCCM SIDO buck converter, the load boundaries are portrayed by MATLAB software, as depicted in Fig. 12.

From Fig. 12, the available load range is the region between the red arrow and the blue arrow. Taking the load $R_a = 12\ \Omega$ as an example, if $R_b > 1.87\ \Omega$, both outputs of the converter operate in PCCM; however, if $\mathrm{R_b} < 1.87\ \Omega$, the circuit is out of PCCM and enters CCM or even unstable operation. Similarly, when $R_b = 5\ \Omega$, if $R_a > 5.77\ \Omega$, both outputs of the converter operate in PCCM, and if $R_a < 5.77\ \Omega$, the circuit is out of PCCM and enters CCM or even unstable operation. Practically, if one load is fixed, another load should avoid being too large or too small, otherwise, it will take the converter out of PCCM.

Taking $I_{dca} = I_{dcb} = 2$ A in VM/VR-CF control as an example, the analysis in [16] shows that $I_{a(\max)} = 1.79$A, $I_{b(\max)} = 1.61$A (i.e., $R_a = 6.7\ \Omega$ and $R_b = 3.1\ \Omega$) are the maximum load. However, in Fig. 12, many operating points beyond this range and work stably, i.e., compared with VM/VR-CF control, CC-DF control can significantly extend the load range of PCCM SIDO buck converter.

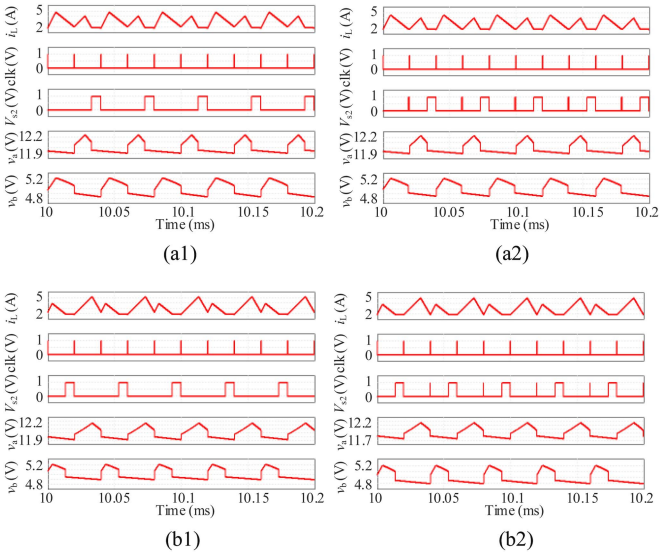

Fig. 14. Simulation waveforms of VM-CF controlled PCCM SIDO buck converter under different load resistances. (a1) $R_a = 12\ \Omega$ and $R_b = 3\ \Omega$. (a2) $R_a = 12\ \Omega$ and $R_b = 3.2\ \Omega$. (b1) $R_a = 6.6\ \Omega$ and $R_b = 5\ \Omega$. (b2) $R_a = 6.8\ \Omega$ and $R_b = 5\ \Omega$.

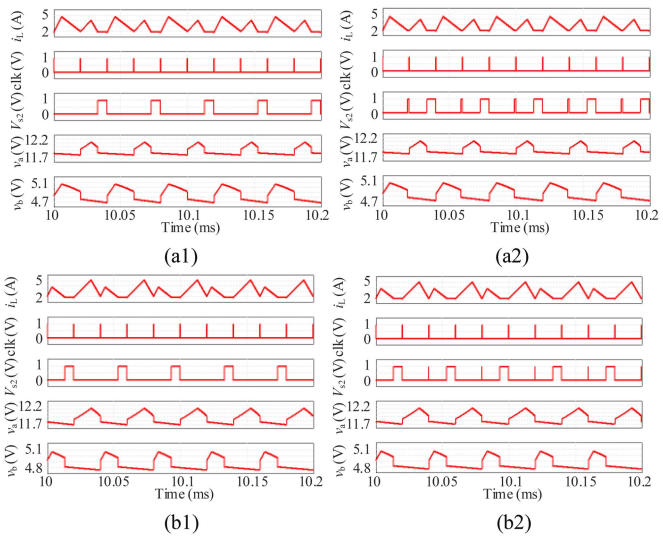

Fig. 15. Simulation waveforms of VR-CF controlled PCCM SIDO buck converter under different load resistances. (a1) $R_a = 12\ \Omega$ and $R_b = 3\ \Omega$. (a2) $R_a = 12\ \Omega$ and $R_b = 3.2\ \Omega$. (b1) $R_a = 6.6\ \Omega$ and $R_b = 5\ \Omega$. (b2) $R_a = 6.8\ \Omega$ and $R_b = 5\ \Omega$.

Figs. 13–15 show the steady-state simulation waveforms of CC-DF control and VM/VR-CF control for PCCM SIDO buck converter under different load resistances. When $R_a > 5.77\ \Omega$ and $R_b > 1.87\ \Omega$, the CC-DF controlled SIDO buck converter operate in PCCM, as shown in Fig. 13(a) and (b). When the constant freewheeling value is 2A, the VM/VR-CF controlled SIDO buck converter operate in PCCM under $R_a > 6.7\ \Omega$ and $R_b > 3.1\ \Omega$, otherwise in CCM, as shown in Figs. 14 and 15. Comparing the simulation waveforms, it is easily known that the proposed CC-DF controlled PCCM SIDO buck converter can broaden the load range.

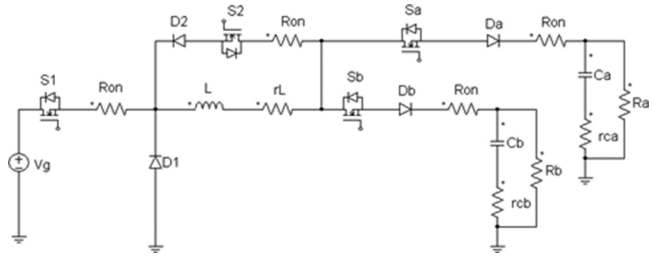

Fig. 16. Equivalent schematic circuit with parasitic parameters.

B. Loss Analysis

In this section, the losses of CC-DF controlled PCCM SIDO buck converter are estimated, which can be categorized into four main parts: MOSFET losses; diode losses; magnetic component losses; and capacitor losses. Any other losses, such as conduction losses PCB trace, and control circuit losses are neglected.

Considering the parasitic parameters and experimental circuit, the equivalent schematic circuit can be obtained in Fig. 16, where defining the ESR of L as r_L; the ON-resistor of MOSFET S_1, S_2, S_a, and S_b as $R_{\rm on}$; the forward voltage of diode D_1, D_2, D_a, and D_b as V_F. The diodes D_2, D_a, and D_b are existed in the experimental hardware circuit to prevent the body diode of MOSFET from misconducting.

1) MOSFET Losses: The two main power losses in MOSFETs are conduction loss and switching loss [18]. The conduction losses can be calculated straightforwardly from

$$P_{S-\rm con} = 2I_{L-a1}^2 R_{\rm on} d_{a1} + I_{L-a2}^2 R_{\rm on} d_{a2} + I_{L-a3}^2 R_{\rm on} d_{a3} + 2I_{L-b1}^2 R_{\rm on} d_{b1} + I_{L-b2}^2 R_{\rm on} d_{b2} + I_{L-b3}^2 R_{\rm on} d_{b3} \quad (24)$$

where $I_{L\text{-}a1}$, $I_{L\text{-}a2}$, $I_{\rm L\text{-}a3}$, $I_{L\text{-}b1}$, $I_{L\text{-}b2}$, and $I_{L\text{-}b3}$ are the rms values of inductor current in different operation modes, respectively; $R_{\rm on}$ is the ON-resistance of MOSFET.

For the switching losses, the turn-on state and turn-off state are linear processes, while the switching process is a highly nonlinear process. Calculating the switching losses is more involved than calculating the conduction losses. A detailed discussion of this loss model is out of the scope in this article. For the sake of simplicity, a simplified switching loss model is utilized in this article, at the cost of sacrificing some degree of accuracy that is deemed acceptable for the analysis, which is widely used in practical engineering [19]. Based on these losses model, the turn-on switching loss can be calculated by

$$P_{\rm loss-ON} = f_s V_{\rm DS} I_{\rm D} t_{\rm SW-on}/2. \quad (25)$$

The turn-OFF switching loss is

$$P_{\rm loss-OFF} = f_s V_{\rm DS} I_D t_{\rm SW-off}/2. \quad (26)$$

From (25) and (26), the total switching losses of PCCM SIDO buck converter can be obtained by

$$P_{S-\rm SW} = 0.5f\left(t_{\rm SW-on} + t_{\rm SW-off}\right)\left(V_g\left(I_{L-a1} + I_{L-b1}\right) + \left(V_b - V_a\right)\left(I_{L-a2} - I_{L-b2}\right)\right) + 0.5f\left(t_{\rm SW-on} + t_{\rm SW-off}\right)\left(\left(V_g - V_a\right) I_{L-a3}\right.$$

$$+\left(V_g - V_b\right) I_{L-b3}\big). \tag{27}$$

2) Diode Losses: Diode loss is mainly divided into switching loss, conduction loss and cut-OFF loss. However, for a Schottky diode, most of the power loss is caused by V_F, and switching power loss is not the majority. From Fig. 12, it is easily known that the diode losses are existed during the whole switching period. As a result, in this article, the diode loss can be simplified as

$$P_D = I_{L1}V_F d_{a1} + 2I_{L2}V_F d_{a2} + I_{L3}V_F d_{a3} + I_{L4}V_F d_{b1} + 2I_{L5}V_F d_{b2} + I_{L6}V_F d_{b3}. \tag{28}$$

3) Magnetic Component Losses: The main magnetic component in PCCM SIDO buck converter is the energy storage inductor L. The loss of L is composed of copper loss P_{Cu} and core loss P_{Fe} [20]. P_{Cu} is the ohmic loss caused by the ESR of the current flowing through the wire around the inductor. P_{Cu} is given as follows:

$$P_{\mathrm{Cu}} = \left(I_{L-a1}^2 d_{a1} + I_{L-a2}^2 d_{a2} + I_{L-a3}^2 d_{a3} + I_{L-b1}^2 d_{b1} + I_{L-b2}^2 d_{b2} + I_{L-b3}^2 d_{b3}\right) r_L \tag{29}$$

P_{Fe} can be calculated by Steinmetz empirical formula, and the formula is shown as

$$P_{\mathrm{Fe}} = B^2 \left(c_1 f_s + c_2 K_e {f_s}^2/\rho\right) \tag{30}$$

where B is the peak magnetic induction value, c_1, c_2, K_e, and ρ are determined by the material characteristic.

4) Filter Capacitor Losses: The loss caused by the filter capacitor mainly comes from the ESR. Combined with the above analysis, the equations for filter capacitor loss are shown as

$$P_{ca\_esr} = \left(I_{ca1}^2 d_{a1} + I_{ca2}^2 d_{a2} + I_{ca3}^2 d_{a3} + I_{ca4}^2 d_{b1} + I_{ca5}^2 d_{b2} + I_{ca6}^2 d_{b3}\right) r_{ca} \tag{31}$$

$$P_{cb\_esr} = \left(I_{cb1}^2 d_{a1} + I_{cb2}^2 d_{a2} + I_{cb3}^2 d_{a3} + I_{cb4}^2 d_{b1} + I_{cb5}^2 d_{b2} + I_{cb6}^2 d_{b3}\right) r_{cb} \tag{32}$$

where $I_{cai(i\,=\,1\ldots6)}$, and $I_{cbi(i\,=\,1\ldots6)}$ are the rms values of capacitor current in different operation modes, respectively.

5) Total Power Losses: Combined with above analysis of this section, the total power loss can be obtained as

$$P_{\mathrm{loss}} = P_{S-\mathrm{con}} + P_{\mathrm{S-SW}} + P_{\mathrm{D}} + P_{\mathrm{Cu}} + P_{\mathrm{Fe}} + P_{ca\_esr} + P_{cb\_esr}. \tag{33}$$

The loss distributions of CC-DF controlled PCCM SIDO buck converter are shown in Fig. 17. It can be seen from Fig. 15 that the diode loss mainly causes the maximum ratio of the total loss. The diode loss accounts for 74.9%, the MOSFET loss accounts for 12.3%, the magnetic component loss accounts for 8.1%, and the filter capacitor loss accounts for 4.7%, respectively.

According to the loss calculation equations given above, Fig. 18 shows the efficiency curves for CC-DF controlled PCCM SIDO buck converter and VM/VR-CF controlled PCCM SIDO buck converter. From Fig. 16, it is illustrated that the following.

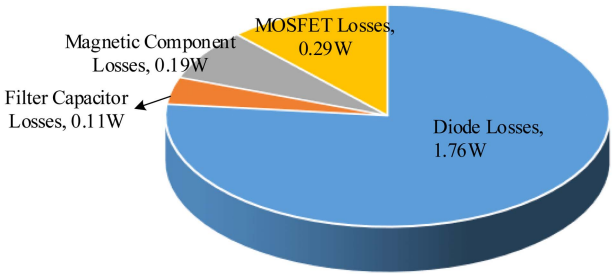

Fig. 17. Loss distribution of CC-DF controlled PCCM SIDO buck converter.

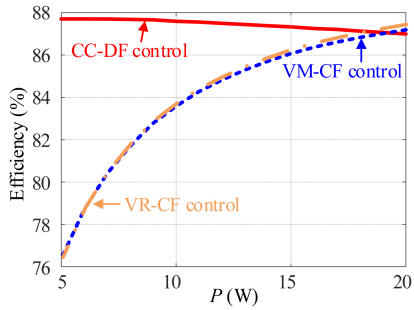

Fig. 18. Efficiency curves for PCCM SIDO buck converter under CC-DF control and VM/VR-CF control.

1) With the decrease of the load power, the efficiency for VM/VR-CF control decrease sharply, while it is slightly increased for CC-DF control.
2) The efficiency for CC-DF control is much higher than VM/VR-CF control under light load.
3) The efficiency curve of VR-CF control is coincided with VM-CF control as the freewheeling switch followed the same control scheme.

V. Experimental Verification

To demonstrate the performance of the proposed CC-DF controlled PCCM SIDO buck converter, the experimental hardware circuit is implemented and the circuit parameters are designed according to Section III.

A. Experiment Setup

The photograph of experimental hardware circuit is added in Fig. 19. In the hardware circuit, the switches S_1, S_2, S_a, and S_b are N-channel power MOSFET BSC010N04LS, the diodes are ES4J, and the driver signals are generated by the driver UCC27512DRST, respectively. The capacitor currents i_{ca}, i_{cb} and load currents i_a, i_b are sampled using sensing resistor 5mΩ and obtained by amplification circuit which is implemented by LM6142. The compensating circuit is implemented by OPA2347. The comparison circuit is realized by using LMV393. For the control circuit, including two multiplexers MUX_1 and MUX_2, two RS triggers RS_1 and RS_2, a D trigger, and a clock signal clk, as its principle described in Section II, it is realized using the Texas Instruments TMS320F28335 DSP system, which has built-in digital PWM, 12-bit A/D converter, and a 32-bit floating-point unit.

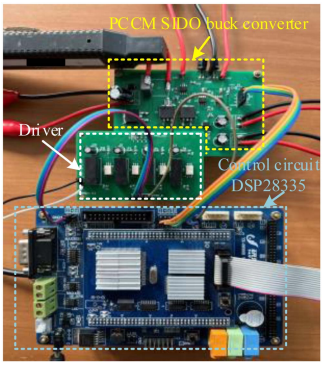

Fig. 19. Photograph of experimental hardware circuit of the PCCM SIDO buck converter.

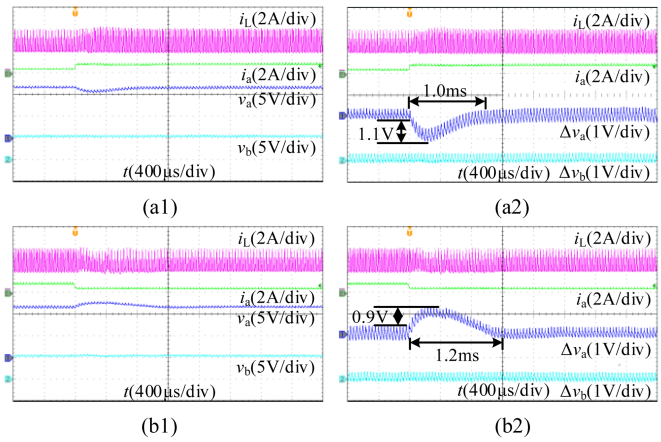

Fig. 20. Experimental waveforms of VM-CF controlled PCCM SIDO buck converter with i_a step variation. (a) Step-up. (b) Step-down.

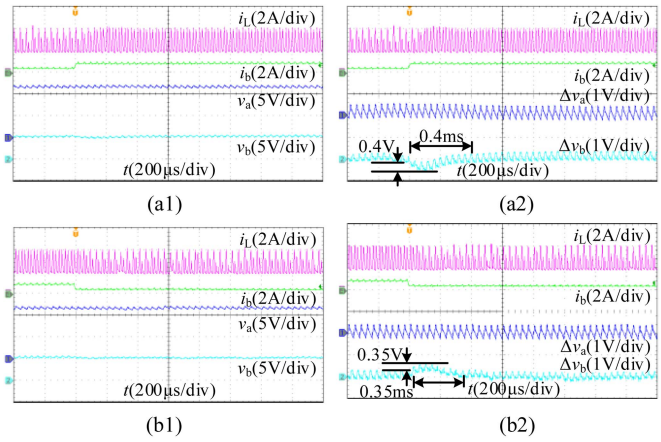

Fig. 21. Experimental waveforms of VM-CF controlled PCCM SIDO buck converter with i_b step variation. (a) Step-up. (b) Step-down.

Based on the experimental hardware circuit, the experimental results of the proposed CC-DF controlled PCCM SIDO buck converter and the traditional VM-CF controlled PCCM SIDO buck converter, including cross-regulation, load transient, load range, efficiency, and comparison analysis, are presented to show the advantages of proposed control scheme.

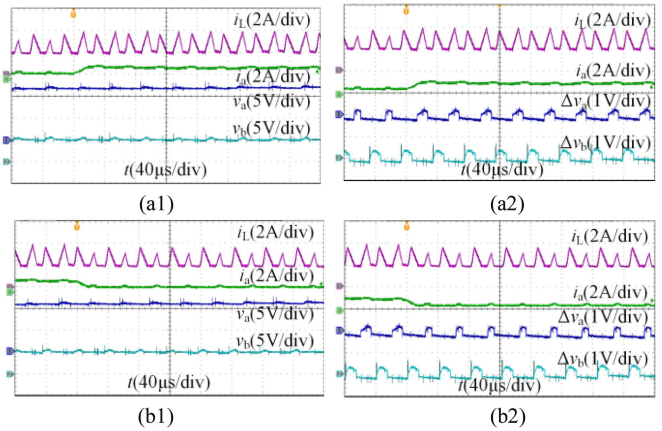

Fig. 22. Experimental waveforms of VR-CF controlled PCCM SIDO buck converter with i_a step variation (a) Step-up. (b) Step-down.

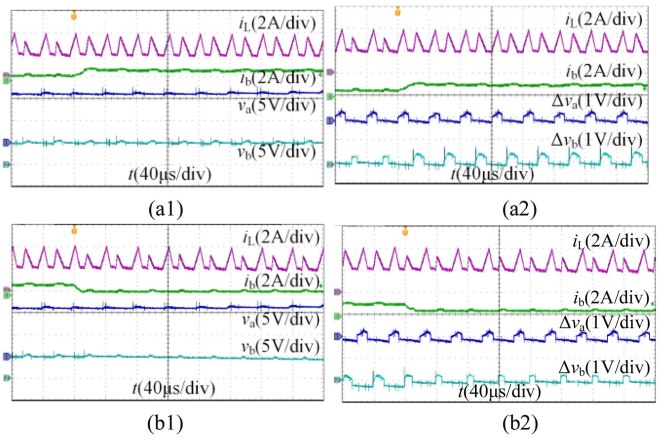

Fig. 23. Experimental waveforms of VR-CF controlled PCCM SIDO buck converter with i_b step variation. (a) Step-up. (b) Step-down.

B. Cross-regulation and Load Transient

Figs. 20–25 show the load transient experimental waveforms of inductor current, load current and output voltages under VM/VR-CF control and CC-DF control, respectively. It can be found that the cross-regulation effect for both control schemes is totally eliminated. In other words, no observable cross-regulation can be seen in Figs. 20–25. However, the transient response time and the overshoot of the output voltages are greatly reduced for the proposed CC-DF control comparing with the VM-CF control. The load transient response of VR-CF control and CC-DF control is similar, both response time of these two controls are one switching period. This indicates that the load transient response of the proposed CC-DF control has fast transient response.

C. Load Range

Figs. 26–28 show the steady-state experimental waveforms of PCCM SIDO buck converter for VM/VR-CF control or CC-DF control under different load resistances. It shows that the proposed CC-DF control can widely broaden the load range.

TABLE III
COMPARISON WITH VM/VR-CF CONTROLLED PCCM SIDO BUCK CONVERTER

Performance		This paper (CC-DF control)	VM-CF control	VR-CF control
FOM(cross)	Output a	0	0	0
	Output b	0	0	0
FOM(self)	Output a	0.017	0.092	0.015
	Output b	0.006	0.08	0.008
Load transient	Output a	1 T_s	30 T_s	1 T_s
	Output b	2 T_s	10 T_s	1 T_s
Load range		$I_{a(max)}$ = 2.08A, $I_{b(max)}$ = 2.67A	$I_{a(max)}$ = 1.24A, $I_{b(max)}$ = 1.19A	$I_{a(max)}$ = 1.24A, $I_{b(max)}$ = 1.19A
Light load efficiency		Higher than 87%	Lower than 82%	Lower than 82%

FOM(self): (overshoot in output voltage in self channel/rated voltage)/(load step in self channel/rated load).

FOM(cross): (overshoot in output voltage in cross channel/rated voltage)/(load step in cross channel/rated load).

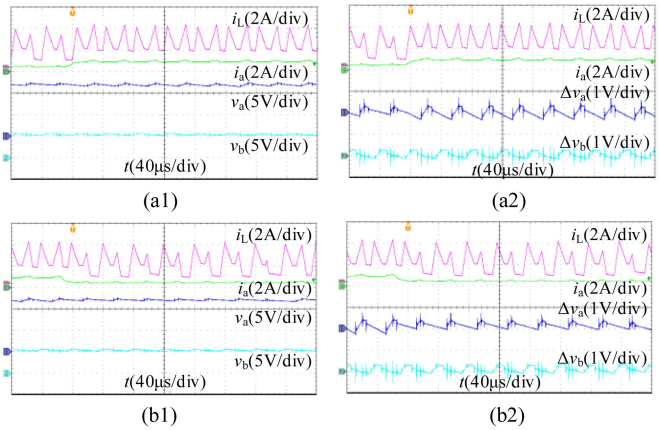

Fig. 24. Experimental waveforms of CC-DF controlled PCCM SIDO buck converter with i_a step variation. (a) Step-up. (b) Step-down.

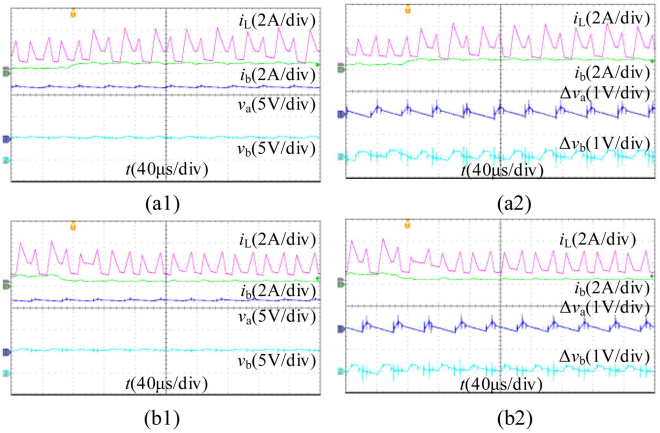

Fig. 25. Experimental waveforms of CC-DF controlled PCCM SIDO buck converter with i_b step variation. (a) Step-up. (b) Step-down.

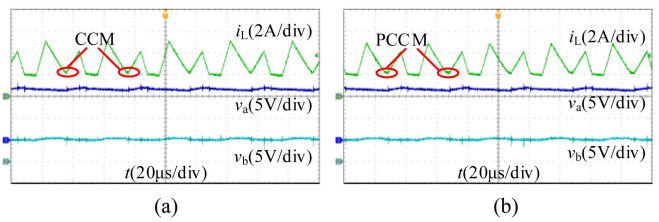

Fig. 26. Experimental waveforms of VM-CF controlled PCCM SIDO buck converter under different load resistances: (a) R_a = 12 Ω and R_b = 3 Ω. (b) R_a = 12 Ω and R_b = 3.2 Ω.

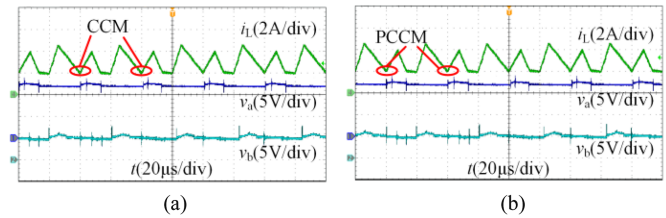

Fig. 27. Experimental waveforms of VR-CF controlled PCCM SIDO buck converter under different load resistances: (a) R_a = 12 Ω and R_b = 3 Ω. (b) R_a = 12 Ω and R_b = 3.2 Ω.

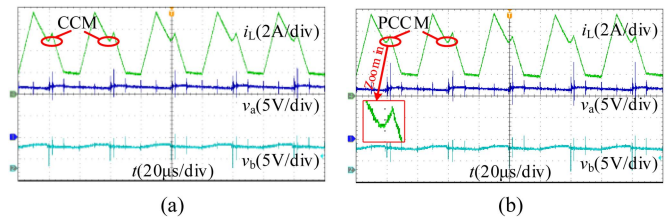

Fig. 28. Experimental waveforms of CC-DF controlled PCCM SIDO buck converter under different load resistances: (a) R_a = 12 Ω and R_b = 1.8 Ω. (b) R_a = 12 Ω and R_b = 1.9 Ω.

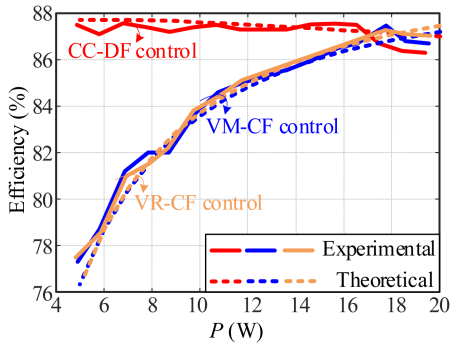

Fig. 29. Experimental and theoretical efficiency curves for PCCM SIDO buck converter under CC-DF control and VM/VR-CF control.

D. Efficiency

Fig. 29 shows the experimental and theoretical efficiency curves for CC-DF and VM/VR-CF controlled PCCM SIDO buck converter under different power conditions. The experimental results are consistent well with the theoretical results. For VM-CF control, the test results present with an 87.3% maximum efficiency at 17.7 W. For VR-CF control, the test results present

with an 87% maximum efficiency at 17.7W. Both efficiency of VM-CF control and VR-CF control would reduce quickly with the power decreasing. However, the proposed CC-DF control shows more than 86% efficiency in all power conditions. With the power decrease, the efficiency for CC-DF control is slightly increased, which is significantly different from the VM-CF control.

E. Comparison Analysis

To examine the performance improvement generated by the proposed control approach, numerical comparison with the VM/VR-CF controlled PCCM SIDO buck converter is carried out and given in Table III. Two critical performance indices FOM(self) and FOM(cross) have been defined in [6] and [21] to estimate the performance of the existing methods for the SIMO dc-dc converter, as shown at the bottom of Table III. Compared to the VM/VR-CF control, the proposed CC-DF controlled PCCM SIDO buck converter has the zero cross-regulation, minimum self-regulation, fast load transient, wide load range, and high efficiency. Therefore, the proposed CC-DF control is a promising control scheme for the PCCM SIDO dc–dc converter.

VI. Conclusion

In this article, a CC-DF control scheme is proposed to optimize the overall efficiency of the PCCM SIDO dc–dc converter with wide load range, minimize cross-regulation and fast load transient performance. Taking PCCM SIDO buck converter as an example, a complete small-signal model for both power circuit and control circuit was established. Based on the small-signal model, the design-oriented analysis of the transient performance and cross-regulation has been carried out to provide design guidance for improving the transient response and steady-state performance. In addition, the Bode plots were displayed to compare the cross-regulation and the transient performance under CC-DF control, VM-CF control, and VR-CF control which was verified through SIMPLIS simulation. The frequency analysis investigation showed that the CC-DF control can improve the load transient response and maintain the minimum cross-regulation. Different from the VM/VR-CF controlled PCCM SIDO dc–dc converter featuring low light load conversion efficiency due to constant freewheeling current and limited load range, the freewheeling current real-time updates through load current and capacitor current in the proposed CC-DF control. Thus, the freewheeling current and freewheeling period can be further reduced and the light-load efficiency can be effectively improved. Moreover, when freewheeling current is small, the load range of the PCCM operation mode can be further broadened. Therefore, the overall efficiency, load range, load transient response and cross-regulation of the PCCM SIDO buck converter can be optimized. All of these are verified by the experimental results.

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