Power Supply Chain With Series Insulation Structure for High Voltage Marx Pulse Generator

Yue Chen, Chenguo Yao, *Member, IEEE*, Feiyu Wu, Shoulong Dong, *Member, IEEE*, and Kai Chen

***Abstract*—Insulation power supply (IPS) for multiple switches is a key issue for solid-state pulse generators (SSPG). The existing parallel structure for IPS is short of insulation similarity, which results in low insulation utilization ratio (IUR) and limited adjustability. Here we propose a power supply chain (PSC) with series insulation structure. The insulation circumstance of PSC maintains the same for each stage, which increases the minimum IUR to almost 90%, compared to the existing parallel structures. The proposed PSC requires purely diodes, capacitors, and inductors to achieve IPS for switches, thus avoiding the customized cost and enhancing insulation adjustability. After analyzing the working principle of PSC, we evaluate the performance of PSC from the perspective of power supply and insulation. Finally, an 8-staged Marx SSPG prototype is developed to examine the compatibility of PSC and the protection circuit for PSC is implemented. The withstand voltage of PSC can be easily adjusted within 14 kV according to the number of diodes. The PSC does not require external control signals and does not interfere with gate driving synchronization or load waveforms, which offers a new solution of IPS for compact Marx generators designed at nanosecond scale.**

***Index Terms*—High voltage nanosecond pulse, insulation power supply (IPS), insulation similarity, Marx, power supply chain (PSC), series structure.**

I. Introduction

NANOSECOND pulse shows a wealth of physical effects in biomedical inactivation [1], cell electroporation [2], and etching of the electron beam [3], [4]. Solid-state pulse generators (SSPG) based on metal oxide semiconductor field effect transistor (MOSFET) or gallium nitride (GaN) switches are critical and widely applied in the above scenarios due to its compactness and controllability [5], [6]. To realize voltage multiplying without increasing the voltage stress of switches, most SSPG employs switch in series connection or a modular stacking structure. Take the classic Marx SSPG as an example [7], [8], [9], the voltage potential of all switches forms a ladder-like trend when SSPG discharges, thus requiring an independent power supply for the gate driver of each switch, which defined as insulation power supply (IPS) in this article. The circuit design and structural layout of IPS are crucial in SSPG [9], [10], [11].

To achieve IPS for all switches under a ladder-like voltage potential, parallel structure was proposed for SSPG insulation, as shown in Fig. 1(a), where the IPS of each stage withstands a high potential difference between a shared power source and each driver [9]. Specifically, the dc energy is transmitted to the gate drivers of each stage through noncontact magnetic field coupling, where a typical example is the transformer-coupled dc–dc power convertor with an optic fiber triggering signal [11], [12], [13], [14]. In recent years, a novel transformer-based IPS is proposed in the parallel structure, which achieves the hybrid delivery of electric power and the control signal by magnetic trigger gate driving [4], [6]. However, the inherent withstand voltage of a transformer-coupled IPS is fixed once the insulation of solid dielectric is customized, which is hard to be compatible with other SSPGs at different amplitudes or application scenarios. To achieve insulation adjustability in the parallel structure, a core-free dc—dc IPS based on air insulation is proposed by Wu et al. [9], where the inherent withstand voltage can be easily adjusted within 40 kV. Different insulation structure for SSPG are summarized in Table I. Although the parallel structure realizes IPS for ladder-like working conditions for staged SSPGs, there is lack of insulation similarity, specifically as follows.

1) At higher stages, the voltage stress of the IPS step increases (e.g.,: 1, 2…8 kV for a voltage stress of 1 kV in each switch). So, the risks of insulation aging and breakdown increase accordingly for higher stages.
2) At lower stages, the insulation utilization ratio (IUR) of the IPS step decreases (e.g.,: 10%, 20% …80% for a voltage stress of 1 kV and the inherent withstand voltage of 10 kV for the IPS), which results in great insulation waste for lower stages.

In this article, we propose a power supply chain (PSC) based on the series insulation structure, which is composed of diodes and capacitors, as in Fig. 1(b). Specifically, the interstage insulation is achieved through the reverse blocking of the diodes when switches are turned ON under a stepped-up potential, while diodes transfer power to the gate driver of each stage when switches are turned off. The PSC works without any external signals and does not interfere with the synchronicity and freedom of the switch trigger, which provides support for generating special pulse waveforms such as high voltage ultrashort pulses [14] or

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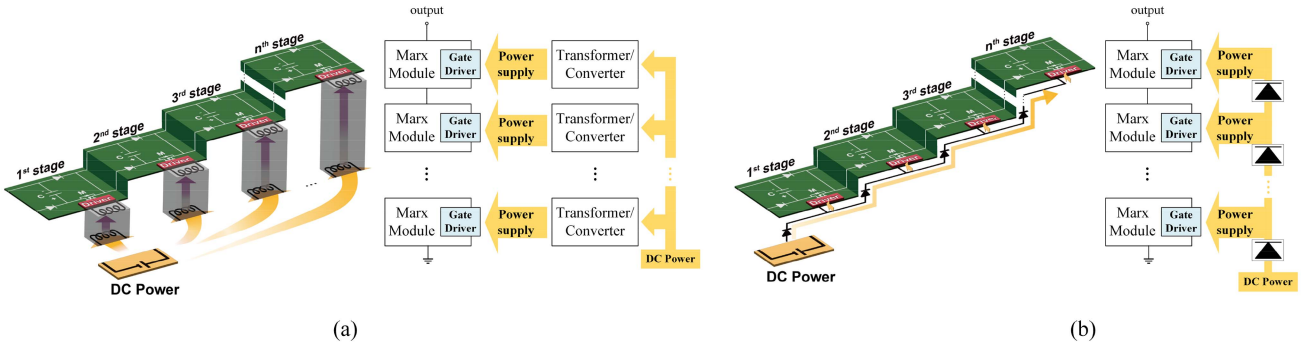

Fig. 1. Two structures of insulation scheme for stacked SSPG. (a) Parallel structure. (b) Series structure.

TABLE I
COMPARISON AND KEY PARAMETERS OF INSULATION FOR SOLID STATE PULSE GENERATORS

Structure	Stage number	Amplitude	Inherent withstand voltage of IPS	Minimum voltage stress among stages	Minimum IUR*	Insulation adjustability	Insulation similarity	Ref
Parallel	10	8kV	15kV	0.8kV	5.33%	No	No	[15]
	10	10kV	15kV	1kV	6.67%			[13]
	7	5kV	15kV	0.714kV	4.76%			[12]
	24	24kV	40kV	1kV	2.5%	Yes		[9]
Series	**8**	**7kV**	**1kV**	**0.875kV**	**87.5%**	**Yes**	**Yes**	**This work**

Note*: For the IPS of each stage, insulation utilization ratio (IUR) is defined as the ratio of the voltage stress to the inherent withstand voltage. For series structure (PSC), the inherent withstand voltage is the repetitive peak reverse voltage of the diode.

multilevel pulses [16]. The PSC based on the series structure takes up the following advantages over the parallel structure.

1) The voltage stress or IUR of every diodes are equal (e.g.,: 0.8, 0.8 … 0.8 kV and 80%, 80% … 80% for 0.8 kV voltage stress and 1 kV inherent withstand voltage).
2) Withstand voltage can be freely adjusted by altering the number of diode chains.

Our work analyzes the working principle and regulatory factors of PSC in detail. Besides, we study the performance of PSC from the aspects of insulation and power supply. Finally, we develop a prototype of nanosecond pulse generator to test the practicability of PSC and the protection circuit for PSC is implemented. Our results from theory, simulation, and measurement reveal that the PSC is well compatible into SSPG, with high IUR in each stage (close to 90%) and high insulation adjustability (from 1 to 14 kV). Besides, the PSC does not interfere with the synchronization (less than 4 ns jitters and close) and high frequency (reach up to 1 MHz in burst mode) of gate drivers. Meanwhile, PSC with protection circuit and control system has the engineering performance of resisting voltage spike and switching overcurrent protection. Our work, from a structural scale, realizes the insulation similarity, which maintains the balance for each stage and offers a new point of view for SSPG interstage insulation.

The rest of this article is organized as follows. The fundamental working principle of PSC is revealed in Section II. Power supply performance and insulation performance are examined in Sections III and IV, respectively. Section V is the tests on the PSC-based prototype of a nanosecond Marx SSPG and the protection and optimization for PSC.

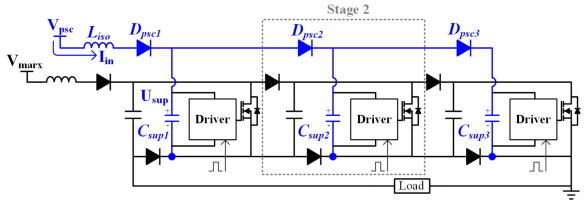

Fig. 2. PSC-based Marx generator for three stages as an example.

II. WORKING PRINCIPLE OF THE PROPOSED PSC

The basic circuit topology of a PSC-based Marx generator for three stages is shown in Fig. 2 as an example, where V_{psc} refers to the input voltage of the auxiliary dc power for PSC and V_{marx} denotes the charging voltage of Marx topology. The isolation inductor L_{iso} of PSC isolates the potential difference between the auxiliary dc power and the main circuit when pulse generator is discharging. Consequently, L_{iso} prevents excessive input current I_{in} of the auxiliary power, protecting the auxiliary power effectively. The diode D_{psc} of PSC in each stage is used to realize interstage insulation and the capacitor C_{sup} of PSC in each stage maintains the energy supply for the drivers. The voltage supplied by PSC to the driver is the voltage U_{sup} across C_{sup}. Besides, independent fiber triggering for each stage is adopted as pulse signal source for drivers.

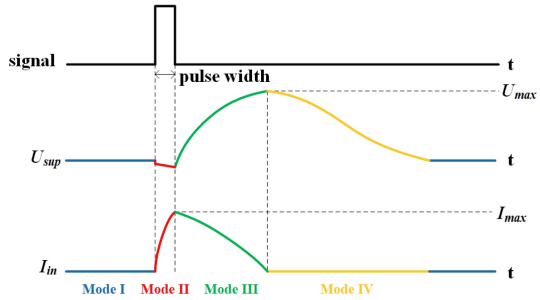

Fig. 3. Waveforms of U_{sup} and I_{in}.

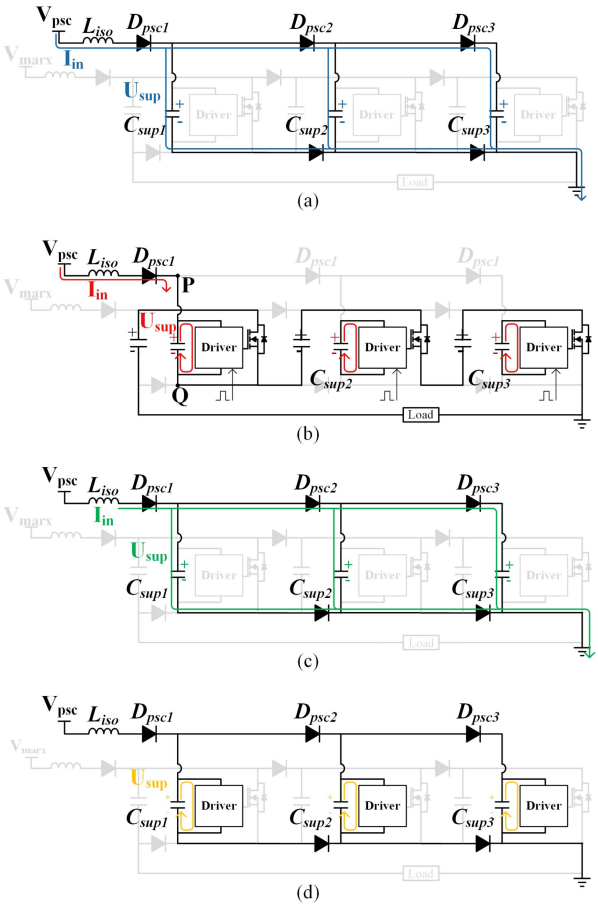

Fig. 4. PSC working mode schematic. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

Fig. 3 illustrates the timing diagram of pulse signal, the waveform of the voltage U_{sup} and I_{in}. The parasitic parameters are ignored during mathematical derivations in this section. However, in Section III, the parasitic parameters are considered to analyze the efficiency of PSC. The four operating modes in one cycle can be explained as follows.

A. Four Working Modes of PSC

1) Mode I: As shown in Fig. 4(a), the system is in a steady state, and waits for the external signal to trigger. U_{sup} and I_{in} maintain a steady value. Meanwhile, C_{sup} are charged by the auxiliary dc power. The charging loop is formed by L_{iso}, D_{psc}, and the diodes of Marx topology, which does not pass through the load.

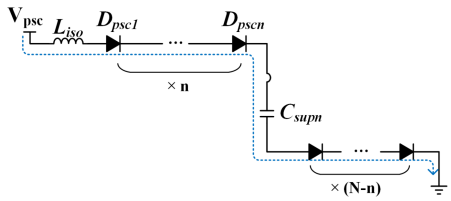

Fig. 5. Charging loop of $C_{\mathrm{sup}\,n}$ in Stage n.

As shown in Fig. 5, $U_{\mathrm{sup}\,n}$ (the U_{sup} of Stage n) can be calculated according to Kirchhoff's voltage law as follows:

$$U_{\mathrm{sup}\,n} = V_{\mathrm{psc}} - n \cdot V_{\mathrm{loss1}} - (N-n) \cdot V_{\mathrm{loss2}} \tag{1}$$

where V_{loss1} and V_{loss2} denote the voltage loss of D_{psc} and the diodes of Marx topology, respectively, and N refers to the total stage number. Particularly, D_{psc} and the diodes of Marx topology are selected the same model in this work, so the voltage loss are regarded the same

$$V_{\mathrm{loss1}} = V_{\mathrm{loss2}} = V_{\mathrm{loss}}. \tag{2}$$

Therefore, U_{sup} of each stage remains the same, which can be described as follows:

$$U_{\mathrm{sup1}} = U_{\mathrm{sup2}} = \cdots = U_{\mathrm{sup}n} = U_{\mathrm{sup}} = V_{\mathrm{psc}} - N \cdot V_{\mathrm{loss}}. \tag{3}$$

2) Mode II: As shown in Fig. 4(b), the Marx generator is in discharging state. The MOSFETs are kept ON from external pulse trigger by C_{sup}, which supply power to the drivers in each stage. During this mode, the potential of the node Q [in the first stage in Fig. 4(b)] V_Q can be described as follows:

$$V_Q = -(N-1)\, V_{\mathrm{marx}}. \tag{4}$$

Correspondingly, the potential of the node P [in the first stage in Fig. 4(b)] V_P is as follows:

$$V_P = V_Q + U_{\mathrm{sup}} = U_{\mathrm{sup}} - (N-1)\, V_{\mathrm{marx}}. \tag{5}$$

L_{iso} is compelled to charge due to the potential difference between the auxiliary dc power and the point P. The inductor charging equation is as follows according to Kirchhoff's voltage law:

$$L_{\mathrm{iso}} \frac{dI_{\mathrm{in}}}{dt} = V_{\mathrm{psc}} - V_P - V_{\mathrm{loss}} = (N-1)\ (V_{\mathrm{marx}} + V_{\mathrm{loss}}). \tag{6}$$

The maximum current of I_{in} can be calculated from (6)

$$\begin{aligned} I_{\mathrm{max}} &= \int_0^{\mathrm{pw}} \frac{(N-1)\,(V_{\mathrm{marx}} + V_{\mathrm{loss}})}{L_{\mathrm{iso}}} dt \\ &= \frac{\mathrm{pw}}{L_{\mathrm{iso}}} (N-1)\,(V_{\mathrm{marx}} + V_{\mathrm{loss}}) \end{aligned} \tag{7}$$

where I_{max} is marked in Fig. 3 and pw is the pulsewidth of the signal.

3) Mode III: As shown in Fig. 4(c), MOSFETS are turned OFF. $L_{\rm iso}$ releases energy into $C_{\rm sup}$ of each stage, which increases the $U_{\rm sup}$ and can be described as follows:

$$NL_{\rm iso}C_{\rm sup}\frac{d^2U_{\rm sup}}{dt} + U_{\rm sup} = V_{\rm psc} - N\cdot V_{\rm loss}. \tag{8}$$

The corresponding characteristic equations and characteristic roots from (8) are as follows:

$$s^2 + \frac{1}{NL_{\rm iso}C_{\rm sup}} = 0,\ s = \pm\sqrt{\frac{1}{NL_{\rm iso}C_{\rm sup}}}j. \tag{9}$$

The expressions for $U_{\rm sup}$ and $I_{\rm in}$ in Mode III are calculated from (8) and (9)

$$U_{\rm sup}(t) = V_{\rm psc} - N\cdot V_{\rm loss} + \frac{(N-1)V_{\rm marx}\cdot {\rm pw}}{\sqrt{NL_{\rm iso}C_{\rm sup}}} \cdot \sin\sqrt{\frac{1}{NL_{\rm iso}C_{\rm sup}}}t \tag{10}$$

$$I_{\rm in}(t) = \frac{V_{\rm psc} - N\cdot V_{\rm loss}}{L}t + (N-1)V_{\rm marx}\frac{\rm pw}{L}\cos\sqrt{\frac{1}{NL_{\rm iso}C_{\rm sup}}}t. \tag{11}$$

When the energy release from $L_{\rm iso}$ finished, $U_{\rm sup}$ reaches its maximum value $U_{\rm max}$, which can be numerically calculated from (10) and (11), which is revealed in Fig. 3.

4) Mode IV: As shown in Fig. 4(d), the charged $C_{\rm sup}$ in each stage releases excessive energy through the driver until $U_{\rm sup}$ returns to the steady value, where the discharging time is affected by $C_{\rm sup}$ and the equivalent resistance $R_{\rm eq}$ of driver's input side.

B. Selection of Key Components

1) Selection of C_{sup}*:* As shown in Fig. 4(b), when PSC is in Mode II, $C_{\rm sup}$ forms an independent discharge loop with the input terminal of the corresponding driver. The expression of $U_{\rm sup}$ is as follows:

$$U_{\rm sup}(t) = U_{\rm steady}\cdot e^{-\frac{t}{R_{\rm eq}\cdot C_{\rm sup}}} \tag{12}$$

where $U_{\rm steady}$ is the voltage of $U_{\rm sup}$ in steady state. Therefore, in Mode II the voltage drop $U_{\rm drop}$ of $U_{\rm sup}$ is as follows:

$$U_{\rm drop} = U_{\rm steady} - U_{\rm sup}(t={\rm pw}) = U_{\rm steady}\left(1 - e^{-\frac{\rm pw}{R_{\rm eq}\cdot C_{\rm sup}}}\right). \tag{13}$$

Furthermore, to prevent excessive $U_{\rm drop}$ in Mode II, we specified that $U_{\rm drop}$ should not exceed 10% of the steady-state value. Therefore, $C_{\rm sup}$ should meet the following requirements:

$$C_{\rm sup} > \frac{\rm pw}{0.1\cdot R_{\rm eq}}. \tag{14}$$

2) Selection of L_{iso}*:* To ensure the safety of the auxiliary dc power, it is important to avoid excessive $I_{\rm in}$. Here, we define that $I_{\rm max}$ should not exceed the safety threshold $I_{\rm safe}$. Therefore, according to the expression of $I_{\rm max}$ in (7), $L_{\rm iso}$ should meet the requirement as follows:

$$L_{\rm iso} > \frac{\rm pw}{I_{\rm safe}}(N-1)(V_{\rm marx} + V_{\rm loss}). \tag{15}$$

TABLE II
CONTROLLED PARAMETERS OF PSC IN SIMULATION

Parameter	Value
Capacitor of PSC, $C_{\rm sup}$	300 nF
Isolation inductor of PSC, $L_{\rm iso}$	2 mH
The input voltage of the auxiliary DC power, $V_{\rm psc}$	24 V
Pulse width, pw	200 ns
The equivalent resistance of driver's input side, $R_{\rm eq}$	100 Ω
Charging Voltage of Marx topology, $V_{\rm marx}$	500 V
Capacitor of Marx topology, $C_{\rm marx}$	1 uF
Isolate inductor of Marx topology, $L_{\rm marx}$	2 mH
Load of Marx topology, $R_{\rm load}$	100 Ω
Stage number, N	10
Parasitic inductance in PSC, L_s	50 nH

C. Limitation of Pulsed Width

By referring to (14), we can determine one upper limit for pw

$${\rm pw} < 0.1\cdot C_{\rm sup}R_{\rm eq}. \tag{16}$$

Besides, we can determine another upper limit for pw from (15)

$${\rm pw} < \frac{I_{\rm safe}L_{\rm iso}}{(N-1)(V_{\rm marx} + V_{\rm loss})} \tag{17}$$

where pw should satisfy both (16) and (17).

III. POWER SUPPLY PERFORMANCE

In this section, we study the supply stability and energy transfer efficiency of PSC. Specifically, the impact of the capacitor voltage $U_{\rm sup}$ is simulated, which includes external regulation factors and internal component values. In addition, we explore the effect of the equivalent resistance $R_{\rm eq}$ of driver's input side on voltage gain. The rest of this section discusses the impact of $R_{\rm eq}$ on energy loss and energy transfer efficiency from an energy perspective. In this simulation, we select DSEP29-12A as diode model, C3M0065100J as MOSFET model and IXDN609 as driver model. Simulation parameters are as Table II.

A. Power Supply Stability

First, the power supply stability is evaluated by observing the fluctuation amplitude of $U_{\rm sup}$ during one cycle.

The impact of the external regulation factors including $V_{\rm marx}$ and pw on $U_{\rm sup}$ is depicted in Fig. 6(a) and (b). The fluctuation amplitude is directly proportional to $V_{\rm marx}$ and pw, which is in accordance with (10) and (11). Therefore, to ensure that the fluctuation amplitude of $U_{\rm sup}$ remains within the safe range, it is recommended that pw should not exceed the microsecond level.

The impact of the internal components including $L_{\rm iso}$ and $C_{\rm sup}$ on $U_{\rm sup}$ is shown in Fig. 6(c) and (d). Increasing the values of $L_{\rm iso}$ and $C_{\rm sup}$ results in a reduction of the voltage fluctuation amplitude. However, this cause $U_{\rm sup}$ taking longer to enter Mode I, which is not beneficial for achieving high-frequency pulses. Consequently, in order to improve the power supply stability

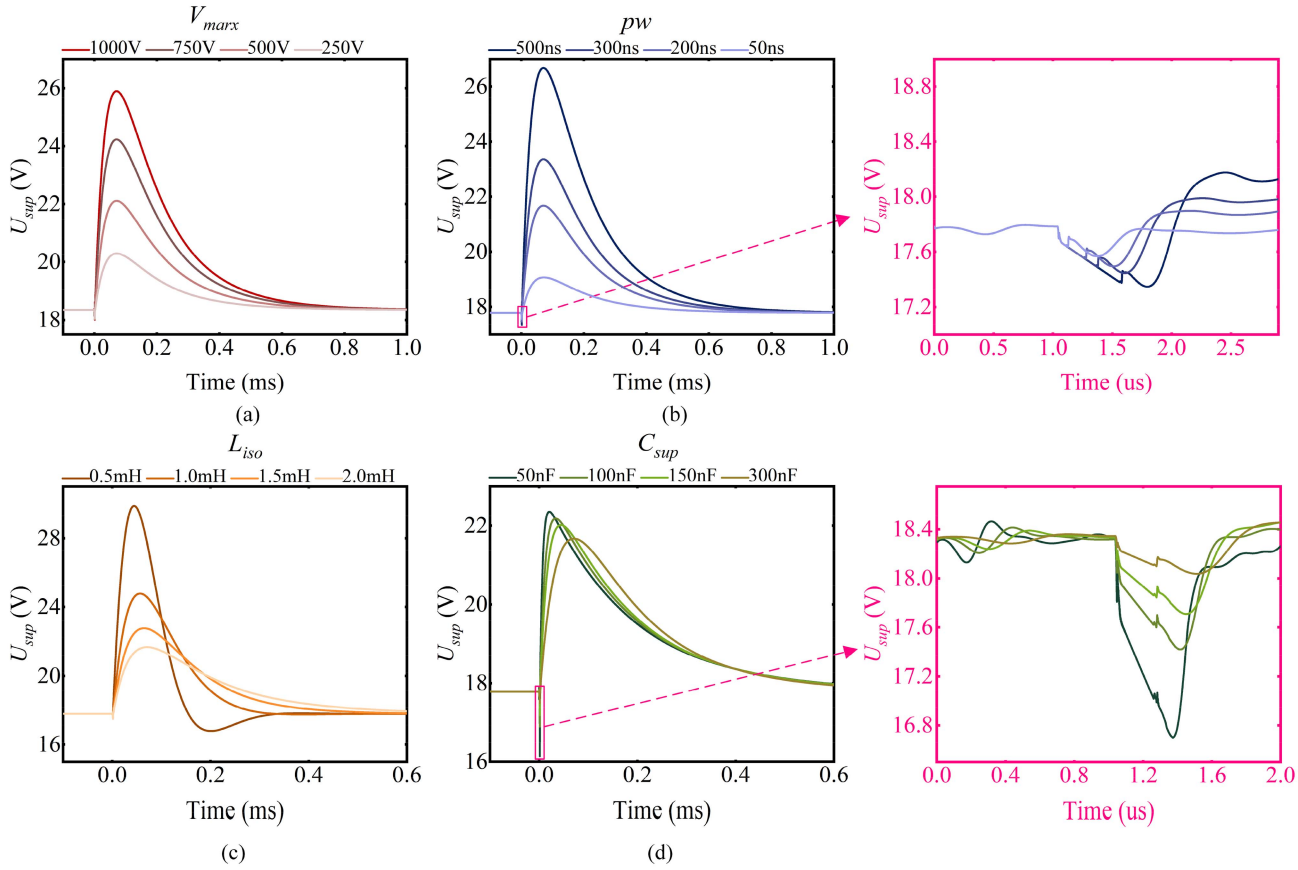

Fig. 6. Simulation of waveforms of U_{sup} in PSC. (a) Impact of V_{marx}. (b) Impact of pw. (c) Impact of L_{iso}. (d) Impact of C_{sup}. Note: In Fig. 6(a)–(d), the trigger signals are all started at the moment $t = 1.0$ μs.

for low frequency SSPG, it is recommended to choose larger L_{iso} and C_{sup} in PSC. Meanwhile, for high-frequency SSPG, it is important to consider both the supply stability and the cycle time of PSC simultaneously.

The power supply stability is not only determined by the fluctuation of U_{sup} after MOSFET returned OFF, but also by the voltage drop of U_{sup} during Mode II. The diagram with pink frame in Fig. 6(b) and (d) illustrate the voltage drop of U_{sup}, which is affected by pw and C_{sup}.

Excessive voltage drop results in inadequate voltage supply for the driver, which impact the maintenance of the switch ON. Therefore, in PSC-based SSPG, it is recommended to ensure that pw does not exceed the subtle level and that C_{sup} is maximized.

U_{sup} in Mode I is greatly affected by R_{eq}, which affects the voltage gain of PSC accordingly, as shown in Fig. 7. The diode experiences on-state losses which results in a reduction of voltage. Hence, selecting a driver with a higher R_{eq} can enhance the voltage gain and minimize the voltage loss.

B. Power Supply Efficiency

The energy loss in PSC is a result of the diode on-state loss and parasitic parameters. Fig. 8 illustrates the energy distribution and transfer efficiency of PSC when R_{eq} is changed at 1 Hz

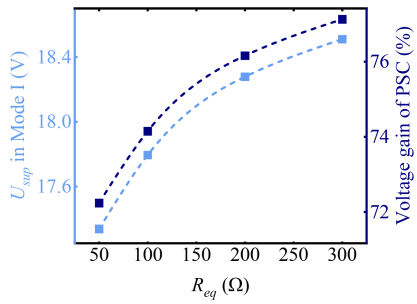

Fig. 7. U_{sup} in Mode I and the voltage gain of PSC with changed R_{eq}.

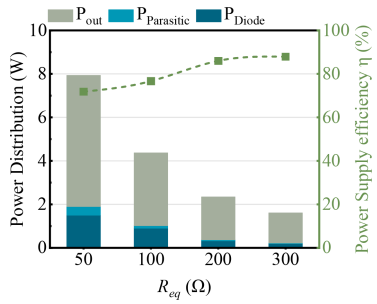

Fig. 8. PSC energy distribution and transfer efficiency with changed R_{eq}.

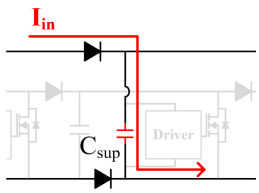

Fig. 9. Short circuit of voltage supply side in PSC.

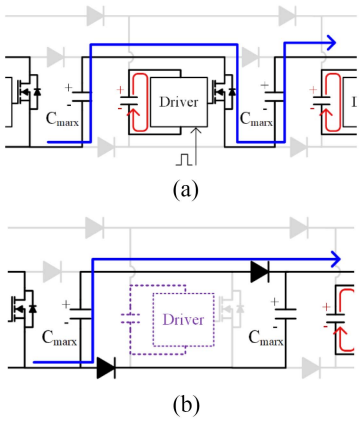

Fig. 10. Short circuit of voltage supply side in PSC. (a) Normal situation. (b) Open circuit of voltage supply side in PSC.

pulse repetition frequency. Selecting drivers with larger R_{eq} contributes to higher efficiency for PSC, which is nearly up to 90% when R_{eq} is set at 300 Ω.

C. Fault Analysis of PSC

The fault analysis of PSC in voltage supply side for the driver is carried out, including short circuit and open circuit.

1) Short Circuit: As depicted in Fig. 9, when the gate driver or C_{sup} in one stage experiences a short circuit, the charging current I_{in} abruptly rises due to the significant decrease in the charging loop resistance of this stage.

This sudden increase of I_{in} triggers the overcurrent protection of the auxiliary power supply V_{psc}, resulting in a temporary disconnection of V_{psc}.

2) Open Circuit: As shown in Fig. 10, in the case of open circuit, the MOSFET in this stage cannot be turned ON, so the capacitors C_{marx} of two adjacent stages are connected in parallel, which lead to the drop of output pulse amplitude.

IV. Insulation Performance

To verify the insulation performance and adjustability of PSC, an experimental platform is constructed to test insulation breakdown, as shown in Fig. 11.

We apply DW-P104-100ACH4 with a capacity of 100 kV/100 mA from DONGWEN company as the high-voltage dc power HVDC. To prevent the damage due to excessive breakdown current, protective resistors (10 kΩ, 300 W) are connected in series with the HVDC. The high-voltage probe

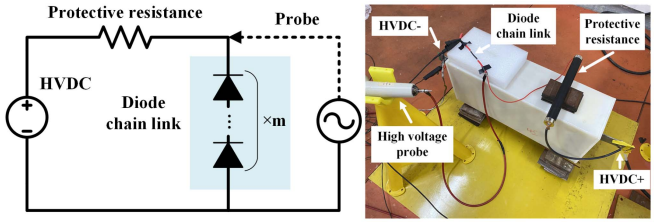

Fig. 11. Schematic and actual breakdown test platform.

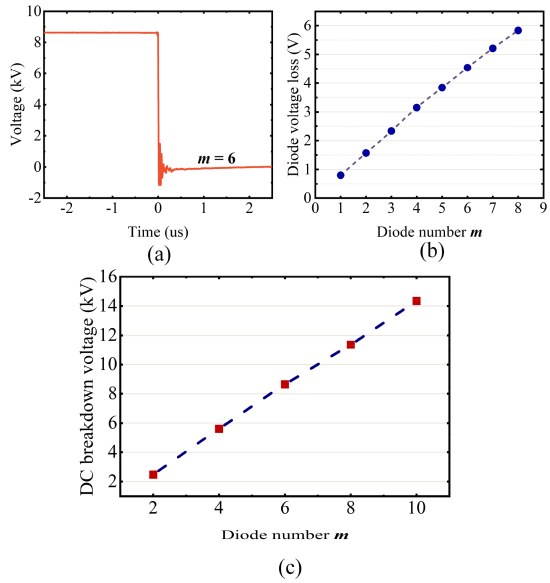

Fig. 12. (a) Measured breakdown waveform when diode number m is 6. (b) Voltage loss with varying diode number m. (c) Relationship between diode number m and breakdown voltage.

(Tektronix P6015A, 20 kV DC) transmits the waveform signal to the oscilloscope (HDO6034A 350 MHz) via the BNC.

The breakdown waveform of the diode can be obtained by setting oscilloscope to trigger the falling edge, shown in Fig. 12(a).

In order to test the insulation adjustability of PSC, dc breakdown voltage at different diode number m is measured as shown in Fig. 12(c). Therefore, the diode we selected or the number of diodes in series should meet the withstand voltage requirements to prevent PSC diodes from being broken down.

More diodes are able to insulate higher voltages. However, this result in an increase in voltage loss, as shown in Fig. 12(b). To compensate for the voltage loss, V_{psc} can be increased according to the requirements.

To verify the insulation similarity, the withstand voltage of each stage are tested in comparison with parallel structure, as shown in Fig. 13. In parallel structure, the IPS withstand voltage rises in steps as the number of stages increases. In contrast, series-based PSC have the identical withstand voltage of 0.88 kV from the second stage onward. This insulation similarity contributes stability and balance in SSPG.

Table III shows the recommended parameter for PSC used in different insulation requirements.

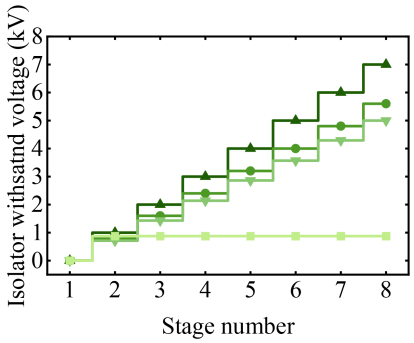

Fig. 13. Comparison of insulation similarity between parallel structure and series structure. In this figure, ▲ refers to Ref [9]. ● refers to Ref [15]. ▼ refers to Ref [12]. ■ refers to this work.

TABLE III
PARAMETERS OF THE PSC-BASED PROTOTYPE

Parameter	Value
Capacitor of PSC, C_{sup}	300 nF
Isolation inductor of PSC, L_{iso}	2.1 mH
The input voltage of the auxiliary DC power, V_{psc}	24 V
Pulse width, pw	200 ns
Charging Voltage of Marx topology, V_{marx}	500 V
Capacitor of Marx topology, C_{marx}	300 nF
Isolate inductor of Marx topology, L_{marx}	2.1 mH
Load of Marx topology, R_{load}	100 Ω
Stage number, N	8

TABLE IV
MAIN COMPONENTS OF THE PSC-BASED PROTOTYPE

Component	Model	Specifications
MOSFET	NVBG160N120SC1	V_{DSS}=1200 V, $I_{D(pulse)}$=78 A, t_r=11 ns, t_f=7.4 ns, $t_{d(off)}$=15 ns
Diode	DSEP12-12A (simulation)	V_r=1200 V, V_f=2.75 V, I_{FAV}=12 A
	US5M (test)	V_r=1000 V, V_f=1.7 V, I_{FAV}=5 A
Driving Chip	IXDN609	I_{drive}=9 A, V_{CC}:-0.3~40 V

Note: V_{DSS}: drain–source breakdown voltage, $I_{D(pulse)}$: maximum pulsed drain current, t_r: rise time, t_f: fall time, $t_{d(off)}$: turn-OFF delay time, V_r: reverse blocking voltage, V_f: forward voltage drop, I_{FAV}: average forward current, I_{drive}: maximum drive current, V_{CC}: safe supplying voltage.

V. TEST ON SSPG PROTOTYPE WITH PSC

To verify compatibility of PSC for SSPG, an 8-stage prototype is designed, as shown in Fig. 14.

The parameters and main components are shown in Tables III and IV.

A. PSC Performance

For component selection, US5M is chosen as PSC diode, which can withstand 1 kV. To prevent magnetic saturation of the inductor, both $L_{\rm iso}$ and $L_{\rm marx}$ utilize 2.1 mH air core inductors. $C_{\rm sup}$ is 300 nF and $V_{\rm psc}$ is 24 V.

Fig. 15(a) and (b) illustrate the measured waveform of $I_{\rm in}$ and $U_{\rm sup}$ in one cycle, with $V_{\rm marx}$ set at 500 V and pw at 200 ns. The maximum amplitude fluctuation of $I_{\rm in}$ is no higher than 4 A,

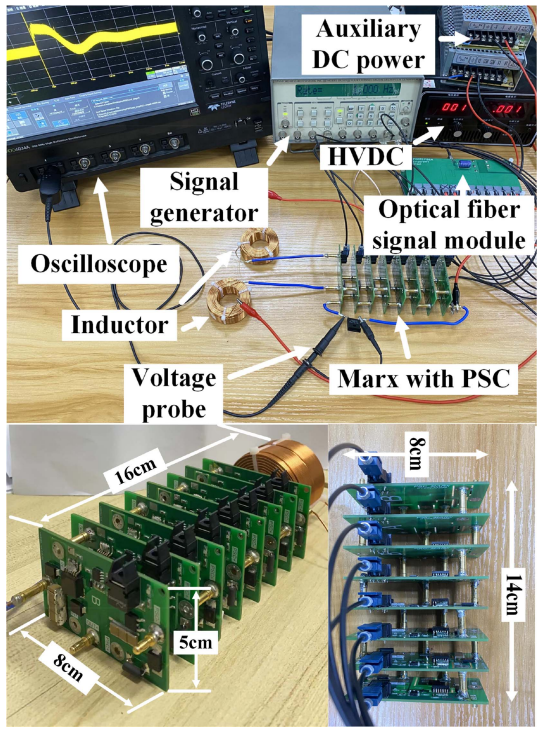

Fig. 14. Test prototype and experiment platform.

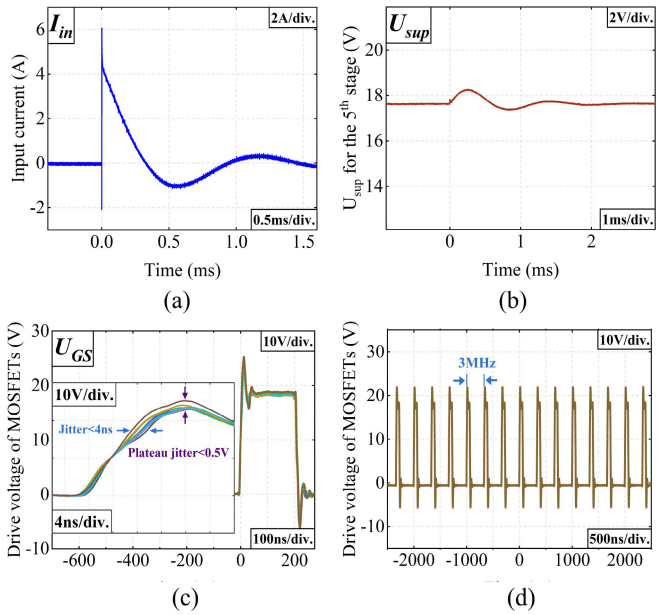

Fig. 15. (a) Measured waveform of input $I_{\rm in}$. (b) Measured waveform of $U_{\rm sup}$ for the 5th stage. (c) Synchronicity of each stage at 200 ns trigger signal. (d) Waveform of U_{GS} at 3 MHz under PSC power supply.

and the voltage fluctuation of $U_{\rm sup}$ is no higher than 3 V, both of which fall within the safe range.

In order to verify the identicalness of voltage supply in PSC at each stage, we measure the waveform of the driving voltage U_{GS} of 8-stage MOSFETS as shown in Fig. 15(c). The driving waveforms of all stages are nearly identical, with plateau value

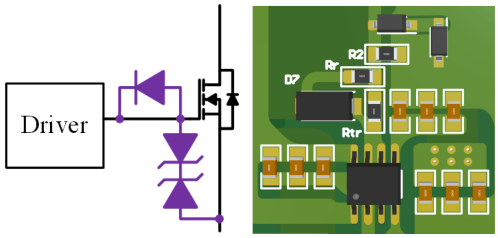

Fig. 16. Gate protection circuit and PCB layout.

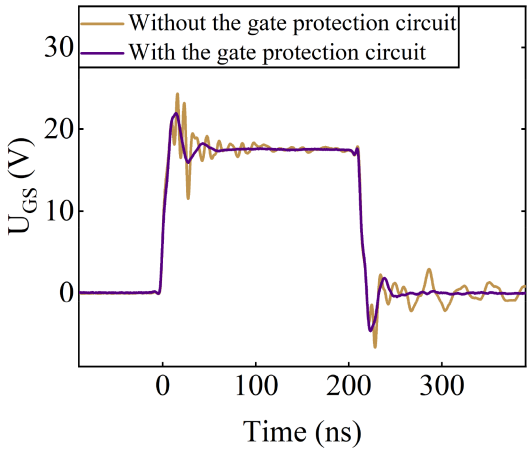

Fig. 17. Waveform of U_{GS} with or without the gate protection circuit.

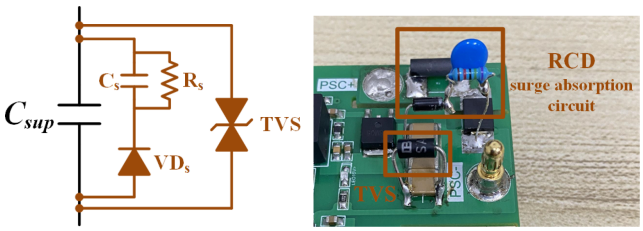

Fig. 18. Schematic and actual surge absorption circuit.

jitter lower than 0.5 V and pulsed edges jitter well controlled within 4 ns. The waveform of U_{GS} at 3 MHz under PSC power supply is shown in Fig. 15(d), which demonstrate the reliable power supply performance of PSC at 3 MHz.

B. Protection and Optimization

To ensure the reliability of the whole system, the protection measures for MOSFET gate side, PSC voltage supply side, and main loop current are implemented as gate protection circuit, surge absorption circuit, and overcurrent protection, respectively.

1) Gate Protection Circuit: To optimize the driving waveform and protect MOSFET from overvoltage on the gate side, the gate protection circuit around the driver is indispensable, as shown in Fig. 16.

In the absence of the surge absorption circuit and the gate protection circuit, the driving waveform is greatly impacted by the surge of the supply voltage and deteriorates. With the gate protection circuit, the influence on the driving waveform is improved, as shown in the Fig. 17.

2) Surge Absorption Circuit: Furthermore, the surge absorption circuit is applied to suppress the surge of the supply voltage, so as to protect the driver and reduce the impact on the driving waveform. An RCD surge absorption circuit [17] and transient

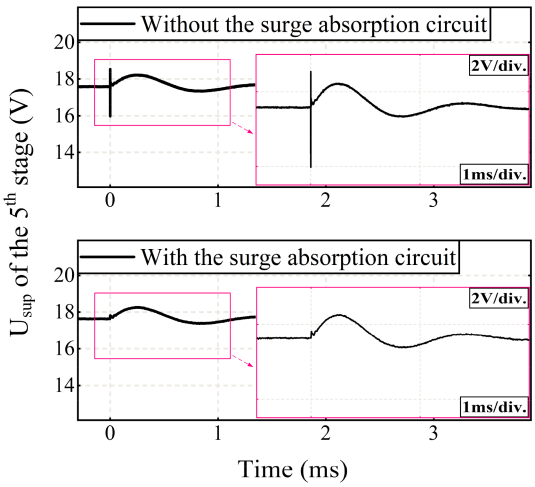

Fig. 19. Voltage supply waveform of U_{sup} with and without the surge absorption circuit.

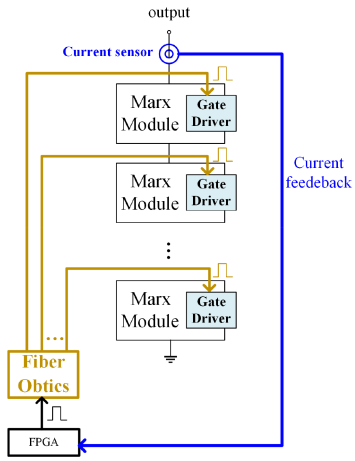

Fig. 20. Current feedback diagram.

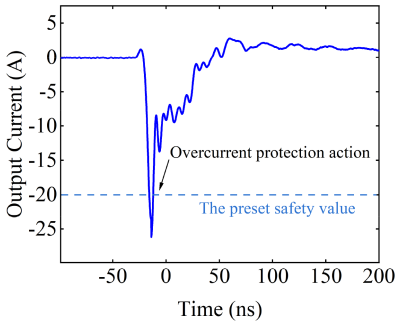

Fig. 21. Overcurrent protection action.

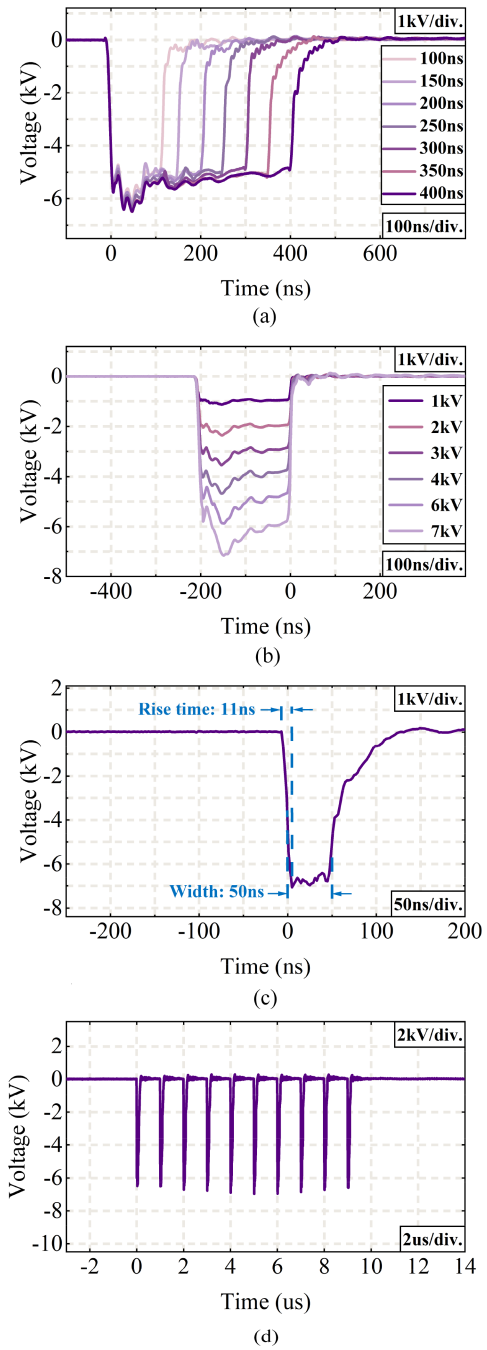

Fig. 22. Output pulse waveform of the PSC-based prototype.

voltage suppressor are implemented to the voltage supply terminal of PSC, as shown in Fig. 18.

The comparison of voltage supply waveform before and after implementing the surge absorption circuit is illustrated in Fig. 19. When faced with other switches or driving situations, it is necessary to add surge absorption circuit and ensure the stable power supply for the drivers to protect the MOSFET.

3) Overcurrent Protection: The control system with field-programmable gate array in practical application has overcurrent feedback protection, as shown in Fig. 20, which operate within 20 ns once the current exceeds the preset safety value to prevent MOSFET from damaged by overcurrent as illustrated in Fig. 21.

C. Pulse Output Performance

For this prototype, the MOSFET selected is NVBG160N120SC1 (ON Semiconductor), which has a voltage tolerance of 1200 V and a full conduction driving voltage of 15 V with a rising edge of 11 ns. The driver is IXDN609 from IXYS Company. The signal generator (DG535) provides the driving signal, which is then converted into an optical signal by an optical fiber signal module and sent to the optical fiber receiving heads (FR50MHIR) of each stage. The fiber signal module is specifically designed in [14].

For pulse output, high voltage probe (LeCroy PPE 6 kV, 400 MHz) is applied, while for low voltage waveforms, a low voltage probe (Tektronix P6139B, 300 V, 500 MHz) is used. These probes transmit the signals to the oscilloscope (HDO6034A).

The output waveform can be well adjusted in pulsed width and amplitudes of the eight-staged Marx SSPG with PSC, as in Fig. 22(a) and (b). The typical minimum pulsewidth can reach 50 ns, as shown in Fig. 22(c). In addition, the output pulse can reach 1 MHz in the burst mode while maintaining 7 kV amplitude as in Fig. 22(d), which verifies the compatibility of PCS in solid-state pulse generators.

VI. Conclusion

In SSPG, parallel structure is applied as the majority of the existing insulated power supply scheme through noncontact magnetic field coupling, which results in the lack of insulation similarity for each stage and low insulation utilization ratio. In this article, a power supply chain based on the series structure is proposed, which breaks the limitations of parallel structure. PSC is purely composed of diodes, capacitors, and inductors, which increases insulation adjustability, thus reducing the manufacturing difficulty and customized cost. Besides, PSC does not require external control signals and does not interfere with gate driving synchronization or freedom. The proposed PSC in this article not only realizes the IPS of nanosecond SSPG in biomedical applications, but also provides a unique perspective for the IPS scheme of SSPG.

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