Grouped Valley Switching Control to Optimize Efficiency and THD for DCM Boost PFC Converters

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***Abstract*—In discontinuous conduction mode boost converters, the switching-node voltage oscillates after the inductor current reaches zero, leading to fluctuating power loss. To investigate this, a circulating energy model is first proposed. Accurate power loss is analyzed with consideration of oscillation damping effect, reverse conduction of power switch, and nonlinear capacitance effect. Analysis shows that the loss can be minimized when the switch is turned ON at specific switching-node voltage valleys. Therefore, to minimize the power loss, a grouped valley switching (GVS) control is proposed to count the valleys and turn ON the switch at the optimal valley. However, dynamic changes in valleys will cause frequency hopping, resulting in degraded total harmonic distortion (THD) in input current. To address this issue, the GVS controller turns ON the switch at constant valleys in a half-line cycle, while adaptively calculating the ON-time with online tracked oscillation duration. For efficiency improvement, the optimal valleys are grouped and tuned based on a comprehensive power loss analysis. Experimental results validate the effectiveness of the proposed control. Compared with conventional variable ON-time controls, the proposed control improves an average efficiency of 0.4% across the entire power range under 110/220 VAC input. The THD is below 3.1% at 250 W rated power.**

***Index Terms*—Boost, discontinuous conduction mode (DCM), efficiency, power factor correction (PFC), total harmonic distortion (THD), valley switching (VS).**

I. Introduction

POWER factor correction (PFC) converters are required for offline devices to meet electromagnetic pollution regulations such as IEC61000-3-2 [1], [2]. Depending on the continuity of the inductor current, they can operate in discontinuous conduction mode (DCM), critical conduction mode (CRM), and continuous conduction mode [3], [4]. Among them, DCM boost PFC converters are widely employed in low-power applications due to the eliminated reverse recovery of diode, high bandwidth, and low-cost implementation [5], [6], [7].

Aiming to improve overall efficiency and reduce heat, numerous studies have been conducted to optimize the power loss in DCM. Bridgeless PFCs can reduce the conduction loss of rectifier bridges [8], [9]. Wide bandgap semiconductor devices feature low conduction resistance and parasitic capacitance, thus facilitating high-frequency and high-efficiency realization [10], [11]. Besides topologies and devices, other researches focus on the development of control strategies. For example, variable ON-time (VoT) and variable frequency controls are effective approaches in optimizing efficiency under dynamic operation conditions [12], [13], [14]. However, these approaches lack accuracy with conventional DCM model, where the switching-node oscillation is not considered.

Specifically, in conventional DCM model, the switching-node voltage is assumed to be equivalent to the input voltage after the inductor current reaches zero [14], [15], [16], [17]. However, owing to parasitics, the practical switching-node voltage can oscillate between zero and the output voltage, leading to energy circulation in the circuit. With ON-time modulation, the circulating energy is randomly dissipated in the channel of power switch, causing fluctuating power loss [18], [19]. This power loss can be reduced by valley switching (VS) technique, which has been proven to be effective in CRM converters. By turning ON the switch at the first valley of the switching-node voltage, the dissipated power loss is greatly reduced [20], [21].

In order to implement VS in DCM, the turn-ON point of the switch should be dynamically changed to the valley points. To realize this, a lot of new control strategies are developed, including programable valley skipping controls [22], [23] and pulse-width-cycle control [24], [25]. However, switching at dynamic changing valleys will cause frequency hopping, leading to considerable current distortion and total harmonic distortion (THD). To avoid repetitive hopping in dynamic operation, a valley-locking strategy with valley latch and hysteresis comparator is proposed [23]. To offset the hopping induced current distortion, the switching ON-time should be compensated to restore the desired current [25]. However, a control strategy with eliminated hopping and consistent VS is still lacking. Furthermore, the optimal VS implementation in DCM should be revealed with analysis of the fluctuating power loss caused by the switching-node oscillation.

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To address the above issues, this article proposes a circulating energy model to investigate the fluctuating power loss during the switching-node oscillation. The energy circulation process is revealed through analysis considering three important parasitic effects: oscillation damping effect, reverse conduction of power switch, and nonlinear capacitance effect. Furthermore, a grouped valley switching (GVS) control is proposed. This control employs a zero current detection (ZCD) method to count the voltage valleys at the switching-node. By initiating the switching cycle at a specific valley, the fluctuating loss is reduced. To improve THD, the specified valley number is fixed as constant during a half-line cycle, thereby eliminating the frequency hopping. Meanwhile, by tracking the oscillation duration online under the specified valley number, the switching ON-time is adaptively tuned for accurate current control. Based on the proposed circulating energy model and GVS control, a comprehensive loss analysis is provided to explore how the valley numbers affect the total loss. To further optimize efficiency, the optimal valley numbers are grouped under different input and load conditions. Finally, the proposed circulating energy model and GVS control are validated by experimental comparisons on efficiency, PF, and THD.

The rest of this article is organized as follows. Section II introduces the circulating energy model. Section III provides the GVS control strategy and gives the optimal $n_{\rm ref}$ groups based on loss analysis. Section IV presents the experimental results of the 250 W prototype, along with a performance analysis of different controls. Finally, Section V concludes this article.

II. Circulating Energy Model to Investigate Loss Fluctuations

For boost PFC converters operating in DCM, parasitic resonance leads to energy circulation in the circuit, which causes loss fluctuations among different switching cycles. However, in current literatures, the modeling and analysis for such loss fluctuations are still lacking, which hinders the improvement of the converter efficiency. To address the issue and provide a theoretical base for GVS control, a circulating energy model is established in the following.

Fig. 1(a) gives the scheme of a boost PFC converter with consideration of parasitics, where the parasitics include: equivalent series resistances (ESR) of the inductor and capacitors (R_L, R_i, R_C), the internal resistances ($R_{\rm ds}$, R_F, $R_{\rm F1}$) and junction capacitances (C_j, $C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$) of the power components, and the forward voltage drops of diode and diode-bridge rectifier (V_F, $V_{\rm F1}$). The energy circulation occurs when both the main power switch and diode are turned OFF, and the energy will circulate between the junction capacitances and the boost inductor.

This circulation process reflected in voltage and current oscillations is given in Fig. 1(b). To model the circulating energy, accurate $v_{\rm ds}(t)$ and $i_L(t)$ should be solved. However, the analytical solutions are lacking, since they are influenced by three important parasitic effects: the oscillation damping effect, reverse conduction of the power switch, and nonlinear capacitance effect. To address the issue, the proposed model

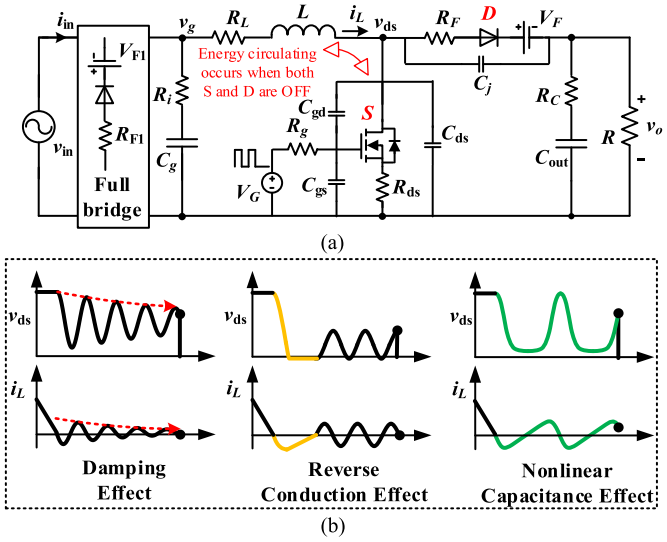

Fig. 1. Boost PFC converter with consideration of parasitics. (a) Circuit scheme. (b) Waveforms considering parasitics.

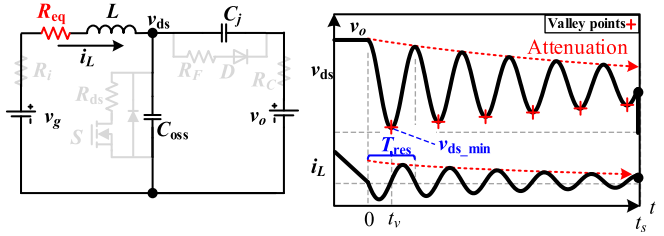

Fig. 2. Equivalent circuit state and dynamics considering damping effect during the oscillation.

adopts equivalent circuits that account for these parasitic effects to calculate of $v_{\rm ds}(t)$ and $i_L(t)$ during the oscillation.

A. Equivalent Circuits and the Analytical Solutions With Consideration of Parasitic Effects

1) Oscillation Damping Effect: First, the oscillation damping effect is considered individually. The equivalent circuit state and dynamics during the oscillation are depicted in Fig. 2.

In the circuit, $R_{\rm eq}$ represents the ESR of the boost inductor at the resonant frequency. It should be noted that when the inductor is designed for low-frequency, $R_{\rm eq}$ becomes much larger than R_L due to the increased resonance frequency. Since R_i and R_C are much smaller than $R_{\rm eq}$, they can be ignored or incorporated into $R_{\rm eq}$. And as the resonant current passes through the junction capacitance $C_{\rm oss}$ ($C_{\rm oss} = C_{\rm gd} + C_{\rm ds}$) and C_j, $R_{\rm ds}$ and R_F have no effect on the resonance. Therefore, the resistance of the circuit is modeled as $R_{\rm eq}$.

Based on the equivalent circuit, differential equations are listed to calculate $v_{\rm ds}(t)$ and $v_{\rm ds}(t)$, which is given by

$$\begin{cases} v_{\rm ds}(t) = v_g - R_{\rm eq} i_L(t) - L\frac{{\rm d}i_L(t)}{{\rm d}t} \\ i_L(t) = C_{\rm oss}\frac{dv_{\rm ds}(t)}{dt} + C_j\frac{d(v_{\rm ds}(t)-v_o)}{dt} \end{cases}. \tag{1}$$

According to the initial conditions at time 0, the total response can be solved. $v_{\rm ds}$ and i_L have time-domain expressions

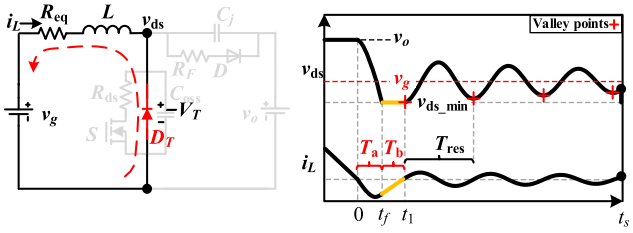

Fig. 3. Equivalent circuit state and dynamics with the occurrence of reverse conduction.

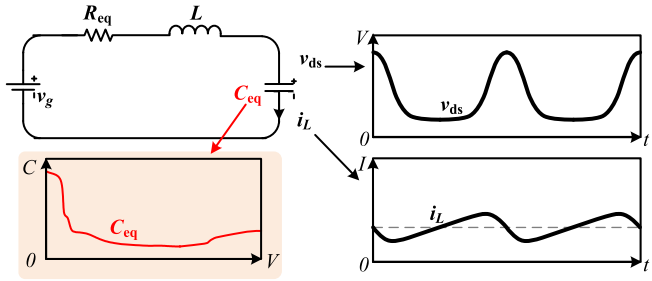

Fig. 4. Resonant process with nonlinear $C_{\rm eq}$ capacitance.

as

$$\begin{cases} v_{\rm ds}(t) = e^{-\alpha t} \cdot K_1 \cos(\omega_d t + \varphi) + v_g \\ i_L(t) = e^{-\alpha t} \cdot \alpha \omega_d K_1 \sin(\omega_d t + \varphi) \end{cases} \tag{2}$$

where the coefficients α, K_1, ω_d, and φ are determined by $R_{\rm eq}$, L, and $C_{\rm eq}(C_{\rm eq} = C_{\rm oss} + C_j)$, as specified in

$$\begin{cases} \alpha = \frac{R_{\rm eq}}{2L}, \omega_0 = \frac{1}{\sqrt{LC_{\rm eq}}}, \omega_d = \sqrt{{\omega_0}^2 - \alpha^2} \\ K_1 = \sqrt{1 + \left(\frac{\alpha}{\omega_d}\right)^2}(v_o - v_g), \varphi = \arctan\frac{\alpha}{\omega_d} \end{cases}. \tag{3}$$

Additionally, the system exhibits a resonant cycle $T_{\rm res}$, which is derived as

$$T_{\rm res} = \frac{2\pi}{\omega_d} = \frac{4\pi\sqrt{LC_{\rm eq}}}{\sqrt{4 - R_{\rm eq}C_{\rm eq} \cdot \frac{R_{\rm eq}}{L}}}. \tag{4}$$

With (2), (3), and (4), dynamics during the oscillation are described. It is observed that v_g determines the center value of $v_{\rm ds}(t)$, $R_{\rm eq}$ and L determine the damping exponent, and $T_{\rm res}$ remains constant under the damping effect.

2) Reverse Conduction Effect: The reverse conduction effect is considered based on the calculations and analysis under the damping effect. The equivalent circuit state and dynamics may change when the reverse conduction occurs, as shown in Fig. 3.

For the circuit, V_T is the reverse conduction voltage drop across the body diode D_T of the MOSFET. Once $v_{\rm ds}$ decreases to $-V_T$ at the t_f instant, the diode conducts and clamps the voltage of $v_{\rm ds}$.

To identify when the reverse conduction should be considered, the minimum value of $v_{\rm ds}$ during the resonance is studied. Since α and ω_d are positive, φ lies within the range of 0-0.5π. Based on (2) and the reverse conduction voltage drop, $v_{\rm ds\_min}$ is given by

$$v_{\rm ds\_min} = \max(v_{\rm ds}(t_v), -V_T), \quad t_v = \frac{\pi - \varphi}{\omega_d}. \tag{5}$$

Furthermore, by setting $v_{\rm ds}(t_v) < -V_T$, the range of $v_{\rm g}$ where the reverse conduction occurs is derived as $[0, -V_T - K_1 \cdot \exp(-\alpha t_v) \cdot \cos(\omega_d t_v + \varphi)]$. With this criterion, the scenario of diode D_T reverse conduction (D_T-ON) and the scenario where the diode D_T remains OFF (D_T-OFF) are distinguished.

In the D_T-ON scenario, the damping resonance first occurs during duration T_a. $i_L(t)$ and $v_{\rm ds}(t)$ during this duration are described by (2). T_a ends when $v_{\rm ds}$ reaches $-V_T$.

To derive T_a, we first estimate T_a as $T_{\rm a\_est}$. Considering that the attenuation within half of the resonant cycle is small, $T_{\rm a\_est}$ is calculated by substituting $v_{\rm ds}(T_{\rm a\_est}) = -V_T$ into (2) and omitting the exponential term $e^{-\alpha T_{\rm a\_est}}$. Then, a more accurate T_a is derived by substituting $v_{\rm ds}(T_{\rm a}) = -V_T$ into (2) and adopting $e^{-\alpha T_a} \approx e^{-\alpha T_{\rm a\_est}}$, given by

$$\begin{cases} T_{\rm a\_est} = \frac{1}{\omega_d}\left(\arccos\left(-\frac{v_g + V_T}{K_1}\right) - \varphi\right) \\ T_a = \frac{1}{\omega_d}\left(\arccos\left(-\frac{v_g + V_T}{e^{-\alpha T_{\rm a\_est}} K_1}\right) - \varphi\right) \end{cases}. \tag{6}$$

During T_b, i_L rises linearly to zero with a slope equal to v_g/L. Therefore, the current is given by

$$i_L(t) = i_L(T_a) + \frac{v_g}{L}(t - T_a). \tag{7}$$

Furthermore, substituting $i_L(t_1) = 0$ into (7) derives the duration

$$T_b = t_1 - t_f = -\frac{L}{v_g} \cdot i_L(T_a). \tag{8}$$

After T_b, the circuit returns to the resonant state. Equation (1) remains valid to describe the subsequent $i_L(t)$ and $v_{\rm ds}(t)$. With conditions at t_1, $v_{\rm ds}(t)$, and $i_L(t)$ after T_b are solved as

$$\begin{cases} v_{ds}(t) = e^{-\alpha(t-t_1)} \cdot K_2 \cos\left(\omega_d (t - t_1) + \varphi\right) + v_g \\ i_L(t) = e^{-\alpha(t-t_1)} \cdot \alpha\omega_d K_2 \sin\left(\omega_d (t - t_1) + \varphi\right) \end{cases} \tag{9}$$

where the new coefficients are derived as

$$\begin{cases} t_1 = T_a + T_b \\ K_2 = -v_g\sqrt{1 + \left(\frac{\alpha}{\omega_d}\right)^2} \end{cases}. \tag{10}$$

Finally, $i_L(t)$ and $v_{\rm ds}(t)$ are predicted during the entire oscillation duration based on the above analysis.

3) Nonlinear Capacitance Effect: The above equations are accurate when $C_{\rm eq}$ has a constant value. However, the value of $C_{\rm eq}$ varies dramatically with the applied voltage, which leads to irregular resonant waveforms in actual applications, as shown in Fig. 4. To overcome this problem, an iterative solving method is proposed.

Fig. 5(a) illustrates the flowchart of the proposed method. First, the initial conditions, $v_{\rm ds}(0) = v_o$ $i_L(0) = 0$, and $n_c = 0$ are provided. The parameter t_i is set to 0 and a small step size ΔV is selected. Within the selected voltage range ΔV, $C_{\rm eq}$ is considered to have a constant value equal to $C_{\rm eq}(v_{\rm ds}(t_i))$. Second, $v_{\rm ds}(t)$ and $i_L(t)$ are solved according to (1). Once $v_{\rm ds}(t)$

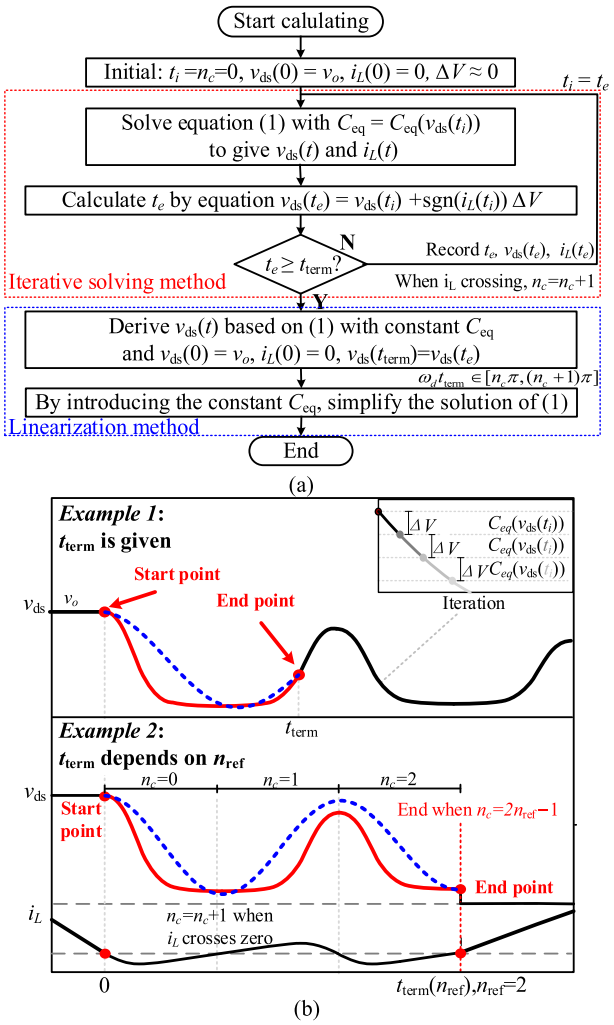

Fig. 5. Iterative solving method and the linearization method. (a) Flowchart. (b) Examples.

is solved, the step end-time t_e, which satisfies $v_{ds}(t_e) = v_{ds}(t_i) + \mathrm{sgn}(i_L(t_i))\Delta V$, becomes numerically computable. Furthermore, $v_{ds}(t_e)$ and $i_L(t_e)$ are recorded. When i_L crosses zero, the number of zero-crossing times n_c increases by one. Third, the conditions of the circuit at t_i are updated to the conditions at t_e. The same calculation process for $v_{ds}(t)$ and $i_L(t)$ during the next step size ΔV begins. Finally, after several iterations, realistic resonant waveforms are obtained according to the recorded time, voltage, and current, as indicated by the red lines in Fig. 5(b).

Since the iterative computations are tedious, a linearization equivalent method is given to simplify the computation. The linearization method fits the start/end point of the actual resonant process [see red lines in Fig. 5(b)] with the resonance under fixed capacitance [see blue lines in Fig. 5(b)], simplifying the iterative calculation. The desired C_{eq} satisfies the relation

$$v_{ds}(t_{term}) = e^{-\alpha t_{term}} \cdot K_1(C_{eq}) \cos\left(\omega_d(C_{eq}) t_{term} + \varphi(C_{eq})\right) + v_g n_c \pi \leq \omega_d(C_{eq}) t_{term} < (n_c+1)\pi. \quad (11)$$

Under the D_T-OFF scenario, the linearized C_{eq} is obtained by numerically solving (11). Under D_T-ON scenario, C_{eq} should be linearized before t_f and after t_1 separately. After t_1, C_{eq} can be derived from the relation based on (9), given by

$$v_{ds}(t_{term}) = e^{-\alpha(t_{term}-t_1)} \cdot K_2(C_{eq}) \cos\left(\omega_d(C_{eq}) \cdot (t_{term} - t_1) + \varphi(C_{eq})\right) + v_g$$
$$n_c\pi \leq \omega_d(C_{eq}) \cdot (t_{term} - t_1) < (n_c+1)\pi. \quad (12)$$

A basic example and a valley switching example are presented in Fig. 5(b). t_{term} is determined by $n_c = 2n_{ref} - 1$ when the valley switching is occurred at "n_{ref}"-th valley of v_{ds}.

To summarize, the iteration is employed for accurately modeling the resonance, while the linearization method is proposed to equivalently characterize the resonance through simplified calculations, thereby facilitating further analysis.

B. Circulating Energy Model to Reveal the Loss Fluctuation

The fluctuating power loss is the focus of the circulating energy model. In the model, the resonance loss, the parasitic capacitance loss, and the core loss are considered.

The resonance loss causes the attenuation of the oscillation. To calculate it, the principle of energy conservation is considered. Therefore, the loss during the resonance is equivalent to the energy reduction corresponding to the initial oscillation amplitude and the final oscillation amplitude, which is derived as

$$E_{res} = \frac{1}{2}C_{eq}{K_1}^2 - \frac{1}{2}C_{eq}(e^{-\alpha t_s}K_1)^2 \text{ s.t. } D_T - \text{OFF} \quad (13)$$

$$E_{res} = \frac{1}{2}C_{eq}{K_1}^2\left(1 - e^{-2\alpha T_a}\right) + \frac{i_L^2(T_a)R_{eq}T_b}{3} + \frac{1}{2}C_{eq}{K_2}^2\left(1 - e^{-2\alpha(t_s - T_a - T_b)}\right) \text{ s.t. } D_T - \text{ON}. \quad (14)$$

Equation (13) is applicable to the D_T-OFF scenario, while (14) is applicable to the D_T-ON scenario when $t_s > T_a + T_b$. t_s is the end time of the oscillation. Equations for D_T-ON scenario with smaller t_s are easy to derive, which is omitted here. Coefficients α, K_1, K_2, T_a, and T_b are already given.

The parasitic capacitance loss primarily causes the loss fluctuation. At the end of the resonance, a portion of the charge may remain in C_{oss}. This remaining charge varies dramatically according to $v_{ds}(t_s)$ and discharges into the switch channel as the switching occurs, causing significant loss fluctuation.

Based on the previously derived $v_{ds}(t)$, the parasitic capacitance loss is calculated by

$$E_{oss} = \frac{1}{2}C_{oss}v_{ds}^2(t_s). \quad (15)$$

The core loss during the oscillation is relatively small due to the minor resonant current. Since the similarity between the oscillation waveform and sinusoidal waveform, the core loss can be estimated based on Steinmetz equation (SE), given by

$$E_{core} = k \cdot {f_{res}}^{\alpha_1} \cdot B_m^{\beta} \cdot V_e \cdot t_s \quad (16)$$

where k, α_1, β are provided by the core manufacturer, the resonant frequency $f_{res} = 1/T_{res}$, V_e is the effective core volume of the inductor, and B_m represents the magnetic flux density corresponding to the peak resonant current. During one resonance cycle, by assuming the peak resonant current equals to

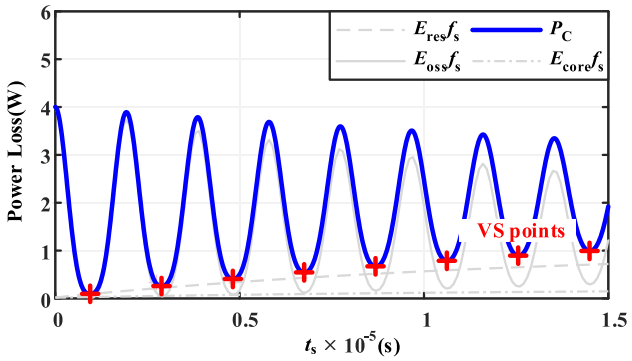

Fig. 6. Power loss fluctuates with the increase of t_s (under the conditions of $v_g = 220$ V, $v_o = 400$ V, $R_{eq,res} = 10\ \Omega$, $C_{oss} = 374$ pF, $C_j = 100$ pF, $f_s = 135$ kHz, $L = 201\ \mu$H, core: POCO NPA158026, $N = 60$).

the positive peak current and neglecting the attenuation, B_m is calculated by

$$B_m(t) \approx \frac{Li_L\left(\left(\left\lfloor\frac{t}{T_{res}}\right\rfloor + \frac{3}{4}\right)T_{res}\right)}{NA_c} \tag{17}$$

where N is the turns of the inductor coil and A_c is the effective core cross-sectional area. Equation (16) can be segmented and calculated based on (17).

Assuming the switching frequency is f_s, the total power loss caused by the resonance across the switching cycle is calculated by

$$P_C = (E_{res} + E_{oss} + E_{core})\, f_s. \tag{18}$$

Based on (18), the loss fluctuation can be predicted under given conditions, as illustrated in Fig. 6. It is observed that P_C periodically reaches valleys with the increase in the oscillation period, and $E_{oss}f_s$ dominates P_C.

Therefore, significant loss reduction can be achieved by controlling the oscillation ends at the valleys. With the proposed model, P_C becomes predictable at different valley points.

III. Grouped Valley Switching Control

A. Control Scheme

Fig. 7(a) gives the control scheme of the proposed GVS control. First, the GVS controller identifies the valleys in each switching cycle by counting the rising edge of the ZCD signal. Then, the counted number (n_v) is compared with a reference number (n_{ref}) to generate the cycle reset signal (rst). With the reset signal, the ramp counter outputs the ramp signal periodically. Finally, this ramp is compared with a calculated ON-time (T_{ON}) to carry out PWM.

The controller incorporates a general PFC sampling and feedback structure. The control variable I_{ref} and the amplitude of the line voltage V_m are updated at the beginning of each half-line cycle. n_{ref} is updated according to V_m, I_{ref}, and v_o. The controller tracks the oscillation duration (T_{osc}) using a timer counter, which is enabled by the falling edge of the ZCD signal and reset by the rst signal. T_{osc} plays a significant role in the calculation of

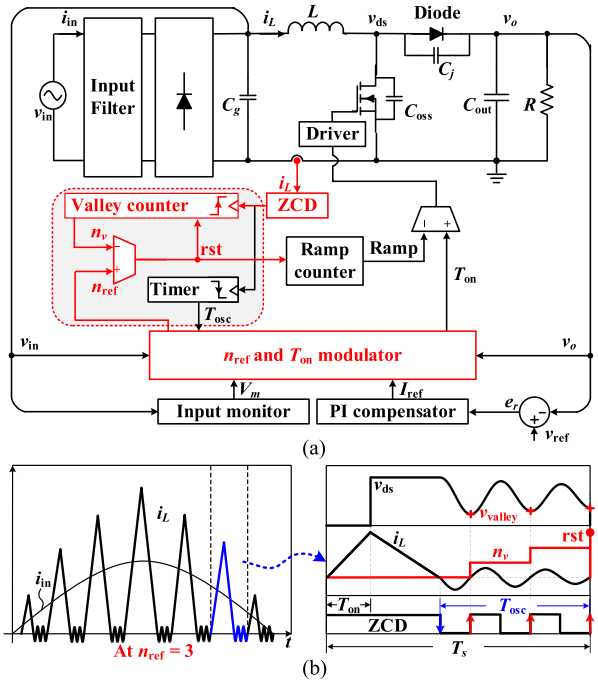

Fig. 7. GVS control and typical waveforms of the converter. (a) Scheme of GVS control. (b) Waveforms with valley switching when $n_{ref} = 3$.

T_{ON}. Fig. 7(b) illustrates the typical waveforms under the GVS control.

The key to GVS controller is the modulation of T_{ON} and n_{ref}. The controller calculates T_{ON} at each switching cycle to achieve low THD, while adjusting n_{ref} at each half-line cycle to optimize the efficiency. The principle of GVS control is given in the following.

First, to achieve low THD, the controller should regulate the input current as a sinusoid, which is expressed as

$$|i_{in}| = I_{ref}\sin(\theta) = I_{ref}\frac{v_g}{V_m} \tag{19}$$

where I_{ref} is the reference amplitude of the input current (i_{in}) and θ is the ac angle of the half-line cycle.

With the input filter, the absolute value of the input current is derived from the average inductor current during the switching cycle, which is given as

$$|i_{in}| = \bar{i}_L = \frac{{T_{on}}^2 v_g v_o}{2\,(v_o - v_g)\,LT_s} \tag{20}$$

where T_s is expressed as

$$T_s = \frac{v_o}{v_o - v_g}T_{on} + T_{osc}. \tag{21}$$

The variables in (20) and (21) belong to the same switching cycle. According to the circulating energy model, T_{osc} is too complex to be predicted online. Therefore, T_{ON} cannot be directly derived due to T_s is unknown.

To determine T_{ON}, T_s is predefined in conventional fixed frequency controls. However, actual T_s should dynamically vary to achieve VS. This leads to frequency hopping and reduces the accuracy of the input current control. The same issue arises

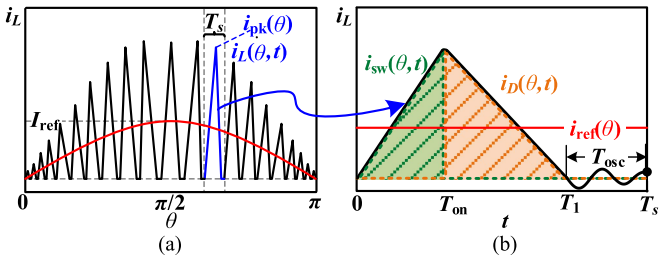

Fig. 8. Current waveforms of DCM boost PFC. (a) Within a half-line cycle scale. (b) Within a switching cycle scale, $T_1 = F_1 T_{ON}$.

when T_{ON} is predefined and T_s is calculated with varying T_{osc}. Moreover, obtaining T_s through online detection will always introduce a one-cycle delay, which is not accurate when T_s changes dynamically.

Under the GVS control, T_{osc} is controlled by a constant n_{ref} to achieve VS. Therefore, T_{osc} of the adjacent cycles are ensured to be approximately equal, and VS is naturally ensured without dynamical variation. Based on this, T_{osc} is tracked online to calculate T_s of the new cycle. Furthermore, T_{ON} of the new cycle is adaptively calculated.

Substituting (21) and (19) into (20) and eliminating the negative solution, T_{ON} is solved and given by

$$T_{on}=\frac{F_1+\sqrt{{F_1}^2+2F_1F_2T_{osc}}}{F_1F_2},\ F_1=\frac{v_o}{v_o-v_g},F_2=\frac{V_m}{LI_{ref}}. \tag{22}$$

In (22), I_{ref} is outputted by the PI compensator, and V_m is outputted by the input monitor. Both I_{ref} and V_m are updated every half-line cycle. F_1 and F_2 are determined by the circuit parameter and the sampled voltage. T_{osc} is provided by a time counter. Therefore, T_{ON} is calculated to make the converter achieve low THD. As the variables in (21) become approximately continuous, the frequency hopping problem is avoided.

Second, since T_{ON} and T_{osc} are regulated by n_{ref}, n_{ref} significantly impacts the current waveform and efficiency of the converter. To achieve high efficiency, optimal n_{ref} values are grouped by the GVS controller for different input (V_m), output (v_o), and power rating ($I_{ref}\cdot V_m$) conditions, relying on efficiency estimations. Thus, a comprehensive loss analysis is conducted in the following.

B. Comprehensive Loss Analysis Utilizing the Circulating Model to Give the Optimal N_{ref} Groups

As illustrated in Fig. 8, the current waveforms of the PFC converter encompass two scales: 1) the half-line cycle scale and 2) the switching cycle scale. Conventional loss analyses are typically conducted within the half-line cycle scale, which lacks accuracy and does not reflect the loss variations with n_{ref} regulation. Thus, the comprehensive loss analysis is conducted within two time-scales to address the issue.

The power loss is estimated by two steps. First, assuming the low-frequency ac angle θ is constant throughout a switching cycle, losses are calculated and averaged over a switching cycle.

TABLE I
LOSS CALCULATIONS WITHIN A SWITCHING CYCLE SCALE

Loss Type	Formulas[a,b]	
	Main Formula	*Supplementary Formula*
Conduction[a]	$P_{X,ESR}=I_{X,rms}^2R_X$ $P_{X,Diode}=V_{X,Voltage\_drop}I_{X,avg}$	$I_{X,rms}=\sqrt{\frac{1}{T_s}\int_0^{T_s}i_X^2(\theta,t)dt}$ $I_{X,avg}=\frac{1}{T_s}\int_0^{T_s}i_X(\theta,t)dt$
Magnetic[b]	$P_{mag}=\frac{1}{T_s}\int_0^{T_s}k_i\left\|\frac{dB(t)}{dt}\right\|^{\alpha_i}\|\Delta B\|^{\beta-\alpha_i}dt$	$k_i=\frac{k}{(2\pi)^{\alpha_i-1}\int_0^{2\pi}\|\cos\theta\|^{\alpha_i}2^{\beta-\alpha_i}d\theta}$ $\left\|\frac{dB}{dt}\right\|=\begin{cases}\frac{\Delta B}{T_{on}} & 0<t\le T_{on}\\ \frac{\Delta B}{T_1-T_{on}} & T_{on}<t\le T_1\\ 0 & T_1<t\le T_s\end{cases}$ $\Delta B=\frac{Li_{pk}}{NA_c}$
Resonance	$P_C=(E_{res}+E_{oss}+E_{core})f_s$	(1)–(17)
Switching[c]	$P_{drive}=Q_GV_Gf_s$ $P_{off}=P_i+\frac{P_{i+1}-P_i}{i_{ds,i+1}-i_{ds,i}}(i_{pk}-i_{ds,i})\ \ i_{pk}\in[i_{ds,i},i_{ds,i+1}]$	

[a] X represents an unspecified component in the circuit.
[b] Effective core volume V_e, effective cross-sectional area A_e, coefficients k, α_1, β are provided by the core manufacturer.
[c] Q_G is gate electrode charge of the MOSFET. P_i ($P_i = E_i f_s$) is the turn-off loss measured at current level $i_{ds,i}$ based on double pulse test.

Second, switching cycle losses corresponding to θ are integrated and averaged over the half-line cycle.

1) Loss Estimation Method: Table I illustrates the loss calculations within a switching cycle scale. To maintain conciseness and clarity, we condensed well-known details. Interested readers can refer to more foundational details in our previous work in [14].

The conduction loss occurs on components where the current flows continuously. For the inductor, the power switch, and the output capacitor, the conduction loss take the form $P_{X,ESR}(\theta)$. For the power diode and the bridge, the conduction loss takes the form $P_{X,ESR}(\theta)+P_{X,Diode}(\theta)$ due to their additional diode voltage-drop. It should be noticed that the currents of the inductor, the switch, and the diode are treated as zero during $[T_1, T_s]$, because this part of the conduction loss is calculated by E_{res} separately.

The magnetic loss includes hysteresis loss, eddy current loss, and residual loss. For PFC converter with a suitable magnetic core, the eddy current loss is typically negligible. The residual loss is generally an order of magnitude smaller than other losses. Consequently, the calculation of magnetic loss is reduced to the calculation of hysteresis loss.

To calculate hysteresis loss under the DCM triangular waveform excitation, Improved Generalized Steinmetz Equations (IGSE) are introduced. IGSE approach takes into account hysteresis loops caused by the specific waveform excitation, offering good accuracy [26]. IGSE uses the same parameters as that used in (16) with SE approach. The excitation during $[T_1, T_s]$

TABLE II
TURN-OFF LOSS BASED ON DOUBLE PULSE TEST

Number i	0	1	2	3	4	5	6
$i_{ds,i}$ (A)	0	0.5	1	2	3	4	5
Loss E_i (μJ)	0	0.977	1.349	2.739	6.653	10.85	14.93

TABLE III
SPECIFICATIONS OF THE PROTOTYPE (@ 25 °C)

Input voltage v_{in}	110 VAC–220 VAC/50 Hz
Output voltage v_o	400 VDC
Maximum power rate P_{max}	250 W
Output capacitor	C_{out}=330 μF, R_C=10 mΩ
Boost inductor	L=201 μH, R_L=100 mΩ
Transistor (IPA65R190C7)	V_{th}=4 V, R_{ds}=190 mΩ C_{oss}=374 pF, Q_G=23 nC, g_{fs}=6 (@ V_G=12 V, v_{ds}=400 V)
Diode (STPSC6H065)	V_F=0.65 V, R_F=125 mΩ C_j=100 pF
Rectifier bridge	V_{FI}=0.55 V, R_{FI}=200 mΩ
Drive condition	V_G=12 V, R_{ON}=5 Ω, R_{OFF}=2 Ω

is also treated as zero since this part of the magnetic loss is calculated by E_{core} separately.

The switching loss contains the drive loss, the turn-ON loss, and the turn-OFF loss. As the driver charges and discharges the gate with rated drive voltage V_G once a switching cycle, the drive loss is derived as $P_{drive}(\theta)$. For turn-ON loss, since the drain-source current (i_{ds}) of the power switch is nearly zero before and after the turn-ON process, the turn-ON loss is close to zero as well. For the converter discussed in this article, the authors simulate the ON loss based on LT-spice model and derive that the turn-ON loss is less than 0.5 mW. Therefore, the turn-ON loss is disregarded in the analysis.

For the turn-OFF loss, accurate data can be provided by double pulse test based on the designed converter. Table II gives an example of the measured data. The turn-OFF loss measured at current level $i_{ds,i}$ is calculated by $P_i = E_i \cdot f_s$.

Finally, the loss analysis is finished within a switching cycle scale. The analysis is easy to be applied when $T_{ON}(\theta)$ and $f_s(\theta)$ are given. For GVS control, $T_{ON}(\theta)$ and $f_s(\theta)$ are calculated based on (21) and (22).

By integrating and averaging all the above losses over the half-line cycle (With frequency f_{hl}), the total loss is calculated by

$$P_{loss} = f_{hl} \int_0^{\pi} \left(\sum P_{cond}(\theta) + P_{mag}(\theta) + P_C(\theta) + P_{drive}(\theta) + P_{off}(\theta) \right) d\theta. \quad (23)$$

2) Simulation Analysis to Give the Optimal N_{ref} Groups.: Based on (23) and specifications in Table III, the total loss is simulated to carry out the optimal n_{ref} groups.

As shown in Fig. 9(a), power loss is simulated with different n_{ref} values under various conditions of input voltage, output voltage, and output power. An optimal n_{ref} value corresponding to the minimal power loss is identified for each condition. Conventional VoT controls in [25], with VS and different rated

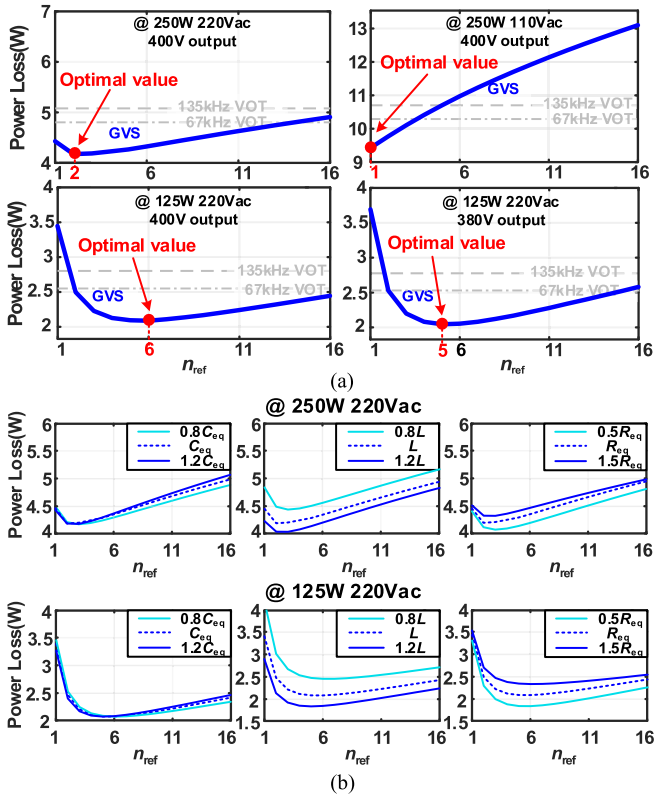

Fig. 9. Power loss for different n_{ref}. (a) Under different input voltage, output voltage, and output power conditions. (b) Regarding the changes in parasitic parameters and inductance deviation.

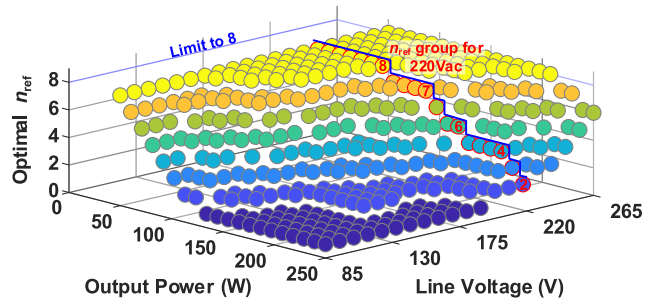

Fig. 10. Optimal n_{ref} groups at 400 V output.

frequencies, are also compared for reference. These loss curves demonstrate the potential of GVS control to optimize efficiency under each operating condition by adjusting n_{ref} to its optimal value.

As shown in Fig. 9(b), power loss variations regarding the changes in parasitic parameters and inductance deviation are provided. It is observed that the changes in parasitic parameters impact the magnitude of the loss curves but have a minor effect on their shapes. Therefore, the proposed control strategy accommodates the changes in parasitic parameters and inductance deviation.

Furthermore, the optimal n_{ref} values are grouped based on power loss simulations. Fig. 10 illustrates the optimal n_{ref} values at 400 V output. The output voltage variation is omitted here due to depicting the n_{ref} groups alongside three variables would be

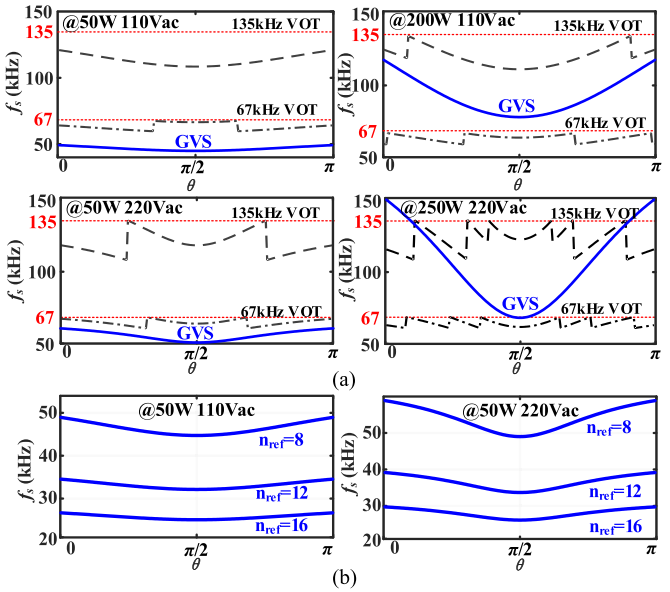

Fig. 11. Switching frequency distributions. (a) Under different controls. (b) With different n_{ref}.

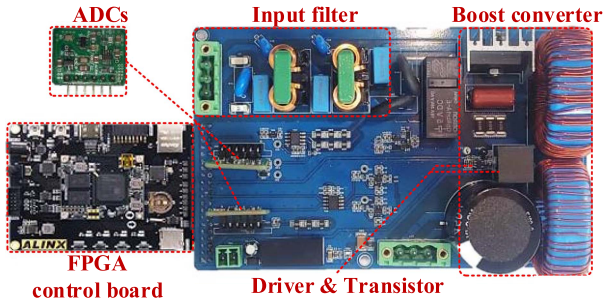

Fig. 12. Photograph of the experimental prototype.

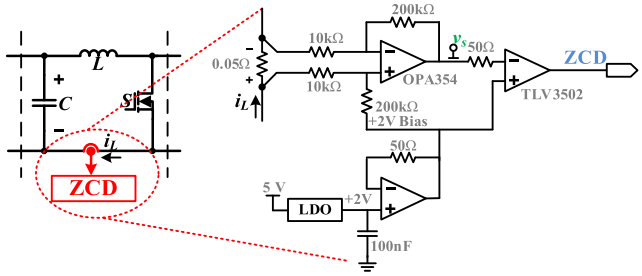

Fig. 13. ZCD subcircuit of the prototype.

overly complex and the changes in output voltage are relatively secondary. In summary, a table will be established according the simulated optimal n_{ref} map, and it will serve as a reference for the controller to determine the n_{ref}.

For the proposed controller, input information and output information are obtained by sampling. The output power is obtained through $V_{\mathrm{m}} \cdot I_{\mathrm{ref}}/2$. The information is updated at each half-line cycle. n_{ref} is changed after looking up the table accordingly.

The simulated switching frequency distributions across the half-line cycle are given in Fig. 11. In the simulation, VS under VoT control is achieved by delaying the cycle to the adjacent valley point, leading to the reduction of the switching frequency and frequency hopping. In contrast, the GVS control addresses the frequency hopping, at the cost of broader operating frequency range.

Consequently, it is preferable to have a limited permissible range for n_{ref}. For the converter in this article, n_{ref} is limited to 8 for two reasons. On the one hand, the optimal value of n_{ref} is larger than 8 only in a few low power ranges. And due to the upward-opening parabolic shape of the loss curve, the efficiency improvement becomes tiny as n_{ref} increases beyond 8. On the other hand, when n_{ref} is limited to 8, the lowest operating frequency is similar to that of a conventional 67 kHz PFC. Increasing n_{ref} beyond 8 yields overly broad operating frequency range for the converter, as shown in Fig. 11(b), making the design of the input filter difficult.

IV. Experiments

An experimental prototype is built to verify the loss analysis and the GVS control strategy, as shown in Fig. 12. After the electromagnetic interference filter, the line voltage is rectified by a 600 V/ 4 A full bridge rectifier GBU806 from Microdiode Semiconductor. A 1.5 μF capacitor and a 500 μH inductor behind the rectifier bridge are used to filter the switching harmonic. The magnetic core of the boost inductor is NPA158026 from POCO. The power switch is IPA65R190C7 from Infineon, and the power diode is STPSC6H065B from ST Microelectronics. A 330-μF capacitor (KN331M45030-35A) is adopted as the output capacitor. The equivalent resistance of the relay and filter circuits is converted into R_L.

The detailed subcircuit of the ZCD module is given in Fig. 13. Small low temperature drift, high-precision alloy resistors are adopted to sample the current to minimize the delay and enhance accuracy. Their resistances are incorporated into R_L. Considering the sampled voltage can be challenging to discern when the resonant current is small, a prestage differential amplifier is designed. A large gain-bandwidth product amplifier and a large amplification factor are selected, which is beneficial for reducing the offset time caused by the hysteresis of the comparator. Additionally, to avoid introducing a negative voltage rail, a +2 V bias is provided. To ensure the stability and accuracy of the bias voltage, both a low dropout regulator and a follower are designed.

All control algorithms are implemented through an FPGA board (Xilinx Spantan-7). Two ADC (LTC2314-14) modules are used to convert the analog values to digital signals. The PI gains are set as $k_P = 0.03$ and $k_I = 0.015$. Detailed parameter values of the components are given in Table III. Experiments are carried out on the prototype. The experimental results are measured by oscilloscope MDO3054 and power analyzer PA5000H.

The experimental waveforms at 110/220 VAC with different loads are shown in Fig. 14. As demonstrated by the zoom-in plots, the GVS control accurately detects the voltage valleys and adjusts n_{ref} according to its optimal value groups, thereby minimizing the power loss and improving efficiency. Since the

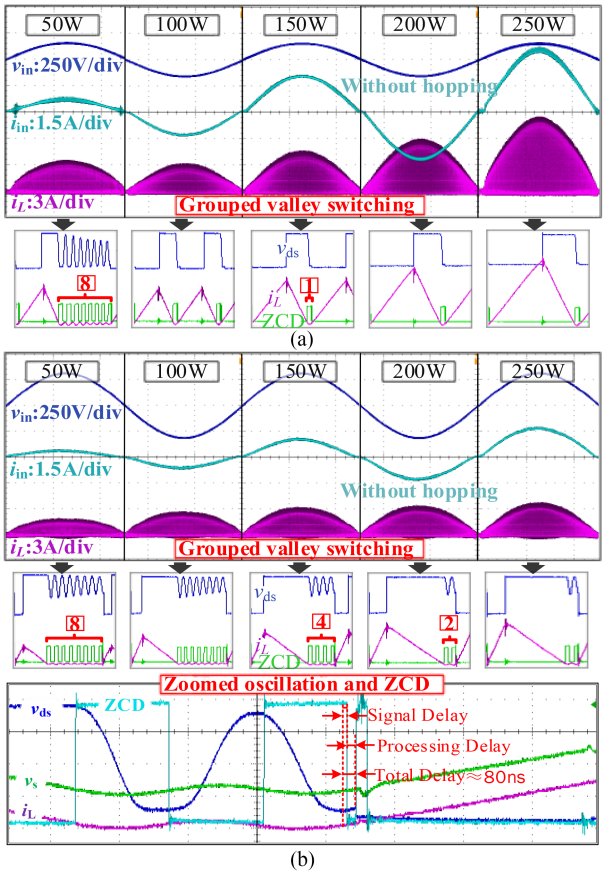

Fig. 14. Typical waveforms under the GVS control. (a) At 110 VAC. (b) At 220 VAC.

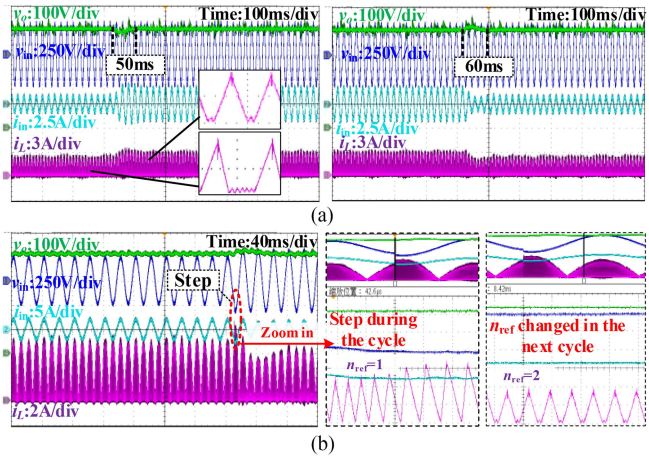

Fig. 15. Transient waveforms under GVS control. (a) Load steps: from 125 W to 250 W and from 250 W to 125 W. (b) Input step from 170 VAC to 220 VAC.

voltage slope and current slope at the valley points are minor and the delay is short, the impact of the delay on the valley switching and the associated loss analysis is negligible.

The transient waveforms under GVS control are presented in Fig. 15. The proposed strategy exhibits good performance during both load and input transients. In fact, when there is a sudden change in the load or input, n_{ref} starts to be changed at the beginning of the subsequent half-line cycle. It may temporarily

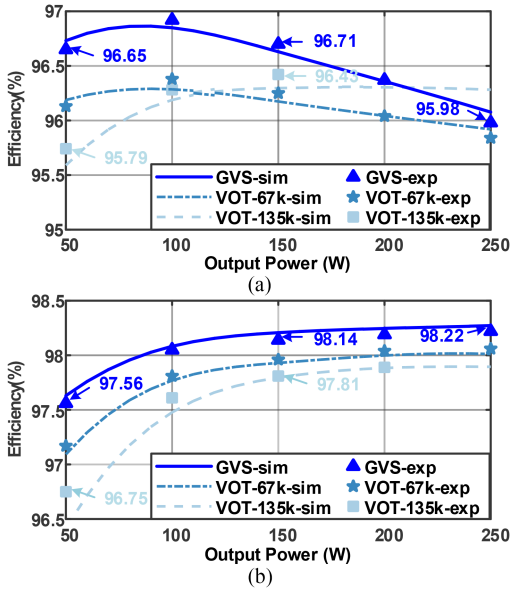

Fig. 16. Efficiency comparisons. (a) At 110 VAC. (b) At 220 VAC.

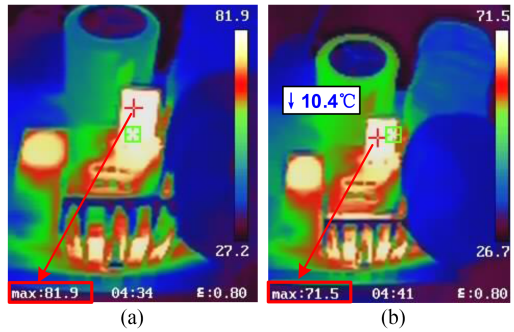

Fig. 17. Measured temperature at 220 VAC input and the rated power. (a) Under the 135 kHz-VoT control. (b) Under the GVS control.

deviate from its optimal value for a few half-line cycles due to loop adjustments. However, this discrepancy does not impact the current control or the feedback adjustment of I_{ref}, ensuring that the controller stabilizes and returns to a steady state after several half-line cycles.

Fig. 16 shows the comparison between the simulated loss data and the measured loss data, which has been normalized to efficiency. Figs. 18 and 19 show the comparisons of different control strategies in aspects of PF and THD. And their power range is also compared in the above figures. A comprehensive comparison with other controls is given in Table IV.

In terms of power loss, the proposed GVS control achieves superior performance at each power rate. When the load is light, the GVS control employs a large n_{ref} to achieve low switching frequency. As the load becomes heavier, GVS control gradually decreases n_{ref} to increase the switching frequency, thereby reducing the peak inductor current.

TABLE IV
COMPARISON WITH OTHER CONTROLS (@ 220 VAC INPUT)

	This paper	[14]	[21]	[22]	[24]	[25]
Output voltage (VDC)	400	390	400	380	400	400
Rated Power (W)	250	310	160	150	55	320
Efficiency (%) @20%load	97.6	95.9	94.3	N/A	90@40%load	96.0
@100%load	98.2	96.4	98.2	N/A	93	97.5
PF (%) @20%load	98.5	N/A	88.8	N/A	98.4@40%load	94.8
@100%load	99.8	99.0	99.2	N/A	99.1	99.6
THD (%) @20%load	6.1	N/A	13.5	4.9	13.5@40%load	4.5
@100%load	3.1	5.4	2.9	2.7	8	4.7
Operation mode	DCM/CRM	DCM	CRM	DCM	DCM	DCM/CRM
Features	Grouped valley switching No frequency hopping	No valley switching	Adaptive valley switching	Valley skipping	Valley switching	Compensated valley switching
FOM[a,b]	1218	127	54	221	87	239

[a] $\text{FOM} = \frac{1}{(1-\text{Average(Efficiency)})} \cdot \frac{1}{(1-\text{Average(PF)})} \cdot \frac{1}{\text{Average(THD)}}$.

[b] Data @40%load is treated as if it were at @20%load. Data marked as N/A is processed by taking the average value in the same row.

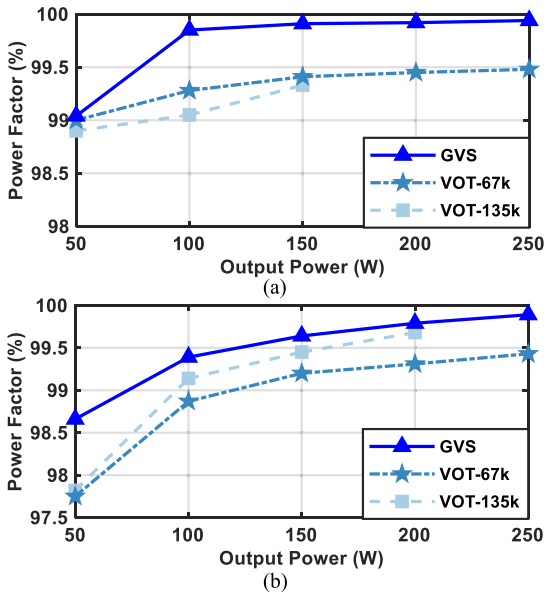

Fig. 18. Comparisons of power factor under different controls and output powers. (a) At 110 VAC. (b) At 220 VAC.

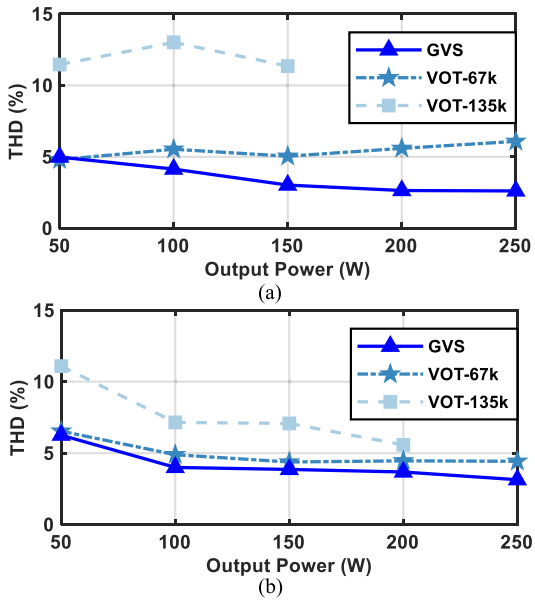

Fig. 19. Comparisons of total harmonic distortion under different controls and output powers. (a) At 110 VAC. (b) At 220 VAC.

Compared with VoT control with different frequencies, the GVS control maintains a lower total loss when operating conditions change. Additionally, a smooth transition to CRM can be achieved when $n_{\text{ref}} = 1$.

The curves in Fig. 16 demonstrate the loss reduction, which is particularly evident at low power rates. Despite an overall improvement of the efficiency is less than 1% under the experimental conditions, this improvement is noticeable as the efficiency is already above 96%. Moreover, the avoided losses are important for heat dissipation and component life-extending. As shown in Fig. 17, a 10.4 °C temperature reduction is achieved on the power switch. This benefit can be more pronounced at high frequency due to full-range VS has been reached. Additionally, because of the exponential terms in magnetic and conduction losses formulas, the proposed strategy may exhibit greater potential in scenarios with higher designed current.

In the aspect of PF and THD, the GVS control has the highest PF and lowest THD in the entire load range. As the control derives accurate cycle time by tracking the resonance duration within each cycle online, the precise ON-time calculation is ensured to achieve the sinusoidal input current, resulting in improved PF and THD.

Figs. 18 and 19 indicate that under the GVS control, the PF changes from 99.1% to 99.9% at 110 VAC input, while the average THD is 3.47% across the entire power range. At 220 VAC input, the PF reaches 99.8% at rated power and remains above 98.5% across most of the power range, with an average THD of 4.28% over the tested range.

In the aspect of power range, Fig. 19 shows that both 135 kHz and 67 kHz VoT controls fail to reach the full operating range. In contrast, the proposed control achieves full range operation. Since the switching is always triggered after the oscillation duration, the frequency is automatically adjusted to avoid PWM saturation problems under the proposed control. Thus, the operation range is extended.

V. Conclusion

This article proposes a novel GVS control strategy and a circulating energy model for DCM boost PFC converter, which aims to optimize efficiency and reduces input current distortion. The proposed strategy achieves consistent VS through a valley-controlled cycle reset mechanism. Furthermore, constant valley number is employed in a half-line cycle and an accurate ON-time calculation method is derived accordingly. They eliminate the frequency hopping and reduce input current distortion, albeit with a broader operating frequency. This trade-OFF proves advantageous when n_{ref} is reasonably limited. The proposed circulating energy model takes parasitic effects into account, quantifying the fluctuating power loss. It allows comprehensive loss analysis of the GVS control to pregroup the optimal valley numbers for different operation conditions, thereby optimizing efficiency. Besides, the proposed strategy also enables a smooth transition between DCM and CRM and eliminates PWM saturation, which leads to a wide operation range. Experimental comparison verifies the effectiveness of the proposed strategy and model. Superior performance is achieved in terms of efficiency, PF, THD, and power range compared with conventional VoT control.

References

[1] X. Y. Ren, Y. T. Zhou, Z. H. Guo, Y. Wu, Z. L. Zhang, and Q. H. Chen, "Simple analog-based accurate variable on-time control for critical conduction mode boost power factor correction converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4025–4036, Dec. 2020.

[2] B. Li, D. Ding, Q. Wang, G. Zhang, G. Wang, and D. Xu, "Virtual admittance reshaping based input current phase shift suppression method for totem-pole bridgeless PFC converter," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 2925–2939, Mar. 2023.

[3] K. Yao, Y. Wang, J. Guo, and K. Chen, "Critical conduction mode boost PFC converter with fixed switching frequency control," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6845–6857, Aug. 2018.

[4] Z. Chen, J. Xu, P. Davari, and H. Wang, "A mixed conduction mode-controlled bridgeless boost PFC converter and its mission profile-based reliability analysis," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9674–9686, Aug. 2022.

[5] M. Lee and J. S. Lai, "Spread-spectrum frequency modulation with adaptive three-level current scheme to improve EMI and efficiency of three-level boost DCM PFC," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2476–2480, Mar. 2021.

[6] T. Tayar, A. Abramovitz, and D. Shmilovitz, "DCM boost PFC for high brightness LED driver applications," *Energies*, vol. 14, no. 17, 2021, Art. no. 5486.

[7] K. Yao, J. Li, F. Shao, and B. Zhang, "Parallel fixed switching frequency CRM and DCM boost PFC converter with high power factor," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3247–3258, Mar. 2022.

[8] L. Huang, F. Chen, W. Yao, and Z. Lu, "Flexible mode bridgeless boost PFC rectifier with high efficiency over a wide range of input voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3513–3524, May 2017.

[9] L. S. Mai, A. Rospirski, S. A. Mussa, and T. B. Lazzarin, "Totem-pole bridgeless PFC converter in DCM with synchronous rectification," in *Proc. IEEE 15th Braz. Power Electron. Conf. 5th IEEE Southern Power Electron. Conf.*, 2019, pp. 1–6.

[10] J. Wu, Y. Qi, F. Muhammad, and X. Wu, "A unified switch loss model and design consideration for multilevel boost PFC with GaN devices," *CPSS Trans. Power Electron. Appl.*, vol. 6, no. 4, pp. 349–358, 2021.

[11] Q. Huang, Q. Ma, P. Liu, A. Q. Huang, and M. A. de Rooij, "99% Efficient 2.5-kW four-level flying capacitor Multilevel GaN totem-pole PFC," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5795–5806, Oct. 2021.

[12] W. Wei-Shung and T. Ying-Yu, "Light load efficiency improvement for AC/DC boost PFC converters by digital multi-mode control method," in *Proc. IEEE 9th Int. Conf. Power Electron. Drive Syst.*, 2011, pp. 1025–1030.

[13] Y. Liu, H. Zhang, H. Wang, G. Xu, and F. Liu, "A unified control for PFC converter with seamless transition between PWM/PFM modes," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14384–14394, Dec. 2022.

[14] L. Li et al., "Maximum efficiency average current controller based on a comprehensive charge rate model for DCM boost PFC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 6046–6055, May 2021.

[15] K. Yao, X. Ruan, X. Mao, and Z. Ye, "Variable-duty-cycle control to achieve high input power factor for DCM boost PFC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1856–1865, May 2011.

[16] L. Wang, Q. H. Wu, W. H. Tang, Z. Y. Yu, and W. Ma, "CCM-DCM average current control for both continuous and discontinuous conduction modes boost PFC converters," in *Proc. IEEE Elect. Power Energy Conf.*, 2017, pp. 1–6.

[17] L. Li, Q. Zhang, R. Min, K. Liu, Q. Tong, and D. Lyu, "A current reshaping strategy to reduce parasitics-induced current distortion in discontinuous conduction mode boost power factor correction converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2215–2224, Mar. 2021.

[18] Y. Zhang, C. Yao, X. Zhang, H. Chen, H. Li, and J. Wang, "Power loss model for GaN-based MHz critical conduction mode Power factor correction circuits," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 141–151, Mar. 2020.

[19] J. Chen, Q. Luo, J. Huang, Q. He, and X. Du, "A complete switching analytical model of low-voltage eGaN HEMTs and its application in loss analysis," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1615–1625, Feb. 2020.

[20] J. Wang, H. Eto, and F. Kurokawa, "Optimal zero-voltage-switching method and variable ON-time control for predictive boundary conduction mode boost PFC converter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 527–540, Jan./Feb. 2020.

[21] X. Ren, Z. Guo, Y. Wu, Z. Zhang, and Q. Chen, "Adaptive LUT-based variable on-time control for CRM boost PFC converters," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8123–8136, Sep. 2018.

[22] A. Bianco, G. Scappatura, and F. Ciappa, "Valley skipping compensation for low THD in constant-on-time control for PFC pre-regulators: Implementation and performance," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 1264–1267.

[23] Q. Wu, X. Li, Y. Han, Z. Di, and Q. Feng, "A valley-locking control scheme for an audible noise-free valley-skip-mode flyback converter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 7285–7294, Jul. 2022.

[24] H. Nene, C. Jiang, and S. Choudhury, "Digital controller with integrated valley switching control for light load efficiency and THD improvements in PFC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 1785–1788.

[25] R. Min, G. Shen, Q. Tong, Q. Zhang, H. Peng, and X. Zou, "Unified pulsewidth-cycle control strategy to achieve mixed DCM/CRM operation and consistent valley switching for boost PFC converter," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13304–13316, Nov. 2021.

[26] T. Yunyu, Z. Fan, M. Jiong, and M. Hao, "A practical core loss calculation method of filter inductors in PWM inverters based on the modified Steinmetz equation," in *Proc. IEEE 23rd Int. Symp. Ind. Electron.*, 2014, pp. 386–391.

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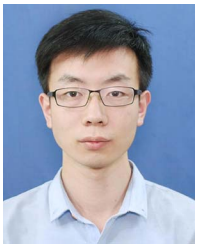

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