Electro-Thermo-Mechanical Analysis and Modeling of High-Power Intergrated Gate Commutated Thyristors

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***Abstract*—As a high-power electronic device, intergrated gate commutated thyristor (IGCT) has the characteristics of strong turn OFF, high surge capability, and high withstand voltage ability, which makes it receive more and more attention and be used more widely, such as circuit breakers and inverters. However, since IGCTs is a whole-wafer device, the current distribution and junction temperature distribution inside the chip cannot be measured, making it impossible to obtain the status of the chip and increasing the risk of device failure. In this case, the margin of the chip can only be increased to avoid failure and improve the reliability of the device, which greatly increases the cost of the device. This article proposes a new method to study the physical characteristics of IGCT chips by establishing the split-ring modeling. First, the characteristic of cells is studied to prove the necessity and effectiveness of split-ring model. Then, the electrical, thermal and pressure characteristics of the chip were studied, and their coupling effects were analyzed. Finally, a multiphysics coupling model was proposed to analyze the current and temperature distribution of IGCT under different working conditions. Experiments were conducted to verify the accuracy of the model.**

***Index Terms*—Current distribution, intergrated gate commutated thyristors (IGCT), junction temperature, multiphysics coupling model, split-ring modeling.**

I. Introduction

DUE to the huge turn-OFF capability, strong surge current capability, and low on-state voltage performance, intergrated gate commutated thyristors (IGCT) is now among the most extensively used high-power electronic devices and frequently used in circuit breakers and converters [1], [2], [3], [4], [5], [6]. Since IGCT in dc circuit breakers only need to turn OFF when a short-circuit fault arises, its turn-OFF loss can be ignored. But whether the IGCT can turn OFF successfully has a strong relationship with the conduction state before turning OFF. The distribution of current inside the IGCT chip and the maximum junction temperature directly affect the reliability of IGCT turn OFF.

However, the research on uniformity of current and temperature inside the chip is still very lacking and comprehensive research is urgently required. Some scholars have conducted research on gate turn-OFF thyristors (GTOs), which have similar structures with IGCT. The current distribution in each area of the GTO is measured during the dynamic process by modifying the tube shell structure and installing a Rogowski coil inside, but the current distribution of chip in the conduction state is not studied [7]. The current distribution is inverted by collecting magnetic field signals around the GTO. The disadvantage of this method is that the current inversion calculation of micron size is difficult and the accuracy is low [8], [9]. Some scholars have proposed optical measurement methods based on carrier infrared absorption method and composite radiation method. However, this method requires exposing the observation surface, causing destructive loss to the chip, and is difficult to test [10], [11], [12], [13].

At present, no scholars have conducted a comprehensive study on the mutual coupling of current, temperature, and pressure in IGCT chips. The current research focus is mainly in the field of insulated gate bipolar transistor (IGBT). A thermal network model of the IGBT chip established inside the press-pack IGBT device and analyzed the transient thermal impedance [14], [15]; Some scholars used the finite element method to analyze the stress and temperature distribution of the IGBT chip during the power cycle [16], [17]. In addition, the internal multichip parallel current sharing problem of press-pack IGBT has also been studied [18], [19], [20]. However, IGBT and IGCT have different structures and different chip packages, which makes it impossible to transfer the research results and methods of IGBT to IGCT.

At present, there is an urgent need on the application side to understand the status of IGCT during operation and accurately grasp the internal current distribution and maximum junction temperature of the chip. However, due to the lack of relevant research and monitoring methods, it is impossible to know the status of the chip during actual operation. In order to avoid IGCT failure, methods such as series and parallel connection are usually used to increase margins to improve reliability,

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which greatly increases the number and volume of devices used, and the cost. Therefore, it is essential to study the internal state of IGCT and the coupling relationship between various physical properties.

In this article, based on the distribution characteristics of IGCT cells, a method of studying IGCT chips in split-rings model is proposed, which can model and study IGCT chips in more detail. On this basis, the electrical, thermal, pressure characteristics, and their mutual coupling of IGCT are studied. An improved ABCD model is proposed to establish the relationship between electrical and thermal characteristics. Besides, the multiphysics coupling model of the IGCT chip is proposed and built in MATLAB/Simulink software. When compared to finite element modeling, the simulation speed is significantly increased in this field-circuit model. Finally, this model was used to examine the chip's current distribution and junction temperature distribution under conditions of surge current and continuous current flow. The surge test was conducted, and the experimental results is in good agreement with the simulation results, verifying the effectiveness and accuracy of the model.

The rest of this article is organized as follows. Section II presents the research method of chip ring division. The chip is divided into rings according to the circumference to study its characteristics. Section III analyzes the multiphysics coupling of the chip, and establishes a mathematical relationship to characterize the coupling relationship. The fourth section establishes a field-circuit coupling simulation model to realize the simulation of the current distribution and junction temperature distribution of the chip under different working conditions, and verifies the validity of the model through experiments. Finally, Section V concludes this article.

II. Split-Ring Model of IGCT Chips

In terms of construction, IGCT chips differ greatly from IGBT chips. The IGCT chip is a whole wafer chip, whereas the press-fit IGBT chip consists of many single tiny wafers. Fig. 1 shows the structure of 4-in IGCT chip. The cells on the IGCT chip are uniformly dispersed throughout its circumference, making cells on adjacent circumferences regarded as similar. Cells on various circumferences might be thought of as having variances because of location and manufacturing method. In order to accomplish improved modeling, the GCT chip is divided into 10 rings according to the radius length and every ring of cells is modeled separately. It is assumed that the characteristics of cells on the same ring are the same, while the characteristics of cells in various rings can be different.

To verify the hypothesis, the I-V property of cells at various places are tested, as shown in Fig. 2(a). The I-V curves of cells on separate rings have obvious differences. The cells on the outside of the chip have a higher equivalent resistance than that of the cells in the middle. Fig. 2(b) shows the voltage of different cell when the current is 1 A. The voltage of the cells located on the same circumference is closer, and the larger the circumference, the higher the voltage. The chip manufacturing procedure is to blame for the variation in cell properties at various sites. The chip manufacturing procedure can explain why the cells at

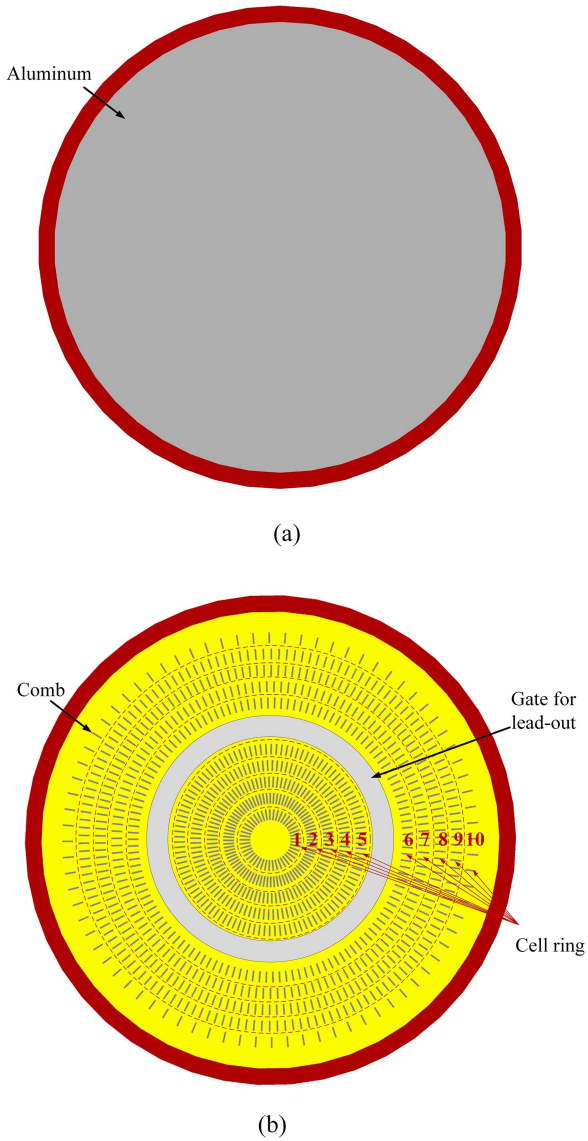


Fig. 1. Structure of 4-in IGCT chip.

various sites have different property. Because the chip is a round wafer, most manufacturing processes are designed for the round shape, so that the cells have similar process parameters in the circumferential direction but distinct process parameters in the radial direction. From the results of the I-V scan, the cell current density on the inside of the chip is higher during the flow process.

Besides, cells in different positions will experience different pressures, tolerate different junction temperatures, resulting in different current distribution. IGCT chips are crimped together to provide firm connections in applications. Fig. 3 shows the shell structure of IGCT. An external pressure of 40 kN is often used to connect a 4-in IGCT device. The distribution of pressure on the chip varies in the radial direction while remaining constant around the circle, which causes variations in the condition of the cells at various locations. However, it is hard to make the height of the molybdenum totally same, so that it is vital to consider the height difference of the cathode side assembly since the molybdenum. So the cathode molybdenum is split to test single

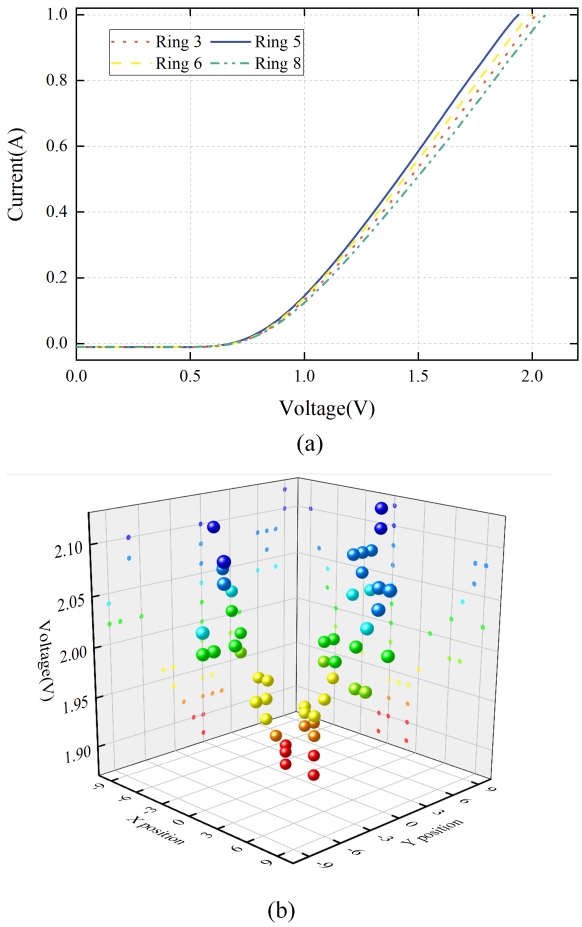


Fig. 2. Comparison of cellular properties at different locations. (a) I-V curves of cells on the different rings. (b) Voltage of cells with various location at 1A.

ring, as shown in Fig. 3. Fig. 4 shows the pressure distribution of GCT chip with different heights of cathode molybdenum. Small component height variations can have a significant impact on the chip in the radial direction. H_{in} and H_{out} are the heights of the inner and out molybdenum ring in the cathode. But the pressure distribution remains the same over the same perimeter. The pressure will result in different contact thermal resistance. This in turn affects junction temperature distribution and current distribution.

The above research leads to the conclusion that cells on different circles may differ in terms of their physical state and attributes and cells on the same circle often have similar characteristics. Ring division modeling is more appropriate to accurately represent the chip and clarify the real status of cells in various locations. With the goal to make it simpler to examine the distinctive qualities of numerous cell rings, the cathode molybdenum sheet is laser sliced. This allows for the independent investigation of the characteristics of each ring cell.

III. Multiphysics Coupling Analysis

The electrical characteristics and junction temperature distribution of the GCT chip are influenced by a few variables, including temperature and pressure. Analysis is more difficult due to the connection of multiphysical fields. This section will look at how the electromagnetic field interacts with the force field and temperature field.

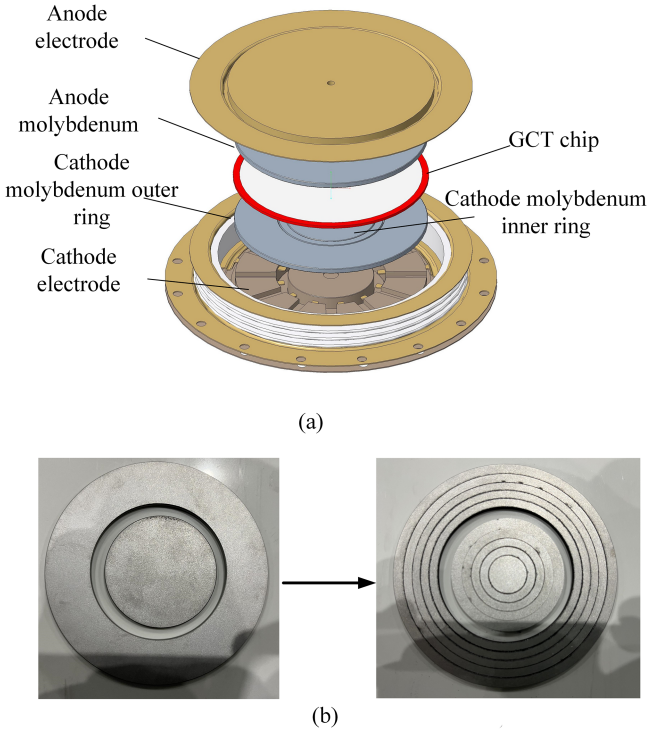


Fig. 3. IGCT shell structure and pressure distribution. (a) IGCT shell structure. (b) Cathode molybdenum cutting.

A. Thermal-Electric Connection

Temperature clearly has an impact on the GCT chip's electrical performance, such as the on-state voltage drop of cells. The electrical properties also influence the temperature distribution in turn because the power loss is the source of heat.

The impact of temperature on the chip's electrical properties is considered first. Since GCT chip is comparable to a p-i-n diode during the turn-ON state, it is possible to roughly determine the electrical characteristics of GCT chip by p-i-n diode model. The forward voltage during conducting can be divided into two parts—junction voltage V_{j} and drop voltage V_{drift}. V_{j} relates to the built-in voltage V_{bi} and the internal voltage drop ΔV

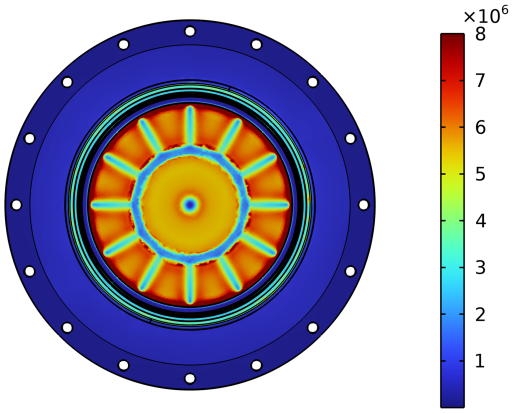
$$V_{\text{j}} = V_{\text{bi}} - \Delta V. \tag{1}$$

For the hole concentration p_{L} near the p^{+}n junction in the neutral base and the electron density n_{R} at the n^{+} side of the base, we can obtain

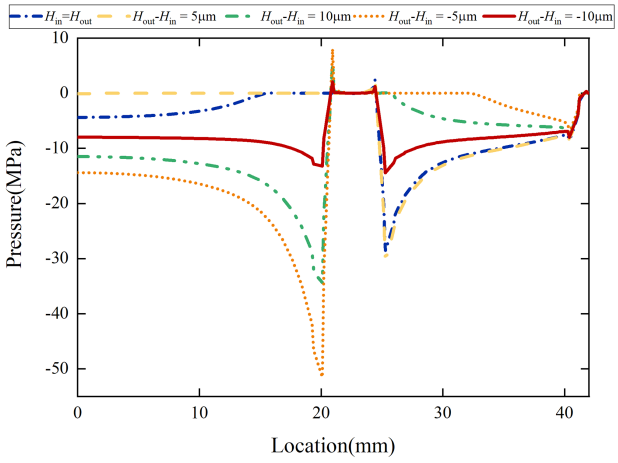
$$\begin{cases} \frac{p_{\text{L}}}{p^{+}} = \exp\left\{-\frac{q\Delta V_1}{kT}\right\}, \frac{p_{\text{n}0}}{p^{+}} = \exp\left\{-\frac{q\Delta V_{\text{bi}1}}{kT}\right\} \\ \frac{n_{\text{R}}}{n^{+}} = \exp\left\{-\frac{q\Delta V_2}{kT}\right\}, \frac{n_{\text{D}}}{n^{+}} = \exp\left\{-\frac{q\Delta V_{\text{bi}2}}{kT}\right\}. \end{cases} \tag{2}$$

The total external junction voltage V_{j} is

$$V_{\text{j}} = V_{\text{j}1} + V_{\text{j}2} = \frac{kT}{q}\ln\frac{p_{\text{L}}n_{\text{R}}}{{n_{\text{i}}}^2} = \frac{kT}{q}\ln(p_{\text{L}}n_{\text{R}}) - \frac{kT}{q}\ln {n_{\text{i}}}^2. \tag{3}$$



(a)



(b)

Fig. 4. Pressure distribution in GCT chip. (a) Stress distribution under ideal crimping. (b) Stress distribution simulation under different height.

The concentration of intrinsic carriers n_{i} increases with temperature

$$n_{\mathrm{i}} \propto T^3 \exp\left\{-\frac{E_{\mathrm{g}}}{kT}\right\}. \tag{4}$$

E_{g} is the band gap energy of the semiconductor. V_{j} is proportional to T and $T\ln T$. For ease of calculation, $T\ln T$ can be amplified to T^2. So V_{j} and temperature can be approximated in a quadratic relationship.

The voltage over the base region V_{drift} is obtained as

$$V_{\mathrm{drift}} = \frac{j}{q(\mu_{\mathrm{n}}+\mu_{\mathrm{p}})}\int_0^{w_{\mathrm{B}}}\frac{\mathrm{d}x}{p(x)} = \frac{jw_{\mathrm{B}}}{q(\mu_{\mathrm{n}}+\mu_{\mathrm{p}})\overline{p}}. \tag{5}$$

μ_{n} and μ_{p} are the mobility of free electrons and holes, respectively. w_{B} is the width of the n^- layer. To make the results more accurate, it is considered that the excess charge in the base is orders of magnitude higher than in the end regions, which is the Hall approximation model. The parameter $\bar{p}$ can be obtained

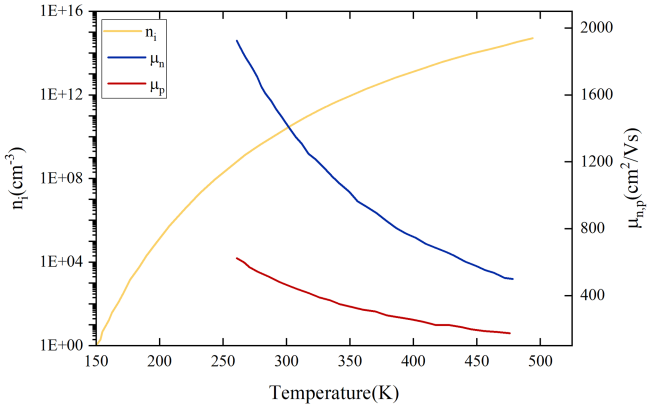


Fig. 5. Wafer parameters vary with temperature.

as

$$\frac{1}{\overline{p}} = \frac{qw_{\mathrm{B}}}{2j\tau_{\mathrm{HL}}}\left[1+\sqrt{1+\frac{2\tau_{\mathrm{HL}}H}{qD_{\mathrm{A}}\tanh^2\left(\frac{w_{\mathrm{B}}}{2L_{\mathrm{A}}}\right)}j}\right]. \tag{6}$$

τ_{HL} means carrier lifetime at high injection level, D_{A} is Ambipolar diffusion constant, L_{A} is Ambipolar diffusion length, and H is related with recombination of emitters and is to a sufficient approximation often independent of $\bar{p}$.

So, one obtains for the voltage drop across the middle region

$$\begin{aligned} V_{\mathrm{drift}} &= \frac{w_{\mathrm{B}}^2}{2(\mu_{\mathrm{n}}+\mu_{\mathrm{p}})\tau_{\mathrm{HL}}}\left[1+\sqrt{1+\frac{2\tau_{\mathrm{HL}}H}{qD_{\mathrm{A}}\tanh^2\left(\frac{w_{\mathrm{B}}}{2L_{\mathrm{A}}}\right)}j}\right] \\ &= \frac{w_{\mathrm{B}}^2}{(\mu_{\mathrm{n}}+\mu_{\mathrm{p}})L_{\mathrm{A}}\tanh\left(\frac{w_{\mathrm{B}}}{2L_{\mathrm{A}}}\right)\sqrt{2}}\sqrt{Hj/q}. \end{aligned} \tag{7}$$

V_{drift} is proportional to the square root of the current density. the influence of temperature is mainly on the mobility μ_{n} and μ_{p}. They can be well described by the Caughey–Thomas formula

$$\mu = \mu_\infty + \frac{\mu_0-\mu_\infty}{1+\left(\frac{N}{N_{\mathrm{ref}}}\right)^\gamma}. \tag{8}$$

For electrons, N_{ref} is 9.7e16 and μ_0 is proportional to $(300/T)^{2.28}$. For holes, N_{ref} is 2.4e17 and μ_0 is proportional to $(300/T)^{2.1}$. Usually, the doping concentration of the base region is smaller than 1e14. So the mobility is approximately μ_0. So $1/(\mu_{\mathrm{n}}+\mu_{\mathrm{p}})$ is proportional to T^2 approximately and V_{drift} can be proportional to T^2. Fig. 5 shows the changes in intrinsic carrier concentration and mobility with temperature [21].

The I-V characteristic test curve and mathematical formula of the chip are usually given in the data sheet of the IGCT device, which is called the ABCD model

$$V_{\mathrm{T}} = A + B\cdot i_{\mathrm{T}} + C\cdot\ln(i_{\mathrm{T}}+1) + \mathrm{D}\cdot\sqrt{i_{\mathrm{T}}}. \tag{9}$$

In the formula, parameter A is related to the threshold voltage of the chip, parameter B is related to the ohmic resistance, the third item is related to the p-n junction voltage and the fourth item is related to the space charge and the voltage drop of base region.

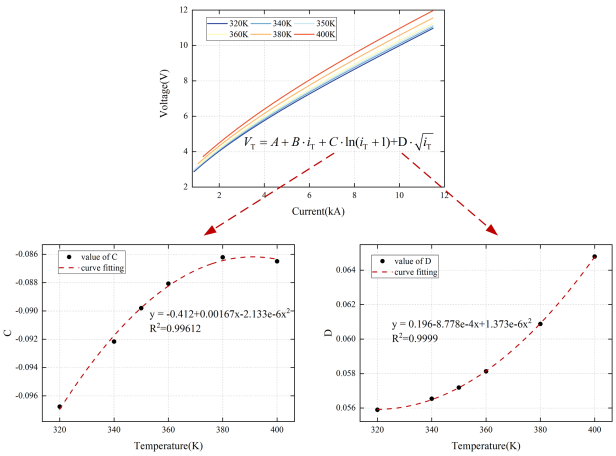


Fig. 6. I-V characteristic simulation and *C,D* parameters are fitted with temperature.

After the above analysis, the parameters *C* and *D* have a quadratic relationship with the temperature T, so that the influence of temperature on the electrical characteristics can be reflected through these two parameters. We simulate the I-V curve of IGCT cell in TCAD software under different temperature and get model parameters *C* and *D* by a fixed parameters *A* and *B*. Through the simulation, it is proved that parameters *C* and *D* do have a good quadratic relationship with temperature. In this way, the impact of temperature on the electrical property can be characterized through parameters *C* and *D*. Fig. 6 shows the fitting of *C* and *D* parameters with temperature.

The loss that occurs when the chip is powered up demonstrates how electrical properties influence temperature. The loss is greater and the temperature is higher the bigger the conduction voltage drop under the same current. The on-state loss of the IGCT chip is

$$P_{\text{loss}} = V_{\text{AK}} I_{\text{AK}} + V_{\text{GK}} I_{\text{GK}}. \tag{10}$$

Since V_{GK} and I_{GK} are much small compared to V_{AK} and I_{AK}, they will not increase significantly even at high currents, so only the power loss caused by the anode current and anode voltage is considered

$$P_{\text{loss}} = V_{\text{AK}} I_{\text{AK}}. \tag{11}$$

The junction temperature of GCT chip may be determined by observing how the heat generated interacts with the shell structure and the ambient temperature. As a result, the electrical properties of GCT chip operate as a heat source and influence thermal properties.

B. Coupling of Pressure and Temperature

The pressure influence on the temperature field is mostly exhibited through contact thermal resistance. The junction temperature of the chip is not only affected by the heating power, but also by the heat dissipation performance of the tube case. The junction temperature of the chip is not only affected by the heating power, but also by the heat dissipation performance of the tube case. Thermal resistance and capacitance networks

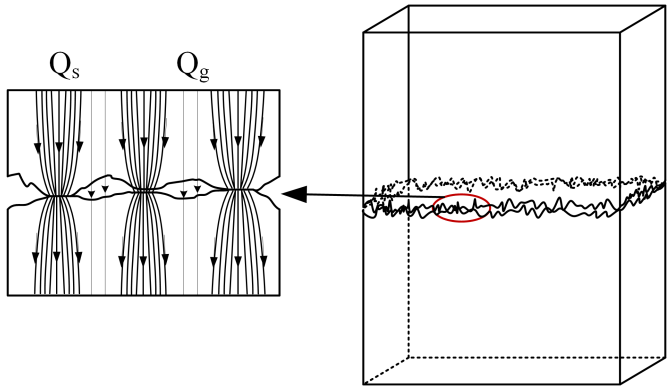


Fig. 7. Schematic diagram of contact thermal resistance.

are often used to describe heat dissipation performance. The lower the thermal resistance, the lower the junction temperature under the same power loss. Contact thermal resistance, as an important source of thermal resistance, which might make up as much as 50% of the total thermal resistance, is mainly affected by contact pressure and surface roughness. Fig. 7 shows the schematic diagram of contact thermal resistance.

Even though the two crimping interfaces are pressed together with a lot of power, only a few locations on the surfaces really make meaningful contact, and these few tiny areas that join bear all the pressure. Gas fills the holes that have yet to be reached. As a result, the shrinkage heat conduction h_s and the gap heat conduction h_g of the gap heat transfer become the principal modes of heat transfer between the parts of IGCT shell. Bahrami et al. [22] derived the contact heat conduction formula by studying a single contact

$$h_s = 1.25 k_s \frac{m}{\sigma} \left(\frac{p}{H_c} \right)^{0.95}. \tag{12}$$

Among them, p is the contact pressure, and k_s is the harmonic mean of the thermal conductivity of the two contact interfaces. H_c is the microhardness of the relatively soft material. Yovanovich [23] puts forward a formula to characterize the microhardness and other factors through many experiments and theoretical fitting, in order to obtain the microhardness

$$H_c = \frac{p}{\left(\frac{p}{c_1 \cdot \left(\frac{1.62\sigma}{m\sigma_0} \right)^{c_2}} \right)^{\frac{1}{1+0.071 \cdot c_2}}}. \tag{13}$$

c_1 and c_2 can be considered as fitting parameters.

The theoretical calculation formula of the gap contact thermal resistance can be used as the following formula:

$$h_g = \frac{k_g}{Y + M}. \tag{14}$$

k_g is the thermal conductivity of the gas filling the void, *M* is the gas parameter, and *Y* is the effective void thickness.

Therefore, the pressure can directly affect the contact thermal resistance, which in turn affects the heat dissipation path the

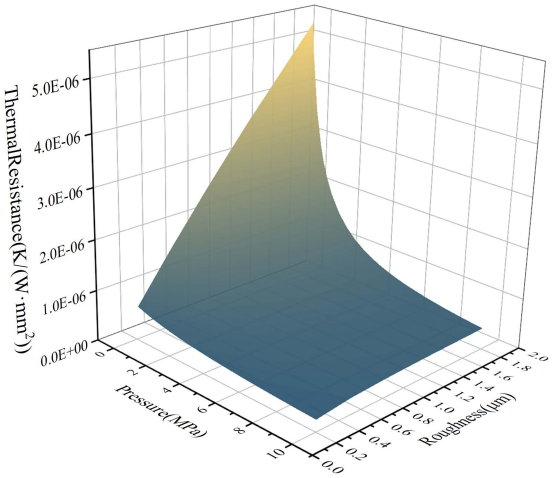


Fig. 8. Change law of contact thermal resistance with pressure and roughness.

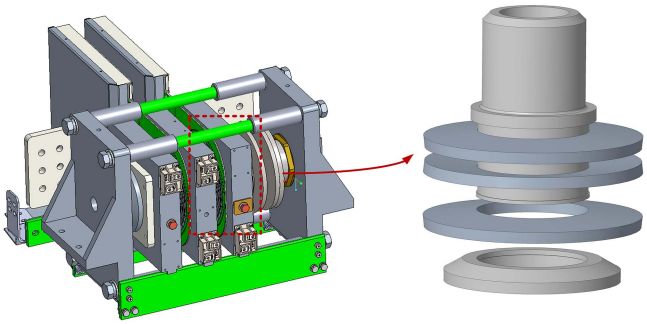


Fig. 9. Schematic diagram of valve string and disc spring.

junction temperature. Fig. 8 shows the relationship between thermal resistance and pressure, roughness.

Conversely, an increase in temperature will cause thermal stress in the material. However, when the IGCT device is crimped, the top plate will have a disc spring to absorb the thermal stress, so high temperature will not produce excessive thermal stress, as shown in Fig. 9. Therefore, the influence of temperature on pressure distribution is often ignored.

C. Coupling of Electrical Properties and Pressure

The influence of pressure on electrical characteristics is mainly realized through contact resistance. However, in the GCT shell, only the resistance of the aluminum layer on the cathode sides and the molybdenum has an impact on the electrical characteristics. The relationship between contact resistance and pressure can be expressed by an empirical formula

$$\ln R_{\mathrm{c}} = K_{\mathrm{c}} - m \ln F. \tag{15}$$

K_{c} is a constant, which depends on the materials. m is also a constant related to the form of contact. F is the force exerted on the material, which equals pressure times area.

The contact resistance between aluminum and molybdenum is simulated in COMSOL. The surface roughness of the two parts is assumed as 1 μm and Fig. 10 shows the results. Through

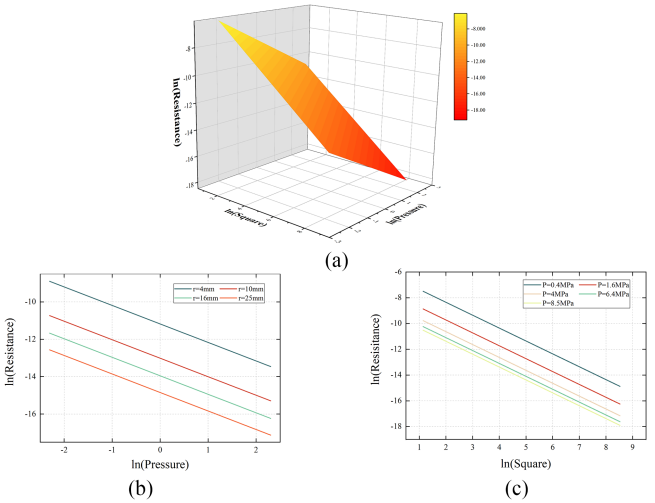


Fig. 10. Relationship between contact resistance and voltage and area.

simulation, it can be observed that the connection between l nR_{c} and l nF is linear. Besides, l nR_{c} is linear with l nP and l nS. The contact resistance changes from 20 nΩ to 1 $\mu\Omega$ as the pressure goes from 0.1 Mpa to 10 Mpa. The impact of the contact resistance may be disregarded when compared to the mΩ-level bulk resistance.

Electrical stress is very small compared to externally applied stress and can be ignored. Therefore, the influence of electrical characteristics on the pressure distribution is not considered.

IV. Model Building

A. Modeling of Electrical Properties of Cell Rings

To obtain the on-state characteristics of each cell ring separately, the cathode molybdenum is cut to keep only one cell ring turned ON. The on-state characteristics of each ring unit cell were tested at different temperatures. The first, second, and third rings were measured because the number of unit cells was too small. Fig. 11 shows the result of experiments and fitting. Since the rings No. 1, 2, and 3 have few cells, the current can not be high, which will reduce the precision. So, the one, two, and three rings are collectively regarded as the 3 ring. The ABCD model is used to fit the I-V curve at different temperature and the parameters C and D are obtained. Then, the quadratic relationship between parameters and temperature is obtained by fitting. Table I shows the parameters of each ring.

B. Thermal Network Model of GCT Chip

The thermal network model is established based on the Cauer model. Each layer of material can be expressed as a thermal capacity and thermal resistance, connected in τ-shape. Adjacent materials can be directly connected in series. The heat conduction process through a certain thin layer can be expressed by the heat conduction equation

$$P_{\mathrm{in}} = -\lambda A \frac{\partial T}{\partial l} + \rho c A l \frac{\partial T}{\partial t}. \tag{16}$$

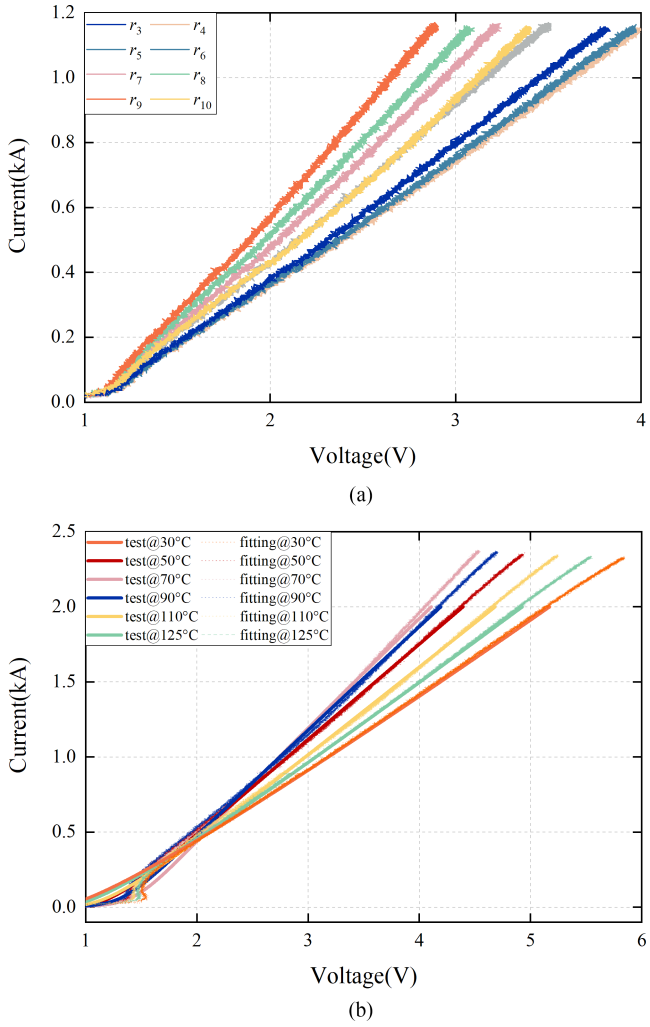


Fig. 11. ABCD model and comparison of single cell rings. (a) I-V characteristic of each ring. (b) I-V characteristic under different temperature.

TABLE I
FITTED PARAMETERS OF THE ABCD MODEL FOR EACH RING

Number of ring	C			D		
	T^2	T	c	T^2	T	c
3(A=0.559,B=0.00202)	9.0532 E-7	−2.3E-3	0.25048	2.2867 E-6	2.8E-4	−0.0204
4(A=0.5,B=0.0023)	−3.8248 E-6	−1.2E-3	0.25136	3.6424 7E-6	−5.7E-5	−0.0212
5(A=0.5151, B=0.0018)	−2.1089 E-6	−1.6E-3	0.17191	2.6785 E-6	1.36E-4	0.0068
6(A=0.7574, B=0.00179)	7.9278 E-6	−3E-3	0.22327	1.0984 E-6	3.6348 E-4	−0.0221
7(A=0.6687, B=0.00147)	2.8156 E-6	−2.2E-3	0.20015	1.4555 E-6	2.9981 E-4	−0.0143
8(A=0.6566, B=0.0017)	5.7453 E-7	−1.95E-3	0.27252	1.3558 E-6	3.3836 E-4	−0.045
9(A=0.5,B=0.0013)	1.5634 E-6	−1.76E-3	0.21	2.8981 E-6	−3.7976 E-5	−0.0039
10(A=0.644, B=0.00163)	−3.6619 E-6	−7.134E-4	0.1222	1.5543 E-6	2.1701 E-4	−0.0092

TABLE II
IGCT SHELL MATERIAL PARAMETERS

Material type	Thermal specific volume(J/gK)	Density(g/cm^3)	Thermal conductivity(W/cmK)
Si	0.7	2.33	1.48
Al	0.76	3.97	0.36
Mo	0.25	10.2	1.38
Cu	0.385	8.96	4.01

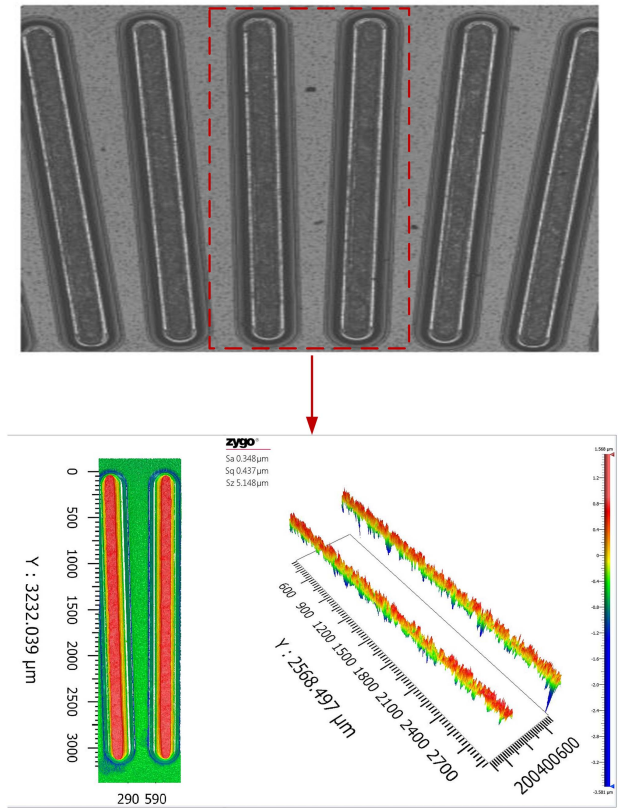


Fig. 12. Chip surface roughness measurement.

P_{in} is the input power and l is the thickness of the layer.

According to (16), we can obtain the thermal resistance and thermal capacitance

$$\begin{cases} R = \frac{l}{A\lambda} \\ C = \rho c A l. \end{cases} \tag{17}$$

Table II gives the properties of materials of IGCT shell. So, we can establish the Thermal network model of IGCT.

A large part of the thermal resistance is the contact thermal resistance between components, which is influenced by the force. So, it is vital to take the contact thermal resistance into account. The surface roughness of the chip cathode comb was measured using a white light interferometer, as shown in Fig. 12. The root mean square value of the error Sq is within 0.5 μm. Table III shows the test result of other materials.

Based on the above analysis, we established a thermal resistance model for each cell ring of the chip, and used thermal resistance to characterize the heat transfer between rings. Fig. 13

TABLE III
SURFACE ROUGHNESS OF EACH LAYER OF THE IGCT

Components	Sq
Cu	0.852
Anode molybdenum	0.702
Anode surface of chip	0.152
Cathode surface of chip	0.437
Cathode molybdenum of out	0.561
Cathode molybdenum of in	0.814

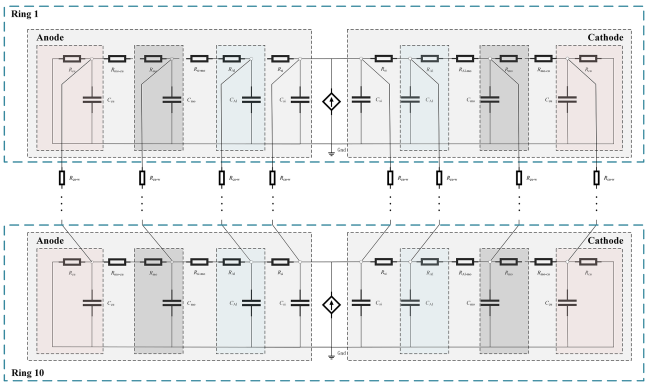


Fig. 13. Thermal resistance capacitance model under multivariate cells.

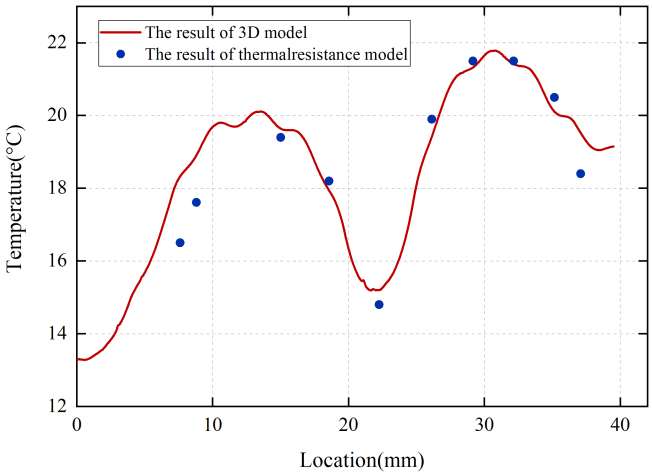


Fig. 14. Comparison of thermal resistance capacitance model and finite element simulation results.

shows the thermal network of IGCT separate-ring model. In order to verify the accuracy of the model, the thermal network model and the three-dimensional finite element model were compared, as shown in Fig. 14. The results of the two simulations are similar, which effectively illustrates the accuracy of the model.

C. Multiphysics Coupling Model of GCT Chip

Based on the above analysis and experiments, a multiphysics coupled model of IGCT is established in MATLAB/Simulink. The pressure of each ring, ambient temperature and total current are external input physical quantity. The pressure determines

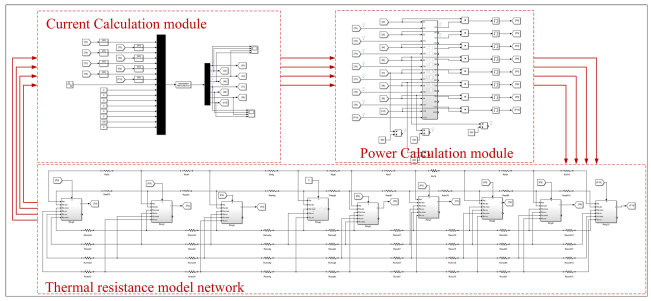


Fig. 15. Schematic diagram of the Multiphysics coupling simulation mode.

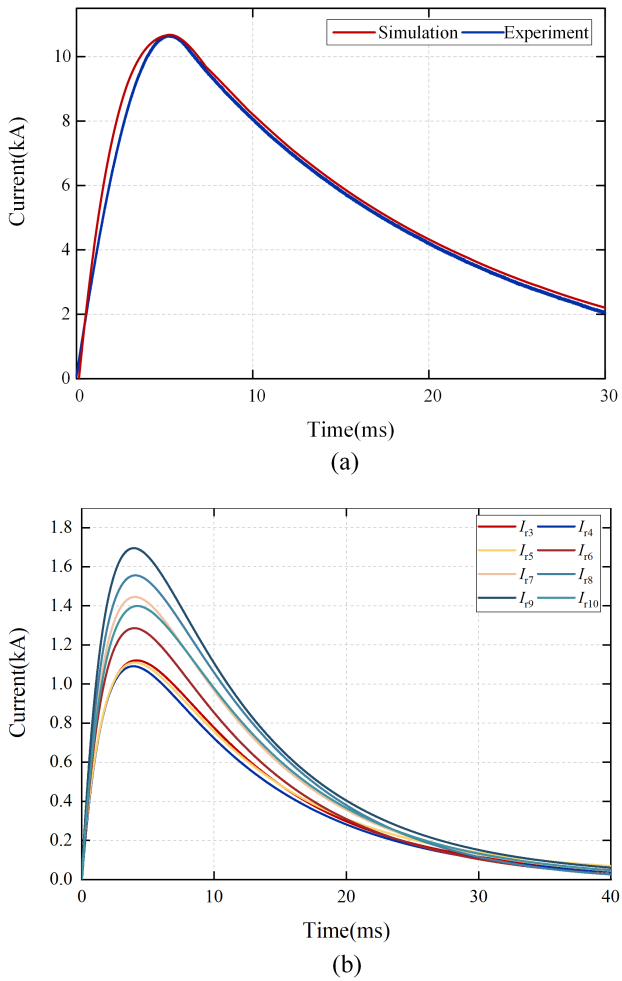


Fig. 16. Surge simulation waveform and current distribution. (a) Current wave. (b) Current of each ring.

the contact thermal resistance of each ring, thus determining the thermal network model. The junction temperature calculated by the thermal network model will determine the I-V characteristic curve of each ring, thereby affecting the current distribution of each cell ring. The current distribution will affect the loss and heating of each cell ring, thereby affecting the input of the thermal network model. The three are coupled to each other and influence each other, making the simulation results more accurate. Fig. 15 shows the multiphysics coupling model of GCT chip in Simulink.

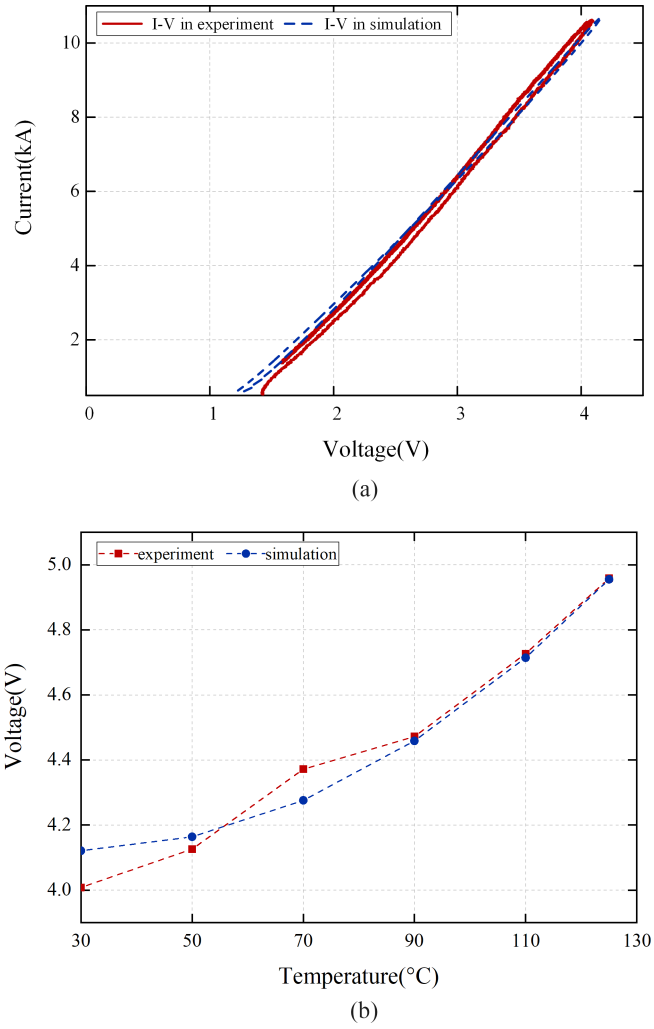


Fig. 17. Comparison of simulation and test results. (a) I-V characteristic curve comparison. (b) Comparison of peak voltages at different temperatures.

V. Simulation and Verification

Using the proposal multiphysics coupling model, surge conditions, and long-term flow conditions were simulated respectively. Fig. 16 shows the current distribution under 10 kA surge current at 110 °C ambient temperature. The current wave in simulation is similar with that in the experiment. The most current flows through the eighth and ninth ring cells and the current flowing through the inner cell ring is almost the same, which is smaller than that of other cell rings. To verify the validity of the model, the I-V characteristic curves of the test and simulation are compared in Fig. 17(a). Fig. 17(b) shows the comparison of maximum on-voltage drops at different temperatures. The maximum difference is less than 0.2 V. Therefore, we can think that the simulation results are in very good agreement with the experimental results, and the accuracy of the model is very high.

We also tested the on-state voltage drop when the chip is turned on for a long time. As shown in Fig. 18, the on-state voltage drop calculated through the coupling model is in very good agreement with the actual measured on-state voltage drop,

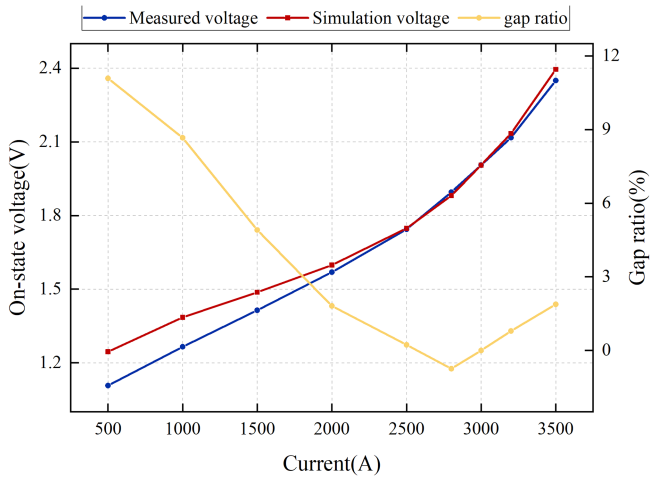


Fig. 18. Simulation comparison results of on-state voltage drop under steady-state current.

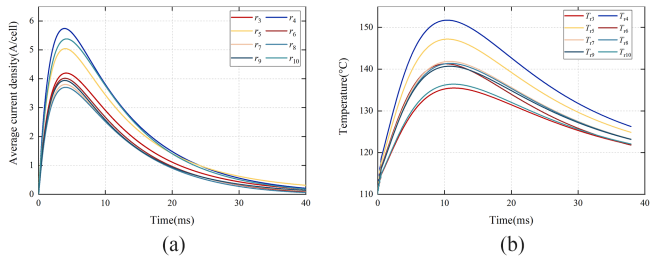


Fig. 19. Current density distribution and junction temperature distribution under surge conditions. (a) Current density of each ring. (b) Junction temperature of each ring.

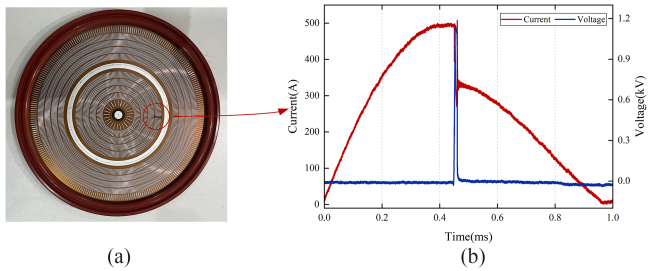
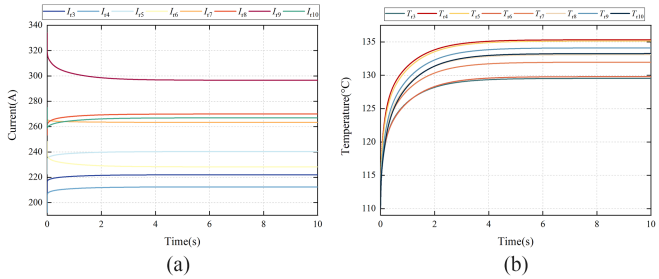


Fig. 20. Failure waveform during turning OFF and failure point positioning. (a) The surface of failed IGCT. (b) Failure breaking waveform.

and the error is within 10%, indicating that the simulation model is very reliable.

Although the most current flows through the eighth and ninth ring cells, the highest current density and junction temperature are located at the ring 5, which means the cells in this ring will have the highest risk of failure, as shown in Fig. 19. Under surge conditions, the current distribution density difference is large, and the maximum junction temperature difference reaches 20 °C.

The current density and temperature of ring 8 and 9 is much less than those in ring 4 and 5. Fig. 20 shows the turn-OFF test failure when using ring 5 and 9. The failure location is exactly in the ring 5.



(a) (b)

Fig. 21. Current distribution and junction temperature under long-term current. (a) Current distribution in each ring. (b) Temperature of each ring.

Besides, the long-term flow conditions are simulated, which is similar with the solid-state circuit breaker condition, as shown in Fig. 21. For long-term conduction, the current distribution is different from the current distribution under the surge, and the ninth ring current is significantly higher than that in other locations. In steady state, the junction temperature distribution inside the chip is more uniform, and the maximum temperature difference is only 6 °C

VI. Conclusion

This article studied the various physical characteristics inside the IGCT chip, and proposes a separate-ring modeling method for the entire wafer structure of the chip. Besides, the coupling relationship between the electrical, thermal, and pressure characteristics of IGCT chip is analyzed and a multiphysics coupling model is established to accurately characterize the current and junction temperature distribution of the chip. Finally, based on the proposed model, the current and temperature conditions of the IGCT chip under surge conditions and long-term flow conditions were studied, and the accuracy and effectiveness of the model were verified through experiments. Under the surge condition, the current distribution and junction temperature difference inside the chip are greater, and the maximum difference in junction temperature is 20 °C, while under the long-term steady-state condition, the current gap inside the chip is small, and the junction temperature gap is smaller.

References

[1] Z. Wang, C. Xu, Z. Yu, Z. Chen, B. Zhao, and R. Zeng, "Low-frequency and sub-synchronous power oscillation suppression and analysis of hybrid line commutated converter for HVDC grid," *IEEE Trans. Power Syst.*, to be published, doi: 10.1109/TPWRS.2023.3288153.

[2] Z. Yu et al., "Comprehensive physical commutation characteristic analysis and test of hybrid line commutated converter based on physics compact model of IGCT," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1924–1934, Feb. 2023, doi: 10.1109/TPEL.2022.3213490.

[3] C. Meyer, M. Kowal, and R. W. De Doncker, "Circuit breaker concepts for future high-power DC-applications," in *Proc. Ind. Appl. Conf.*, Oct. 2005, vol. 2, pp. 860–866.

[4] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.

[5] X. Yan et al., "A novel oscillating-commutation solid-State DC breaker based on compound IGCTs," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1418–1422, Feb. 2023, doi: 10.1109/TPEL.2022.3211856.

[6] C. Ren et al., "Deciphering the effect of corrugated p-base on reverse blocking IGCT," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 5059–5067, Sep. 2022.

[7] T. Yatsuo, S. Kimura, and Y. Sato, "Design considerations for large-current gtos," *IEEE Trans. Electron Devices*, vol. 36, no. 6, pp. 1196–1202, Jun. 1989.

[8] C. M. Johnson et al., "Correlation between local segment characteristics and dynamic current redistribution in gto power thyristors," in *Proc. 3rd Int. Symp. Power Semicond. Devices ICs*, 1991, pp. 121–127.

[9] P. R. Palmer and C. M. Johnson, "Measurement of the redistribution of current in gto thyristors during turn-off," in *Proc. Eur. Power Electron. Conf.*, 1989, pp. 1621–1625.

[10] M. Lundqvist, H. Bleichner, and E. Nordlander, "An optical system for bilateral recombination-radiation diagnostics of the carrier redistribution in switching power devices," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 6, pp. 956–961, Dec. 1991.

[11] H. Bleichner, E. Nordlander, M. Rosling, and S. Berg, "A time-resolved optical system for spatial characterization of the carrier distribution in a gate turn-off thyristor(gto)," *IEEE Trans. Instrum. Meas.*, vol. 39, no. 3, pp. 473–478, Jun. 1990.

[12] H. Ohashi and A. Nakagawa, "A study on gto turn-off failure mechanism," in *Proc. 1981 Int. Electron Devices Meet.*, Washington, DC, USA, 1981, pp. 414–417, doi: 10.1109/IEDM.1981.190102.

[13] M. Hatle and J. Vobecky, "Infrared observation of gate turn-off thyristor segment parameter nonuniformlty," *IEEE Trans. Electron Devices*, vol. 37, no. 4, pp. 1169–1171, Apr. 1990.

[14] C. Busca, R. Teodorescu, F. Blaabjerg, L. Helle, and T. Abeyasekera, "Dynamic thermal dodelling and analysis of press-pack IGBTs both at component-level and chip-level," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Vienna Austria, 2013, pp. 677–682.

[15] A. A. Hasmasan, C. Busca, and R. Teodorescu, "Electro-thermo-mechanical analysis of high-power press-pack insulated gate bipolar transistors under various mechanical clamping conditions," *IEEJ J. Ind. Appl.*, vol. 3, no. 3, pp. 192–197, 2014.

[16] T. Poller, "Mechanical analysis of press-pack IGBTs," *Microelectronics Rel.*, vol. 52, no. 9, pp. 2397–1759, 2012.

[17] T. Poller, "Influence of the clamping pressure on the electrical, thermal and mechanical behavior of press-pack IGBTs," *Microelectronics Rel.*, vol. 53, pp. 1755–1759, 2013.

[18] H. Y. Long, M. R. Sweet, E. M. S. Narayanan, and G. Li, "Reliability study and modelling of IGBT press-pack power modules," in *Proc. Appl. Power Electron. Conf. Expo.*, 2017, pp. 2711–2717.

[19] A. Müsing, G. Ortiz, and J. W. Kolar, "Optimization of the current distribution in press-pack high power IGBT modules," in *Proc. Int. Power Electron. Conf. - ECCE ASIA*, Sapporo, Japan, 2010, pp. 1139–1146, doi: 10.1109/IPEC.2010.5543573.

[20] R. Wu, L. Smirnova, H. Wang, F. Iannuzzo, and F. Blaabjerg, "Comprehensive investigation on current imbalance among parallel chips inside MW-scale IGBT power modules," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, Seoul, South Korea, 2015, pp. 850–856, doi: 10.1109/ICPE.2015.7167881.

[21] J. Luts, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices, Physics, Characteristics, Reliability*, 2nd ed. Cham, Switzerland: Springer, 2018.

[22] M. Bahrami, R. Culham, and M. Yovanovich, "Thermal resistances of gaseous gap for conforming rough contacts," *42nd AIAA Aerosp. Sci. Meeting Exhibit.*, p. 821, Jan. 2004.

[23] M. M. Yovanovich, "Four decades of research on thermal contact, gap, and joint resistance in microelectronics," *IEEE Trans. Compon. Packag. Technol.*, vol. 28, no. 2, pp. 182–206, Jun. 2005, doi: doi: 10.1109/TCAPT.2005.848483.