Dynamic Current Sharing Mechanism Analysis of Paralleled SiC MOSFETs Considering Parasitic Mutual Inductances Based on an Improved Model

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***Abstract*—The dynamic current imbalance between paralleled SiC MOSFETs can cause unbalanced switching losses and limit the current capacity. It is essential to investigate the influences of the circuit parameters. However, the influences of the unbalanced parasitic mutual inductances and the influences of the common values between the paralleled parameters are unclear. To address these issues, an improved current sharing model is established considering all the parasitic mutual inductances. Based on this model, it is found that the influence degrees of the unbalanced power-drive source mutual inductance (ΔM_{pk}), the unbalanced drain-source mutual inductance (ΔM_{ds}) and the unbalanced power-source inductance (ΔL_{s}), the unbalanced power-gate mutual inductance (ΔM_{pg}), and the unbalanced threshold voltages (ΔV_{th}) increase in order. The influence mechanisms of the unbalanced parasitic mutual inductances are also analyzed. Moreover, the effects of the common values between the paralleled parameters (M_{gk}, R_{gin}, M_{pg}, M_{pk}, M_{ds}, and L_{s}) are also investigated. Increasing M_{pg}, M_{ds}, and L_{s} or decreasing M_{pk} and M_{gk} can help reduce the current imbalance. Increasing R_{gin} can also decrease the unbalanced currents if ΔV_{th} is small. All conclusions are well verified by experiments, and their contributions to the design of circuit layouts and current sharing methods are discussed.**

***Index Terms*—Dynamic current sharing mechanisms, dynamic current sharing model, multichip SiC power modules, paralleled SiC MOSFETs, parasitic mutual inductances.**

NOMENCLATURE

MOSFET Parameters

g_{m}	MOSFET transconductance.
V_{th}	MOSFET threshold voltage.
C_{dg}	MOSFET drain-gate capacitance.
C_{gs}	MOSFET gate-source capacitance.
C_{ds}	MOSFET drain-source capacitance.
C_{iss}	MOSFET input capacitance.

Circuit Parasitic Inductances

L_{sm}	Power-source self-inductance of the m_{th} power-source branch.
M_{dmsn}	Drain-source mutual inductance between the m_{th} drain branch and the n_{th} power-source branch.
M_{dmgn}	Drain-gate mutual inductance between the m_{th} drain branch and the n_{th} gate branch.
M_{smgn}	Power source-gate mutual inductance between the m_{th} power-source branch and the n_{th} gate branch.
M_{dmkn}	Drain-drive source mutual inductance between the m_{th} drain branch and the n_{th} drive-source branch.
M_{smkn}	Power source-drive source mutual inductance between the m_{th} power-source branch and the n_{th} drive-source branch.
M_{gmkn}	Gate-drive source mutual inductance between the m_{th} gate branch and the n_{th} drive-source branch.
M_{pmgn}	Power-gate mutual inductance between the m_{th} power branch and the n_{th} gate branch.
M_{pmkn}	Power-drive source mutual inductance between the m_{th} power branch and the n_{th} drive-source branch.
M_{s1s2}	Mutual inductance between paralleled power-source branches.
M_{g1g2}	Mutual inductance between paralleled gate branches.
M_{k1k2}	Mutual inductance between paralleled drive-source branches.
ΔM_{pg}, M_{pg}, M_{pg}'	Differential and common parameters of power-gate mutual inductances.
ΔM_{pk}, M_{pk}, M_{pk}'	Differential and common parameters of power-drive source mutual inductances.
ΔM_{ds}, M_{ds}	Differential and common parameters of drain-source mutual inductances.
ΔL_{s}, L_{s}	Differential and common parameters of power-source self-inductance and mutual inductance
	$m, n = 1, 2$.

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Voltage Sources in Driving Circuit

$\Delta v_{\rm pg}$, $v_{\rm pg}$	Differential and common induced voltages in gate branches.
$\Delta v_{\rm pk}$, $v_{\rm pk}$	Differential and common induced voltages in drive-source branches.
$\Delta v_{\rm ps\text{-}d}$	Differential induced voltage in power-source branches caused by drain-source mutual inductances.
$\Delta v_{\rm ps\text{-}s}$	Differential induced voltage in power-source branches caused by power-source self-inductance and mutual inductance.
$V_{\rm dri}$	Driving voltage.
$i_{\rm c}$	Current caused by $C_{\rm dg}{\rm d}v_{\rm ds}/{\rm d}t$.

I. Introduction

DUE to the high switching speed, high operating junction temperature, and high thermal conductivity, SiC MOSFETs have been attracting more attention and are widely used in many applications [1], [2], [3]. Limited by the manufacturability and costs, the maximum current rating of SiC MOSFET dies is generally lower than 150 A [4]. So, SiC MOSFETs are paralleled in high-power applications to improve the power rating [5]. However, unbalanced static and dynamic currents between the paralleled chips can cause unbalanced conduction and switching losses, which cause unbalanced junction temperatures. The solder layer of the chip with a higher junction temperature will degrade earlier, increasing the thermal resistance of this chip. Then, the junction temperature of this chip will be further increased, shortening the device's lifetime [6]. Moreover, the threshold voltage of this chip will be lower, which will cause higher switching currents and switching losses on this chip. The junction temperature will further increase, aggravating the problems. Thus, it is necessary to balance static and dynamic currents. The static current imbalance is caused by unbalanced conduction resistances $R_{\rm dson}$, and unbalanced parasitic parameters in the paralleled branches [7], which is easier to address. However, due to the complex switching transients, the unbalanced dynamic currents are influenced by numerous circuit parameters, and the mechanisms are complicated. In practical circuits, it is hard to achieve completely symmetrical layouts. So, it is significant to investigate the dynamic current sharing mechanisms under the unsymmetrical circuit parameters to balance the dynamic currents [7]. It can give researchers a clear insight into the impacts of the various parameters to optimize circuit layouts and present current balancing methods.

There are many works investigating the influences of unbalanced circuit parameters on dynamic current sharing in circuits without Kelvin-source connections. In [8], [9], and [10], it is found that unbalanced device parameters and parasitic inductances can cause dynamic current imbalance. The influences are explicitly investigated in [11], [12], [13], and [14]. It is found that the MOSFET with a lower $V_{\rm th}$ will bear higher dynamic currents [11]. Moreover, the difference between the common source inductances greatly influences dynamic current sharing [12], [13]. In contrast, the difference between the drain inductances has little effect [14]. The chip with a larger common source inductance will bear lower turn-ON and higher turn-OFF currents. In order to increase the switching speed and decrease the coupling between the power loop and the driving loop, Kelvin-source connections are widely used in circuits with SiC MOSFETs [15], [16]. In [17], the effects of the Kelvin-source connection are investigated. It is found that it can help reduce the dynamic current imbalance. Zeng et al. [18] investigated the influences of unbalanced circuit layouts, by establishing the coefficients that can reflect the dynamic current sharing performance. In [7], the influences of unbalanced parasitic inductances and junction temperatures are investigated. It is further concluded that unbalanced power-source inductances and unbalanced threshold voltages $V_{\rm th}$ are the main factors causing unbalanced dynamic currents. In contrast, unbalanced driving-loop and drain inductances have little effect, similar to the circuits without Kelvin-source connections. Based on the conclusions, Zhao et al. [19] investigated the current sharing performances of circuits with different power-source confluence points. The dynamic currents can be most balanced when the confluence point is located at the middle point of the paralleled chips. In [20], it is revealed that unbalanced power-source inductances can cause unbalanced source voltage potentials, inducing unbalanced gate currents, and then causing unbalanced gate-source voltages and drain currents. The above conclusions can be directly used to find current balancing methods or design circuit layouts. However, the parasitic mutual inductances induced by magnetic couples are neglected, which can reduce the effectiveness of the existing current balancing layouts and methods [21], [22]. To achieve more effective current balancing layouts and methods, it is first necessary to clearly analyze the effect degrees, effect directions, and mechanisms of the unbalanced parasitic mutual inductances. In [21], the current sharing performances of different layouts are analyzed considering the mutual inductances between the drain and source branches. In [22], all the parasitic mutual inductances are considered. However, the mutual inductances between branches of different MOSFETs are assumed equal, and the paralleled dynamic currents are assumed balanced, to obtain the criteria for balanced dynamic currents. The influences of the unbalanced mutual inductances have not been proved directly. The effect degrees of the unbalanced parasitic self-inductance and mutual inductance have not been compared and analyzed. The mechanisms by which the unbalanced parasitic mutual inductances cause unbalanced dynamic currents and the effect directions are also unclear. Moreover, the common values of the circuit parameters also influence the current sharing performance, which has not been investigated.

To address the above issues and provide more guidance for the current balancing design, this article further investigates the dynamic current sharing mechanisms under parasitic mutual inductances. The works and contributions of this article are as follows.

1) A dynamic current sharing model is established, which can reflect all the influences of the circuit parameters. Compared to the existing models, the presented model considers all the mutual inductances, decouples the influences of various unbalanced parameters, and clearly reflects their effect degrees, effect directions and mechanisms. Besides, the feedback effect induced from $\Delta i_{\rm d}$

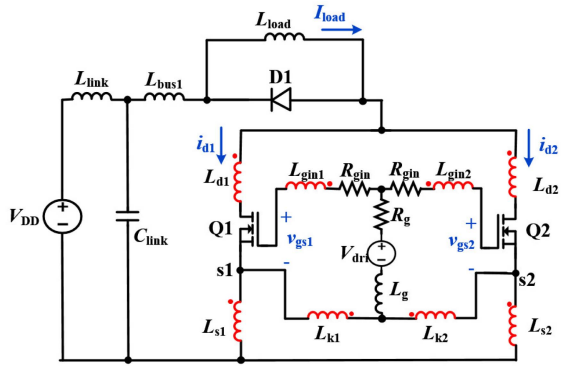

Fig. 1. Circuit model with two paralleled SiC MOSFETs.

through the common parameters M_{pg}, M_{pk}, M_{ds}, and L_s are clearly revealed, so that the influences and mechanisms of the common parameters can be clearly analyzed. Moreover, the presented model provides an effective tool for current sharing analysis and design considering the parasitic mutual inductances.

2) Based on this model, the effect degrees of the parasitic mutual inductances are analyzed. The current sharing mechanisms and effect directions under the unbalanced mutual inductances are concluded. Compared to existing research, the influences of the unbalanced mutual inductances are investigated for the first time. The conclusions can provide more specific and explicit theoretical guidance for PCB/DBC layout design.
3) Based on this model, the influences of the common parameters are investigated for the first time, which can guide the investigations of current balancing methods.
4) To prove the contributions of this article in the current sharing design, the model and conclusions are used to analyze the current sharing performance of an actual layout, and the layout optimizing methods are discussed. New current sharing methods are also discussed based on the influences of the common parameters. These contents can guide future research on layout optimization and current sharing methods using the theories of this article.

The rest of this article is organized as follows. In Section II, the current sharing model considering the parasitic mutual inductances is established to provide the analysis tool. The influence mechanisms and effect degrees of the unbalanced mutual inductances are analyzed in Section III based on this model. The influences of the common parameters are investigated as well. In Section IV, experiments are conducted to verify the conclusions. In Section V, the applications of the model and conclusions into practical current sharing design are discussed. Finally, Section VI concludes this article.

II. Dynamic Current Sharing Model

A dynamic current sharing model considering all the parasitic parameters is established first in this Section. The typical DPT circuit model with two paralleled SiC MOSFETs is shown in Fig. 1. The meanings of each circuit component are shown in Table I. The dc link capacitors C_{link} can also be replaced by an *RC* branch or a composite structure of *C* and

TABLE I
Meanings of Each Circuit Component

Symbols	Implications
V_{DD}	DC bus voltage
V_{dri}	Driving voltage
D1	Freewheeling diode
Q1, Q2	Paralleled MOSFETs
C_{link}	DC-link bulk capacitance
R_g	External gate resistance
L_{link}	Parasitic bus inductance outside dc capacitors
L_{bus1}	Parasitic bus inductance inside dc capacitors
L_{load}	Load inductance
L_g	Gate inductance outside the paralleled gate branches
L_{d1}, L_{d2}	MOSFETs paralleled drain parasitic inductances
L_{s1}, L_{s2}	MOSFETs paralleled power-source parasitic inductances
L_{gin1}, L_{gin2}	MOSFETs paralleled gate parasitic inductances
R_{gin1}, R_{gin2}	Internal gate resistances
L_{k1}, L_{k2}	MOSFETs paralleled drive-source parasitic inductances

RC branches. The self-inductance and mutual inductance of the branches close to the MOSFETs are equivalent to the paralleled branches. The self-inductances are depicted by L_{d1}, L_{d2}, L_{s1}, L_{s2}, L_{gin1}, L_{gin2}, L_{k1}, and L_{k2}. The mutual inductances between them are defined as follows: M_{dmgn} ($m = 1, 2$, $n = 1, 2$) is the drain-gate mutual inductance between the m_{th} drain branch and the n_{th} gate branch. M_{smgn}, M_{dmkn}, M_{smkn}, M_{dmsn}, and M_{gmkn} have similar definitions. M_{d1d2} is the mutual inductance between the paralleled drain branches. M_{s1s2}, M_{g1g2}, and M_{k1k2} are the mutual inductances between the paralleled power-source, gate, and drive-source branches, respectively. The positive directions of the magnetic couplings are defined as the red dots in Fig. 1. When the currents on two branches are positive, if the magnetic flux links strengthen each other, the mutual inductance value is positive. If the magnetic flux links cancel each other, the mutual inductance value is negative. For the busbar and external drive branches that are far enough away, their magnetic couplings with the paralleled branches can be neglected, and their line inductances are defined as L_{ink}, L_{bus1}, and L_g. The following assumptions and equivalences can be made during the current commutation periods.

1) The MOSFETs work in the saturation region. The MOSFET channels can be equivalent to the current sources i_{ch1} and i_{ch2}, controlled by the gate-source voltages v_{gs1} and v_{gs2}, which can be expressed as

$$\begin{cases} i_{ch1} = g_m(v_{gs1} - V_{th1}) \\ i_{ch2} = g_m(v_{gs2} - V_{th2}) \end{cases}. \tag{1}$$

Then, the circuit model can be equivalent to Fig. 2(a).
2) As for the power loop, during the current commutating periods, the drain-source voltages v_{ds1} and v_{ds2} are mainly borne by the drain-gate capacitances C_{dg}. The series connected gate-source capacitances C_{gs} can be considered a short circuit. As for the driving loop, v_{gs1} and v_{gs2} can be expressed as

$$\begin{cases} v_{gs1} = \frac{1}{C_{iss}} \int \left(i_{g1} + C_{dg} \frac{dv_{ds1}}{dt}\right) dt \\ v_{gs2} = \frac{1}{C_{iss}} \int \left(i_{g2} + C_{dg} \frac{dv_{ds2}}{dt}\right) dt \end{cases} \tag{2}$$

where $C_{iss} = C_{dg} + C_{gs}$. The change of v_{gs} is caused by the charge and discharge of C_{iss} by the gate currents i_g.

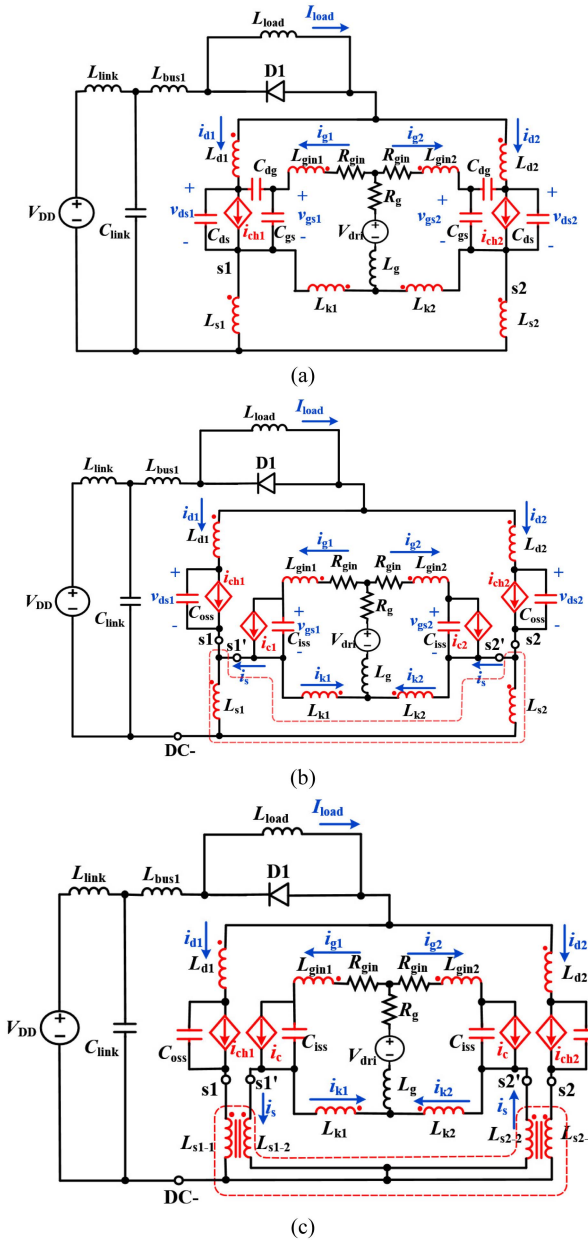

Fig. 2. Equivalent dynamic circuit models. (a) Circuit with equivalent MOSFET models. (b) Circuit with simplified MOSFET models. (c) Circuit with equivalent power-source full-coupled inductors.

Moreover, the effects of $C_{\rm dg}{\rm d}v_{\rm ds1}/{\rm d}t$ and $C_{\rm dg}{\rm d}v_{\rm ds2}/{\rm d}t$ are equivalent to the current sources $i_{\rm c1}$ and $i_{\rm c2}$ controlled by $v_{\rm ds1}$ and $v_{\rm ds2}$, which can be expressed as

$$\begin{cases} i_{\rm c1} = -C_{\rm dg}{\rm d}v_{\rm ds1}/{\rm d}t \\ i_{\rm c2} = -C_{\rm dg}{\rm d}v_{\rm ds2}/{\rm d}t \end{cases}. \tag{3}$$

Then, the circuit model can be equivalent to Fig. 2(b), where $C_{\rm oss} = C_{\rm ds} + C_{\rm dg}$.

3) Suppose that $v_{\rm ds1} = v_{\rm ds2}$ during the current commutating periods. Then

$$i_{\rm c1} = i_{\rm c2} = i_{\rm c} \tag{4}$$

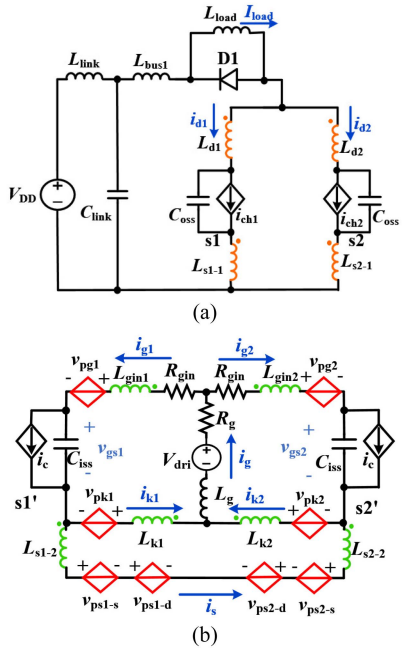

Fig. 3. Simplified dynamic circuit model. (a) Power circuit. (b) Driving circuit.

and the currents on the two $C_{\rm oss}$ are the same. Then

$$\Delta i_{\rm d} = \Delta i_{\rm ch} \tag{5}$$

where

$$\begin{cases} \Delta i_{\rm d} = i_{\rm d1} - i_{\rm d2} \\ \Delta i_{\rm ch} = i_{\rm ch1} - i_{\rm ch2} \end{cases}. \tag{6}$$

According to (1), (5), and (6), it can be further obtained that

$$\Delta i_{\rm d} = g_{\rm m}(\Delta v_{\rm gs} - \Delta V_{\rm th}). \tag{7}$$

4) The circuit inside the red frame line in Fig. 2(b) has five external connection points: s1, s1', s2, s2', and dc-. Taking dc- as the zero potential point, the potentials of other points can be expressed as (8) shown at the bottom of the next page, Based on (8), the circuit model can be equivalent to Fig. 2(c), where $L_{\rm s1}$ and $L_{\rm s2}$ are equivalent to two full-coupled inductors. Then, the power loop and driving loop can be separated. The values of $L_{\rm s1\text{-}1}$ and $L_{\rm s1\text{-}2}$ are both equal to $L_{\rm s1}$. The magnetic couplings of $L_{\rm s1\text{-}1}$ or $L_{\rm s1\text{-}2}$ with other branches are the same as that of $L_{\rm s1}$. The same relationships go for $L_{\rm s2\text{-}1}$, $L_{\rm s2\text{-}2}$, and $L_{\rm s2}$. The voltage potentials of s1, s1', s2, and s2' still satisfy (8).

5) Compared with the currents in the power loop, the currents in the driving loop are much smaller. Then, the induced voltages in the power loop generated by the driving-loop currents through the mutual inductances are ignored. The power loop in Fig. 2(c) can be simplified into Fig. 3(a), where there are mutual inductances between $L_{\rm d1}$, $L_{\rm d2}$, $L_{\rm s1\text{-}1}$, and $L_{\rm s2\text{-}1}$. The induced voltages in the driving loop generated by $i_{\rm d1}$ and $i_{\rm d2}$ through the mutual inductances are equivalent to controlled voltage sources. Then, the

driving loop in Fig. 2(c) is simplified into Fig. 3(b), where there are mutual inductances between L_{gin1}, L_{gin2}, L_{k1}, L_{k2}, $L_{\mathrm{s1\text{-}2}}$, and $L_{\mathrm{s2\text{-}2}}$. v_{pg1} and v_{pg2} represent the induced voltages in the two gate branches through the power-gate mutual inductances. v_{pk1} and v_{pk2} represent that in the drive source branches. $v_{\mathrm{ps1\text{-}d}}$ and $v_{\mathrm{ps2\text{-}d}}$ represent the induced voltages on $L_{\mathrm{s1\text{-}2}}$ and $L_{\mathrm{s2\text{-}2}}$ through the drain-source mutual inductances. $v_{\mathrm{ps1\text{-}s}}$ and $v_{\mathrm{ps2\text{-}s}}$ represent the induced voltages on $L_{\mathrm{s1\text{-}2}}$ and $L_{\mathrm{s2\text{-}2}}$ through the two full-coupled inductors. The controlled voltages can be expressed as

$$\begin{cases} \begin{bmatrix} v_{\mathrm{pg1}} \\ v_{\mathrm{pg2}} \end{bmatrix} = \begin{bmatrix} M_{\mathrm{p1g1}} & M_{\mathrm{p2g1}} \\ M_{\mathrm{p1g2}} & M_{\mathrm{p2g2}} \end{bmatrix} \begin{bmatrix} \frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} \end{bmatrix} \\ \begin{bmatrix} v_{\mathrm{pk1}} \\ v_{\mathrm{pk2}} \end{bmatrix} = \begin{bmatrix} M_{\mathrm{p1k1}} & M_{\mathrm{p2k1}} \\ M_{\mathrm{p1k2}} & M_{\mathrm{p2k2}} \end{bmatrix} \begin{bmatrix} \frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} \end{bmatrix} \\ \begin{bmatrix} v_{\mathrm{ps1-d}} \\ v_{\mathrm{ps2-d}} \end{bmatrix} = \begin{bmatrix} M_{\mathrm{d1s1}} & M_{\mathrm{d2s1}} \\ M_{\mathrm{d1s2}} & M_{\mathrm{d2s2}} \end{bmatrix} \begin{bmatrix} \frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} \end{bmatrix} \\ \begin{bmatrix} v_{\mathrm{ps1-s}} \\ v_{\mathrm{ps2-s}} \end{bmatrix} = \begin{bmatrix} L_{\mathrm{s1}} & M_{\mathrm{s1s2}} \\ M_{\mathrm{s1s2}} & L_{\mathrm{s2}} \end{bmatrix} \begin{bmatrix} \frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} \end{bmatrix} \end{cases} \tag{9}$$

where M_{pmgn} ($m, n = 1, 2$) represents the mutual inductances between the m_{th} power branch and the n_{th} gate branch, which can be expressed as

$$\begin{cases} M_{\mathrm{p1g1}} = M_{\mathrm{d1g1}} + M_{\mathrm{s1g1}} \\ M_{\mathrm{p2g1}} = M_{\mathrm{d2g1}} + M_{\mathrm{s2g1}} \\ M_{\mathrm{p1g2}} = M_{\mathrm{d1g2}} + M_{\mathrm{s1g2}} \\ M_{\mathrm{p2g2}} = M_{\mathrm{d2g2}} + M_{\mathrm{s2g2}} \end{cases}. \tag{10}$$

M_{pmkn} represents the mutual inductances between the m_{th} power branch and the n_{th} drive-source branch, which can be expressed as

$$\begin{cases} M_{\mathrm{p1k1}} = M_{\mathrm{d1k1}} + M_{\mathrm{s1k1}} \\ M_{\mathrm{p2k1}} = M_{\mathrm{d2k1}} + M_{\mathrm{s2k1}} \\ M_{\mathrm{p1k2}} = M_{\mathrm{d1k2}} + M_{\mathrm{s1k2}} \\ M_{\mathrm{p2k2}} = M_{\mathrm{d2k2}} + M_{\mathrm{s2k2}} \end{cases}. \tag{11}$$

It can be concluded from (7) that Δi_{d} is caused by Δv_{gs} and ΔV_{th}. So, the driving circuit in Fig. 3(b) should be first analyzed to analyze Δi_{d}. The driving circuit model contains all the influences of the power circuit. Based on the driving circuit model, the mathematical model is established.

A. Mathematical Model of Controlled Voltage Sources

For any paralleled parameters x_1 and x_2, the differential parameter Δx and the common parameter x are defined in this article as

$$\begin{cases} \Delta x = x_1 - x_2 \\ x = (x_1 + x_2)/2 \end{cases}. \tag{12}$$

Then, according to (9) and (12), the differential and common controlled voltages can be derived as

$$\begin{cases} \Delta v_{\mathrm{pg}} = v_{\mathrm{pg1}} - v_{\mathrm{pg2}} = M_{\mathrm{pg}} \frac{\mathrm{d}\Delta i_{\mathrm{d}}}{\mathrm{d}t} + \Delta M_{\mathrm{pg}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \\ v_{\mathrm{pg}} = \frac{v_{\mathrm{pg1}} + v_{\mathrm{pg2}}}{2} = M'_{\mathrm{pg}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \end{cases} \tag{13}$$

$$\begin{cases} \Delta v_{\mathrm{pk}} = v_{\mathrm{pk1}} - v_{\mathrm{pk2}} = M_{\mathrm{pk}} \frac{\mathrm{d}\Delta i_{\mathrm{d}}}{\mathrm{d}t} + \Delta M_{\mathrm{pk}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \\ v_{\mathrm{pk}} = \frac{v_{\mathrm{pk1}} + v_{\mathrm{pk2}}}{2} = M'_{\mathrm{pk}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \end{cases} \tag{14}$$

and

$$\begin{cases} \Delta v_{\mathrm{ps-d}} = v_{\mathrm{ps1-d}} - v_{\mathrm{ps2-d}} = M_{\mathrm{ds}} \frac{\mathrm{d}\Delta i_{\mathrm{d}}}{\mathrm{d}t} + \Delta M_{\mathrm{ds}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \\ \Delta v_{\mathrm{ps-s}} = v_{\mathrm{ps1-s}} - v_{\mathrm{ps2-s}} = L_{\mathrm{s}} \frac{\mathrm{d}\Delta i_{\mathrm{d}}}{\mathrm{d}t} + \Delta L_{\mathrm{s}} \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} \end{cases} \tag{15}$$

where M_{pg}, M_{pg}', M_{pk}, M_{pk}', M_{ds}, and L_{s} are defined as the common inductances between the paralleled branches, and ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, and ΔL_{s} are defined as the differential inductances, which can be expressed as (A1)–(A8).

It is concluded in [20] that ΔL_{s} can cause the voltage difference $\Delta v_{\mathrm{ps\text{-}s}}$ as shown in (15), inducing Δv_{gs}. However, (13)–(15) indicate that differential mutual inductances ΔM_{pg}, ΔM_{pk}, and ΔM_{ds} can also cause voltage differences Δv_{pg}, Δv_{pk}, and $\Delta v_{\mathrm{ps\text{-}d}}$, inducing Δv_{gs}. Moreover, Δi_{d} can in turn cause unbalanced controlled voltages through the common inductances M_{pg}, M_{pk}, M_{ds}, and L_{s}, introducing a feedback effect.

B. Mathematical Model of Driving Circuit

The equations of the circuit in Fig. 3(b) can be written as (A9). Solving (12) and the Laplace transform of (A9), the equation of ΔV_{gs} can be derived as

$$\begin{aligned} \Delta V_{\mathrm{gs}} = {} & G_{\mathrm{g}} \Delta V_{\mathrm{pg}} + G_{\mathrm{k}} \Delta V_{\mathrm{pk}} + G_{\mathrm{s}} (\Delta V_{\mathrm{ps-d}} + \Delta V_{\mathrm{ps-s}}) \\ & + \Delta G_{\mathrm{gs}} \left(-V_{\mathrm{pg}} + V_{\mathrm{pk}} + \frac{V_{\mathrm{dri}}}{s} + \frac{I_{\mathrm{c}}}{sC_{\mathrm{iss}}} \right) \end{aligned} \tag{16}$$

where ΔV_{gs} is the Laplace transform of Δv_{gs}. ΔV_{pg}, ΔV_{pk}, $\Delta V_{\mathrm{ps\text{-}d}}$, $\Delta V_{\mathrm{ps\text{-}s}}$, V_{pg}, and V_{pk} are the Laplace transforms of the voltage sources. I_{c} is the Laplace transform of i_{c}. V_{dri} is the driving voltage. G_{g}, G_{k}, G_{s}, and ΔG_{gs} are the transfer functions and are given by (A10)–(A12).

According to (16), ΔV_{gs} can be caused by the unbalanced controlled voltages. Moreover, ΔV_{gs} can also be caused by ΔG_{gs}, which is induced by the unbalanced parameters in the driving circuit.

C. Dynamic Current Sharing Model

The Laplace transforms of (7), (13)–(15), and (16) can be expressed in block diagram form and shown in Fig. 4. ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_{s}, ΔG_{gs}, and ΔV_{th} are the uneven factors, and are marked in red. Considering the influences of each unbalanced parameter separately, the model in Fig. 4 can be divided into the five parts shown in Fig. 5(a)–(e), where the structure of the

$$\begin{cases} v_{\mathrm{s1}} = v_{\mathrm{s1}}' = L_{\mathrm{s1}} \left(\frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} + \frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \right) + M_{\mathrm{d1s1}} \frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} + M_{\mathrm{d2s1}} \frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} + M_{\mathrm{s1s2}} \left(\frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} - \frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \right) + M_{\mathrm{s1g1}} \frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} + M_{\mathrm{s1g2}} \frac{\mathrm{d}i_{g2}}{\mathrm{d}t} - M_{\mathrm{s1k1}} \frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} - M_{\mathrm{s1k2}} \frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} \\ v_{\mathrm{s2}} = v_{\mathrm{s2}}' = L_{\mathrm{s2}} \left(\frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} - \frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \right) + M_{\mathrm{d1s2}} \frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} + M_{\mathrm{d2s2}} \frac{\mathrm{d}i_{\mathrm{d2}}}{\mathrm{d}t} + M_{\mathrm{s1s2}} \left(\frac{\mathrm{d}i_{\mathrm{d1}}}{\mathrm{d}t} + \frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \right) + M_{\mathrm{s2g1}} \frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} + M_{\mathrm{s2g2}} \frac{\mathrm{d}i_{g2}}{\mathrm{d}t} - M_{\mathrm{s2k1}} \frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} - M_{\mathrm{s2k2}} \frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} \end{cases} \tag{8}$$

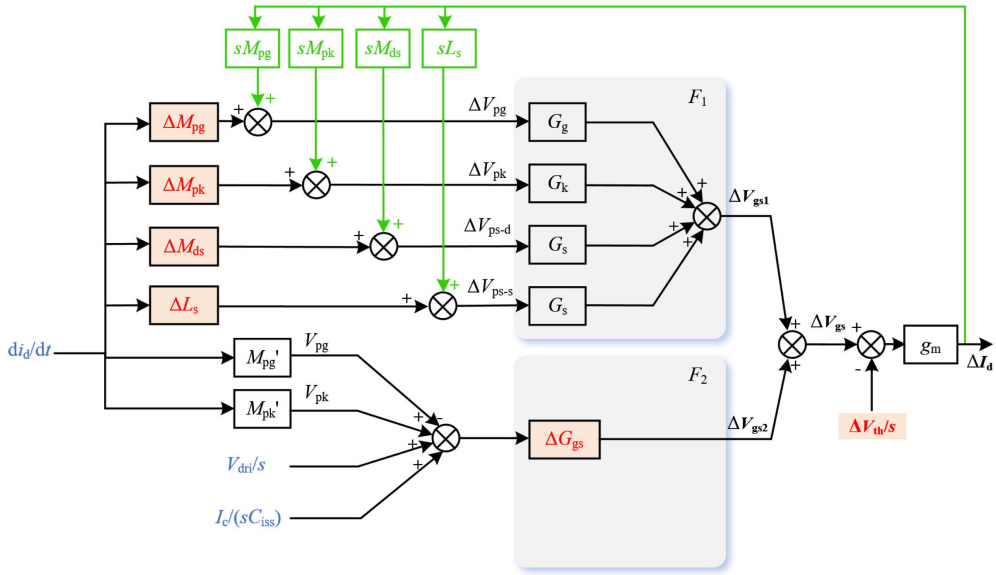

Fig. 4. Dynamic current sharing model.

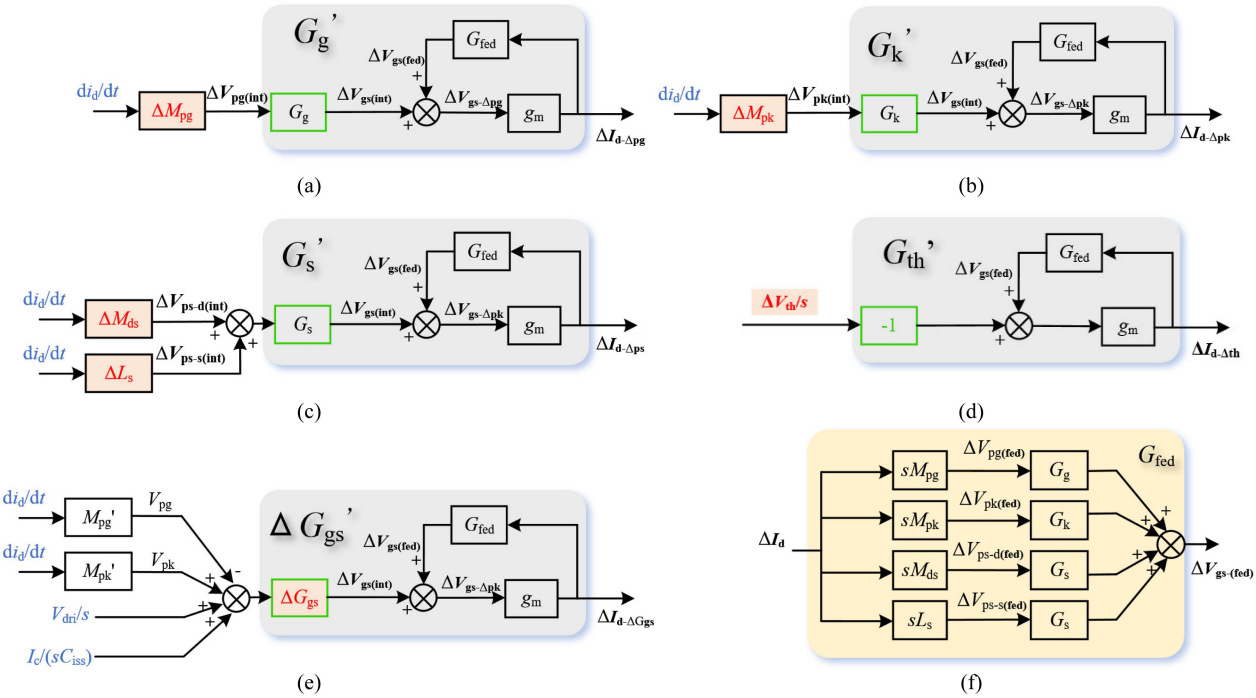

Fig. 5. Separated dynamic current sharing models under (a) $\Delta M_{\rm pg}$, (b) $\Delta M_{\rm pk}$, (c) $\Delta M_{\rm ds}$, $\Delta L_{\rm s}$, (d) $\Delta V_{\rm th}$, and (e) $\Delta G_{\rm gs}$. (f) Model of $G_{\rm fed}$.

feedback function $G_{\rm fed}$ is shown in Fig. 5(f). Fig. 5(a)–(c) shows that $\Delta M_{\rm pg}$, $\Delta M_{\rm pk}$, $\Delta M_{\rm ds,}$ and $\Delta L_{\rm s}$ can induce the differential voltages $\Delta v_{\rm pg(int)}$, $\Delta v_{\rm pk(int)}$, $\Delta v_{\rm ps\text{-}d(int)}$, and $\Delta v_{\rm ps\text{-}s(int)}$, then inducing $\Delta v_{\rm gs(int)}$, causing $\Delta i_{\rm d}$. Fig. 5(d) shows that $\Delta V_{\rm th}$ can induce $\Delta i_{\rm d}$ directly. When the parameters of the driving circuit are unbalanced, the nonzero $\Delta G_{\rm gs}$ can also induce $\Delta v_{\rm gs(int)}$, causing $\Delta i_{\rm d}$, as shown in Fig. 5(e). As shown in Fig. 5(f), $\Delta i_{\rm d}$ in turn introduces feedback unbalanced controlled voltages by $M_{\rm pg}$, $M_{\rm pk}$, $M_{\rm ds}$, and $L_{\rm s}$, causing feedback $\Delta v_{\rm gs(fed)}$.

Moreover, the equation of $\Delta I_{\rm d}$ can be derived from Fig. 5 as (17) shown at the bottom of this page, where $G_{\rm g}$', $G_{\rm k}$', $G_{\rm s}$', $G_{\rm th}$', and $\Delta G_{\rm gs}$' are the closed-loop transfer functions of the gray boxes in Fig. 5(a)–(e), and are expressed as

$$\Delta I_{\rm d} = G_{\rm g}'\mathcal{L}\left[\Delta M_{\rm pg}\frac{{\rm d}i_{\rm d}}{{\rm d}t}\right] + G_{\rm k}'\mathcal{L}\left[\Delta M_{\rm pk}\frac{{\rm d}i_{\rm d}}{{\rm d}t}\right] + G_{\rm s}'\left(\mathcal{L}\left[\Delta M_{\rm ds}\frac{{\rm d}i_{\rm d}}{{\rm d}t}\right] + \mathcal{L}\left[\Delta L_{\rm s}\frac{{\rm d}i_{\rm d}}{{\rm d}t}\right]\right) + G_{\rm th}'\frac{\Delta V_{\rm th}}{s}$$

$$+\Delta G'_{\rm gs}\left(-\mathcal{L}\left[M'_{\rm pg}\frac{{\rm d}i_{\rm d}}{{\rm d}t}\right]+\mathcal{L}\left[M'_{\rm pk}\frac{{\rm d}i_{\rm d}}{{\rm d}t}\right]+\frac{V_{\rm dri}}{s}+\frac{I_{\rm c}}{sC_{\rm iss}}\right) \tag{17}$$

$$\begin{cases} G'_{\rm g}=G_{\rm g}\cdot\frac{g_{\rm m}}{1-g_{\rm m}(sM_{\rm pg}G_{\rm g}+sM_{\rm pk}G_{\rm k}+sM_{\rm ds}G_{\rm s}+sL_{\rm s}G_{\rm s})} \\ G'_{\rm k}=G_{\rm k}\cdot\frac{g_{\rm m}}{1-g_{\rm m}(sM_{\rm pg}G_{\rm g}+sM_{\rm pk}G_{\rm k}+sM_{\rm ds}G_{\rm s}+sL_{\rm s}G_{\rm s})} \\ G'_{\rm s}=G_{\rm s}\cdot\frac{g_{\rm m}}{1-g_{\rm m}(sM_{\rm pg}G_{\rm g}+sM_{\rm pk}G_{\rm k}+sM_{\rm ds}G_{\rm s}+sL_{\rm s}G_{\rm s})} \\ G'_{\rm th}=-1\cdot\frac{g_{\rm m}}{1-g_{\rm m}(sM_{\rm pg}G_{\rm g}+sM_{\rm pk}G_{\rm k}+sM_{\rm ds}G_{\rm s}+sL_{\rm s}G_{\rm s})} \\ \Delta G'_{\rm gs}=\Delta G_{\rm gs}\cdot\frac{g_{\rm m}}{1-g_{\rm m}(sM_{\rm pg}G_{\rm g}+sM_{\rm pk}G_{\rm k}+sM_{\rm ds}G_{\rm s}+sL_{\rm s}G_{\rm s})} \end{cases} \tag{18}$$

The effect degrees of the unbalanced circuit parameters and the influences of the common parameters can be analyzed by the closed-loop transfer function gains.

III. Analysis of Current Sharing Mechanisms

The current sharing mechanisms are analyzed in this section based on the established model. It can be concluded from Fig. 5(a)–(e) that the effect degrees of $\Delta M_{\rm pg}$, $\Delta M_{\rm pk}$, $\Delta M_{\rm ds}$, $\Delta L_{\rm s}$, $\Delta V_{\rm th}$, and unbalanced driving parameters can be represented by the gains of $G_{\rm g}$', $G_{\rm k}$', $G_{\rm s}$', $G_{\rm th}$', and $\Delta G_{\rm gs}$', respectively. By comparing the transfer function gains, the effect degrees are compared. Moreover, the influences of the common parameters ($M_{\rm pg}$, $M_{\rm pk}$, $M_{\rm ds}$, $L_{\rm s}$ and the common parameters in the driving loop) are also investigated by analyzing the changes in the transfer function gains.

The parameter values of the test circuit board with symmetrical parameters are used, as shown in Table II. The MOSFET parameters are obtained from the datasheet. The parasitic inductances are obtained by Q3D simulations. The simulation model is shown in Appendix C. The negative inductance values are caused by the negative magnetic coupling between the two branches under positive currents. The calculated differential and common parameter values are shown in Table III, where the differential values are almost zero. Based on the balanced parameters, asymmetrical parameters are deliberately induced to investigate the influences of the different parameters.

A. Effect Degrees and Mechanisms of Differential Parameters

Analyzing the influences of the unbalanced driving inductances give

TABLE II
Parameter Values of the Test Circuit

Parameter	Value	Parameter	Value	Parameter	Value
$L_{\rm d1}$	52.0 nH	$M_{\rm g1g2}$	0.84 nH	$M_{\rm d1k1}$	1.90 nH
$L_{\rm d2}$	52.0 nH	$M_{\rm k1k2}$	2.67 nH	$M_{\rm d1k2}$	-0.42 nH
$L_{\rm s1}$	29.6 nH	$M_{\rm d1s1}$	-6.39 nH	$M_{\rm d2k1}$	-0.40 nH
$L_{\rm s2}$	29.6 nH	$M_{\rm d1s2}$	-2.52 nH	$M_{\rm d2k2}$	1.91 nH
$L_{\rm gin1}$	42.8 nH	$M_{\rm d2s1}$	-2.50 nH	$M_{\rm s1k1}$	-4.22 nH
$L_{\rm gin2}$	42.3 nH	$M_{\rm d2s2}$	-6.36 nH	$M_{\rm s1k2}$	0.57 nH
$L_{\rm k1}$	40.6 nH	$M_{\rm d1g1}$	1.39 nH	$M_{\rm s2k1}$	0.54 nH
$L_{\rm k2}$	40.7 nH	$M_{\rm d1g2}$	-0.33 nH	$M_{\rm s2k2}$	-4.24 nH
$M_{\rm g1k1}$	6.83 nH	$M_{\rm d2g1}$	-0.35 nH	$L_{\rm g}$	26.1 nH
$M_{\rm g1k2}$	0.92 nH	$M_{\rm d2g2}$	1.36 nH	$C_{\rm iss}$	2.98 nF
$M_{\rm g2k1}$	1.05 nH	$M_{\rm s1g1}$	-2.79 nH	$g_{\rm m}$	25 S
$M_{\rm g2k2}$	6.84 nH	$M_{\rm s1g2}$	0.41 nH	$R_{\rm gin}$	11.3 Ω
$M_{\rm d1d2}$	16.5 nH	$M_{\rm s2g1}$	0.44 nH	$R_{\rm g}$	20 Ω
$M_{\rm s1s2}$	4.62 nH	$M_{\rm s2g2}$	-2.75 nH		

TABLE III
Common and Differential Parameter Values

Parameter	$M_{\rm pg}$	$M_{\rm pk}$	$M_{\rm ds}$	$L_{\rm s}$	$M_{\rm pg}$'
Value/nH	−1.48	−2.47	−3.87	25.0	−1.31
Parameter	$M_{\rm pk}$'	$\Delta M_{\rm pg}$	$\Delta M_{\rm pk}$	$\Delta M_{\rm ds}$	$\Delta L_{\rm s}$
Value/nH	−2.18	0	0	0.01	0

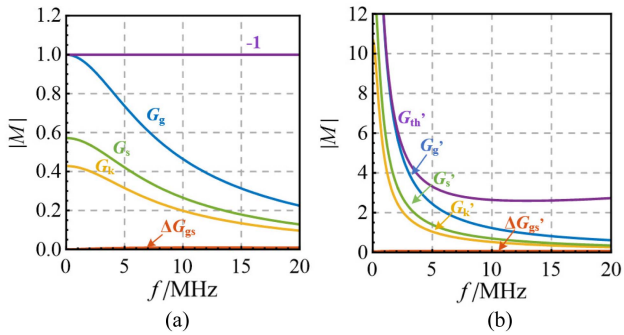

Fig. 6. Magnitude-frequency plots of (a) $G_{\rm g}$, $G_{\rm k}$, $G_{\rm s}$, and $\Delta G_{\rm gs}$ and (b) $G_{\rm g}$', $G_{\rm k}$', $G_{\rm s}$', $G_{\rm th}$', and $\Delta G_{\rm gs}$'.

$$\begin{cases} \Delta L_{\rm gin}=L_{\rm gin1}-L_{\rm gin2}=10\ {\rm nH} \\ \Delta L_k=L_{\rm k1}-L_{\rm k2}=10\ {\rm nH} \\ \Delta M_{gk}=M_{g1k1}-M_{g2k2}=-1.6\ {\rm nH} \end{cases} \tag{19}$$

Then, the equations of $G_{\rm g}$, $G_{\rm k}$, $G_{\rm s}$, $\Delta G_{\rm gs}$, and $G_{\rm fed}$ are calculated to the following equation: (20) shown at the bottom of this page, where $G_{\rm fed}$ induces a negative feedback for ${\rm d}\Delta i_{\rm d}/{\rm d}t$.

Then, the amplitude-frequency curves of $G_{\rm g}$, $G_{\rm k}$, $G_{\rm s}$, and $\Delta G_{\rm gs}$ are shown in Fig. 6(a) and the curves of the closed-loop

$$\begin{cases} G_{\rm g}=\dfrac{-(1.0+1.529\times10^{-7}s+3.670\times10^{-16}s^2)}{1.0+1.865\times10^{-7}s+5.665\times10^{-15}s^2+3.535\times10^{-23}s^3+5.519\times10^{-32}s^4} \\ G_{\rm k}=\dfrac{0.428+6.544\times10^{-8}s+1.571\times10^{-16}s^2}{1.0+1.865\times10^{-7}s+5.665\times10^{-15}s^2+3.535\times10^{-23}s^3+5.519\times10^{-32}s^4} \\ G_{\rm s}=\dfrac{-(0.572+8.743\times10^{-8}s+2.099\times10^{-16}s^2)}{1.0+1.865\times10^{-7}s+5.665\times10^{-15}s^2+3.535\times10^{-23}s^3+5.519\times10^{-32}s^4} \\ \Delta G_{\rm gs}=\dfrac{-5.079\times10^{-17}s^2}{1.0+1.865\times10^{-7}s+5.665\times10^{-15}s^2+3.535\times10^{-23}s^3+5.519\times10^{-32}s^4} \\ G_{\rm fed}=\dfrac{-s(1.164\times10^{-8}+1.780\times10^{-15}s+4.272\times10^{-24}s^2)}{1.0+1.865\times10^{-7}s+5.665\times10^{-15}s^2+3.535\times10^{-23}s^3+5.519\times10^{-32}s^4} \end{cases} \tag{20}$$

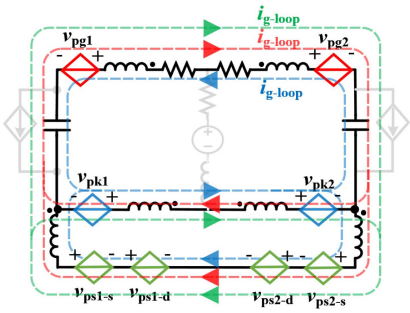

Fig. 7. Loop currents caused by unbalanced induced voltages during turn-ON period when differential inductance values are positive. Red: Loop current caused by Δv_{pg}. Blue: Loop current caused by Δv_{pk}. Green: Loop current caused by $\Delta v_{ps\text{-}s}$ or $\Delta v_{ps\text{-}d}$.

transfer functions G_g', G_k', G_s', G_{th}', and ΔG_{gs}' are shown in Fig. 6(b). The gains of G_g, G_k, G_s, and -1 are much larger than that of ΔG_{gs}, making the gains of G_g', G_k', G_s', and G_{th}' much larger than ΔG_{gs}'. According to Fig. 5(a)–(e), it can be concluded that the main factors causing unbalanced dynamic currents are ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_s, and ΔV_{th}, whereas the influences of the unbalanced driving-loop inductances can be neglected. Moreover, According to Fig. 6(a) and (b), the effect degrees can be ranked as: $\Delta V_{th} > \Delta M_{pg} > \Delta L_s$ and $\Delta M_{ds} > \Delta M_{pk}$, which can be explained by its physical mechanisms: 1) ΔV_{th} directly causes Δi_d through g_m as depicted in (7). But Δv_{pg}, Δv_{pk}, $\Delta v_{ps\text{-}s}$ and $\Delta v_{ps\text{-}d}$ induced by ΔM_{pg}, ΔM_{pk}, ΔL_s and ΔM_{ds} need to produce a Δi_g through the circuit impedances first, then Δv_{gs} and Δi_d are produced. So, under the same differential voltage values, ΔV_{th} has the largest effect. 2) Fig. 7 shows the loop currents caused by the unbalanced induced voltages, where the red current is caused by Δv_{pg}, the blue current is caused by Δv_{pk} and the green current is caused by $\Delta v_{ps\text{-}s}$ or $\Delta v_{ps\text{-}d}$. As for the influences of the unbalanced parasitic inductances, Δv_{pg} directly works in the gate branches; the induced Δi_g and the corresponding Δv_{gs} are the largest. Δv_{ps} and Δv_{pk} work in the power-source and drive-source brances. Due to the shunting effect of the additional branches paralleled with gate branches as shown in Fig. 7, Δi_g and the corresponding Δv_{gs} in the gate branches are smaller. Moreover, since the parasitic inductances in the drive-source branches are larger than that in the power-source branches, currents under Δv_{ps} flow more easily into the gate branches than under Δv_{pk}, making Δi_g larger. So, the effect degrees of the differential inductance values are ranked as $\Delta M_{pg} > \Delta L_s$ and $\Delta M_{ds} > \Delta M_{pk}$. Moreover, the following conclusions can be drawn.

1) As shown in Fig. 5(a)–(d), when the circuit parameters, load current I_{load} and switching time are constant, Δi_d is proportional to ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_s, and ΔV_{th}.
2) Equation (20) shows that the steady-state gain of G_g is negative. Then, it can be concluded from Fig. 5(a) that the sign of $\Delta i_{d\text{-}\Delta pg}$ is opposite to that of di_d/dt when $\Delta M_{pg} > 0$. It can be explained by Fig. 7 that during the turn-ON period, $v_{pg1} > v_{pg2}$ induces the red loop current, making $v_{gs1} < v_{gs2}$ and $i_{d1} < i_{d2}$. The relationships are reversed during the turn-OFF period. It means that the MOSFET with larger power-gate mutual inductances tends to carry lower turn-ON and higher turn-OFF currents.
3) The steady-state gain of G_k is positive, as shown in (20). It can be concluded from Fig. 5(b) that the signs of $\Delta i_{d\text{-}\Delta pk}$ and di_d/dt are the same when $\Delta M_{pk} > 0$. During the turn-ON period, the loop current induced by the larger v_{pk1} and smaller v_{pk2} is shown by the blue path in Fig. 7, making $v_{gs1} > v_{gs2}$ and $i_{d1} > i_{d2}$. It means that the MOSFET with larger power-drive source mutual inductances tends to bear higher turn-ON and lower turn-OFF currents.
4) The steady-state gain of G_s is also negative, as shown in (20). Then, it can be concluded from Fig. 5(c) that the sign of $\Delta i_{d\text{-}\Delta ps}$ is opposite to that of di_d/dt when $\Delta M_{ds} > 0$. During the turn-ON period, the loop current caused by the positive ΔM_{ds} is shown by the green path in Fig. 7, making $v_{gs1} < v_{gs2}$. During the turn-OFF period, $v_{gs1} > v_{gs2}$. It reveals that the MOSFET with larger drain-source mutual inductances tend to bear lower turn-ON and higher turn-OFF currents. The mechanisms of ΔL_s are the same.
5) It can be concluded from Fig. 5(d) that $\Delta i_{d\text{-}\Delta th} < 0$ when $\Delta V_{th} > 0$, which means that the MOSFET with larger V_{th} tends to carry lower turn-ON and turn-OFF currents, which can be directly explained by (7). Moreover, when $\Delta V_{th} > 0$, $\Delta i_d < 0$, positive $\Delta v_{gs(fed)}$ will be induced by the negative feedback effect G_{fed}, reducing the current difference.

Table IV summarizes the relationships between the signs of the differential parameter values and the induced Δi_d. In Table IV, "+" represents "positive," whereas "-" represents "negative." For example, when ΔM_{pg} is "+, positive", then the caused Δi_d is "-, negative" during turn-ON periods, and is "+, positive" during turn-OFF periods.

B. Influences of Common Parameters

Fig. 5(a)–(d) shows that the gains of G_g', G_k', and G_s' are determined by the gains of G_g, G_k, and G_s, respectively, and are influenced by the feedback function G_{fed}. The gain of G_{th}' is only influenced by G_{fed}. Increased $|G_g|$, $|G_k|$, and $|G_s|$ can cause increased $|G_g'|$, $|G_k'|$, and $|G_s'|$, respectively. Decreased $|G_{fed}|$ can cause increased $|G_g'|$, $|G_k'|$, $|G_s'|$, and $|G_{th}'|$. The common parameters can influence the gains of G_g, G_k, G_s, and G_{fed}, then influence the gains of G_g', G_k', G_s', and G_{th}', and change the effect degrees of the unbalanced parameters. So, the influences of the common parameters can be analyzed by the changes in the gains of the transfer functions.

1) Influences of M_{gk}: To investigate the influences of gate-drive source mutual inductance, the transfer function gains under different values of M_{gk} are calculated as shown in Fig. 8, where $M_{gk} = (M_{g1k1} + M_{g2k2})/2$. As shown in Fig. 8(a), $|G_g|$ is almost unchanged under different M_{gk}. It can be explained that M_{gk} has little influence on the total impedance of the red current path in Fig. 7. Then, the gain of the transfer function G_g is not changed. As shown in Fig. 8(b), the larger M_{gk}, the larger $|G_k|$. It can be explained that when M_{gk} is increased, the blue current in Fig. 7 will flow more into the gate branches, inducing larger Δv_{gs}. As shown in Fig. 8(c), the larger M_{gk}, the lower $|G_s|$. This is because

TABLE IV
RELATIONSHIPS BETWEEN SIGNS OF DIFFERENTIAL PARAMETERS AND INDUCED ΔI_D

Parameter	ΔM_{pg}		ΔM_{pk}		ΔM_{ds}	
Sign	+	-	+	-	+	-
Sign of Δi_d (turn ON)	-	+	+	-	-	+
Sign of Δi_d (turn OFF)	+	-	-	+	+	-
Parameter	ΔL_s		ΔV_{th}			
Sign	+	-	+	-		
Sign of Δi_d (turn ON)	-	+	-	+		
Sign of Δi_d (turn OFF)	+	-	-	+		

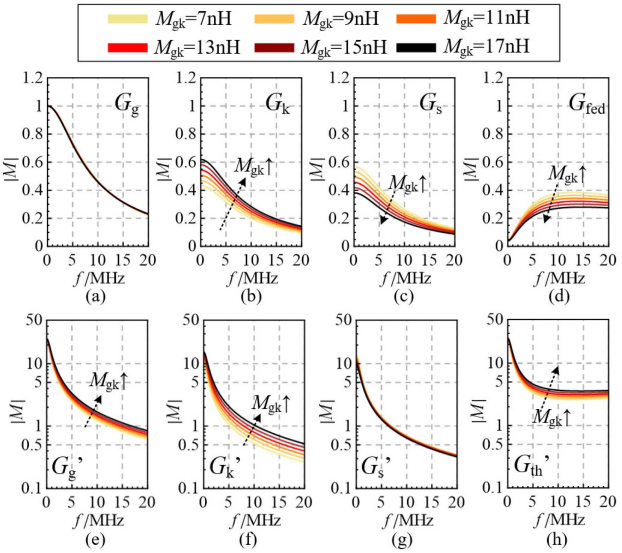

Fig. 8. Magnitude-frequency plots of transfer functions (a) G_g, (b) G_k, (c) G_s, (d) G_{fed}, (e) G_g', (f) G_k', (g) G_s' and (h) G_{th}' under different values of M_{gk}.

the impedance of the green current path in Fig. 7 is larger under larger M_{gk}, then inducing smaller Δv_{gs}. As shown in Fig. 8(d), $|G_{fed}|$ decreases with the increase of M_{gk}, which is caused by the changing of $|G_k|$ and $|G_s|$.

Under the decreased $|G_{fed}|$, $|G_g'|$, and $|G_{th}'|$ slightly increase under larger M_{gk}, as shown in Fig. 8(e) and (h). $|G_k'|$ is increased more, as shown in Fig. 8(f), because the effects of the increased $|G_k|$ and decreased $|G_{fed}|$ prompt each other. As shown in Fig. 8(g), $|G_s'|$ is unchanged because the effects of the decreased $|G_s|$ and decreased $|G_{fed}|$ cancel each other out. It can be concluded that when increasing M_{gk}, such as reducing the spacing between the gate and drive source branches, $|\Delta i_d|$ caused by ΔM_{pg} and ΔV_{th} will be slightly increased, and $|\Delta i_d|$ caused by ΔM_{pk} will be largely increased, whereas $|\Delta i_d|$ caused by ΔL_s and ΔM_{ds} will be unchanged.

2) Influences of the Full-Coupled Inductors in the Driving Loops: It is proved that inserting full-coupled inductors in each driving loop can help reduce the dynamic current difference and the gate oscillation [23], [24]. The circuit is shown in Fig. 9. Fig. 10 shows the transfer functions' gains under the inductors' different self-inductances. The changing tendencies and mechanisms are almost the same as changing M_{gk}, whereas the change degrees are larger under the significant change of L_0. Moreover, as shown in Fig. 10(g), $|G_s'|$ decreases with the increased L_0

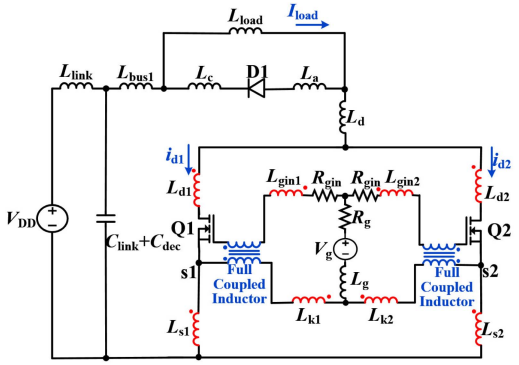

Fig. 9. Circuit with full-coupled inductors in each paralleled driving loop.

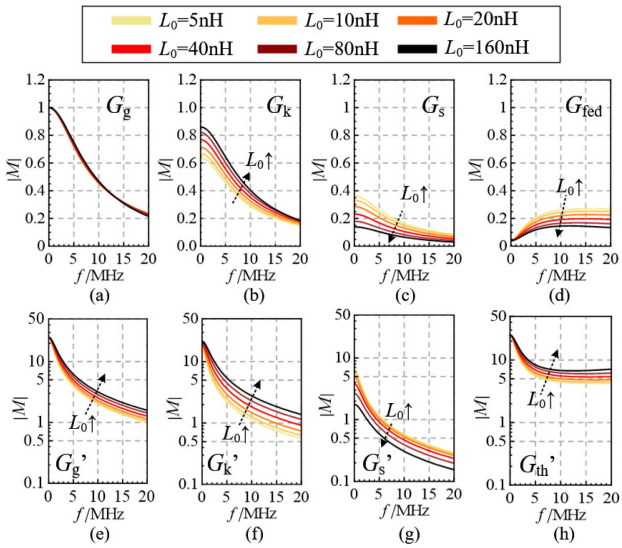

Fig. 10. Magnitude-frequency plots of transfer functions (a) G_g, (b) G_k, (c) G_s, (d) G_{fed}, (e) G_g', (f) G_k', (g) G_s', and (h) G_{th}' under different values of self-inductance L_0 of inserted gate-loop full-coupled inductors.

caused by the more decreased $|G_s|$ shown in Fig. 10(c). It can be concluded that inserting full-coupled inductors can help reduce the unbalanced currents caused by ΔL_s and ΔM_{ds}, whereas the unbalanced current caused by ΔM_{pg}, ΔM_{pk}, and ΔV_{th} will be significantly increased.

3) Influences of R_{gin}: The transfer function gains under different values of R_{gin} are shown in Fig. 11. As shown in Fig. 11(a)–(c), the gains of G_g, G_k, and G_s largely decrease with the increased R_{gin}, which is caused by the increased impedances of the gate branches. Then, the feedback effect is

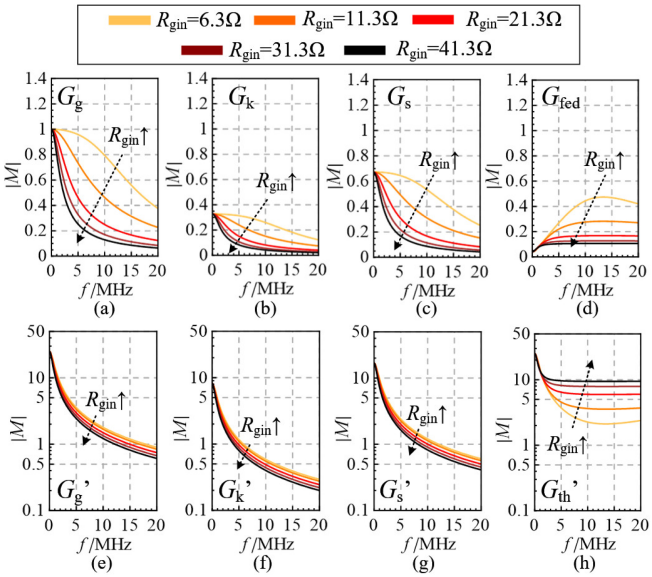

Fig. 11. Magnitude-frequency plots of transfer functions (a) G_g, (b) G_k, (c) G_s, (d) G_{fed}, (e) G_g', (f) G_k', (g) G_s', and (h) G_{th}' under different values of R_{gin}.

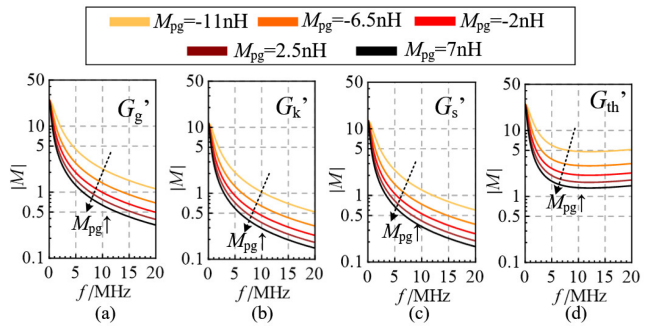

Fig. 12. Magnitude-frequency plots of transfer functions (a) G_g', (b) G_k', (c) G_s', and (d) G_{th}' under different values of M_{pg}.

largely decreased, as shown in Fig. 11(d). The effect of decreased $|G_{fed}|$ is canceled by the decreased $|G_g|$, $|G_k|$, and $|G_s|$, making $|G_g'|$, $|G_k'|$, and $|G_s'|$ reduced. $|G_{th}'|$ largely increases due to the decreased $|G_{fed}|$. It can be concluded that the larger R_{gin}, the lower $|\Delta i_d|$ caused by ΔM_{pg}, ΔM_{pk}, ΔL_s, and ΔM_{ds}, the much larger $|\Delta i_d|$ caused by ΔV_{th}. When ΔV_{th} is small, replacing the external gate resistor R_g with inside gate resistors R_{gin} can help reduce the dynamic current difference and dampen the oscillation in the paralleled drive loops.

4) Influences of M_{pg}, M_{pk}, M_{ds}, and L_s: M_{pg}, M_{pk}, M_{ds}, and L_s influence the gain of G_{fed} directly, as shown in Fig. 5(f). With larger M_{pg}, lower M_{pk} or larger M_{ds}, the negative feedback effect is enhanced, making $|G_g'|$, $|G_k'|$, $|G_s'|$, and $|G_{th}'|$ significantly reduced, as shown in Figs. 12–14. The effect of M_{pg} is larger than M_{pk} and M_{ds} due to the larger gain of G_g.

Significantly increasing L_s also helps increase the negative feedback effect, as shown in Fig. 15(d), making $|G_g'|$, $|G_s'|$, and $|G_{th}'|$ reduced, as shown in Fig. 15(e), (g), and (h). However, when increasing L_s, due to the increase of the impedance in

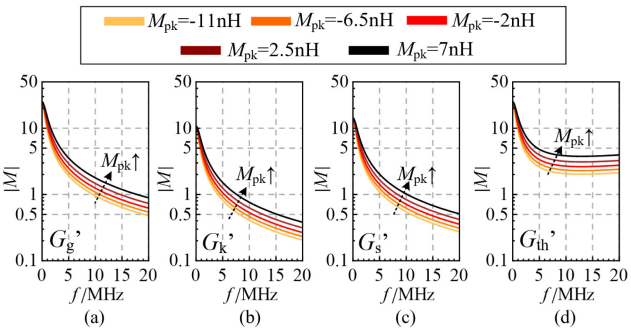

Fig. 13. Magnitude-frequency plots of transfer functions (a) G_g', (b) G_k', (c) G_s', and (d) G_{th}' under different values of M_{pk}.

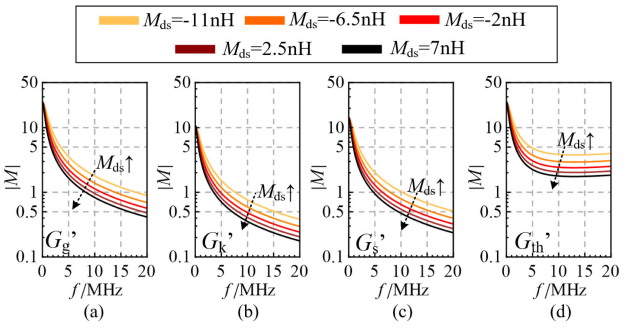

Fig. 14. Magnitude-frequency plots of transfer functions (a) G_g', (b) G_k', (c) G_s', and (d) G_{th}' under different values of M_{ds}.

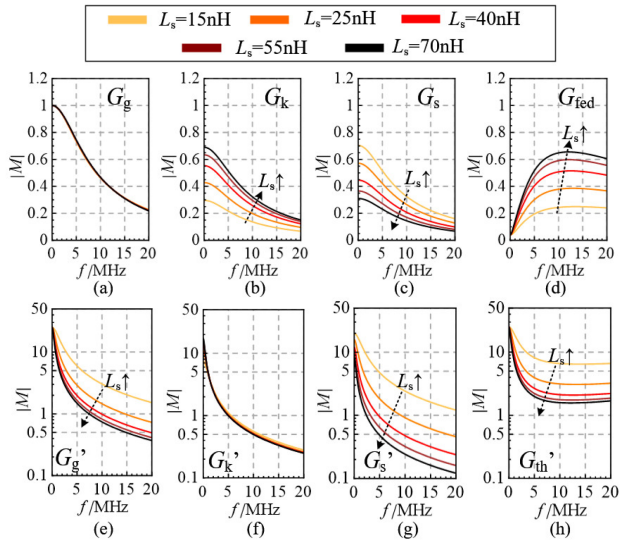

Fig. 15. Magnitude-frequency plots of transfer functions (a) G_g, (b) G_k, (c) G_s, (d) G_{fed}, (e) G_g', (f) G_k', (g) G_s', and (h) G_{th}' under different values of L_s.

power-source branches, the blue current caused by Δv_{pk} will flow more into the gate branches as shown in Fig. 7, $|G_k|$ will be increased, making $|G_k'|$ unchanged, as shown in Fig. 15(b) and (f).

It can be concluded that the current imbalance can be reduced by increasing M_{pg} and M_{ds} or decreasing M_{pk}. Under the same parameter changes, the effect of M_{pg} is the largest, caused by

the largest gain of G_g. A large value of L_s can also help reduce the current imbalance caused by ΔM_{pg}, ΔL_s, ΔM_{ds}, and ΔV_{th}, whereas the current imbalance caused by ΔM_{pk} is not changed. Changing M_{pg} and M_{pk} will induce a couple between the power loop and driving loop, and increasing M_{ds} and L_s will induce a larger power-loop inductance, which requires much attention.

Based on the analyses of the physical mechanisms, it can be concluded that the influences and mechanisms are determined by the impedance structure of the circuit. The conclusions are unrelated to the bus voltage and load current. And they still hold under different gate resistances and parasitic parameter values of different circuits. To clearly investigate the current sharing mechanisms, the circuit with two paralleled devices is used to analyze. When more devices are paralleled, the physical mechanisms remain unchanged, and the conclusions remain valid.

IV. Experimental Verifications

In this section, double pulse tests under different circuit parameter values are conducted to verify the current sharing conclusions using the test circuit shown in Fig. 16(a) and (b). The test board is a symmetrical structure. Two SiC MOSFETs, C3M0025065K from Cree, are paralleled as the device under tests (DUTs), and a SiC Schottky diode, GD60MPS06H from Gene SiC, is used as the freewheeling diode. There are solder pads in each branch connected to the MOSFETs, where two air-core solenoidal inductors or windings of air-core coupled inductors are soldered, as shown in Fig. 16(c) and (d). The parameters of the inductors and coupled inductors are changed to control the differential and common inductance values. Then, the influences of different parameters can be verified. Except for the parameter being investigated, other parameters are controlled unchanged and consistent between different tests. Two 10 Ω resistors are added to the two paralleled gate branches as shown in Fig. 16(c). Adding the internal gate resistance of the MOSFETs, the total R_{gin} is 11.3 Ω. The equivalent circuit of the test rig is shown in Fig. 16(e), where the soldered air-core inductors are highlighted in blue color to clearly depict the connection locations. The parasitic inductances of the PCB wires are highlighted in red color. Moreover, the purpose of using a PCB circuit is to easily change and control the inductance values to verify the conclusions, which is rather difficult in a power module with a DBC circuit. However, the conclusions are also applicable to power modules.

The test setup is shown in Fig. 16(f). i_{d1} and i_{d2} are measured on the terminals of the MOSFETs using two 120 A/30 MHz Rogowski coils. v_{gs1} and v_{gs2} are measured on the MOSFETs' gate and drive-source terminals using two 400 V/500 MHz voltage probes. i_{g1} and i_{g2} are measured on the two 10 Ω gate resistors using two 50 V/25 MHZ differential probes. The testing dc bus voltage V_{DD} and load current I_{load} are 350 V/100 A. Since the inductors will induce a large loop parasitic inductance, causing large switching overvoltages, oscillations, and even false turn-ON, influencing the circuit stability and security, and influencing the current difference measurement. So, relatively large gate resistances $R_g = 20$ Ω are used to ensure the stability of the

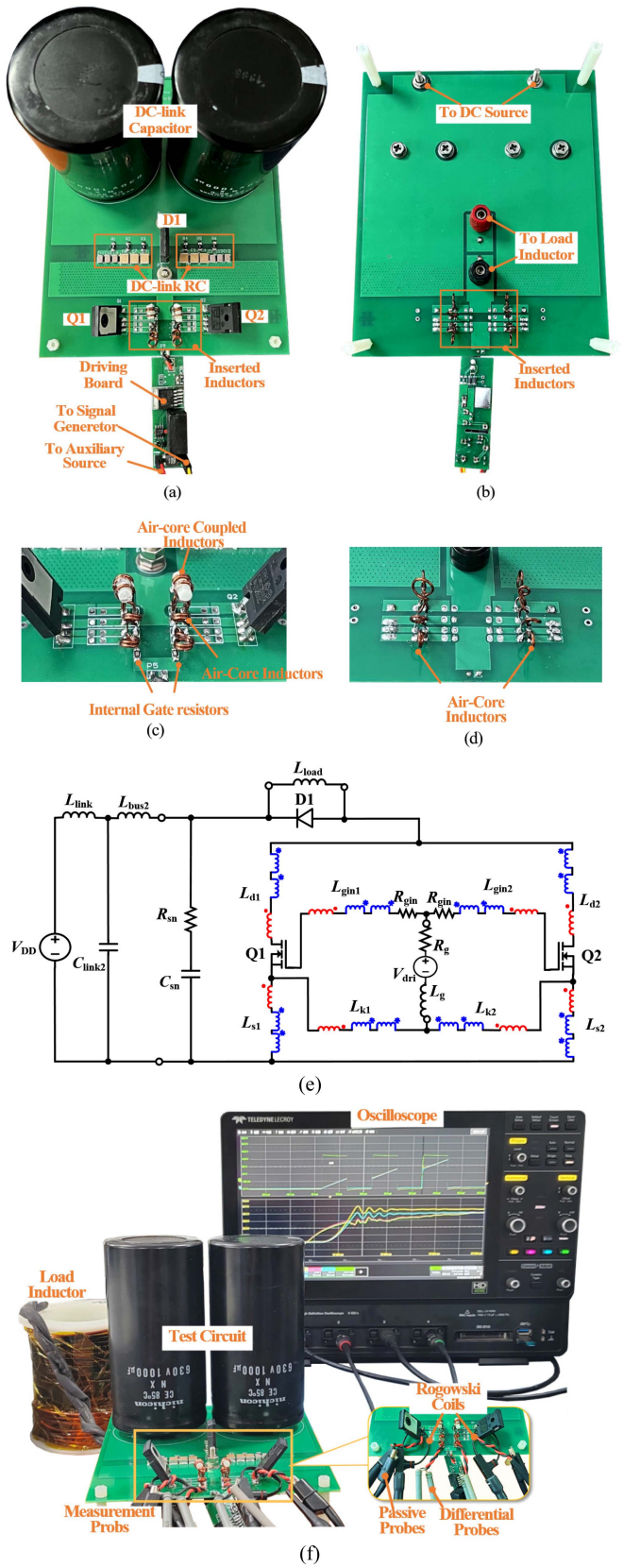

Fig. 16. Experimental test rig. (a) Top view of the test circuit. (b) Bottom view of the test circuit. (c) View of the connected inductors on the top side. (d) View of the connected inductors on the bottom side. (e) Equivalent circuit of the test rig. (f) Test setup.

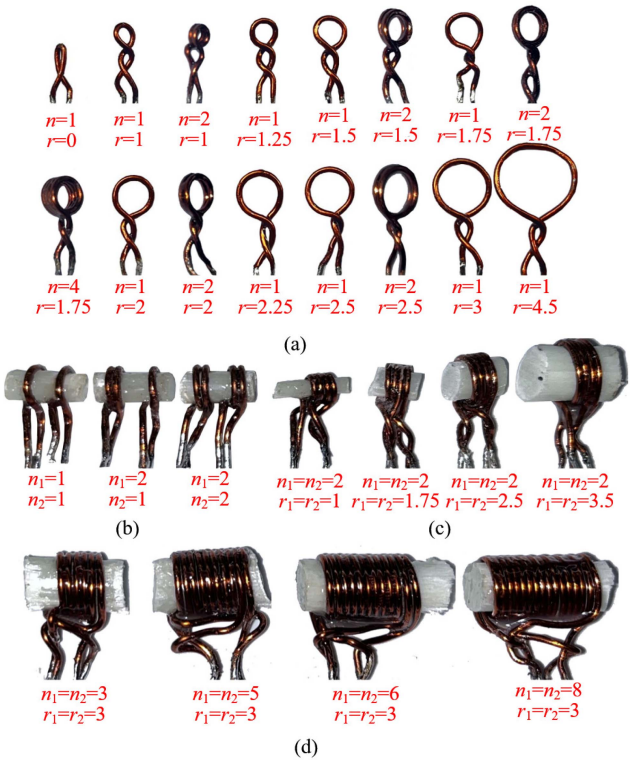

Fig. 17. Air-core uncoupled and coupled solenoidal inductors. (a) Uncoupled inductors. (b) Coupled coaxial inductors. (c) Full-coupled coaxial inductors with different radii. (d) Full-coupled coaxial inductors with different turn numbers. The units of radii r, r_1, and r_2 are mm.

circuit and clean waveforms. Although the gate resistance is relatively large, the current rise time t_r and fall time t_f are 66 ns and 34 ns, respectively, which are reasonable. The experiments under the conditions can well achieve the verification purpose.

The air-core inductors to control the self-inductances are shown in Fig. 17(a), consisting of a top coil and two bottom leads. The inductance of the top coil can be expressed as

$$L = \frac{(r + d/2)^2 n^2}{8(r + d/2) + 11l} \tag{21}$$

where r is the internal radius of the coil, d is the wire diameter, l is the axial width, and n is the turn number [25]. Keeping $d = 0.7$ mm and $l = n{\cdot}d$, the inductance values of the inductors are adjusted by changing r and n. The inductance values of the inductors are obtained by Q3D simulations, which are accurate enough [22]. In the simulations, the lead wires are added with the same length and shape as that of the actual inductors.

The coupled inductors to control the mutual inductances are shown in Fig. 17(b), where polyamide plastic cylinders are used as the inductor skeletons, which are hard enough to provide good support for the coils. The mutual inductance between two coaxial coils is expressed as

$$M = \frac{\mu_0}{4\pi} \oint_{c1} \oint_{c2} \frac{1}{R} \mathrm{d}\vec{l}_1 \cdot \mathrm{d}\vec{l}_2 \tag{22}$$

where μ_0 is the vacuum permeability, c_1 and c_2 are the current paths of the two coils, $\mathrm{d}\vec{l}_1$ and $\mathrm{d}\vec{l}_2$ are two differential space vectors on the two paths, respectively, and R is the distance between $\mathrm{d}\vec{l}_1$ and $\mathrm{d}\vec{l}_2$, which can be expressed as

$$R = \sqrt{r_1{}^2 + r_2{}^2 + D^2 - 2r_1 r_2 \cos(\varphi_1 - \varphi_2)} \tag{23}$$

where r_1 and r_2 are the radii of the two coils, D is the axial distance between the two coils, and φ_1 and φ_2 are the angles of $\mathrm{d}\vec{l}_1$ and $\mathrm{d}\vec{l}_2$ relative to the central axis, respectively [26]. Keeping $r_1 = r_2 = 1.75$ mm and keeping the turn numbers of the two coils fixed, the mutual inductance values are adjusted by changing the coil distance D. The signs of the mutual inductances are controlled by the coupling direction. The mutual inductance values are also obtained by Q3D simulations. The full-coupled inductors inserted into the driving loop are shown in Fig. 17(c) and (d). The self-inductances L_0 of the coils are adjusted by changing the turn numbers and radii.

TABLE V
STATIC PARAMETERS OF USED SiC MOSFETs

No. of MOSFETs	1	2	3	4
R_{dson}/mΩ	24.21	24.21	25.35	26.58
V_{th}/V	5.835	5.843	6.246	6.620

To control the MOSFET parameter and investigate the influences of ΔV_{th}, R_{dson}, and V_{th} of several MOSFETs are measured using Agilent B1505A and its N1265 UHC (ultrahigh current) fixture [27], [28]. When measuring R_{dson}, the MOSFET channel is turned ON by giving a 15-V driving signal. Then, the corresponding v_{ds} under 50 A i_d is measured. Then, R_{dson} can be obtained by $R_{dson} = v_{ds}/i_d$. When measuring V_{th}, a constant $v_{ds} = 20$ V is given, and i_d under gradually increased v_{gs} are measured. V_{th} is v_{gs} when i_d reaches the given value. The voltage and current measurement resolutions can reach 1×10^{-4} V and 5×10^{-4} A, respectively, fully meeting the test requirements. The parameters of the four MOSFETs used are shown in Table V. MOSFET 1 and MOSFET 2 are used as the DUTs with $\Delta V_{th} \approx 0$. MOSFET 1 and MOSFET 3 are used as the DUTs with $\Delta V_{th} = 0.411$ V. MOSFET 1 and MOSFET 4 are used as the DUTs with $\Delta V_{th} = 0.785$ V.

A. Verification of Influences of Differential Parameters

The turn-ON and turn-OFF waveforms under the unbalanced gate and drive source inductances are shown in Fig. 18(a). The waveforms under unbalanced M_{gk} are shown in Fig. 18(b). The waveforms of i_{d1} and i_{d2} overlap. It is proved that the unbalanced parasitic inductances in the driving loop have little influence on dynamic current sharing.

The experimental waveforms under the nonzero ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_s, and ΔV_{th} are shown in Figs. 19–23, respectively. It is proved that ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_s and ΔV_{th} can cause unbalanced dynamic currents. As shown in Fig. 19, when $\Delta M_{pg} > 0$, during the turn-ON period, $i_{g1} < i_{g2}$ due to the positive Δv_{pg}, making $v_{gs1} < v_{gs2}$ and $i_{d1} < i_{d2}$. Reversely, $i_{g1} > i_{g2}$, $v_{gs1} > v_{gs2}$ and $i_{d1} > i_{d2}$, during the turn-OFF period. As shown in Fig. 20, when $\Delta M_{pk} > 0$, during the turn-ON period, $i_{g1} > i_{g2}$ due to the positive Δv_{pk}, making $v_{gs1} > v_{gs2}$ and $i_{d1} > i_{d2}$. Reversely, $i_{g1} < i_{g2}$, $v_{gs1} < v_{gs2}$ and $i_{d1} < i_{d2}$, during the turn-OFF period. It is shown in Figs. 21 and 22

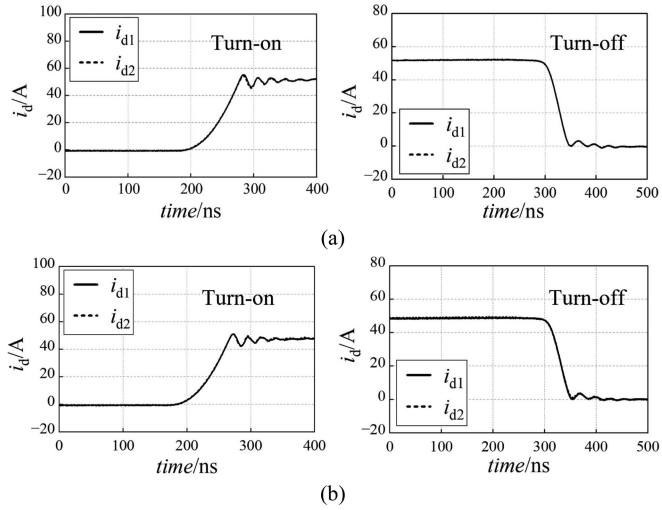

Fig. 18. Experimental turn-ON and turn-OFF current waveforms. (a) Waveforms when $\Delta L_{\mathrm{gin}} = \Delta L_{\mathrm{k}} = 17.0$ nH. (b) Waveforms when $\Delta M_{\mathrm{gk}} = 16.1$ nH.

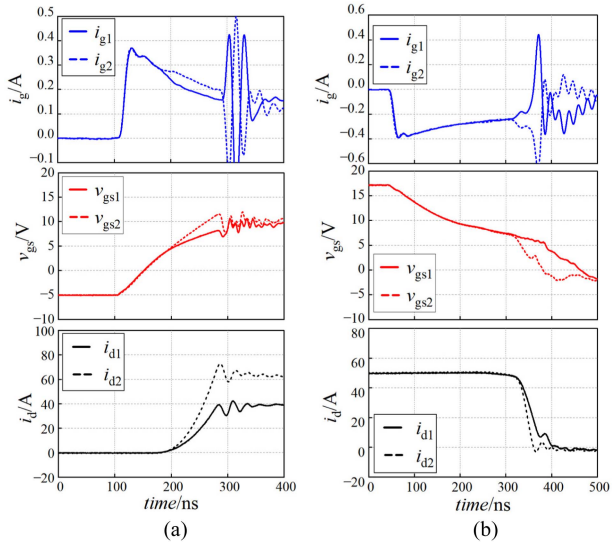

Fig. 19. Experimental waveforms when $\Delta M_{\mathrm{pg}} = 9.7$ nH. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

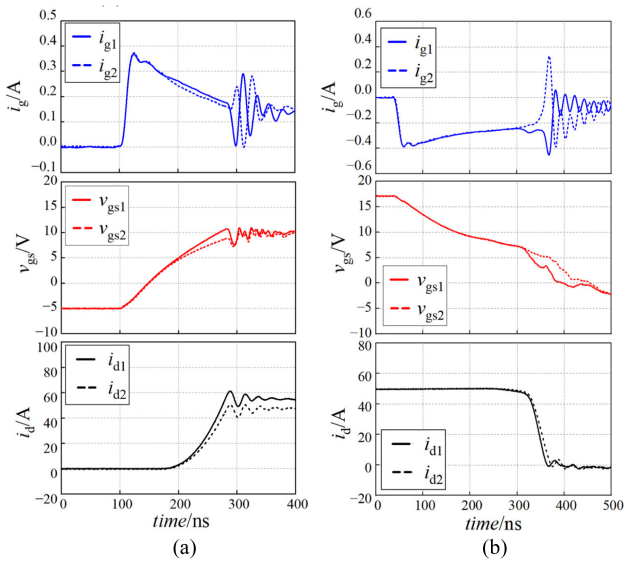

Fig. 20. Experimental waveforms when $\Delta M_{\mathrm{pk}} = 9.7$ nH. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

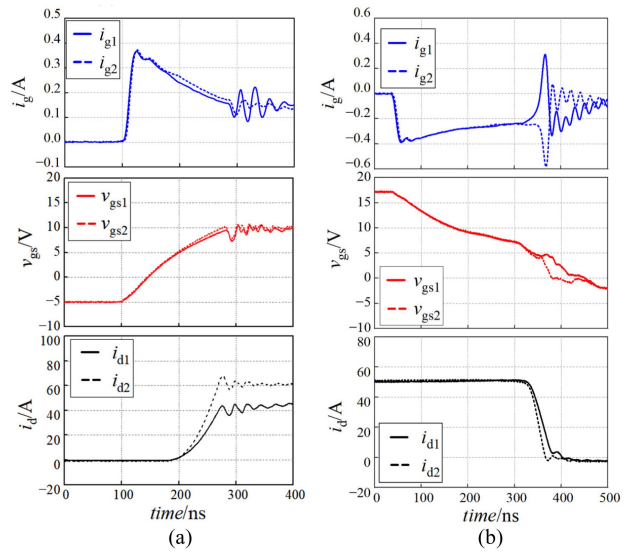

Fig. 21. Experimental waveforms when $\Delta M_{\mathrm{ds}} = 12$ nH. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

that when ΔM_{ds} or $\Delta L_{\mathrm{s}} > 0$, $i_{\mathrm{g1}} < i_{\mathrm{g2}}$ due to the positive $\Delta v_{\mathrm{ps\text{-}d}}$ or $\Delta v_{\mathrm{ps\text{-}s}}$ during the turn-ON period, making $v_{\mathrm{gs1}} < v_{\mathrm{gs2}}$ and $i_{\mathrm{d1}} < i_{\mathrm{d2}}$. Reversely, $i_{\mathrm{g1}} > i_{\mathrm{g2}}$, $v_{\mathrm{gs1}} > v_{\mathrm{gs2}}$ and $i_{\mathrm{d1}} > i_{\mathrm{d2}}$, during the turn-OFF period. The i_{d} difference under ΔM_{pk} is smaller than that under ΔM_{ds} or ΔL_{s}. However, the measured Δv_{gs} under ΔM_{pk} is larger. This is because v_{gs1} and v_{gs2} are measured on the terminals of the MOSFETs. The waveforms include voltage drops on the parasitic inductances and gate resistances inside the MOSFETs. The voltages on the internal parasitic inductances and resistances make the measured Δv_{gs} under ΔM_{pk} much larger than the actual signal and larger than that under ΔM_{ds} and ΔL_{s}. As shown in Fig. 23, when $\Delta V_{\mathrm{th}} > 0$, $i_{\mathrm{d1}} < i_{\mathrm{d2}}$ during the turn-ON and turn-OFF periods. Moreover, due to the negative feedback effect, $i_{\mathrm{g1}} > i_{\mathrm{g2}}$ and $v_{\mathrm{gs1}} > v_{\mathrm{gs2}}$ during the current commutating periods. The difference between v_{gs1} and v_{gs2} is relatively small. It is because the voltages on the MOSFET internal parasitic inductances and resistances cancel some measured v_{gs} differences.

Maximum $|\Delta i_{\mathrm{d}}|$ under different values of ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_{s}, and ΔV_{th} are depicted in Fig. 24. Since the unit of ΔV_{th} is different from that of the unbalanced inductance values, the effect degree of ΔV_{th} cannot be compared to other factors directly. The following consideration is taken: Taking ΔM_{pg} as an example, the influence source $\Delta V_{\mathrm{pg(int)}}$ in Fig. 5(a) caused by ΔM_{pg} is equal to $\Delta V_{\mathrm{th}}/s$ in Fig. 5(d) when (24) is satisfied.

$$\Delta V_{\mathrm{th}} = \Delta M_{\mathrm{pg}} \mathrm{d}i_{\mathrm{d}}/\mathrm{d}t \tag{24}$$

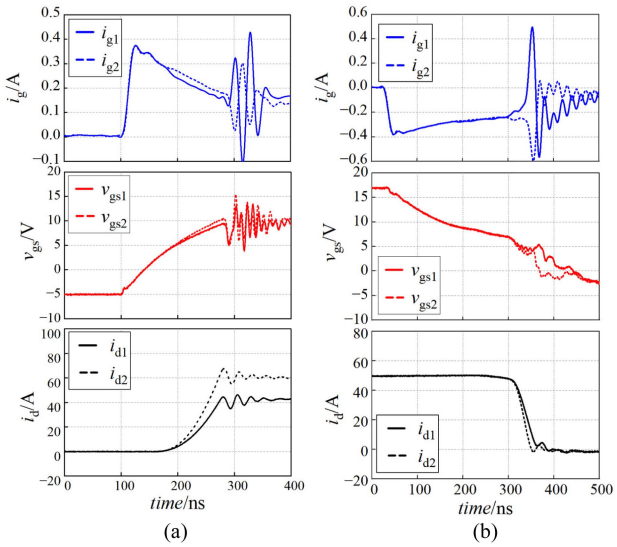

Fig. 22. Experimental waveforms when $\Delta L_s = 10.6$ nH. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

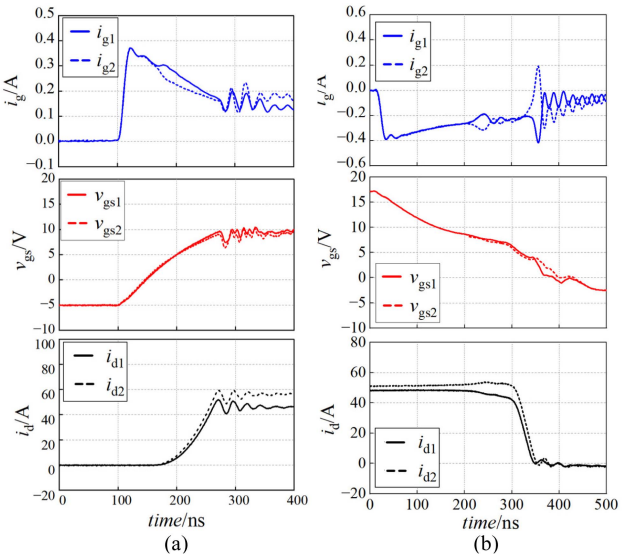

Fig. 23. Experimental waveforms when $\Delta V_{th} = 0.785$ V. (a) Turn-ON waveforms. (b) Turn-OFF waveforms.

where

$$di_d/dt = I_{load}/t_{sw} \tag{25}$$

and t_{sw} is the current rise or fall time. Then, the effect degrees of ΔV_{th} and ΔM_{pg} can be compared through $|\Delta i_{d(max)}|$, which can be concluded from Fig. 5(a) and (d). The scales of the top and bottom axis in Fig. 23 are adjusted and correspond by (24). Then, the effect degrees of the differential parameters can be ranked as: $\Delta V_{th} > \Delta M_{pg} > \Delta L_s$ and $\Delta M_{ds} > \Delta M_{pk}$. In Fig. 24(a), the difference between the turn-ON $|\Delta i_{d(max)}|$ under ΔV_{th} and ΔM_{pg} is not obvious. This is because the turn-ON time (66 ns) is almost twice the turn-OFF time (34 ns), making the equivalent frequency of turn-ON currents lower. The gains of

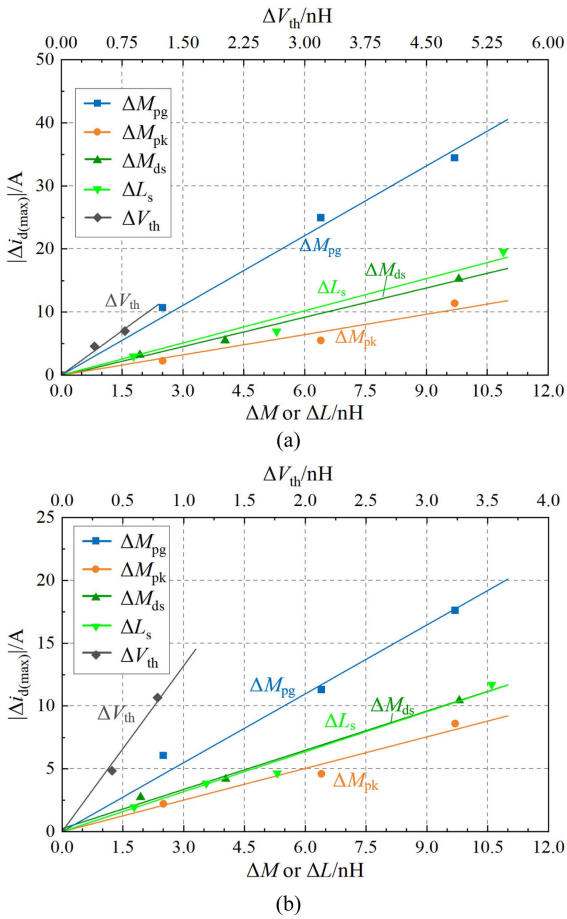

Fig. 24. Maximum $|\Delta i_d|$ under different values of ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_s, and ΔV_{th}. (a) Turn-ON $|\Delta i_{d(max)}|$. (b) Turn-OFF $|\Delta i_{d(max)}|$.

G_{th}' and G_g' are close in the low-frequency region, as shown in Fig. 6(b), making the turn-ON $|\Delta i_{d(max)}|$ under ΔV_{th} and ΔM_{pg} close. Moreover, another reason is that there are also some measurement errors.

All the results are consistent with the conclusions drawn by the theoretical analysis in Section III.

B. Verifications of Influences of Common Parameters

The influences of M_{gk} are shown in Fig. 25. With the increased M_{gk}, $|\Delta i_d|$ caused by ΔM_{pg} and ΔV_{th} are slightly increased. $|\Delta i_d|$ caused by ΔM_{pk} is increased more. $|\Delta i_d|$ caused by ΔM_{ds} and ΔL_s are almost unchanged. For example, during the turn-ON period with 100 A I_{load}, when M_{gk} increases from 6.8 nH to 17.2 nH, $|\Delta i_{d(max)}|$ caused by ΔM_{pg} and ΔV_{th} is increased by 20.5% and 19.9%, respectively. $|\Delta i_{d(max)}|$ caused by ΔM_{pk} is increased by 61.7%, whereas the change of $|\Delta i_d|$ caused by ΔM_{ds} and ΔL_s are only 0.9% and 1.6%, respectively.

The influences of the inserted full-coupled inductors in the driving loop are shown in Fig. 26. $|\Delta i_d|$ caused by ΔM_{pg}, ΔM_{pk}, and ΔV_{th} are increased with the increased L_0, whereas $|\Delta i_d|$ caused by ΔM_{ds} and ΔL_s are reduced. During the turn-ON period with 100A I_{load}, when L_0 increases from 5 nH to 160 nH, $|\Delta i_{d(max)}|$ caused by ΔM_{pg}, ΔM_{pk}, and ΔV_{th} are increased

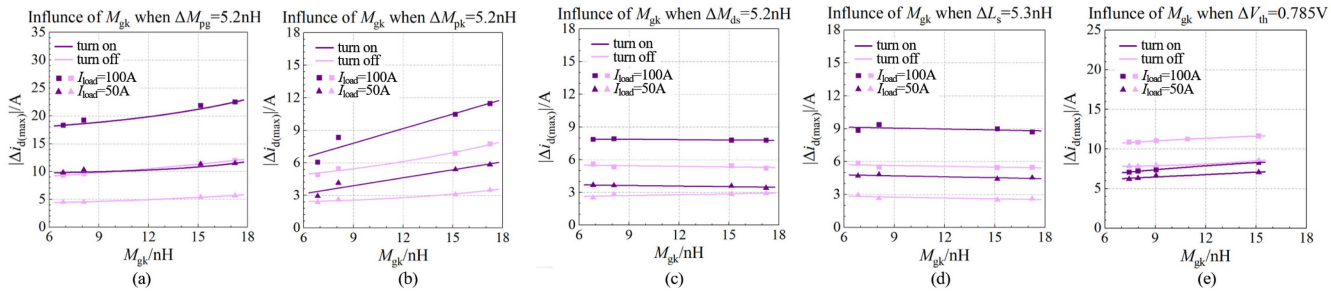

Fig. 25. $|\Delta i_{\mathrm{d(max)}}|$ under different values of M_{gk} when (a) $\Delta M_{\mathrm{pg}} = 5.2$ nH, (b) $\Delta M_{\mathrm{pk}} = 5.2$ nH, (c) $\Delta M_{\mathrm{ds}} = 5.2$ nH, (d) $\Delta L_{\mathrm{s}} = 5.3$ nH, and (e) $\Delta V_{\mathrm{th}} = 0.785$ V.

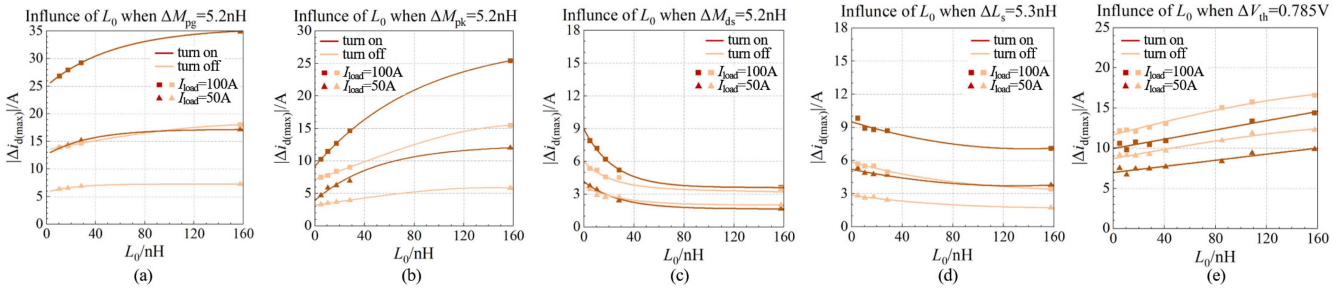

Fig. 26. $|\Delta i_{\mathrm{d(max)}}|$ under different values of L_0 of inserted gate-loop full-coupled inductors when (a) $\Delta M_{\mathrm{pg}} = 5.2$ nH, (b) $\Delta M_{\mathrm{pk}} = 5.2$ nH, (c) $\Delta M_{\mathrm{ds}} = 5.2$ nH, (d) $\Delta L_{\mathrm{s}} = 5.3$ nH, and (e) $\Delta V_{\mathrm{th}} = 0.785$ V.

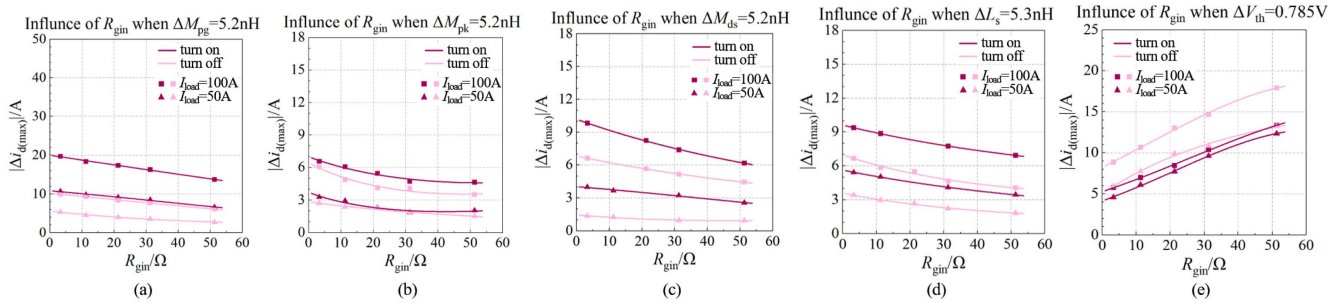

Fig. 27. $|\Delta i_{\mathrm{d(max)}}|$ under different values of R_{gin} when (a) $\Delta M_{\mathrm{pg}} = 5.2$ nH, (b) $\Delta M_{\mathrm{pk}} = 5.2$ nH, (c) $\Delta M_{\mathrm{ds}} = 5.2$ nH, (d) $\Delta L_{\mathrm{s}} = 5.3$ nH, and (e) $\Delta V_{\mathrm{th}} = 0.785$ V.

by 29.6%, 85.2%, and 30.1%, respectively, whereas $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔM_{ds} and ΔL_{s} are decreased by 74.2% and 32.2%, respectively.

The influences of R_{gin} are shown in Fig. 27. $|\Delta i_{\mathrm{d}}|$ caused by ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, and ΔL_{s} are reduced with the increased R_{gin}, whereas $|\Delta i_{\mathrm{d}}|$ caused by ΔV_{th} is significantly increased. During the turn-ON period with 100 A I_{load}, when R_{gin} increases from 3.3 Ω to 51.3 Ω, $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, and ΔL_{s} are decreased by 35.9%, 34.4%, 45.6%, and 30.1%, respectively, whereas $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔV_{th} is increased by 79.2%.

The influences of M_{pg} are shown in Fig. 28. With the increased M_{pg}, $|\Delta i_{\mathrm{d}}|$ caused by the unbalanced parameters are all largely decreased. During the turn-ON period with 100A I_{load}, when M_{pg} increases from -10nH to 3nH, $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_{s}, and ΔV_{th} are decreased by 66.7%, 97.1%, 82.3%, 70.5%, and 86.8%, respectively.

The influences of M_{pk} are shown in Fig. 29. With the increased M_{pk}, $|\Delta i_{\mathrm{d}}|$ caused by the unbalanced parameters are all increased. During the turn-ON period with 100 A I_{load}, when M_{pk} increases from -10 nH to 3 nH, $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_{s}, and ΔV_{th} are increased by 37.8%, 48.8%, 38.1%, 31.4%, and 44.8%, respectively.

The influences of M_{ds} are shown in Fig. 30. With the increased M_{ds}, $|\Delta i_{\mathrm{d}}|$ are largely decreased. During the turn-ON period with 100 A I_{load}, when M_{ds} increases from -10 nH to 3 nH, $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_{s}, and ΔV_{th} are decreased by 45.8%, 81.3%, 81.5%, 56.0%, and 74.4%, respectively. Moreover, it can be concluded that the effect of M_{pg} is larger than M_{pk} and M_{ds}.

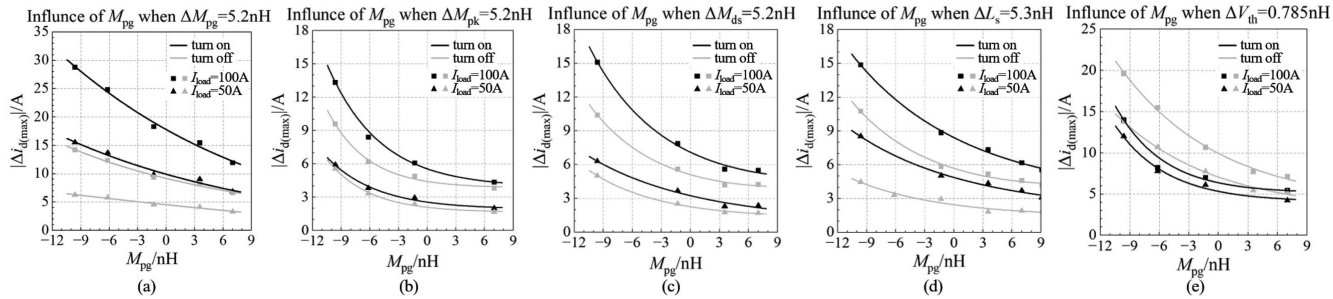

Fig. 28. $|\Delta i_{\mathrm{d(max)}}|$ under different values of M_{pg} when (a) $\Delta M_{\mathrm{pg}} = 5.2$ nH, (b) $\Delta M_{\mathrm{pk}} = 5.2$ nH, (c) $\Delta M_{\mathrm{ds}} = 5.2$ nH, (d) $\Delta L_{\mathrm{s}} = 5.3$ nH, and (e) $\Delta V_{\mathrm{th}} = 0.785$ V.

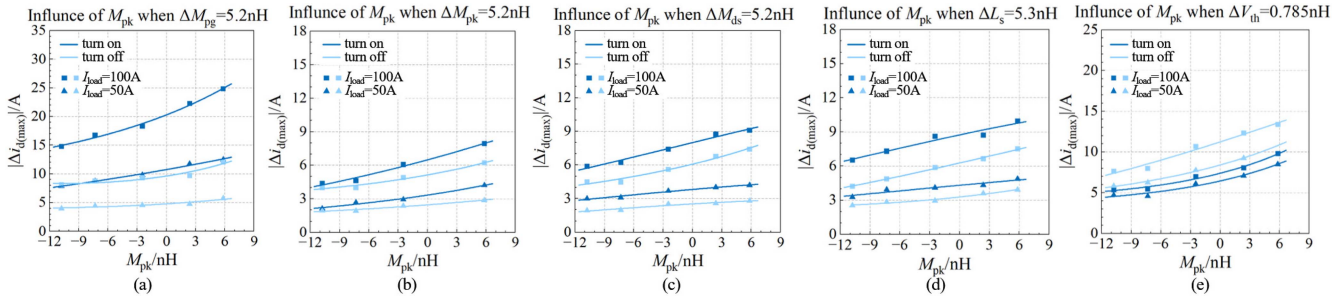

Fig. 29. $|\Delta i_{\mathrm{d(max)}}|$ under different values of M_{pk} when (a) $\Delta M_{\mathrm{pg}} = 5.2$ nH, (b) $\Delta M_{\mathrm{pk}} = 5.2$ nH, (c) $\Delta M_{\mathrm{ds}} = 5.2$ nH, (d) $\Delta L_{\mathrm{s}} = 5.3$ nH, and (e) $\Delta V_{\mathrm{th}} = 0.785$ V.

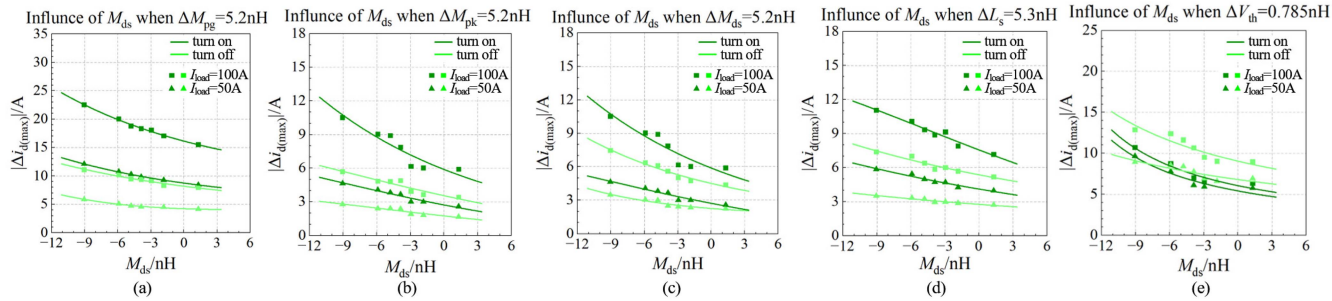

Fig. 30. $|\Delta i_{\mathrm{d(max)}}|$ under different values of M_{ds} when (a) $\Delta M_{\mathrm{pg}} = 5.2$ nH, (b) $\Delta M_{\mathrm{pk}} = 5.2$ nH, (c) $\Delta M_{\mathrm{ds}} = 5.2$ nH, (d) $\Delta L_{\mathrm{s}} = 5.3$ nH, and (e) $\Delta V_{\mathrm{th}} = 0.785$ V.

The influences of L_{s} are shown in Fig. 31. With the increased L_{s}, $|\Delta i_{\mathrm{d}}|$ caused by ΔM_{pg}, ΔM_{ds}, ΔL_{s}, and ΔV_{th} are largely decreased, whereas $|\Delta i_{\mathrm{d}}|$ caused by ΔM_{pk} is almost not changed. During the turn-ON period with 100 A I_{load}, when L_{s} increases from 12 nH to 43 nH, $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔM_{pg}, ΔM_{ds}, ΔL_{s}, and ΔV_{th} are decreased by 82.8%, 105.7%, 83.4%, and 105.3%, respectively, whereas the change of $|\Delta i_{\mathrm{d(max)}}|$ caused by ΔM_{pk} is only 0.5%.

The influences of the common parameters are consistent with the analysis in Section III. The conclusions are well verified.

V. Discussions of Current Balancing Design

In practical circuits, the parameters complexly affect together. The contributions to Δi_{d} and the effect directions of the unbalanced parameters are inconsistent. In this section, to further describe the contributions of this article in actual current balancing design, the current sharing performance and the optimizing methods in practical circuit layouts are preliminarily discussed based on the proposed model and the conclusions. Moreover, new current balancing methods are discussed based on the influences of the common parameters. These contents can provide guidance for future research on layout optimization and current sharing methods.

A. Analysis of a Practical Circuit Layout

The power module with a conventional layout and two paralleled SiC MOSFETs is used for preliminary analysis, as shown in Fig. 32. The SiC chips are ROHM S4601 (1200 V/120 A, $R_{\mathrm{dson}} = 11$ mΩ, $C_{\mathrm{iss}} = 7.87$ nF, $g_{\mathrm{m}} = 47$ S). When the low-side MOSFETs work as the main switches and the high-side MOSFETs

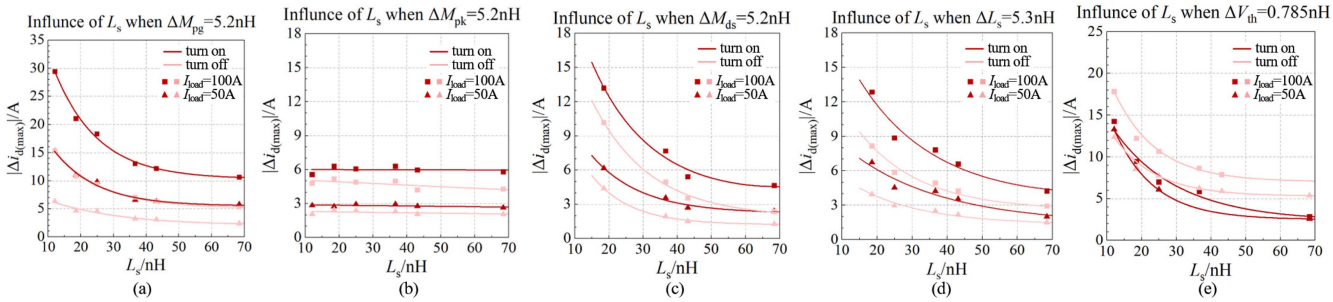

Fig. 31. $|\Delta i_{\mathrm{d(max)}}|$ under different values of L_{s} when (a) $\Delta M_{\mathrm{pg}} = 5.2$ nH, (b) $\Delta M_{\mathrm{pk}} = 5.2$ nH, (c) $\Delta M_{\mathrm{ds}} = 5.2$ nH, (d) $\Delta L_{\mathrm{s}} = 5.3$ nH, and (e) $\Delta V_{\mathrm{th}} = 0.785$ V.

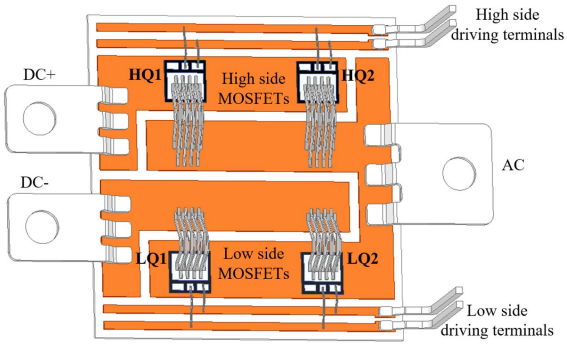

Fig. 32. Power module with unbalanced layout.

TABLE VI
PARAMETER VALUES OF THE POWER MODULE

Parameter	Value /nH	Parameter	Value /nH	Parameter	Value /nH
$L_{\mathrm{d1\text{-}L}}$'	15.2	$M_{\mathrm{d1d2\text{-}L}}$'	14.5	$M_{\mathrm{s1g1\text{-}L}}$	2
$L_{\mathrm{d2\text{-}L}}$'	18.5	$M_{\mathrm{s1s2\text{-}L}}$	7.08	$M_{\mathrm{s1g2\text{-}L}}$	0.62
$L_{\mathrm{s1\text{-}L}}$	7.29	$M_{\mathrm{g1g2\text{-}L}}$	19.1	$M_{\mathrm{s2g1\text{-}L}}$	6.25
$L_{\mathrm{s2\text{-}L}}$	14.96	$M_{\mathrm{k1k2\text{-}L}}$	17.9	$M_{\mathrm{s2g2\text{-}L}}$	1.9
$L_{\mathrm{gin1\text{-}L}}$	31.2	$M_{\mathrm{d1s1\text{-}L}}$'	−3.17	$M_{\mathrm{d1k1\text{-}L}}$'	−0.54
$L_{\mathrm{gin2\text{-}L}}$	20.2	$M_{\mathrm{d1s2\text{-}L}}$'	−4.06	$M_{\mathrm{d1k2\text{-}L}}$'	−0.31
$L_{\mathrm{k1\text{-}L}}$	29.7	$M_{\mathrm{d2s1\text{-}L}}$'	−4.58	$M_{\mathrm{d2k1\text{-}L}}$'	−5.20
$L_{\mathrm{k2\text{-}L}}$	18.4	$M_{\mathrm{d2s2\text{-}L}}$'	−8.78	$M_{\mathrm{d2k2\text{-}L}}$'	−1.40
$M_{\mathrm{g1k1\text{-}L}}$	17.5	$M_{\mathrm{d1g1\text{-}L}}$'	−1.01	$M_{\mathrm{s1k1\text{-}L}}$	1.76
$M_{\mathrm{g1k2\text{-}L}}$	11.7	$M_{\mathrm{d1g2\text{-}L}}$'	−0.49	$M_{\mathrm{s1k2\text{-}L}}$	0.5
$M_{\mathrm{g2k1\text{-}L}}$	12.3	$M_{\mathrm{d2g1\text{-}L}}$'	−5.59	$M_{\mathrm{s2k1\text{-}L}}$	5.98
$M_{\mathrm{g2k2\text{-}L}}$	10.9	$M_{\mathrm{d2g2\text{-}L}}$'	−1.80	$M_{\mathrm{s2k2\text{-}L}}$	1.59

work as the freewheeling diodes, the DPT circuit model is shown in Fig. 33(a), where the black parts are the components of the power module, the blue parts are the components of the outside circuits. Supposing the voltages on the freewheeling diodes are equal, the diodes can be moved outside the paralleled branches. The connecting point of L_{load} is also moved with the diodes from ac to outside the paralleled branches. Then, combining the parasitic inductances from dc+ to the drains of LQ1 and LQ2, the circuit can be equivalent to Fig. 33(b), which is the same as Fig. 1. The parameters in Fig. 33(b) can be directly obtained by Q3D simulation by shorting the high-side MOSFETs, setting Sinks on the module terminals and setting Sources on the electrodes of the low-side MOSFETs. The parameter values are shown in Table VI, and the calculated common and differential parameter values are shown in Table VII.

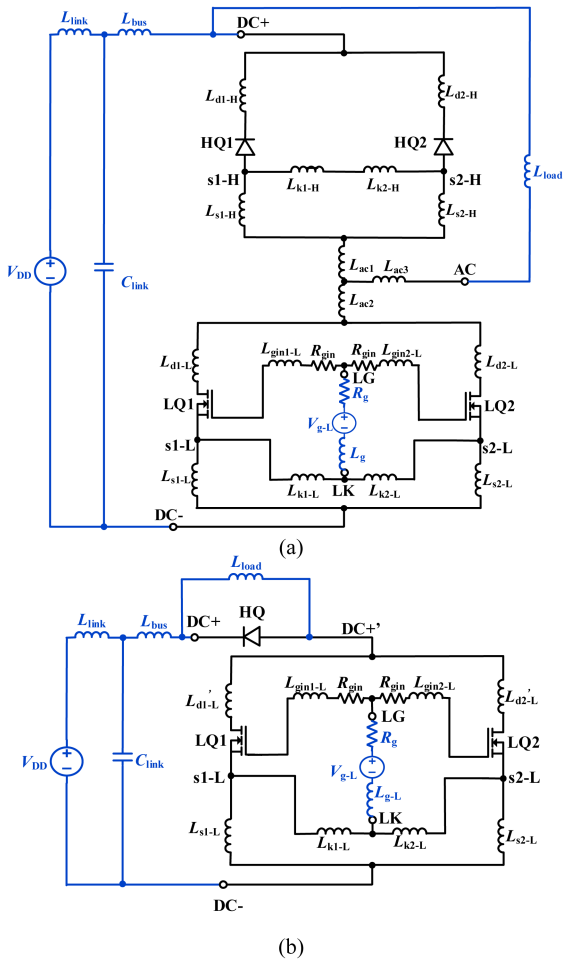

Fig. 33. DPT circuit models of the power module. (a) Original circuit model. (b) Equivalent circuit model.

TABLE VII
COMMON AND DIFFERENTIAL PARAMETER VALUES

Parameter	$M_{\mathrm{pg\text{-}L}}$	$M_{\mathrm{pk\text{-}L}}$	$M_{\mathrm{ds\text{-}L}}$	$L_{\mathrm{s\text{-}L}}$	$M_{\mathrm{pg\text{-}L}}$'
Value /nH	0.15	0.22	−1.66	4.03	0.94
Parameter	$M_{\mathrm{pk\text{-}L}}$'	$\Delta M_{\mathrm{pg\text{-}L}}$	$\Delta M_{\mathrm{pk\text{-}L}}$	$\Delta M_{\mathrm{ds\text{-}L}}$	$\Delta L_{\mathrm{s\text{-}L}}$
Value /nH	1.19	1.42	1.62	5.1	−7.6

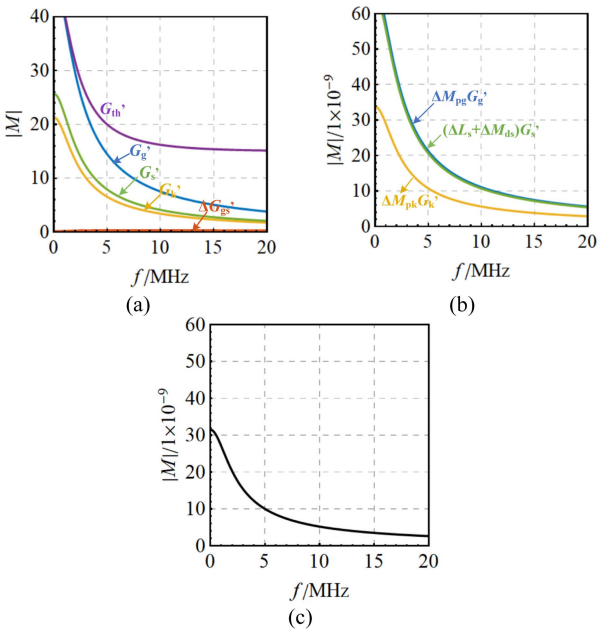

Fig. 34. Magnitude-frequency plots of (a) G_g', G_k', G_s', G_{th}', and ΔG_{gs}', (b) $\Delta M_{pg}G_g$', $\Delta M_{pk}G_k$', and $(\Delta M_{ds}+\Delta L_s)G_s$', and (c) $G_{tol}=\Delta M_{pg}G_g$'$+\Delta M_{pk}G_k$'$+(\Delta M_{ds}+\Delta L_s)G_s$'.

Considering the influences of the unbalanced layout and neglecting the influences of the unbalanced driving-loop inductances, (17) can be rewritten as

$$\Delta I_d = \left(\Delta M_{pg}G_g' + \Delta M_{pk}G_k' + (\Delta M_{ds}+\Delta L_s)G_s'\right) = \mathcal{L}\left[\frac{di_d}{dt}\right] G_{tol}\mathcal{L}\left[\frac{di_d}{dt}\right]. \quad (26)$$

It can be concluded by (26) that the Δi_d contributions of ΔM_{pg}, ΔM_{pk}, and $\Delta M_{ds}+\Delta L_s$ can be analyzed and compared by the gains of $\Delta M_{pg}G_g$', $\Delta M_{pk}G_k$', and $(\Delta M_{ds}+\Delta L_s)G_s$'. The total Δi_d can be represented by the gain of $G_{tol}=\Delta M_{pg}G_g$'$+\Delta M_{pk}G_k$'$+(\Delta M_{ds}+\Delta L_s)G_s$'. Based on the parameter values in Tables VI and VII, the gains of G_g', G_k', G_s', G_{th}', and ΔG_{gs}' are shown in Fig. 34(a), and the gains of $\Delta M_{pg}G_g$', $\Delta M_{pk}G_k$', and $(\Delta M_{ds}+\Delta L_s)G_s$' are shown in Fig. 34(b). It can be concluded from Fig. 34(b) that ΔM_{pg} and ΔM_{pk} can cause the same level of unbalanced current as $\Delta M_{ds}+\Delta L_s$. Therefore, ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, and ΔL_s are all the dominant factors causing unbalanced current.

1) The absolute values of ΔL_s and ΔM_{ds} are the largest, as shown in Table VII, but their signs are opposite, making $\Delta L_s+\Delta M_{ds}=-2.5$ nH.
2) ΔM_{pg} is 1.42 nH. The direction of the caused Δi_d is opposite to that of $\Delta L_s+\Delta M_{ds}$, according to the conclusions of this article. Due to the larger $|G_g'|$, Δi_d caused by the smaller ΔM_{pg} almost completely cancels that caused by $\Delta L_s+\Delta M_{ds}$, as shown by the blue and green curves in Fig. 34(b).
3) ΔM_{pk} is 1.62 nH. The direction of its caused Δi_d is the same as that of $\Delta L_s+\Delta M_{ds}$, promoting the generation of Δi_d.
4) The gain of G_{tol} is shown in Fig. 34(c), which is almost coincident with $\Delta M_{pk}G_k$'.

In circuits with more paralleled devices, the Δi_d contribution between any two of the paralleled devices can be analyzed with a similar analysis, which will be investigated in detail in future work.

B. Discussions of Layout Optimization

The dynamic current can be balanced by using absolutely symmetrical layouts. However, this method requires changing the terminal structures and locations, and even using a circular layout [19], which leads to extra production costs and waste of material and space. Considering the applicability, it is significant to optimize the unsymmetrical layout based on the original terminals and the circuit shapes. The conclusions of this article can provide theoretical guidance for layout optimization, and the presented model provides an effective tool. In practical layout design, besides the power-source inductances, the drain-source mutual inductances, power-gate mutual inductances, and power-drive source mutual inductances also need to be considered. By adjusting the unbalanced parameters through layout optimization, the effects can be adjusted to cancel each other out, making $G_{tol}=\Delta M_{pg}G_g$'$+\Delta M_{pk}G_k$'$+(\Delta M_{ds}+\Delta L_s)G_s$' smallest. Then, the dynamic currents can be balanced. The mutual inductances ΔM_{pg} and ΔM_{pk} can be adjusted by modifying the driving copper layers' locations, layouts and widths, or by adjusting their distances from the power coppers. $\Delta L_s+\Delta M_{ds}$ can be adjusted by modifying the spacings and widths of the power copper layers. Moreover, in DBC circuits, ΔL_s can also be adjusted by changing the lengths and connection points of the power bonding wires. ΔM_{pg} and ΔM_{pk} can be adjusted by changing the connection points of the driving bonding wires. In PCB circuits with middle and large power ratings, paralleled discrete SiC MOSFETs are also usually used to enlarge the current capacity. The imbalanced currents can also induce unbalanced losses and junction temperatures, and there is also a demand to balance the dynamic currents [11]. In PCB circuits, ΔM_{ds} can be changed by directly coupling the drain and power-source traces by PCB wiring, and ΔM_{pg} and ΔM_{pk} can be adjusted by coupling the driving and the power traces. Moreover, this article finds that the dynamic current imbalance can also be reduced by increasing L_s, M_{ds}, and M_{pg}, or decreasing M_{pk}. These parameters can also be directly adjusted by inducing magnetic couplings through PCB wiring.

The low-side layout of the power module in Fig. 32 is preliminarily optimized here as an example. ΔM_{pg} can completely compensate for the effect of $\Delta L_s+\Delta M_{ds}$. However, the presence of 1.39 nH ΔM_{pk} can still produce a large Δi_d. Increasing ΔM_{pg}, decreasing ΔM_{pk}, and decreasing the absolute value of $\Delta L_s+\Delta M_{ds}$ can all decrease $|G_{tol}|$, reducing the current imbalance. Since $|G_g'|$ is larger than $|G_k'|$ and $|G_s'|$, adjusting ΔM_{pg} is the most effective. The locations of gate and drive-source coppers are exchanged, and the distance between gate and power copper

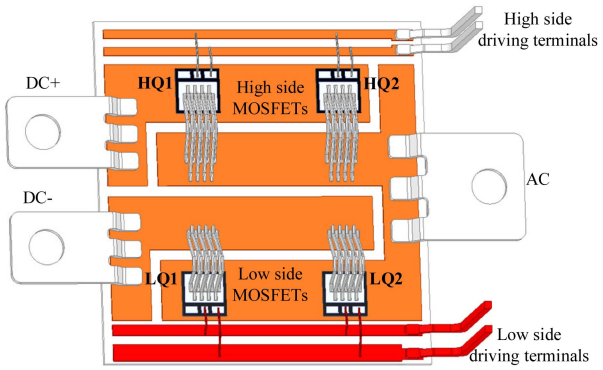

Fig. 35. Optimized power module layout.

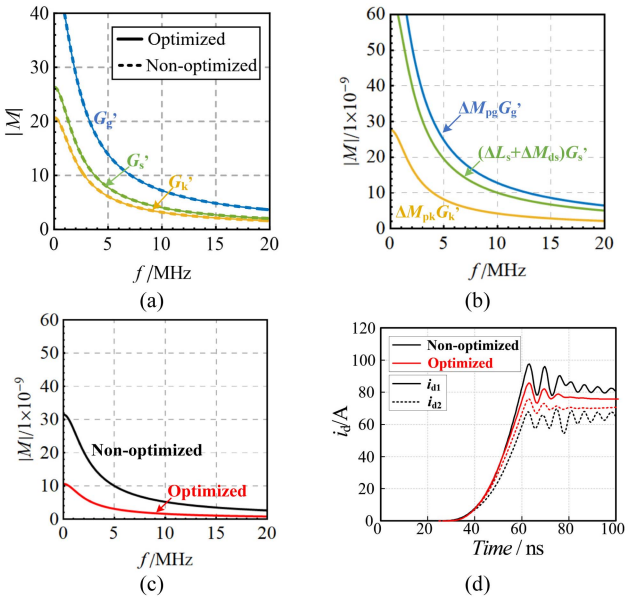

Fig. 36. Comparison of the layouts before and after optimizing. (a) Gains of G_g', G_k', and G_s'. (b) Gains of $\Delta M_{pg}G_g$', $\Delta M_{pk}G_k$', and $(\Delta M_{ds}+\Delta L_s)G_s$' of the optimized layout. (c) Gains of G_{tol}. (d) Turn-ON waveforms (V_{DD} = 600 V, I_{load} = 150 A, R_g = 4 Ω).

layers is reduced, as shown by the red coppers in Fig. 35. Then, ΔM_{pg} is increased to 1.77 nH, ΔM_{pk} is decreased to 1.31 nH, and $\Delta M_{ds}+\Delta L_s$ is not changed due to the unchanged power layout. Then, the dynamic current differences can be reduced. The gains of G_g', G_k', and G_s' before and after the optimization are shown in Fig. 36(a). It can be seen that the gains are almost not changed by the layout optimization. The gains of $\Delta M_{pg}G_g$', $\Delta M_{pk}G_k$', and $(\Delta M_{ds}+\Delta L_s)G_s$' after optimization are shown in Fig. 36(b). Due to the unchanged $\Delta M_{ds}+\Delta L_s$, $|(\Delta M_{ds}+\Delta L_s)G_s'|$ is unchanged compared to Fig. 34(b). Under the increased ΔM_{pg}, $|\Delta M_{pg}G_g'|$ is increased, enlarging its cancel effect on Δi_d. Under the reduced ΔM_{pk}, $|\Delta M_{pk}G_k'|$ is decreased, and its contribution to Δi_d is reduced. Then, $|G_{tol}|$ can be significantly reduced, as shown in Fig. 36(c), and the maximum turn-ON current difference can be reduced by 67.7%, from 29.7 to 9.6 A, as shown in Fig. 36(d). Under the same condition, the switching losses before and after the optimization are shown in Table VIII, where E_1 is the losses

TABLE VIII
COMPARISON OF SWITCHING LOSSES BEFORE AND AFTER OPTIMIZATION

Layout	E_1/ uJ	E_2/ uJ	ΔE/ uJ	E_{ave}/ uJ	$\Delta E/E_{ave}$
Nonoptimized	1189.8	996.2	193.5	1093.0	17.7%
Optimized	1143.5	1075.3	68.2	1109.4	6.1%

of LQ1, E_2 is the losses of LQ2, $E_{ave}=(E_1+E_2)/2$ is the average losses, and $\Delta E=E_1$-E_2 is the unbalanced losses. The unbalanced losses are reduced from 193.5 uJ to 68.2 uJ by the layout optimization. And the unbalanced degree is reduced from 17.7% to 6.1%. On this basis, if ΔM_{pg} and ΔM_{pk} can be further optimized in more effective ways (such as changing the connection points of the drive bonding wires and increasing the distance of the drive-source copper), or if $|\Delta L_s|$ is further decreased (such as by changing the length and connection points of power-source bonding wires), the current imbalance can be further reduced or even eliminated.

The optimal layout in circuits with more paralleled devices will be investigated in future works.

C. Discussions of New Current Balancing Methods

The dynamic current imbalance can also be reduced by increasing L_s, M_{ds}, and M_{pg}, or decreasing M_{pk}. The common parameters can be easily adjusted by inserting coupled inductors into the circuit. For example, in [29], L_s is increased by connecting a full-coupled inductor in the power-source branches to reduce the influence of ΔV_{th}. In PCB circuits, they can also be adjusted by directly coupling the circuit lines.

It is found that inserting full-coupled inductors in the driving loops cannot reduce the unbalanced currents caused by ΔM_{pg} and ΔM_{pk}. If additional coupling is induced in the paralleled gate branches to suppress Δi_g caused by ΔM_{pg} and ΔM_{pk}, the currents can be more balanced.

VI. CONCLUSION

This article further investigates dynamic current sharing mechanisms considering the parasitic mutual inductances to provide more detailed guidance for circuit layout design and current sharing method design.

A dynamic current sharing model considering all the mutual inductances is established. Based on the model, the effect degrees and mechanisms of the unbalanced parameters are compared and analyzed. The main factors causing unbalanced dynamic currents are ΔM_{pg}, ΔM_{pk}, ΔM_{ds}, ΔL_s, and ΔV_{th}, where the effect degrees can be ranked as: $\Delta V_{th}>\Delta M_{pg}>\Delta L_s$ and $\Delta M_{ds}>\Delta M_{pk}$. Moreover, the MOSFET with larger power-gate mutual inductances, smaller power-drive source mutual inductances, larger drain-source mutual inductances, or larger power-source inductances tends to bear lower turn-ON currents and higher turn-OFF currents, which are caused by the induced voltages in the driving circuit. The MOSFET with a larger V_{th} tends to bear lower turn-ON and turn-OFF currents. The proposed model and the conclusions can guide the design of PCB/DBC layouts.

The influences of the common parameters between paralleled branches are also investigated, which can guide the investigations of current balancing methods. The conclusions are summarized as follows.

1) When increasing $M_{\rm gk}$, $|\Delta i_{\rm d}|$ caused by $\Delta M_{\rm pg}$ and $\Delta V_{\rm th}$ will be slightly increased, and $|\Delta i_{\rm d}|$ caused by $\Delta M_{\rm pk}$ will be largely increased, whereas $|\Delta i_{\rm d}|$ caused by $\Delta L_{\rm s}$ and $\Delta M_{\rm ds}$ will be unchanged.
2) Inserting full-coupled inductors in the driving loops can help reduce the unbalanced dynamic currents caused by $\Delta L_{\rm s}$ and $\Delta M_{\rm ds}$, whereas the unbalanced currents caused by $\Delta M_{\rm pg}$, $\Delta M_{\rm pk}$ and $\Delta V_{\rm th}$ will be largely increased. So, when inserting full-coupled inductors, much attention must be paid to $\Delta M_{\rm pg}$, $\Delta M_{\rm pk}$ and $\Delta V_{\rm th}$.
3) The larger $R_{\rm gin}$, the lower $|\Delta i_{\rm d}|$ caused by $\Delta M_{\rm pg}$, $\Delta M_{\rm pk}$, $\Delta L_{\rm s}$ and $\Delta M_{\rm ds}$, the much larger $|\Delta i_{\rm d}|$ caused by $\Delta V_{\rm th}$. When $\Delta V_{\rm th}$ is small, replacing the external gate resistor $R_{\rm g}$ with inside gate resistors $R_{\rm gin}$ can help reduce the dynamic current difference, which can also dampen the oscillation in the paralleled drive loops.
4) Increasing $M_{\rm pg}$ and $M_{\rm ds}$ or decreasing $M_{\rm pk}$ can reduce the current imbalance. Under the same parameter changes, the effect of $M_{\rm pg}$ is the largest. A large value of $L_{\rm s}$ can also help reduce the current imbalance caused by $\Delta M_{\rm pg}$, $\Delta L_{\rm s}$, $\Delta M_{\rm ds}$, and $\Delta V_{\rm th}$. However, changing $M_{\rm pg}$ and $M_{\rm pk}$ will induce a couple between the power loop and driving loop, and increasing $M_{\rm ds}$ and $L_{\rm s}$ will induce a larger power-loop inductance, which requires much attention.

Finally, the contributions of the current sharing model and conclusions in practical current sharing design are discussed. When designing a practical circuit layout, the gains and effect directions of $\Delta M_{\rm pg}G_{\rm g}$', $\Delta M_{\rm pk}G_{\rm k}$', and $(\Delta M_{\rm ds}+\Delta L_{\rm s})G_{\rm s}$' can be analyzed based on the proposed model. The optimizing guidance of $\Delta M_{\rm pg}$ and $\Delta M_{\rm pk}$ and $\Delta M_{\rm ds}$ and $\Delta L_{\rm s}$ can be summarized, making the gain of $G_{\rm tol}=\Delta M_{\rm pg}G_{\rm g}$'$+\Delta M_{\rm pk}G_{\rm k}$'$+(\Delta M_{\rm ds}+\Delta L_{\rm s})G_{\rm s}$' smallest. The unbalanced parameters can be adjusted by modifying the positions, layouts, widths, and spacings of the copper traces, or by modifying the connection points and lengths of the bonding wires. Moreover, new current balancing methods can be investigated based on the influences of the common parameters. By inserting coupled inductors into the circuit or directly coupling the circuit wires, the common parameters $L_{\rm s}$, $M_{\rm ds}$, $M_{\rm pg,}$ and $M_{\rm pk}$ can be easily adjusted. The optimal layout design with more paralleled MOSFETs considering all the effects and the new current sharing methods will be investigated in the future.

APPENDIX

A. Expressions of Common and Differential Inductances

The common and differential power-gate mutual inductances can be expressed as

$$\begin{cases} M_{\rm pg}^{'}=\frac{M_{\rm pg1}^{'}+M_{\rm pg2}^{'}}{2} \\ M_{\rm pg}=\frac{M_{\rm pg1}+M_{\rm pg2}}{2} \\ \Delta M_{\rm pg}=M_{\rm pg1}-M_{\rm pg2} \end{cases} \tag{A1}$$

where

$$\begin{cases} M_{\rm pg1}^{'}=M_{\rm p1g1}+M_{\rm p1g2} \\ M_{\rm pg2}^{'}=M_{\rm p2g2}+M_{\rm p2g1} \\ M_{\rm pg1}=M_{\rm p1g1}-M_{\rm p1g2} \\ M_{\rm pg2}=M_{\rm p2g2}-M_{\rm p2g1}. \end{cases} \tag{A2}$$

The common and differential power-drive source mutual inductances can be expressed as

$$\begin{cases} M_{\rm pk}^{'}=\frac{M_{\rm pk1}^{'}+M_{\rm pk2}^{'}}{2} \\ M_{\rm pk}=\frac{M_{\rm pk1}+M_{\rm pk2}}{2} \\ \Delta M_{\rm pk}=M_{\rm pk1}-M_{\rm pk2} \end{cases} \tag{A3}$$

where

$$\begin{cases} M_{\rm pk1}^{'}=M_{\rm p1k1}+M_{\rm p1k2} \\ M_{\rm pk2}^{'}=M_{\rm p2k2}+M_{\rm p2k1} \\ M_{\rm pk1}=M_{\rm p1k1}-M_{\rm p1k2} \\ M_{\rm pk2}=M_{\rm p2k2}-M_{\rm p2k1}. \end{cases} \tag{A4}$$

The common and differential drain-source mutual inductances can be expressed as

$$\begin{cases} M_{\rm ds}=\frac{M_{\rm ds1}+M_{\rm ds2}}{2} \\ \Delta M_{\rm ds}=M_{\rm ds1}-M_{\rm ds2} \end{cases} \tag{A5}$$

where

$$\begin{cases} M_{\rm ds1}=M_{\rm d1s1}-M_{\rm d1s2} \\ M_{\rm ds2}=M_{\rm d2s2}-M_{\rm d2s1} \end{cases}. \tag{A6}$$

The common and differential power-source inductances can be expressed as follows:

$$\begin{cases} L_{\rm s}=\frac{L_{\rm s1}^{'}+L_{\rm s2}^{'}}{2} \\ \Delta L_{\rm s}=L_{\rm s1}^{'}-L_{\rm s2}^{'} \end{cases} \tag{A7}$$

where

$$\begin{cases} L_{\rm s1}^{'}=L_{\rm s1}-M_{\rm s1s2} \\ L_{\rm s2}^{'}=L_{\rm s2}-M_{\rm s1s2} \end{cases}. \tag{A8}$$

B. Equations of Driving Circuit

The circuit equations of the driving circuit in Fig. 3(b) can be written as follows: (A9) shown at the bottom of the next page.

The transfer functions $G_{\rm g}$, $G_{\rm k}$, $G_{\rm s}$, and $\Delta G_{\rm gs}$ are given by (A10),

$$\begin{cases} G_{\rm g}=\dfrac{b_0+b_1s+b_2s^2}{a_0+a_1s+a_2s^2+a_3s^3+a_4s^4} \\ G_{\rm k}=\dfrac{b_3+b_4s+b_5s^2}{a_0+a_1s+a_2s^2+a_3s^3+a_4s^4} \\ G_{\rm s}=\dfrac{b_6+b_7s+b_8s^2}{a_0+a_1s+a_2s^2+a_3s^3+a_4s^4} \\ \Delta G_{\rm gs}=\dfrac{b_9s^2}{a_0+a_1s+a_2s^2+a_3s^3+a_4s^4} \end{cases} \tag{A10}$$

where b_0–b_9 and a_0–a_4 are given by (A11) and (A12) shown at the bottom of the next page.

C. Simulation Model of Test Circuit

The circuit parameters used in theoretical analysis, as shown in Table II, are the values of the test circuit shown in Fig. 16 with soldered symmetrical inductors. The parameter values are obtained by Q3D simulation. First, the 3-D model of the test circuit without soldered inductors is established in Q3D. The magnetic couplings from the driving board and the circuit outside the dc-link *RC* can be neglected. Then the parasitic inductances in Table II can be obtained by simulating the local circuit shown in Fig. 37(a)–(d). The freewheeling diode is set as a short circuit, the positive side of dc-link *RC* is set as Sink, and the drain electrodes of the MOSFETs are set as Sources. Then, the drain Net is obtained, as shown in Fig. 37(a). The negative side of dc-link *RC* is set as Sink, and the power-source electrodes of the MOSFETs

$$
\begin{cases}
V_{\mathrm{dri}} = v_{\mathrm{pg1}} - v_{\mathrm{pk1}} + L_{\mathrm{gin1}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} + R_{\mathrm{gin}}i_{\mathrm{g1}} + v_{\mathrm{gs1}} + L_{\mathrm{k1}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} + L_{\mathrm{g}}\frac{\mathrm{d}i_{\mathrm{g}}}{\mathrm{d}t} + R_{\mathrm{g}}i_{\mathrm{g}} + M_{\mathrm{g1g2}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} - M_{\mathrm{g1k1}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} - M_{\mathrm{g1k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} \\
\qquad + M_{\mathrm{s1g1}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} - M_{\mathrm{s2g1}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} - M_{\mathrm{g1k1}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} - M_{\mathrm{g2k1}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} + M_{\mathrm{k1k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} - M_{\mathrm{s1k1}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} + M_{\mathrm{s2k1}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \\
V_{\mathrm{dri}} = v_{\mathrm{pg2}} - v_{\mathrm{pk2}} + L_{\mathrm{gin2}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} + R_{\mathrm{gin}}i_{\mathrm{g2}} + v_{\mathrm{gs2}} + L_{\mathrm{k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} + L_{\mathrm{g}}\frac{\mathrm{d}i_{\mathrm{g}}}{\mathrm{d}t} + R_{\mathrm{g}}i_{\mathrm{g}} + M_{\mathrm{g1g2}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} - M_{\mathrm{g2k1}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} - M_{\mathrm{g2k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} \\
\qquad + M_{\mathrm{s1g2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} - M_{\mathrm{s2g2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} - M_{\mathrm{g1k2}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} - M_{\mathrm{g2k2}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} + M_{\mathrm{k1k2}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} - M_{\mathrm{s1k2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} + M_{\mathrm{s2k2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \\
v_{\mathrm{pk1}} + v_{\mathrm{ps1-s}} + v_{\mathrm{ps1-d}} - L_{\mathrm{k1}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} + L_{\mathrm{s1}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} + M_{\mathrm{g1k1}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} + M_{\mathrm{g2k1}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} - M_{\mathrm{k1k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} \\
\qquad + M_{\mathrm{s1k1}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} - M_{\mathrm{s2k1}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} + M_{\mathrm{s1g1}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} + M_{\mathrm{s1g2}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} - M_{\mathrm{s1k1}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} - M_{\mathrm{s1k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} - M_{\mathrm{s1s2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \\
= v_{\mathrm{pk2}} + v_{\mathrm{ps2-s}} + v_{\mathrm{ps2-d}} - L_{\mathrm{k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} - L_{\mathrm{s2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} + M_{\mathrm{g1k2}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} + M_{\mathrm{g2k2}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} - M_{\mathrm{k1k2}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} \\
\qquad + M_{\mathrm{s1k2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} - M_{\mathrm{s2k2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} + M_{\mathrm{s2g1}}\frac{\mathrm{d}i_{\mathrm{g1}}}{\mathrm{d}t} + M_{\mathrm{s2g2}}\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} - M_{\mathrm{s2k1}}\frac{\mathrm{d}i_{\mathrm{k1}}}{\mathrm{d}t} - M_{\mathrm{s2k2}}\frac{\mathrm{d}i_{\mathrm{k2}}}{\mathrm{d}t} + M_{\mathrm{s1s2}}\frac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} \\
v_{\mathrm{gs1}} = \frac{1}{C_{\mathrm{iss}}}\int_0^t (i_{\mathrm{g1}} - i_{\mathrm{c}})\mathrm{d}t \\
v_{\mathrm{gs2}} = \frac{1}{C_{\mathrm{iss}}}\int_0^t (i_{\mathrm{g2}} - i_{\mathrm{c}})\mathrm{d}t \\
i_{\mathrm{k1}} + i_{\mathrm{k2}} = i_{\mathrm{g}} \\
i_{\mathrm{g}} = i_{\mathrm{g1}} + i_{\mathrm{g2}} \\
i_{\mathrm{g1}} = i_{\mathrm{k1}} + i_{\mathrm{s}}
\end{cases}
\tag{A9}
$$

$$
\begin{cases}
b_0 = -\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) \\
b_1 = -C_{\mathrm{iss}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right)\left(2R_{\mathrm{g}} + R_{\mathrm{gin}}\right) \\
b_2 = -0.5C_{\mathrm{iss}}\begin{pmatrix} L'_{\mathrm{gin2}}L'_{\mathrm{k1}} + L'_{\mathrm{gin2}}L'_{\mathrm{k2}} + 4L'_{\mathrm{k1}}L'_{\mathrm{k2}} + L'_{\mathrm{gin2}}L'_{\mathrm{s}} + L'_{\mathrm{k1}}L'_{\mathrm{s}} + L'_{\mathrm{k2}}L'_{\mathrm{s}} + 4L'_{\mathrm{g}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) + L'_{\mathrm{gin1}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) \\ -4L'_{\mathrm{k1}}M_{\mathrm{g1k2}} - 2L'_{\mathrm{s}}M_{\mathrm{g1k2}} - {M_{\mathrm{g1k2}}}^2 - 2\left(2L'_{\mathrm{k2}} + L'_{\mathrm{s}} - M_{\mathrm{g1k2}}\right)M_{\mathrm{g2k1}} - {M_{\mathrm{g2k1}}}^2 \end{pmatrix} \\
b_3 = \left(L'_{\mathrm{s}} - M_{\mathrm{g1k2}} - M_{\mathrm{g2k1}}\right) \\
b_4 = C_{\mathrm{iss}}\left(L'_{\mathrm{s}} - M_{\mathrm{g1k2}} - M_{\mathrm{g2k1}}\right)\left(2R_{\mathrm{g}} + R_{\mathrm{gin}}\right) \\
b_5 = 0.5C_{\mathrm{iss}}\begin{pmatrix} 4L'_{\mathrm{g}}L'_{\mathrm{s}} + L'_{\mathrm{k1}}L'_{\mathrm{s}} + L'_{\mathrm{k2}}L'_{\mathrm{s}} + L'_{\mathrm{gin2}}\left(-L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}} - 2M_{\mathrm{g1k2}}\right) - 4L'_{\mathrm{g}}M_{\mathrm{g1k2}} - 2L'_{\mathrm{k1}}M_{\mathrm{g1k2}} - 2L'_{\mathrm{s}}M_{\mathrm{g1k2}} + {M_{\mathrm{g1k2}}}^2 + \\ L'_{\mathrm{gin1}}\left(L'_{\mathrm{k1}} - L'_{\mathrm{k2}} + L'_{\mathrm{s}} - 2M_{\mathrm{g2k1}}\right) - 2\left(2L'_{\mathrm{g}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}} - 3M_{\mathrm{g1k2}}\right)M_{\mathrm{g2k1}} + {M_{\mathrm{g2k1}}}^2 \end{pmatrix} \\
b_6 = -L'_{\mathrm{k1}} - L'_{\mathrm{k2}} - M_{\mathrm{g1k2}} - M_{\mathrm{g2k1}} \\
b_7 = -C_{\mathrm{iss}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + M_{\mathrm{g1k2}} + M_{\mathrm{g2k1}}\right)\left(2R_{\mathrm{g}} + R_{\mathrm{gin}}\right) \\
b_8 = -C_{\mathrm{iss}}\begin{pmatrix} 2L'_{\mathrm{k1}}L'_{\mathrm{k2}} - L'_{\mathrm{k1}}M_{\mathrm{g1k2}} - {M_{\mathrm{g1k2}}}^2 + L'_{\mathrm{gin2}}\left(L'_{\mathrm{k1}} + M_{\mathrm{g1k2}}\right) - \left(L'_{\mathrm{k2}} + 2M_{\mathrm{g1k2}}\right)M_{\mathrm{g2k1}} + 2L'_{\mathrm{g}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + M_{\mathrm{g1k2}} + M_{\mathrm{g2k1}}\right) \\ +L'_{\mathrm{gin1}}\left(L'_{\mathrm{k2}} + M_{\mathrm{g2k1}}\right) - {M_{\mathrm{g2k1}}}^2 \end{pmatrix} \\
b_9 = C_{\mathrm{iss}}\left(-L'_{\mathrm{k1}}L'_{\mathrm{s}} + L'_{\mathrm{k2}}L'_{\mathrm{s}} - L'_{\mathrm{gin1}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L_{\mathrm{s}}\right)\prime + L'_{\mathrm{gin2}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) + 2L'_{\mathrm{k1}}M_{\mathrm{g1k2}} + {M_{\mathrm{g1k2}}}^2 - 2L'_{\mathrm{k2}}M_{\mathrm{g2k1}} - {M_{\mathrm{g2k1}}}^2\right) \\
a_0 = \left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) \\
a_1 = 2C_{\mathrm{iss}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right)\left(R_{\mathrm{g}} + R_{\mathrm{gin}}\right) \\
a_2 = C_{\mathrm{iss}}\begin{pmatrix} L'_{\mathrm{gin2}}L'_{\mathrm{k1}} + L'_{\mathrm{gin2}}L'_{\mathrm{k2}} + 2L'_{\mathrm{k1}}L'_{\mathrm{k2}} + L'_{\mathrm{gin2}}L'_{\mathrm{s}} + L'_{\mathrm{k1}}L'_{\mathrm{s}} + L'_{\mathrm{k2}}L'_{\mathrm{s}} + 2L'_{\mathrm{g}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) + L'_{\mathrm{gin1}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) \\ -2L'_{\mathrm{k1}}M_{\mathrm{g1k2}} - {M_{\mathrm{g1k2}}}^2 - 2L'_{\mathrm{k2}}M_{\mathrm{g2k1}} - {M_{\mathrm{g2k1}}}^2 + 2C_{\mathrm{iss}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right)R_{\mathrm{g}}R_{\mathrm{gin}} + C_{\mathrm{iss}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right){R_{\mathrm{gin}}}^2 \end{pmatrix} \\
a_3 = {C_{\mathrm{iss}}}^2\begin{pmatrix} \left(L'_{\mathrm{k1}}L'_{\mathrm{s}} + L'_{\mathrm{k2}}L'_{\mathrm{s}} + \left(2L'_{\mathrm{s}} - M_{\mathrm{g1k2}} - M_{\mathrm{g2k1}}\right)\left(M_{\mathrm{g1k2}} + M_{\mathrm{g2k1}}\right)\right)R_{\mathrm{g}} + L'_{\mathrm{gin1}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right)\left(R_{\mathrm{g}} + R_{\mathrm{gin}}\right) \\ + \left(L'_{\mathrm{k2}}L'_{\mathrm{s}} + 2L'_{\mathrm{g}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + Ls\right) + L'_{\mathrm{k1}}\left(2L'_{\mathrm{k2}} + L'_{\mathrm{s}} - 2M_{\mathrm{g1k2}}\right) - {M_{\mathrm{g1k2}}}^2 - 2L'_{\mathrm{k2}}M_{\mathrm{g2k1}} - {M_{\mathrm{g2k1}}}^2\right)R_{\mathrm{gin}} \\ +L'_{\mathrm{gin2}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right)\left(R_{\mathrm{g}} + R_{\mathrm{gin}}\right) \end{pmatrix} \\
a_4 = {C_{\mathrm{iss}}}^2\begin{pmatrix} L'_{\mathrm{gin1}}L'_{\mathrm{gin2}}L'_{\mathrm{k1}} + L'_{\mathrm{gin1}}L'_{\mathrm{gin2}}L'_{\mathrm{k2}} + L'_{\mathrm{gin1}}L'_{\mathrm{k1}}L'_{\mathrm{k2}} + L'_{\mathrm{gin2}}L'_{\mathrm{k1}}L'_{\mathrm{k2}} + L'_{\mathrm{gin1}}L'_{\mathrm{gin2}}L'_{\mathrm{s}} + L'_{\mathrm{gin2}}L'_{\mathrm{k1}}L'_{\mathrm{s}} + L'_{\mathrm{gin1}}L'_{\mathrm{k2}}L'_{\mathrm{s}} + \\ L'_{\mathrm{k1}}L'_{\mathrm{k2}}L'_{\mathrm{s}} - 2L'_{\mathrm{gin2}}L'_{\mathrm{k1}}M_{\mathrm{g1k2}} - L'_{\mathrm{gin2}}{M_{\mathrm{g1k2}}}^2 - L'_{\mathrm{k1}}{M_{\mathrm{g1k2}}}^2 - L'_{\mathrm{s}}{M_{\mathrm{g1k2}}}^2 - 2\left(L'_{\mathrm{gin1}}L'_{\mathrm{k2}} + \left(L'_{\mathrm{s}} - M_{\mathrm{g1k2}}\right)M_{\mathrm{g1k2}}\right)M_{\mathrm{g2k1}} \\ -\left(L'_{\mathrm{gin1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}} - 2M_{\mathrm{g1k2}}\right){M_{\mathrm{g2k1}}}^2 + L'_{\mathrm{g}}\begin{pmatrix} L'_{\mathrm{k1}}L'_{\mathrm{s}} + L'_{\mathrm{k2}}L'_{\mathrm{s}} + L'_{\mathrm{gin1}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) + L'_{\mathrm{gin2}}\left(L'_{\mathrm{k1}} + L'_{\mathrm{k2}} + L'_{\mathrm{s}}\right) \\ +2L'_{\mathrm{s}}M_{\mathrm{g1k2}} - {M_{\mathrm{g1k2}}}^2 + 2L'_{\mathrm{s}}M_{\mathrm{g2k1}} - 2M_{\mathrm{g1k2}}M_{\mathrm{g2k1}} - {M_{\mathrm{g2k1}}}^2 \end{pmatrix} \end{pmatrix}
\end{cases}
\tag{A11}
$$

where

$$
\begin{cases}
L_{\mathrm{g}} = L_{\mathrm{g}} + M_{\mathrm{g1g2}} + M_{\mathrm{k1k2}} \\
L_{\mathrm{gin1}} = L_{\mathrm{gin1}} - M_{\mathrm{g1g2}} - M_{\mathrm{g1k1}} + \left(M_{\mathrm{s1g1}} - M_{\mathrm{s2g1}}\right) - \left(M_{\mathrm{s1k1}} - M_{\mathrm{s2k1}}\right) \\
L_{\mathrm{gin2}} = L_{\mathrm{gin2}} - M_{\mathrm{g1g2}} - M_{\mathrm{g2k2}} - \left(M_{\mathrm{s1g2}} - M_{\mathrm{s2g2}}\right) + \left(M_{\mathrm{s1k2}} - M_{\mathrm{s2k2}}\right) \\
L_{\mathrm{k1}} = L_{\mathrm{k1}} - M_{\mathrm{k1k2}} - M_{\mathrm{g1k1}} - \left(M_{\mathrm{s1g1}} - M_{\mathrm{s2g1}}\right) + \left(M_{\mathrm{s1k1}} - M_{\mathrm{s2k1}}\right) \\
L_{\mathrm{k2}} = L_{\mathrm{k2}} - M_{\mathrm{k1k2}} - M_{\mathrm{g2k2}} - \left(M_{\mathrm{s1k2}} - M_{\mathrm{s2k2}}\right) + \left(M_{\mathrm{s1g2}} - M_{\mathrm{s2g2}}\right) \\
L_{\mathrm{s}} = L_{\mathrm{s1}} + L_{\mathrm{s2}} - 2M_{\mathrm{s1s2}} + M_{\mathrm{g1k1}} + M_{\mathrm{g2k2}} - \left(M_{\mathrm{s1g2}} - M_{\mathrm{s2g2}}\right) - \left(M_{\mathrm{s1k2}} - M_{\mathrm{s2k2}}\right) + \left(M_{\mathrm{s1g1}} - M_{\mathrm{s2g1}}\right) + \left(M_{\mathrm{s1k1}} - M_{\mathrm{s2k1}}\right).
\end{cases}
\tag{A12}
$$

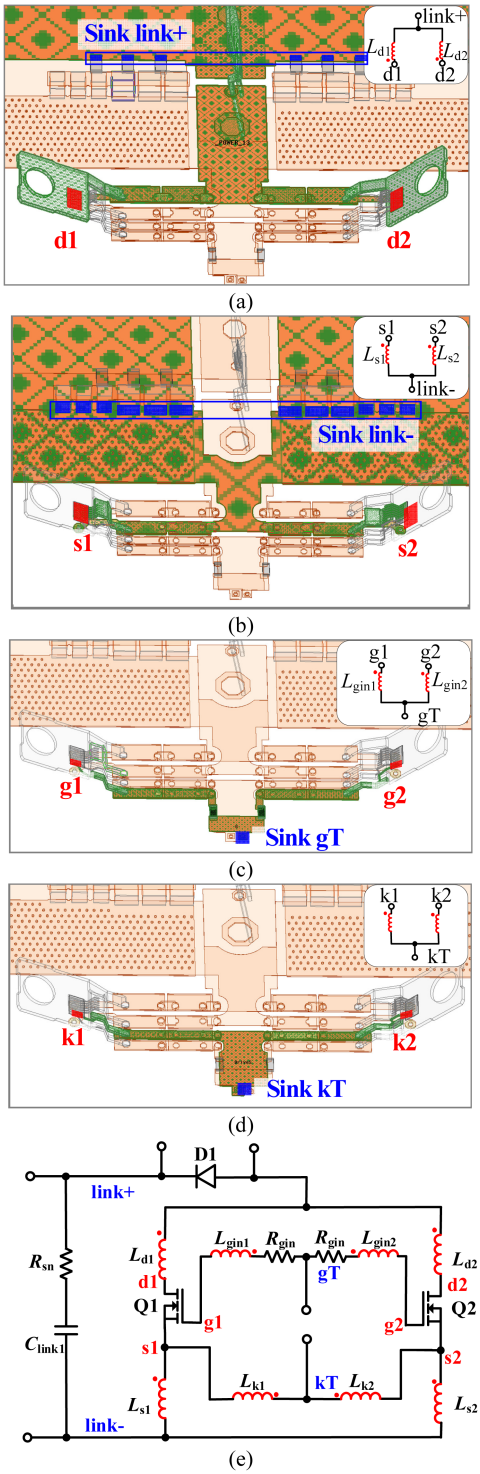

Fig. 37. Simulation setups and equivalent circuit. (a) Drain net. (b) Power-source net. (c) Gate net. (d) Drive-source net. (e) Equivalent circuit.

are set as Sources. Then, the power-source Net is obtained, as shown in Fig. 37(b). The gate terminal is set as Sink, and the gate electrodes of the MOSFETs are set as Sources. Then, the gate Net can be obtained as shown in Fig. 37(c). The drive-source terminal is set as Sink, and the drive-source electrodes of the MOSFETs are set as Sources. Then, the drive-source Net is shown in Fig. 37(d).

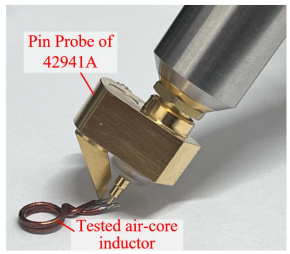

Fig. 38. Test setup of the air-core inductors.

TABLE IX
COMPARISON OF MEASURED AND SIMULATED INDUCTANCES OF AIR-CORE INDUCTORS

Inductor parameters	Experiment/ nH	Q3D simulation/nH	Error
$n = 1, r = 1.75$ mm	7.93	7.74	2.4 %
$n = 1, r = 2.5$ mm	13.38	12.93	3.4 %
$n = 2, r = 1.75$ mm	19.12	19.45	1.7 %
$n = 2, r = 2.5$ mm	29.45	30.47	3.5 %

The partial inductance matrix is calculated based on these setups, where the board self-inductance and mutual inductance can be obtained. Since the positive directions of the branches in the simulation are not the same as the definitions in Fig. 1, the signs of the simulated mutual inductances are corrected. Finally, the self-inductance and mutual inductance in Table II are obtained by adding the soldered inductors, where the inductances of the inductors are also obtained by Q3D simulation. The equivalent circuit of the simulation model is shown in Fig. 37(e).

To verify the accuracy and validity of the Q3D simulation model, we tested the inductance values of several air-core inductors and branches of the PCB test circuit for comparison. The tested inductance values are obtained by Agilent 4294A Impedance Analyzer, which can provide high precision. The test setup of the air-core inductors is shown in Fig. 38. The inductances are measured directly on the two terminals. 42941A Impedance Probe and its pin probe are used to guarantee accuracy, which are carefully calibrated and compensated. Four inductors with different parameters are tested. The measured and simulated parasitic inductances under 5 MHz are compared, as shown in Table IX. The errors between the measured and simulated values are all within 4%. When testing the PCB test circuit, since it is impossible to mount the probe on the internal dies of the TO-247 MOSFETs, only the inductances of the PCB are measured. Due to the limited distance between the two pins of the probe, only the four partial branches shown in Fig. 38 are measured, including the partial drain path DP, the partial power-source path SP, the partial gate path GP, and the partial drive-source path KP. The air-core inductors are soldered on the back side of the PCB to facilitate measurement, which are not depicted in Fig. 39. In the drain, gate, or drive-source branches, one $n = 1, r = 1.75$ mm and one $n = 2, r = 1.75$ mm inductors are soldered. In the power-source branch, two $n = 1$, $r = 1.75$ mm inductors are connected. Moreover, to eliminate the influences of the paralleled paths, the MOSFETs are removed from the PCB. The tested and Q3D simulated results under 5 MHz are compared as shown in Table X, where the errors are all within 8%. Since

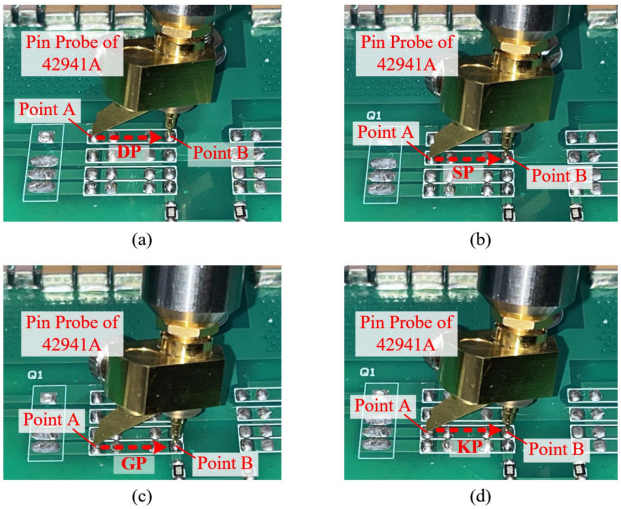

Fig. 39. Test setup of the test circuit branches. (a) Partial drain path DP. (b) Partial power-source path SP. (c) Partial gate path GP. (d) Partial drive-source path KP.

TABLE X
COMPARISON OF MEASURED AND SIMULATED INDUCTANCES OF PCB BRANCHES

Branches	Experiment/nH	Q3D simulation model/nH	Error
DP	35.92	33.4	7.0%
SP	23.87	22.51	5.7%
GP	36.44	33.66	7.6%
KP	35.06	34.61	1.3%

the theoretical and experimental analyses do not require very high accuracy of the inductance values, the small errors of the Q3D simulation models can well satisfy the demand for analyses.

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