Decoupled Continuous Control Set Model Predictive Control for T-Type Three-Phase Four-Leg Three-Level Inverters Driving Constant Power Loads

Yi Zhu, *Graduate Student Member, IEEE*, Huiqing Wen, *Senior Member, IEEE*, Yong Yang, *Senior Member, IEEE*, Jianliang Mao, Pan Wang, Weiguo Huang, and Jose Rodriguez, *Life Fellow, IEEE*

***Abstract*—The control coupling and stability of three-phase photovoltaic systems with constant power loads (CPLs) are two key technical issues that urgently need to be addressed. However, current methods are difficult to solve both technical challenges simultaneously. To address these issues, this article proposes a novel decoupled continuous control set model predictive control (CCS-MPC) strategy for *LC*-filter T-type three-phase four-leg three-level voltage source inverters (3P4L-3L-VSIs) driving CPLs. The control strategy is developed in $\alpha\beta\gamma$ frame. The model of 3P4L-3L-VSIs is first transformed from *abc* frame to the $\alpha\beta\gamma$ frame to remove the coupling effects in the *abc* frame. Then based on the decoupled model in the $\alpha\beta\gamma$ frame, a novel CCS-MPC strategy is proposed to provide balanced sinusoidal voltages. The α and β components are regulated by the A, B, and C legs, while the zero-sequence component is regulated by the N leg. To confirm the effectiveness of the proposed strategy, both simulation and experimental results are presented to verify the proposed decoupled CCS-MPC strategy. The results show that the proposed control achieves low computational burden and total harmonic distortion and can increase the stability margin especially for CPLs compared with the commonly used PI-based control, PR-based control, and deadbeat control.**

***Index Terms*—Continuous control set model predictive control (CCS-MPC), fixing control frequency, three-phase four-leg voltage source inverter.**

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Yi Zhu and Huiqing Wen are with the Xi'an Jiaotong-Liverpool University, Suzhou 215123, China (e-mail: yi.zhu2304@student.xjtlu.edu.cn; huiqing.wen@xjtlu.edu.cn).

Yong Yang and Weiguo Huang are with the School of Rail Transportation, Soochow University, Suzhou 215131, China (e-mail: yangy1981@suda.edu.cn; wghuang@suda.edu.cn).

Jianliang Mao and Pan Wang are with the Jiangsu Koyoe Energy Technology Company Ltd., Suzhou 215128, China (e-mail: maojianliang@koyoe.com; wangpan@koyoe.com).

Jose Rodriguez is with the Faculty of Engineering, Universidad San Sebastian Santiago, Santiago 8370146, Chile (e-mail: jose.rodriguezp@uss.cl).

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I. Introduction

With the growing demand for sustainable energy sources worldwide, voltage source inverters (VSIs) have been widely regarded as the preferred interface between dc distributed power supplies such as photovoltaic panels and ac loads. To achieve low total harmonic distortion (THD), three-level is recommended for power converters [1]. Three-level technologies of VSIs can be achieved by neutral-point-clamped topology, flying-capacitor topology, T-type topology, and a family of modular multilevel cascaded topology. Among the various three-level topologies, T-type topology, as shown in Fig. 1, is preferred for three-level VSIs due to its distinct merits of fewer components, high efficiency, and easy implementation [2]. As a result, T-type three-level VSIs have gained wide attention from both the industrial field and research field. To supply unbalanced and nonlinear loads, the three-level four-wire voltage source inverter is proposed, which has been widely employed in energy storage systems. However, in order to eliminate the zero-sequence component of output current, dc components must be injected into the modulation signals [3], which is a factor that can cause instability of the system. As a result, T-type three-phase four-leg three-level voltage source inverters (3P4L-3L-VSIs) are proposed for unbalanced and nonlinear loads [4]. Three of the four legs are responsible for regulating the output voltage and the rest is responsible for eliminating the zero-sequence components. As a result, with the control of the fourth leg, the zero-sequence components can be decoupled from the positive and negative sequences. However, the main difficulties of the design of 3P4L-3L-VSIs lie in the control strategy due to the THD and transient response requirement of modern power grids [5]. Thus, the control strategies of 3P4L-3L-VSIs have been extensively investigated.

The control strategies of T-type 3P4L-3L-VSIs can be categorized as linear control strategies and nonlinear control strategies. Linear control strategies usually perform in the *dq* frame or $\alpha\beta\gamma$

frame with a combined structure of proportional–integral (PI) controllers and proportional–resonant (PR) controllers [6], [7], [8], [9]. For instance, T-type 3P4L-3L-VSIs usually employ PI control or PR control to regulate the output voltage. In order to eliminate the steady-state error, PR control is preferred in tracking the ac reference. Another commonly used method is to apply the park transformation to the measured ac voltages and references, thus, the ac values are transformed to dc values and PI control can be used to regulate the output voltage without steady-state error [8], [9]. However, the inertia produced by PI-based controllers can cause limited dynamic performance [10], bringing challenges to drive complex loads in ac grids. Considering the nonlinear property of VSI systems caused by the switching behaviors, dead zones, and the load systems, some nonlinear control strategies have been proposed to improve the control performance of VSIs. Yang et al. [11] proposed a novel cascaded repetitive controller, which simultaneously achieves excellent dynamic and steady-state responses. A deadbeat control of four-legs VSIs is proposed in [12]. The control strategy is verified by nonlinear and unbalanced loads. Another important issue of T-type three-level inverters is the neutral-point (NP) voltage balance. For three-level power converters, when NP voltage unbalance happens, the power quality will be affected.

As a nonlinear control strategy, model predictive control (MPC) can achieve both fast transient response and good robustness compared with PI-based controllers when applied in power converters [13], which has been applied in ac–dc [14], dc–ac [15], [16], [17], dc–dc converters [18], [19], [20], and motor drive systems [21], [22], [23]. MPC strategies can be categorized as finite control set MPC (FCS-MPC) [24] and continuous control set MPC (CCS-MPC) [3].

FCS-MPC is featured as a predefined FCS. A cost function is defined and the best element is selected from the FCS according to the rule of minimizing the cost function [25], [26]. Neutral-potential (NP) balance is an important issue in FCS-MPC for T-type three-phase three-level (3P-3L) VSIs. In [27], an improved FCS-MPC for T-Type 3P-3L converters is proposed. The authors propose a sector optimization method with combined virtual vectors, which achieves NP balance and low THD. FCS-MPC strategies are also studied for four-leg VSIs with unbalanced load [28]. In [29], a weighting factor is introduced to the cost function considering the need of the NP balance. However, the tunning process of the weighting factor is time-wasting, and the weighting factor can also be an unstable factor for the inverter. As a result, Yang et al. [15], [30] proposed an FCS-MPC strategy without weighting factors, which avoids the process of tunning the weighting factor. To decrease the system complexity and cost, Zheng et al. [25] proposed a current sensorless FCS-MPC strategy for *LC*-filter VSIs. The load and inductor currents are estimated online with system variables. The control strategy is verified by various loads.

Different from FCS-MPC, CCS-MPC adopts continuous control sets instead of FCSs. In each control period, duty cycles for each phase are calculated by solving the optimization problems analytically with the Lagrange multiplier method or other analytical methods [3], [26]. In [3], a CCS-MPC strategy for three-phase four-wire three-level VSIs (3P4L-3L-VSIs) is proposed. NP balance is achieved by dc component injection. Compared with FCS-MPC for 3P4L-3L-VSIs in [15], the online optimization process is avoided by solving the optimization problems analytically offline, which reduces the calculation burden of digital controllers. In [26], the Lagrange multiplier method is employed to solve the optimization problem analytically. Generally speaking, CCS-MPC can achieve low computational burden and THD when applied in dc–ac converters.

Deadbeat control is another model-based control strategy as a substitute for PI-based control strategies, which has been applied to dc–dc [31] and dc–ac converters [12], [32]. Instead of calculating the duty cycle based on the optimization model, deadbeat control generates the reference signal for pulse width modulation (PWM) based on control error at the end of each control period. When the model parameters in the control algorithm are matched with the parameters in the physical system, low THD and less computational burden can be achieved.

With the widespread use of motor loads or cascaded converters with voltage feedback regulation, the instability of power electronic systems has become increasingly challenging due to the negative impedance characteristics of these constant power loads (CPLs) [33].

To address the stability issues caused by CPLs, much research has been conducted to reveal the mechanism of the system instability. In [34], a stability criterion based on the ratio of source impedance and load impedance has been proposed. As a result, the problem lies in the impedance modeling technologies of power converters. The researchers have proposed the impedance model of VSIs in *abc* [35], *dq* [36], and sequence [37] frames. Yang et al. [38] showed that the voltage source converters (VSCs) reach a high impedance in the low frequency, which can cause crossovers of (-1,0j) in the Nyquist plot of the source-load impedance ratio. As a result, works have been done to shape the source converter's output impedance [39] or the load converter's input impedance [40], [41] through virtual impedance. The virtual impedance method is also applied to ac systems to prevent the instability caused by the weak grid [42]. Therefore, a consensus has been reached on improving the stability of electrical systems under CPLs, which is to meet the impedance matching principle of system stability by effectively adjusting the output impedance of VSCs or the input impedance of CPLs. However, the output impedance shaping effect of MPC has not been considered right now.

In this article, a novel continuous control set MPC strategy for T-type 3P4L-3L-VSIs is proposed. The control strategy is developed in $\alpha\beta\gamma$ frame, which realizes zero steady-state error. NP balance is achieved through zero-sequence voltage injection in the N leg modulation signal. The control strategy shows improved steady-state and dynamic performance when driving unbalanced and nonlinear loads. Moreover, the control strategy provides extra stability margin when driving CPLs. To evaluate the practicability of the control strategy, considering the computing power of digital controllers, the execution time and THD of the proposed control strategy are compared with the PI-based control in the *dq* frame [8], the PR-based control in the *abc* frame [50], and deadbeat control [12]. The control strategy proposed in this article takes less time than the PI-based

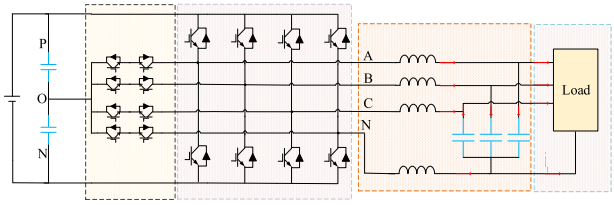

Fig. 1. Topology of the T-type 3P4L-3L-VSIs.

TABLE I
RELATIONSHIPS BETWEEN SWITCH STATE AND OUTPUT VOLTAGE

S_1	S_2	S_3	S_4	Output Voltage
1	1	0	0	V_P
0	1	1	0	0
0	0	1	1	$-V_n$

control and PR-based control and shows lower THD than both of the three control strategies.

The rest of this article is organized as follows. Section II presents the topology and mathematical model of T-type 3P4L-3L-VSIs. The principles of the proposed FCS-MPC and the stability issue when driving CPLs are explained in Section III. Both simulation and experimental results are presented in Section IV. Finally, Section V concludes this article.

II. Topology and Mathematical Model

A. Topology of the Inverter

Fig. 1 shows the topology of T-type 3P4L-3L-VSIs. The topology contains four legs, which are denoted as Phase A, Phase B, Phase C, and Phase N. Each phase of the leg contains four power switches, by controlling the ON–OFF sequence of the power switches, three-level can be achieved. V_P and V_L are the voltage of the upper dc-link capacitor and the lower dc-link capacitor. V_{ca}, V_{cb}, and V_{cc} are the output voltage. i_{La}, i_{Lb}, and i_{Lc} are the output current. i_{ca}, i_{cb}, and i_{cc} are the currents flowing through the output capacitors. i_a, i_b, and i_c are the currents on the load. The filter inductance and capacitors are denoted as L_f and C_f. It should be mentioned that the filter inductance of phase N is denoted as L_n.

Table I illustrates the relationships between the ON–OFF states of S_1, S_2, S_3, S_4 and the output voltage of the inverter. The output voltage of phases A, B, and C is denoted as V_{aN}, V_{bN}, and V_{cN}. In Table I, "1" means that the power switch is on while "0" means that the power switch is OFF. When S_1, S_2 is ON and S_3, S_4 is OFF, the output of the bridge is connected to the "P" point and the output voltage is V_p. When S_2, S_3 is ON and S_1, S_4 is OFF, the output voltage of the bridge is clamped to the neutral-point voltage of the bus capacitors. When S_3, S_4 are ON and S_1, S_2 are OFF, the output of the bridge is connected to the "N" point and the output voltage is V_n [3]. When the NP balance is achieved, it can be assumed that $V_p = V_n$.

The relationships between the switch logic and the output voltage are illustrated in Fig. 2. The current path can also be developed according to the output voltage of the bridge.

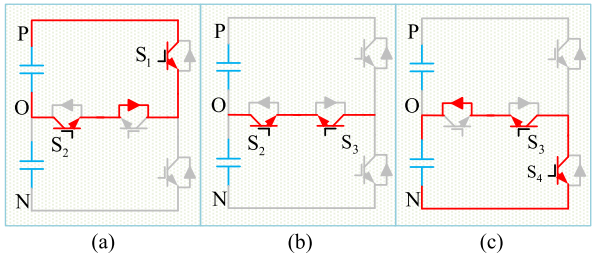

Fig. 2. Switch logic. (a) Output V_p. (b) Output 0. (c) Output V_n.

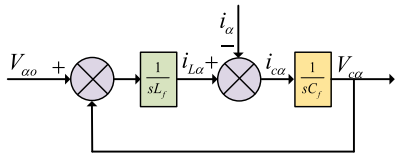

Fig. 3. Block diagram of the filter in phase α.

For simplicity, only the output voltage of a single bridge is considered in Fig. 2.

It should be mentioned that the control strategy is developed in the $\alpha\beta\gamma$ frame. As a result, the system variables are transformed into the $\alpha\beta\gamma$ frame with the Clark transformation, as is shown in

$$\begin{pmatrix} V_{c\alpha} \\ V_{c\beta} \\ V_{c\gamma} \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \begin{pmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{pmatrix}. \tag{1}$$

B. Mathematical Model of the Inverter

In (1), $V_{c\alpha}$, $V_{c\beta}$, and $V_{c\gamma}$ are V_{ca}, V_{cb}, and V_{cc} in $\alpha\beta\gamma$ frame, respectively. As Clark transformation is a linear transformation, the model of the inverter in the *abc* frame can also be applied in $\alpha\beta\gamma$ frame.

The block diagram of the low-pass filter is illustrated in Fig. 3. Only the block diagram in phase α is considered as there are no differences between phases α, β, and γ.

To derive the system model, the dynamic of the energy storage components should be considered first. It is worth mentioning that considering the easy implementation of the CCS-MPC, the series resistance of the filter inductance is ignored. The dynamic of the filter inductance is derived according to Kirchhoff's second law

$$\begin{pmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{pmatrix} = \begin{pmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{pmatrix} + \begin{pmatrix} L_f & 0 & 0 \\ 0 & L_f & 0 \\ 0 & 0 & L_f \end{pmatrix} \frac{d}{dt} \begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} - \begin{pmatrix} L_n & 0 & 0 \\ 0 & L_n & 0 \\ 0 & 0 & L_n \end{pmatrix} \frac{d}{dt} \begin{pmatrix} i_{Ln} \\ i_{Ln} \\ i_{Ln} \end{pmatrix}. \tag{2}$$

It should be mentioned that the sum of the currents on each is zero

$$i_{La} + i_{Lb} + i_{Lc} + i_{Ln} = 0. \tag{3}$$

In the normal state, the sum of the three-phase voltage is zero. Thus,

$$V_{AN} + V_{BN} + V_{CN} = 0 \tag{4}$$

$$V_{ca} + V_{cb} + V_{cc} = 0. \tag{5}$$

Substitute (3), (4), and (5) into (2), then multiplying both sides of (2) with (1) [12], we can derive

$$\frac{d}{dt}\begin{pmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L\gamma} \end{pmatrix} = \begin{pmatrix} \frac{1}{L_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f+3L_n} \end{pmatrix} \begin{pmatrix} V_{\alpha N} - V_{c\alpha} \\ V_{\beta N} - V_{c\beta} \\ V_{\gamma N} - V_{c\gamma} \end{pmatrix}. \tag{6}$$

The dynamic of the filter capacitors is also considered according to the Kirchhoff second law

$$\frac{d}{dt}\begin{pmatrix} V_{c\alpha} \\ V_{c\beta} \\ V_{c\gamma} \end{pmatrix} = \frac{1}{C_f}\begin{pmatrix} i_{L\alpha} - i_{\alpha} \\ i_{L\beta} - i_{\beta} \\ i_{L\gamma} - i_{\gamma} \end{pmatrix}. \tag{7}$$

It should be mentioned that the control signals of phase N are generated according to the law

$$V_{No} = -\frac{V_{aN} + V_{bN} + V_{cN}}{3}. \tag{8}$$

Considering that

$$V_{ao} + V_{bo} + V_{co} = 0. \tag{9}$$

As a result, we can derive

$$\begin{cases} V_{ao} = V_{aN} + V_{No} \\ V_{bo} = V_{bN} + V_{No} \\ V_{co} = V_{cN} + V_{No} \end{cases} \tag{10}$$

which means that the control signals can be derived according to the calculated voltages V_{aN}, V_{bN}, and V_{cN}.

In (6) and (7), $V_{c\alpha}$, $V_{c\beta}$, and $V_{c\gamma}$ are the Clark transformation of V_{ca}, V_{cb}, and V_{cc}. $i_{L\alpha}$, $i_{L\beta}$, and $i_{L\gamma}$ are the Clark transformation of i_{La}, i_{Lb}, and i_{Lc}. $V_{\alpha N}$, $V_{\beta N}$, and $V_{\gamma N}$ are the Clark transformation of V_{aN}, V_{bN}, and V_{cN}. i_{α}, i_{β}, and i_{γ} are the Clark transformation of i_a, i_b, and i_c.

III. Principle of CCS-MPC

A. Proposed CCS-MPC

The reference voltage of output filter capacitors is calculated as

$$\begin{cases} V_{ca}{}^*(t) = V_m \cos(w_{ref}t) \\ V_{cb}{}^*(t) = V_m \cos\left(w_{ref}t - \frac{2\pi}{3}\right) \\ V_{cc}{}^*(t) = V_m \cos\left(w_{ref}t + \frac{2\pi}{3}\right) \end{cases} \tag{11}$$

where $V_{ca}{}^*(t)$, $V_{cb}{}^*(t)$, and $V_{cc}{}^*(t)$ are the output voltage reference. V_m is the maximum value of output voltage. w_{ref} is the reference angular frequency. $V_{c\alpha}$, $V_{c\beta}$, and $V_{c\gamma}$ are derived by applying Clark transformation to (11). A cost function is defined according to the deviation of the output voltage

$$CF = (V_{c\alpha}{}^*(k+2) - V_{c\alpha}(k+2))^2 + \Big(V_{c\beta}{}^*(k+2) - V_{c\beta}(k+2)\Big)^2 + (V_{c\gamma}{}^*(k+2) - V_{c\gamma}(k+2))^2. \tag{12}$$

In this article, *x(k)* means the value of state variable *x* in the control period *k*. It is mentioned that there is a control delay when implementing the control algorithm in the digital signal processor (DSP) [44]. As a result, the cost function is defined according to the deviation of the output voltage in the next two control periods.

The key of MPC is selecting a duty cycle to minimize the cost function. As a result, the output voltage in the following two control periods ($V_{c\alpha}(k+2)$, $V_{c\beta}(k+2)$, and $V_{c\gamma}(k+2)$) should be predicted. The discrete model of the three-phase four-leg three-level VSIs is derived according to the dynamic equations of the energy-storage components. The Euler method is applied to discretize (6) and (7)

$$i_{L\alpha}(k+1) = i_{L\alpha}(k) + \frac{T_s}{L_f}(V_{\alpha N}(k) - V_{c\alpha}(k)) \tag{13}$$

$$V_{c\alpha}(k+1) = V_{c\alpha}(k) + \frac{T_s}{C_f}(i_{L\alpha}(k) - i_{\alpha}(k)) \tag{14}$$

where T_s is the time of a control period. Substitute k with $k+1$, we can derive

$$i_{L\alpha}(k+2) = i_{L\alpha}(k+1) + \frac{T_s}{L_f}(V_{\alpha N}(k+1) - V_{c\alpha}(k+1)) \tag{15}$$

$$V_{c\alpha}(k+2) = V_{c\alpha}(k+1) + \frac{T_s}{C_f}(i_{L\alpha}(k+1) - i_{\alpha}(k+1)). \tag{16}$$

The load currents can be assumed as a constant in the adjacent two control periods, as is shown in [12].

$$i_{\alpha}(k+1) = i_{\alpha}(k). \tag{17}$$

Substitute (14) into (15), we can derive

$$V_{c\alpha}(k+2) = \frac{{T_s}^2}{L_f C_f}V_{\alpha N}(k) + \left(1 - \frac{{T_s}^2}{L_f C_f}\right)V_{c\alpha}(k) + \frac{2T_s}{C_f}(i_{L\alpha}(k) - i_{\alpha}(k)). \tag{18}$$

The duty cycle in each control period can be calculated by minimizing the cost function in (12)

$$\frac{\partial CF}{\partial V_{\alpha N}(k)} = 0, \frac{\partial CF}{\partial V_{\beta N}(k)} = 0, \frac{\partial CF}{\partial V_{\gamma N}(k)} = 0. \tag{19}$$

By solving (19), we can derive

$$\begin{cases} V_{c\alpha}(k+2) = V_{c\alpha}{}^*(k+2) \\ V_{c\beta}(k+2) = V_{c\beta}{}^*(k+2) \\ V_{c\gamma}(k+2) = V_{c\gamma}{}^*(k+2). \end{cases} \tag{20}$$

The output voltage references in the next two control periods are calculated according to (11)

$$\begin{cases} V_{ca}{}^*(k+2) = V_m \cos(w_{ref}t(k+2)) \\ V_{cb}{}^*(k+2) = V_m \cos\left(w_{ref}t(k+2) - \frac{2\pi}{3}\right) \\ V_{cc}{}^*(k+2) = V_m \cos\left(w_{ref}t(k+2) + \frac{2\pi}{3}\right). \end{cases} \tag{21}$$

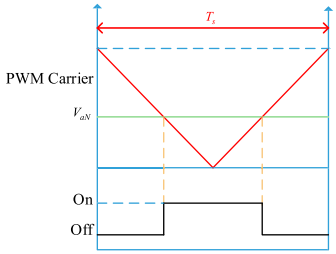

Fig. 4. Carrierd-based pulsewidth modulation.

Substitute (18) and (21) into (20), we can derive

$$V_{\alpha N}(k) = \frac{2L_f}{T_s}(i_\alpha(k) - i_{L\alpha}(k)) + \left(1 - \frac{L_f C_f}{{T_s}^2}\right) V_{c\alpha}(k) + \frac{L_f C_f}{{T_s}^2} {V_{c\alpha}}^*(k+2) \tag{22}$$

$V_{\beta N}(k)$and $V_{\gamma N}(k)$ can also be calculated, as shown in (10)–(19). The signals of power switches are generated by carried-based pulse-width modulation (CBPWM) technology due to its distinct merits of easy implementation. The principle of CBPWM is shown in Fig. 4.

The control diagram of the proposed CCS-MPC for three-phase three-level four-leg converters is illustrated in Fig. 5. The sampled values are transformed to $\alpha\beta\gamma$ frame, and then the output voltage reference is calculated according to (22). The calculated reference ${V^*}_{\alpha o}$, ${V^*}_{\beta o}$, and ${V^*}_{\gamma o}$ is applied to the inverter after an inverse Clark transformation.

It should be mentioned that the zero-sequence component of the output voltage is regulated by phase N through (8) and (10). NP voltage balance can be achieved when the zero-sequence component of the output voltage is well-regulated by phase N, which will be described in detail in the following section.

B. NP Voltage Balance Control

To balance the NP voltage for the 3P4L-3L-VSIs, zero-sequence voltage is injected into the modulation signals. In 3P3L-3L-VSIs, zero sequence current injection is achieved through dc voltage injection in the voltage [3], [49]. However, in 3P4L-3L-VSIs, the zero-sequence voltage can be directly injected into the N phase modulation signal, which can be expressed as

$$V_{No} = -\frac{V_{aN} + V_{bN} + V_{cN}}{3} - V_{\text{offset}}. \tag{23}$$

The injected zero-sequence voltage should satisfy the following condition:

$$-\frac{V_{dc}}{2} + {V_{\max}}^* \le V_{\text{offset}} \le \frac{V_{dc}}{2} - {V_{\max}}^* \tag{24}$$

where ${V_{\max}}^*$ is the amplitude of the output voltage reference. The injected zero-sequence voltage is calculated as

$$V_{\text{offset}} = \begin{cases} -\frac{V_{\text{dc}}}{2} + {V_{\max}}^*(V_P < V_N) \\ \frac{V_{\text{dc}}}{2} - {V_{\max}}^*(V_P > V_N). \end{cases} \tag{25}$$

As a result, the zero-sequence voltage V_{offset} is positive when $V_P > V_N$ and negative when $V_P < V_N$. The NP balance can be achieved through the zero-sequence voltage injection in the N phase modulation signal.

C. Stability Analysis Under Constant Power Load

Fig. 6 shows the system diagram of the VSIs under PI control [45]. The voltage outer PI loop regulates the output voltage and the output current is regulated by the inner current loop. It should be mentioned that the sampled voltages and currents are transformed into the *dq* frame and the control is performed in the *dq* frame.

The system can be depicted using the following equation:

$$\begin{cases} \widehat{d}(s) = G_{del}\left(G_{dei}\widehat{i}_L + G_{ci}\left(i_{L,\text{Ref}} - \widehat{i}_L\right)\right) \\ i_{L,\text{Ref}} = -G_{cv}\widehat{v}_L \\ \widehat{i}_L = G_{id}\widehat{d} + G_{ii}\widehat{i}_o \\ \widehat{v}_o = G_{vd}\widehat{d} + Z_o\widehat{i}_o \end{cases} \tag{26}$$

where G_{del} is the delay matrix caused by the digital controller, G_{dei} is the decoupling matrix, and G_{cv} and G_{ci} are the voltage controller and current controller, respectively. The transfer matrix G_{id}, G_{ii}, G_{vd}, and Z_o can be derived by forcing some of the variables 0 in (26), which is shown in the Appendix. Based on the control diagram and (26), the output impedance of the VSI can be derived as

$$\begin{pmatrix} v_d \\ v_q \end{pmatrix} = \begin{pmatrix} z_{dd} & z_{dq} \\ z_{qd} & z_{qq} \end{pmatrix} \begin{pmatrix} i_d \\ i_q \end{pmatrix}. \tag{27}$$

In this article, the CPL is a motor driving constant torque load. The load is counted as an ideal CPL, as a result, $Z_{dq,\text{CPL}}$, $Z_{qd,\text{CPL}}$, $Z_{qq,\text{CPL}} = 0$. According to [46], the ac stability is fully determined by the single input single output (SISO) return-ratio of the d-d channel, as a result, to simplify the stability analysis process, only the output impedance and the input impedance in the d-d channel are considered. The amplitude of $Z_{dd,\text{CPL}}$ will decrease in the start process to overcome the friction, as shown in Fig. 7(a).

Fig. 7(a) shows the bode plot of Z_{dd} and $Z_{dd,\text{CPL}}$, and Fig. 7(b) shows the Nyquist plot of $Z_{dd}/Z_{dd,\text{CPL}}$ when the power level of CPL varies. The small-signal model of the inverter is verified in the PLECS simulation using the method explained in [43], as illustrated in Fig. 7(a). The rated power of the CPL is 2200 W. In the starting process, the amplitude of $Z_{dd,\text{CPL}}$ decreases and the Nyquist plot crossovers (−1,0j), which means the cascaded system turns to instability in the starting process.

As a result, it is an essential issue to smooth the output impedance of VSIs through nonlinear control strategies.

In the following part of this article, the mechanism that the proposed CCS-MPC can smooth the output impedance of the VSIs is explained. After Z-transforming (13), (14), (22), and [47], we can derive

$$Z_o(z) = -\frac{v_o(z)}{i_o(z)} = \frac{1}{C_f T_s}\frac{z-1}{z^2}. \tag{28}$$

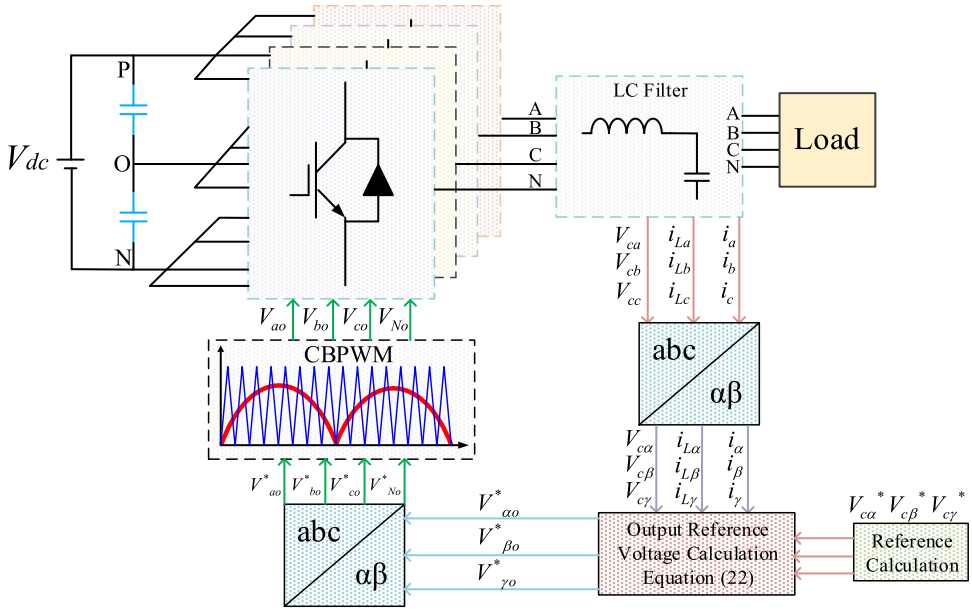

Fig. 5. Diagram of the proposed CCS-MPC.

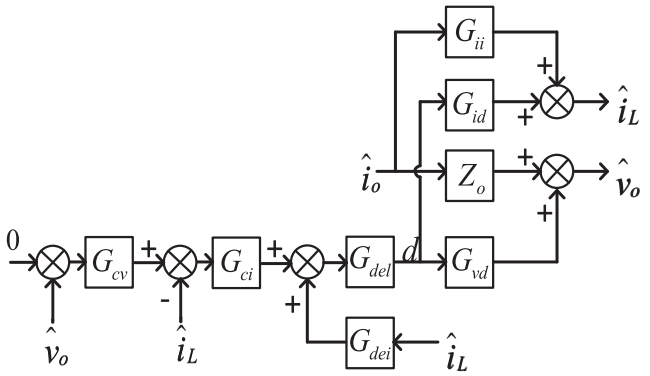

Fig. 6. PI-based control in *dq* domain.

TABLE II
PARAMETERS OF THE EXPERIMENTAL PLATFORM

Parameter	Value
Dc side voltage V_{dc}	600 V
Switching frequency f	20 kHz
Filter inductances phase A, B,and C L_f	535 μH
Filter inductance phase N L_n	535 μH
Filter capacitors C_f	4.4 μF
Dc capacitor C_{up}, C_{low}	2340 μF
Reference angel frequency w_{ref}	50 Hz
Reference amplitude of output voltage V_m	282.8 V

In the low frequency, considering the extreme case, $s->0$, since $z = e^{sTs}$, (28) can be reduced to

$$Z_o(s) = \frac{1}{C_f T_s} \frac{T_s/2 * s}{1 + T_s * s}. \tag{29}$$

Similarly, in the high frequency, considering the extreme case, s->∞, (28) can be estimated as

$$Z_o(s) = \frac{1}{C_f s}. \tag{30}$$

The bode plot of (29) and (30) is shown in Fig. 8. The small-signal model is also verified through ac sweep analysis in PLECS simulation. Actually, the input impedance of the load system will not remain constant at high frequency; it will increase with the frequency [38]. As a result, the intersection of the impedances will not happen. Then, according to [46], there is no crossover of (-1,0j) in the Nyquist plot, which can ensure the stability of the cascaded system.

In addition, the output impedance Z_{dd} under the proposed MPC is compared with that under PI control, as illustrated in Fig. 7(a). It can be observed that Z_{dd} under MPC is smaller than that under PI control in amplitude, which means that the inverter can operate smoothly under disturbance when MPC is applied.

IV. Simulation and Experimental Results

Simulation results are presented to verify the control strategy. The simulations are done with MATLAB/SIMULINK software. Also, experimental verifications and comparisons are presented with the same parameters of the simulations, as shown in Table II.

In the first case, a 120 Ω linear resistor load is connected to the three-phase four-leg three-level VSI. The simulation result is shown in Fig. 9.

Fast Fourier transform (FFT) of V_{ca} under a 120 Ω linear resistor load is presented in Fig. 10. The harmonics are concentrated around 20 kHz, which is the switching frequency. As a result, most of the harmonics are introduced by the switching of MOSFETs.

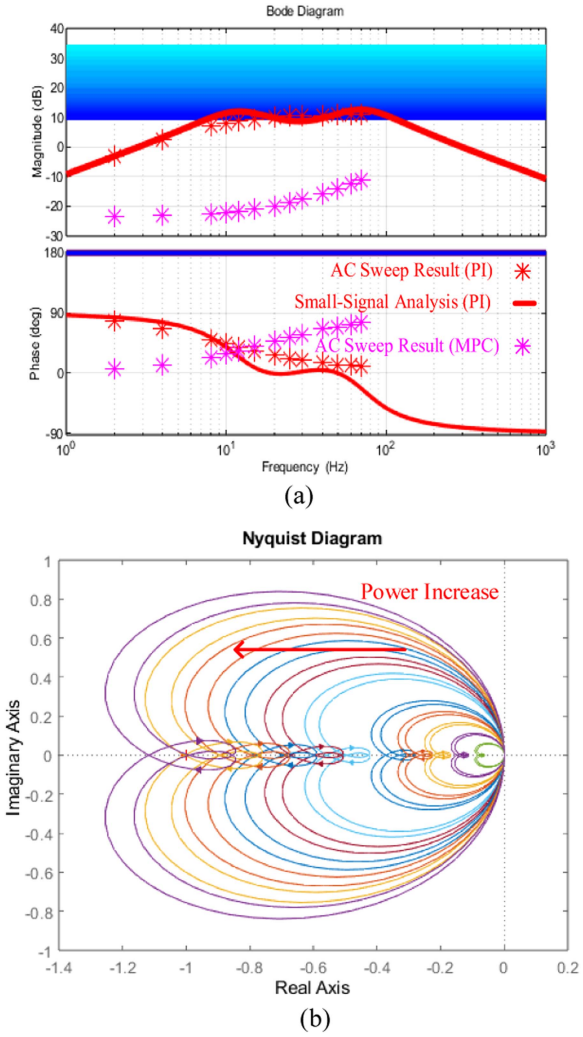

Fig. 7. (a) Bode plot of Z_{dd} and $Z_{dd,\mathrm{CPL}}$. (b) Nyquist plot of $Z_{dd}/Z_{dd,\mathrm{CPL}}$.

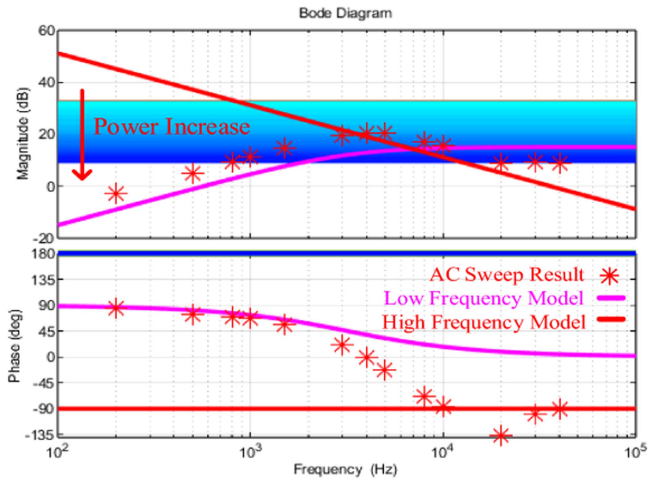

Fig. 8. Bode plot of Z_{dd} under CCS-MPC and $Z_{dd,\mathrm{CPL}}$.

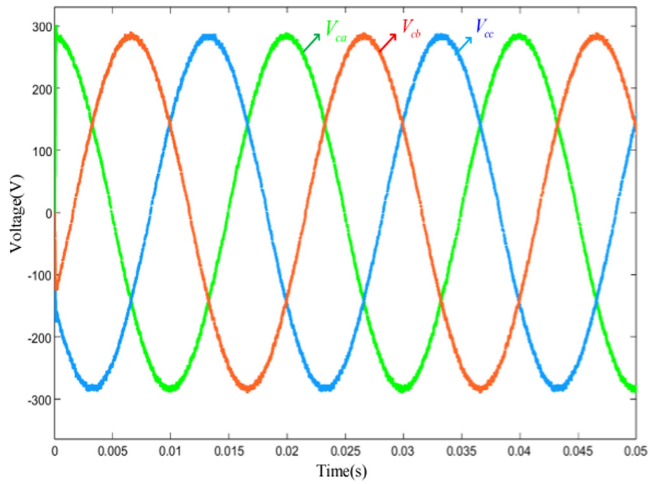

Fig. 9. Simulation result under linear load.

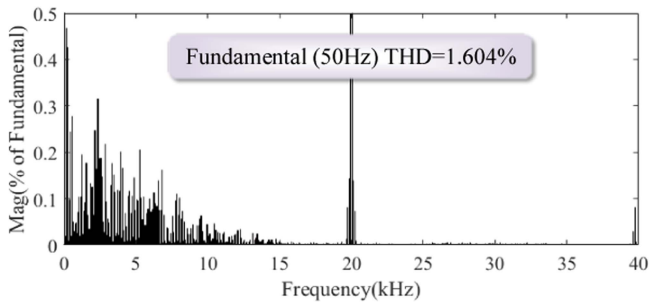

Fig. 10. FFT analysis under linear load.

In Fig. 11, before 0.15 s, phase A of the inverter is supplying a 1000 W resistor load while there is no load in phases B and C. In 0.15 s, a 1000 W resistor load is connected to phase B of the inverter. Due to the sudden step-up of the load, the zero-sequence component increases in the output voltage of the inverter. The NP balance is also illustrated in Fig. 11(b).

In order to verify the current-tracking performance of the proposed CCS-MPC, a nonlinear load, as displayed in Fig. 12, is connected to the inverter. The inductor is set as 1.06 mH and the capacitor is set as 390 μF. The resistor load is 70 Ω.

The output voltage and the output current of the inverter is shown in Fig. 13. The corresponding FFT analysis is shown in Fig. 14. The THD is 3.2737%, and the triple frequency harmonic is introduced by the nonlinear current of the load.

To verify the effectiveness of the proposed CCS-MPC strategy, a platform is built. The platform is built based on a DSP TMS320F28374S. The output voltage V_{ca}, V_{cb}, and V_{cc} are sampled by isolated voltage sensors. The inductor currents i_{La}, i_{Lb}, i_{Lc}, and output currents i_a, i_b, i_c are sampled by hall current sensors. The parameters of the platform are shown in Table II and the picture of the platform is shown in Fig. 15.

A. *Experimental Results of CCS-MPC*

In order to verify the effectiveness of the proposed CCS-MPC, experimental results are presented in this section. The proposed

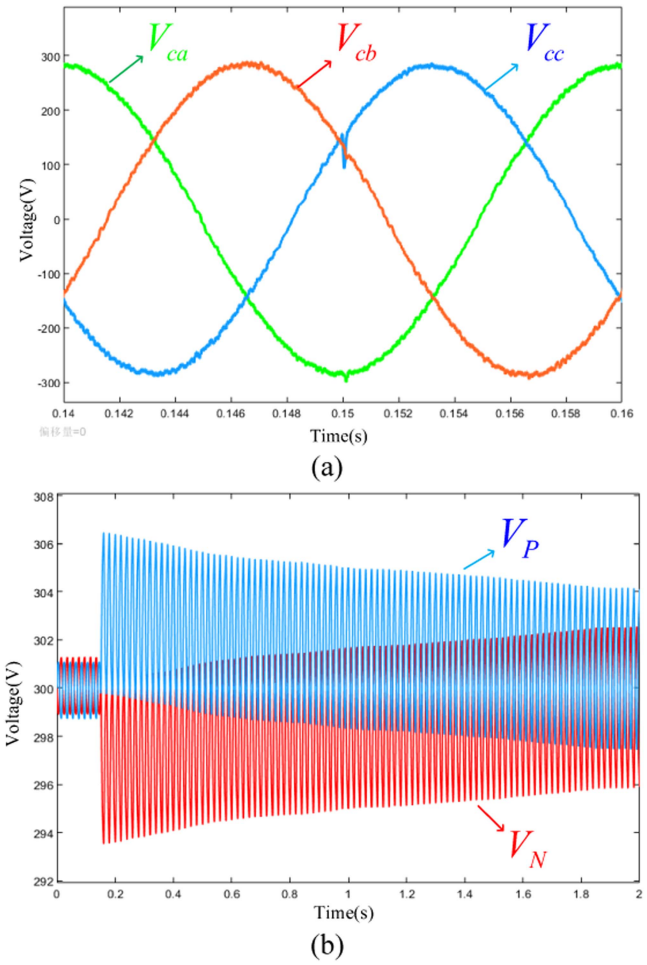

Fig. 11. (a) Simulation result under step load. (b) NP balance.

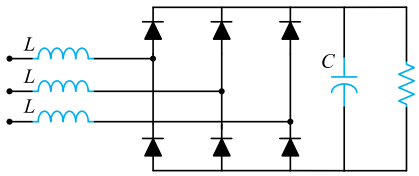

Fig. 12. Three-phase nonlinear load.

CCS-MPC is compared with the PI-based control in the *dq* domain proposed in [8] and the deadbeat control proposed in [12].

First, the proposed CCS-MPC is verified on the platform shown in Fig. 15. Fig. 16 presents the steady-state voltage of the inverter under the proposed CCS-MPC. The inverter is supplying a 1000 W balanced resistor load (120 Ω for each phase).

Fig. 17 shows the THD of the proposed CCS-MPC under linear resistor load, which is almost the same as the simulation result (1.604% and 1.7956%).

In order to verify the current-tracking performance of the proposed CCS-MPC, the inverter is connected to the nonlinear load, as illustrated in Fig. 12. The inductor is set as 1.06 mH and the capacitor is set as 390 μF. The resistor load is 100 Ω.

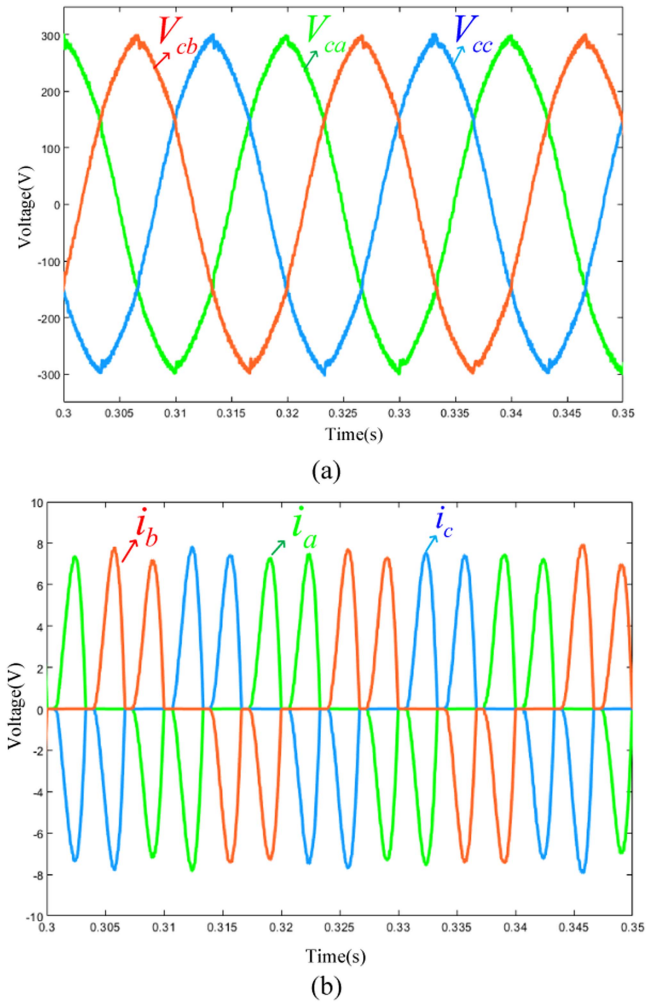

Fig. 13. Simulation results under nonlinear load. (a) Output voltage. (b) Output current.

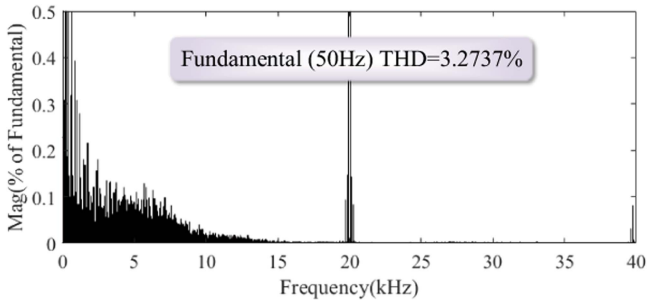

Fig. 14. FFT analysis under nonlinear load.

As is shown in Figs. 18 and 19, due to the nonlinear current caused by the nonlinear load, the third harmonic content in the output voltage increases in Fig. 19. However, the CCS-MPC can still track the output voltage reference with low THD, which demonstrates the effectiveness of the proposed control strategy.

The experimental results of the dynamic performance of the proposed control strategy are also presented. It should be mentioned that the inductance and capacitance in the control

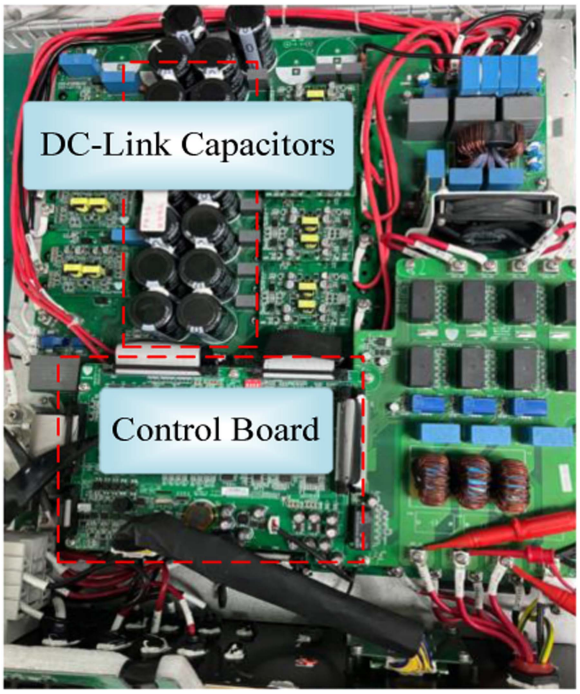

Fig. 15. Experimental platform.

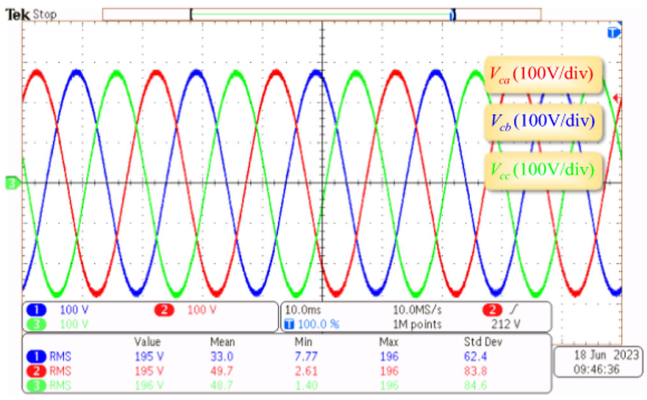

Fig. 16. Steady-state voltage under CCS-MPC (V_{ca}, V_{cb}, and V_{cc}).

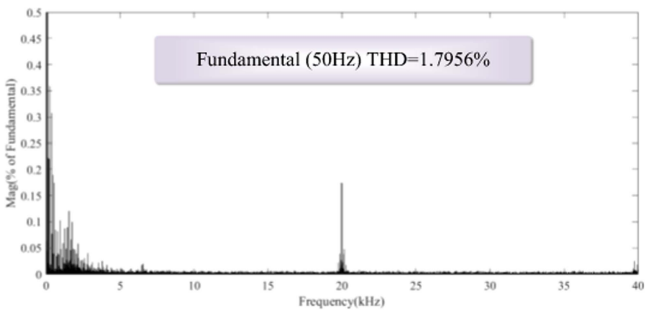

Fig. 17. FFT analysis in steady-state under CCS-MPC.

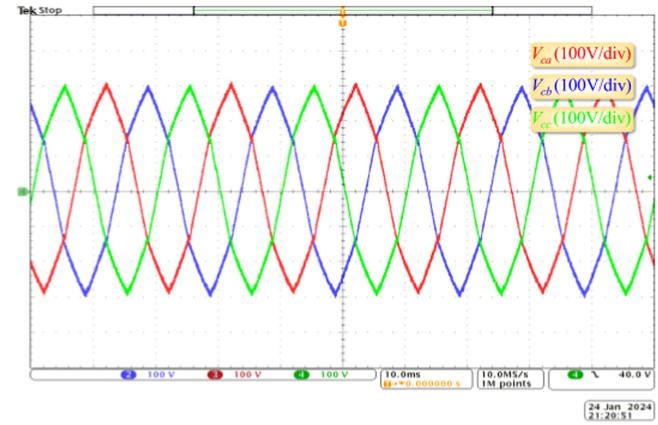

Fig. 18. Voltage under CCS-MPC driving the nonlinear load (V_{ca}, V_{cb}, and V_{cc}).

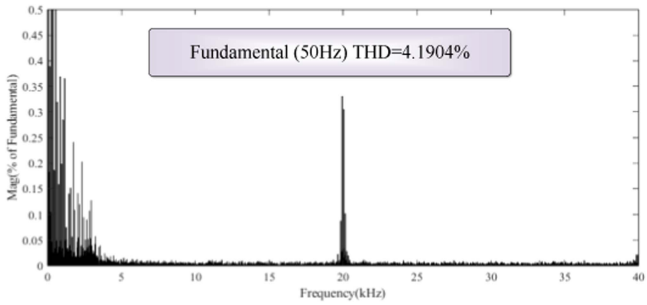

Fig. 19. FFT analysis under nonlinear load.

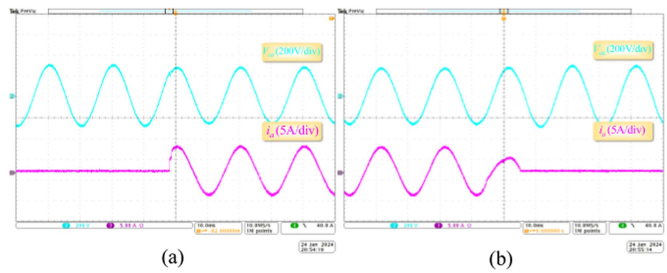

Fig. 20. Dynamic performance. (a) Load step up. (b) Load step down.

strategy have been decreased to lower the THD and guarantee the smooth operation of the inverter according to [3]. In Fig. 20, the three-phase resistor load is switched from 0 W to 3000 W and in Fig. 20(b), the load is switched from 3000 W to 0 W. It can be observed there is almost no oscillation when the load changes, which proves the good dynamic performance of the proposed control strategy.

The NP-balance performance of the proposed control strategy is also presented in Fig. 21. The NP-balance is achieved through the control of the N bridge. A 1000 W resistor load is connected to phase B as the simulation and the neutral point voltage is still balanced. The deviation of V_p and V_n is within 10 V.

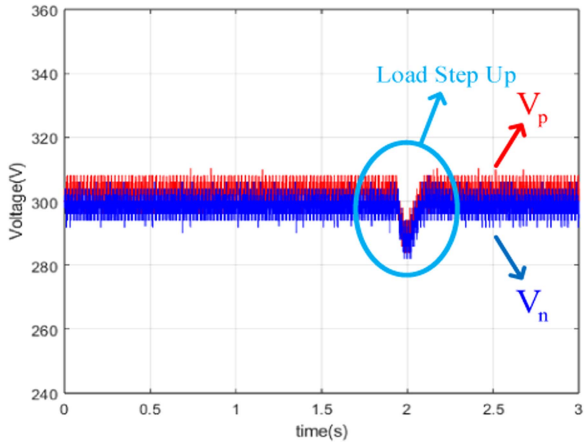

Fig. 21. NP-balance performance.

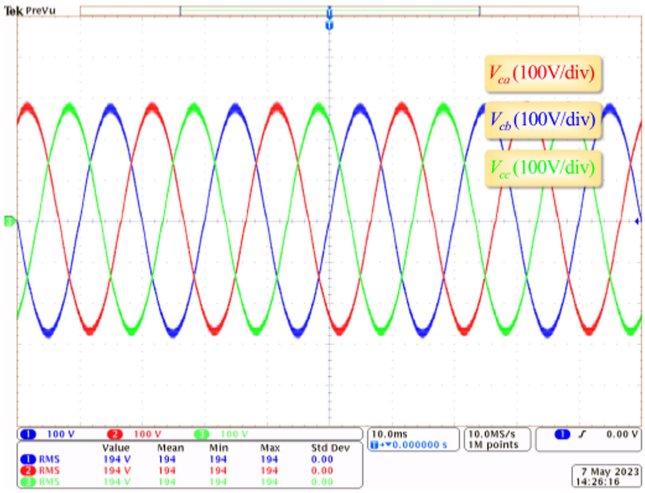

Fig. 22. Steady-state voltage under PI-based strategy (V_{ca}, V_{cb}, and V_{cc}).

B. *Experimental Results of PI-Based Control in* dq *Domain*

To demonstrate that the CCS-MPC proposed in this article is better than the mostly common PI-based control for three-phase four-leg three-level VSIs from the degree of THD and executing time, the experimental results of PI-based control in *dq* domain are compared with the proposed CCS-MPC.

The output voltage and its THD analysis are shown in Figs. 22 and 23. The inverter is supplying a 1000 W resistor load. Due to the inertia of the PI-based controller, the harmonic around the 20 kHz (control frequency) increases. Compared with CCS-MPC, the THD increases from 1.7956% to 2.0834%. Detailed comparisons will be presented in Section IV-E.

The inverter under the PI-based controller is also connected to the nonlinear load, as shown in Fig. 12. The output of the inverter is illustrated in Figs. 24 and 25. Due to the nonlinear current of the load and the inertia of the PI-based controller, there exists a great deal of three-order harmonic in Fig. 25. The THD is high (4.3217%) compared to the CCS-MPC proposed in this article (4.1904%).

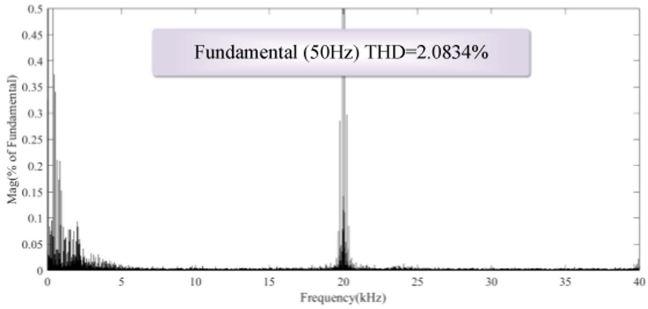

Fig. 23. FFT analysis of PI-based strategy under linear load.

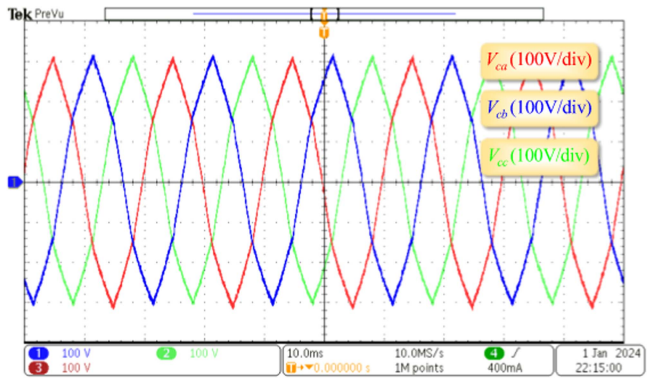

Fig. 24. Voltage under PI-based control driving the nonlinear load (V_{ca}, V_{cb}, and V_{cc}).

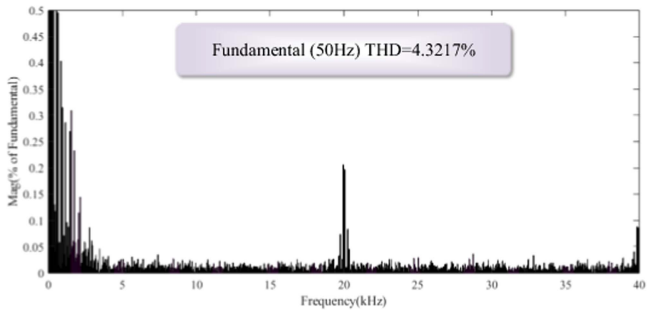

Fig. 25. FFT analysis of PI-based control under nonlinear load.

C. *Experimental Results of Deadbeat Control*

Another commonly used model-based control strategy of the three-phase four-leg three-level VSI is the deadbeat control [12]. The key of the control strategy is to predict the output current and voltage at each control period and calculate the duty cycle to track the reference. The prediction process can be explained by the following equations:

$$i_{L\alpha,\mathrm{Ref}}(k) = i_{\alpha}(k) + \frac{C}{T_s}(V^*{}_{c\alpha}(k) - V_{\alpha N}(k)) \tag{31}$$

$$V_{\alpha N,\mathrm{Ref}}(k) = V^*{}_{c\alpha}(k) + \frac{L}{T_s}(i_{L\alpha,\mathrm{Ref}}(k) - i_{L\alpha}(k)) \tag{32}$$

where $i_{L\alpha,Ref}(k)$ is the reference inductor current in period k and $V_{\alpha N,Ref}(k)$ is the reference output voltage in period k.

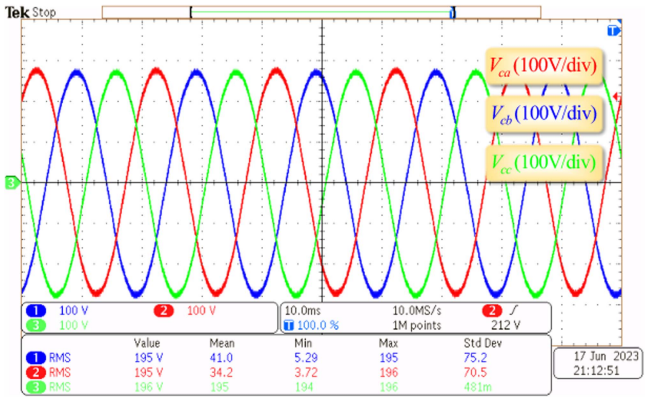

Fig. 26. Voltage under deadbeat control driving the linear load (V_{ca}, V_{cb}, and V_{cc}).

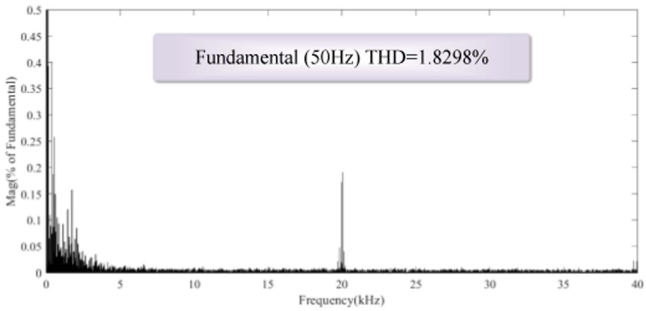

Fig. 27. FFT analysis of deadbeat control under linear load.

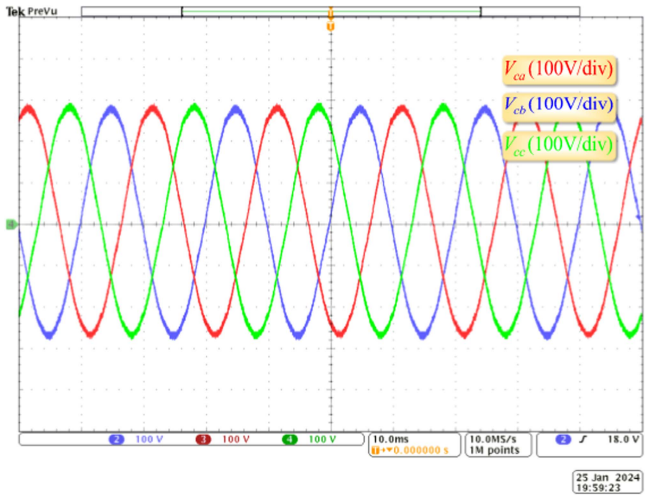

Fig. 28. Steady-state voltage under PR-based strategy (V_{ca}, V_{cb}, and V_{cc}).

Figs. 26 and 27 show the output voltage of the inverter under deadbeat control. The THD (1.8298%) is higher than that of the proposed CCS-MPC. A more detailed comparison will be given in Section IV-E.

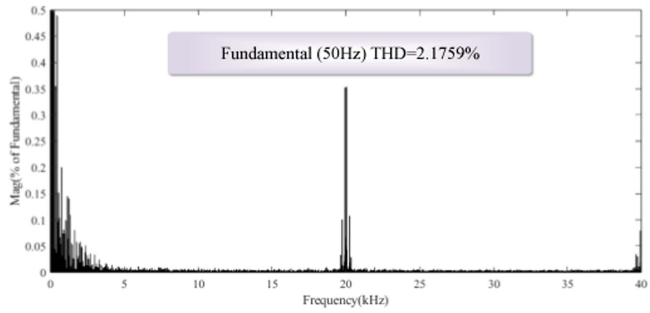

Fig. 29. FFT analysis of PR-based strategy under linear load.

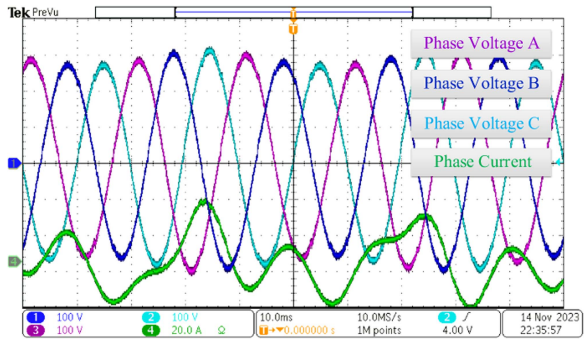

Fig. 30. Voltage loop instable due to CPL in PI-based control in Fig. 6.

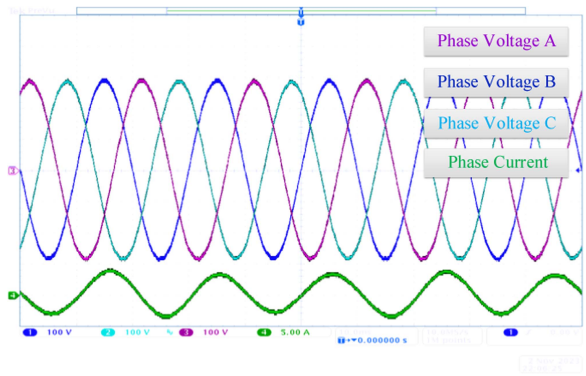

Fig. 31. Proposed CCS-MPC stable under CPL.

TABLE III
COMPARISONS OF THE CONTROL STRATEGIES

Control Strategy	Steady-State THD	CPL THD	Execution time in DSP
CCS-MPC in this article	1.7956%	1.4481%	8 μs
PI-based control in dq domain	2.0834%	Fail	12.8 μs
Deadbeat control	1.8298%	1.5344%	7.8 μs
PR-based control in *abc* domain	2.1759%	1.8204%	18.4 μs

D. *Experimental Results of PR-Based Control in* abc *Domain*

Another commonly used control strategy for VSIs is the proportional resonance (PR) controller [48]. In this paper, the PR controller is also compared with the proposed MPC.

$$Z(s) = -\frac{v_o(s)}{i_o(s)} = -\frac{\boldsymbol{Z_o - G_{ci}G_{del}G_{ii}G_{vd} + G_{dei}G_{del}G_{ii}G_{vd} + G_{ci}G_{del}G_{id}Z_o - G_{dei}G_{del}G_{id}Z_o}}{\boldsymbol{E + G_{ci}G_{del}G_{id} - G_{dei}G_{del}G_{id} + G_{ci}G_{cv}G_{del}G_{vd}}}. \quad \text{(A11)}$$

The control structure can be found in [50]. The control is conducted in the *abc* frame. The output voltage of the inverter is regulated by the PR controller and the output current is regulated by the PI controller. Only the fundamental frequency (50 Hz) is compensated in the PR controller.

Fig. 28 shows the output voltage of the inverter under PR-based control. The inverter is supplying a 1000 W balanced resistor load. The THD in Fig. 29 is 2.1759%, which is larger than the proposed control strategy(1.7956%). The THD results of the inverter feeding CPL under PR-based control will be given in the following section.

E. Comparisons of the Control Strategies

To confirm that the proposed CCS-MPC is better than the existent control strategies illustrated in Section IV-B, IV-C, and IV-D, detailed comparisons are given in Table III.

It can be seen that the CCS-MPC has the lowest THD among the three control strategies under the same load (1000 W resistor load or 2200 W CPL). The execution time of the three control strategies is also measured in the DSP. Due to the complex calculation in the PI-based control in the *dq* domain and the PR-based control in the *abc* frame, the linear control strategies take a longer time (12.8 μs and 18.4 μs). CCS-MPC proposed in this article and the deadbeat control take almost the same time (8 μs and 7.8 μs).

The stability of the control strategy under CPL is also tested. In Fig. 30, the converter is driving a 2200 W machine under the control strategy in Fig. 6. The voltage loop turns unstable due to the negative impedance characteristics of the CPL. However, the system is stable under CCS-MPC, as shown in Fig. 31, which verifies the effectiveness of the CCS-MPC under CPL.

V. Conclusion

This article proposes a novel CCS-MPC strategy for three-phase four-leg three-level voltage source inverters. The control strategy is developed in the $\alpha\beta\gamma$ frame based on the decoupled model of the three-phase four-leg three-level VSI. Compared with the FCS-MPC strategy, the proposed control strategy adopts offline optimization instead of online optimization, which can reduce the computational burden of the digital controllers. The control strategy is compared with the existent three control strategies (PI-based control in *dq* domain, PR-based control in the *abc* domain and deadbeat control), and the results prove that the control strategy shows the lowest THD among the four control strategies and takes less execution time compared with the commonly used PI-based control and PR-based control. It can also increase the stability margin compared with PI-based control, which is verified by both simulation and experiments.

Appendix

The specific expressions of G_{del}, G_{dei}, G_{cv}, G_{ci}, G_{id}, G_{ii}, G_{vd}, and Z_o in (23) are given as follows:

$$G_{del} = \begin{pmatrix} \frac{1-0.5T_s s+1/12{T_s}^2 s^2}{1+-0.5T_s s+1/12{T_s}^2 s^2} & 0 \\ 0 & \frac{1-0.5T_s s+1/12{T_s}^2 s^2}{1+-0.5T_s s+1/12{T_s}^2 s^2} \end{pmatrix} \quad \text{(A1)}$$

$$G_{dei} = \begin{pmatrix} 0 & -wL_f \\ wL_f & 0 \end{pmatrix} \quad \text{(A2)}$$

$$G_{cv} = \begin{pmatrix} k_{pv} + k_{iv}/s & 0 \\ 0 & k_{pv} + k_{iv}/s \end{pmatrix} \quad \text{(A3)}$$

$$G_{ci} = \begin{pmatrix} k_{pi} + k_{ii}/s & 0 \\ 0 & k_{pi} + k_{ii}/s \end{pmatrix} \quad \text{(A4)}$$

$$G_{id} = V_{dc}\boldsymbol{Y_c}(\boldsymbol{Y_c Y_L + E})^{-1} \quad \text{(A5)}$$

$$G_{ii} = (\boldsymbol{Y_c Y_L + E})^{-1} \quad \text{(A6)}$$

$$G_{vd} = V_{\mathrm{dc}}(\boldsymbol{Y_c Y_L + E})^{-1} \quad \text{(A7)}$$

$$Z_o = -\boldsymbol{Y_L}(\boldsymbol{Y_c Y_L + E})^{-1} \quad \text{(A8)}$$

where w is the fundamental frequency of the output voltage and E is the Identity matrix. Y_c and Y_L are impedance matrix of line inductors and capacitors, which is defined as

$$Y_L = \begin{pmatrix} R + sL_f & -wL_f \\ wL_f & R + sL_f \end{pmatrix} \quad \text{(A9)}$$

$$Y_C = \begin{pmatrix} sC_f & -wC_f \\ wC_f & sC_f \end{pmatrix}. \quad \text{(A10)}$$

Z_{dd} is calculated as (A11), is shown at the top of this page.

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Yi Zhu (Graduate Student Member, IEEE) received the B.E. degree from Soochow University, Suzhou, China, in 2023. Since 2023, he has been working toward the Ph.D. degree with the University of Liverpool, Liverpool, U.K., both in electrical engineering.

His research interests include modeling, control, and stability analysis of power electronic converters.

Huiqing Wen (Senior Member, IEEE) received the B.S. and M.S. degrees from Zhejiang University, Hangzhou, China, in 2002 and 2006, respectively, and the Ph.D. degree from the Chinese Academy of Sciences, Beijing, China, in 2009, all in electrical engineering.

From 2009 to 2010, he was an Electrical Engineer with the GE (China) Research and Development Center Company, Ltd., Shanghai, China. From 2010 to 2011, he was an Engineer with the China Coal Research Institute, Beijing, China. From 2011 to 2012, he was a Postdoctoral Fellow with the Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates. Since 2013, he has been with the Department of Electrical and Electronic Engineering, Xi'an Jiaotong-Liverpool University, Suzhou, China, where he is currently a Professor. He has authored or coauthored more than 50 peer-reviewed technical papers in leading journals. His research interests include renewable energy, electric vehicle, power electronics, microgrid, and power semiconductor devices.

Dr. Wen is a Fellow of the Institution of Engineering and Technology. He is an Associate Editor for IEEE Access, *International Journal of Photoenergy*, and *Journal of Power Electronics*.

Yong Yang (Senior Member, IEEE) received the B.S. degree in automation from Xiangtan University, Xiangtan, China, in 2003, the M.S. degree in electrical engineering from Guizhou University, Guiyang, China, in 2006, and the Ph.D. degree in electrical engineering from Shanghai University, Shanghai, China, in 2010.

He is currently a Full Professor with the School of Rail Transportation, Soochow University. From 2017 to 2018, he was a Visiting Scholar with Center for High Performance Power Electronics, The Ohio State University, Columbus, USA. He has coauthored more than 100 journal and conference papers. His current research interests include model predictive control in power electronic converters, distributed energy resource interfacing, and high-performance motor drive control.

Jianliang Mao received the B.E. degree in mechanical manufacturing and automation from Northwestern Polytechnical University, Xi'an, China, in 2017.

He is currently an Academician with the European Academy of Natural Sciences, a Senior Power Engineer, and the Chairperson with Jiangsu Koyoe Energy Technology Company Ltd., Suzhou, China. His research interests include the control of solar inverters and solar power systems.

Pan Wang received the bachelor's degree in electrical engineering from Anhui University, Hefei, China, in 2011.

He is currently the Director with Jiangsu Koyoe Energy Technology Company Ltd., Suzhou, China. His research interests include the control of solar inverters and solar power systems.

Weiguo Huang received the B.S. and Ph.D. degrees in precision machinery and precision instruments from the University of Science and Technology of China, Hefei, China, in 2004 and 2010, respectively.

He is currently a Full Professor with the School of Rail Transportation, Soochow University, Suzhou, China. His current research interests include mechanical signal processing, image processing, mechanical dynamics, and fault diagnosis.

Jose Rodriguez (Life Fellow, IEEE) received the Engineer degree from the Universidad Tecnica Federico Santa Maria, Valparaiso, Chile, in 1977 and the Dr.-Ing. degree from the University of Erlangen, Erlangen, Germany, in 1985, both in electrical engineering.

Since 1977, he has been with the Department of Electronics Engineering, Universidad Tecnica Federico Santa Maria, where he was Full Professor and President. Since 2015 to 2019, he was the President with Universidad Andres Bello, Santiago, Chile. Since 2022 to 2023, he was the President with Universidad San Sebastian, Santiago, Chile. He is currently the Director with the Center for Energy Transition, Universidad San Sebastian. He has coauthored two books, several book chapters and more than 700 journal and conference papers. His main research interests include multilevel inverters, new converter topologies, control of power converters, and adjustable-speed drives.

Prof. Rodriguez was the recipient of number of best paper awards from journals of the IEEE. He is member of the Chilean Academy of Engineering. In 2014, he was the recipient of the National Award of Applied Sciences and Technology from the government of Chile, and also the recipient of the Eugene Mittelmann Award from the Industrial Electronics Society of the IEEE, in 2015. In 2014–2022, he was included in the list of Highly Cited Researchers published by Web of Science.