An Improved GHA-Enabled Steady State Model-Derived Semiconductor Loss Optimization for a Three-Port C3L3 Resonant Converter

Shubham Mungekar, *Student Member, IEEE*, and Ayan Mallik, *Senior Member, IEEE*

***Abstract*—This article presents a new modeling approach for a multiport resonant converter that accounts for the nonapproximated effects of all switching harmonics on determination of the natures of port currents and power transfer dynamics. As proved in this work, resonant converter modeling performed with resistive approximation of the ac equivalent impedance introduces $\geq 10\%$ error in port current rms, peak and switching instant values estimation. This error further propagates in semiconductor loss calculation process yielding incorrect losses during converter operation and inaccuracies in optimum control variables determination required for generating desired power and voltage at the output ports. This error is rectified using a reconceived modeling approach called improved generalized harmonic approximation (GHA). This modeling approach is compared with the simulation results and the contemporary state-of-the-art approaches, GHA and first harmonic approximation,—both of which use equivalent resistance approximation. A semiconductor loss model developed using this redefined approach serves as the basis for categorical as well as total semiconductor loss optimization. To benchmark the converter performance vis-à-vis the developed analytical model, an all-GaN-based 2 kW three-port C3L3 prototype is developed for a resonant frequency of 490 kHz. Experimental validations for various loading conditions are presented for a wide-gain three-port power conversion (400 to 500–600 V and 22–28 V) at corner conditions to verify the derived modeling methodology.**

***Index Terms*—CLLC, control variables, dc–dc conversion, electric vehicle (EV) charging, multiport resonant converter, optimization, switching losses, synchronous rectification (SR).**

I. Introduction

PLUG-IN electric vehicles (EVs) are furnished with onboard level-1 and level-2 grid-to-vehicle chargers to charge the high-voltage (HV) traction batteries. Typically, an onboard charger uses an ac–dc converter as the first stage, followed by an isolated dc–dc converter as the second stage [1], [2]. Both these converters should be capable of feeding power back to the grid from the battery in case of peak power requirements and ease the load shaving [3], also referred to as vehicle-to-grid, thus defining the requirement of a bidirectional isolated dc–dc topology in this application. Several studies have been conducted in the past on isolated dc/dc converter topologies, such as the dual active bridge (DAB) [4], resonant *LLC,* and *CLLC* topologies [5], with an aim to achieve higher efficiency and superior power density. The major challenge in a DAB topology is to achieve soft switching for all power and voltage range especially in applications with wide gain requirements, such as battery charging [6]. Comparatively, *CLLC* resonant topologies allow zero-voltage switching (ZVS) at turn-ON for almost the entire power range and wide output voltage requirements and thus reduce switching losses and improve converter efficiency [7]. Recently there is an impetus for HV batteries to move toward 600 and 800 V nominal levels, primarily in order to reduce the conduction losses of the traction inverters involved in the drive-train [8] and also to facilitate an efficient fast-charging system [9]. In addition, the charger topology also consists of a discrete dc–dc bidirectional converter to charge the auxiliary battery (typically at 12/28/48 V), which is required to drive low-voltage (LV) loads including the control unit for the main charger, air conditioning unit, etc. In that regard, owing to the target of achieving a power dense integrated solution, lowering of system-level losses and simultaneous charging for the HV and LV batteries inside an EV, integrated multi-port converters (MPC) have proved to be a promising solution by facilitating a unified power electronics platform.

A. MPC and Control Variables

Several studies [10], [11], [12] have been published on the modeling, design, control, and optimization of three-port pulsewidth modulation (PWM)-controlled MPCs, such as triple active bridge (TAB) converters. These converters follow three-port extended DAB topology and hence suffer from the common limitations as those in DABs. As the voltage gain drifts from unity, TAB fails to achieve full soft-switching for all semiconductor devices on the three bridges, thus incurring higher turn-ON losses on account of partial or no ZVS. In addition to that, at lighter loading conditions, TAB suffers from degraded efficiency due to higher winding rms currents, as evidenced from several existing works. This problem is solved to an extent in some works which have focused on developing hybrid phase, duty control-based modulation schemes to improve

Manuscript received 10 October 2023; revised 20 December 2023 and 9 February 2024; accepted 28 February 2024. Date of publication 5 March 2024; date of current version 19 April 2024. This work was supported in part by CoolCAD Electronics LLC as part of Army SBIR/STTR program. Recommended for publication by Associate Editor N. M. L. Tan. *(Corresponding author: Ayan Mallik.)*

The authors are with the Fulton Schools of Engineering, Arizona State University, Mesa, AZ 85212 USA (e-mail: ayan.mallik@asu.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3373514.

Digital Object Identifier 10.1109/TPEL.2024.3373514

the efficiency of MPCs. However, most of these methods use time domain models with high number of control variables to compute the rms and switching instant currents resulting in a complicated and computationally intensive process, which, therefore severely restricts the performance of adaptive optimization. The work in [13] presented a cumulative loss reduction strategy executed on TAB by developing loss objective functions and running an optimization routine to obtain the most optimum set of control parameters. Although the study thoroughly elucidates the ZVS criteria for devices on all the bridges, the scope of efficiency improvement on account of switching frequency parameter and corresponding phase-frequency modulation to achieve synchronous rectification (SR)-based minimized turn-OFF losses is not included. Therefore, based on the current literature study and the loss distribution in DAB and *CLLC*, it is concluded that the realization of MPC using an extension of resonant *CLLC* topology could be a better alternative with wider scopes for soft-switching accomplishment as well as total loss optimization, when compared with the TAB counterparts.

B. Resonant MPC Topologies

Multiport power transfer capabilities with resonant topologies are explored in a few studies summarized below. The manuscript in [14] is considered to be one of the earliest works in resonant topologies serving as the foundation for subsequent works. The work in [15] investigates an immittance-based multiport bidirectional converter by focusing on decoupled power transfer. In addition, a modified phase shift modulation is proposed to alleviate the negative effects of higher order harmonics with an objective to efficiently facilitate a multidirectional power flow mechanism without introducing excessive circulating reactive power. Solid-state transformer implemented with a three-port resonant *LLC* converter intended for use in energy storage solutions is presented in [16]. Although the abovementioned works diligently characterize the operation of the MPC topologies, the presented analyses are only valid for a limited set of operating conditions. Furthermore, the impact of varying terminal voltages at wide-ranging power levels and their effects on the control variables generation are not studied in those references.

This problem is solved to a certain extent by Asa et al. [17], in which a novel multiport *CLL* resonant converter with a phase shift and asymmetrical duty-cycle control is analyzed for application in renewable energy platforms. In this study, two discrete primary half bridges are interfaced with the passive secondary bridge through a high-frequency transformer achieving ZVS/zero current switching (ZCS) on primary ports and zero-current turn-OFF (ZCS) on passive secondary bridge. Another study in [18] presents a three-port bidirectional resonant converter with power coupling analysis and its corresponding decoupling control theory. Furthermore, it is followed by a small signal model to select appropriate parameters for the converter achieving easier control implementation and soft switching on all the ports. In almost all these modeling approaches presented by the authors in [16], [17], [18], [19], [20], [21], [22], [23], and [24] followed First Harmonic Approximation (FHA) for deriving their port parameter relationships.

C. Knowledge Gaps in Literature and Problem Statement Formulation

In the literature survey, two major gaps in multiport resonant converter modeling are identified. First there is lack of a fundamental generalized approach to clearly define an accurate relationship between the control variables, such as frequency, and phase to output voltage and output power for MPC. Second, majority of the literature works discussed above, utilize FHA-based modeling approach instead of GHA. Although, FHA-based modeling is acceptable when the operating switching frequency is closer to the resonant frequency, this approach introduces intolerable error in the model when switching frequency moves further away from resonant point, which is the case in wide-gain power conversion. This bottleneck led the authors in [7] and [9] to develop generalized harmonic approximation (GHA), in which the voltage and current waveforms in the active full bridges are modeled by accounting for fundamental and higher order harmonics. Sankar et al. [7] utilized the GHA approach to improve estimation accuracy of secondary port current zero-crossing phase angle determination in active full bridges to achieve SR for efficiency improvement, which is further discussed in Section II of this article. This concept was further developed by Chandwani et al. [9] where they were able to derive analytical expressions for voltage and current reconstructions to obtain control variables based on required voltage and power in a three-port resonant converter. Although the authors in [7] and [9] used the concept of GHA for converter modeling, they both assume a resistive approximation for the reflected ac impedance modeling on the load side. This approximation simplifies the converter modeling; however, it leads to inaccuracies in deriving the time-domain dynamics of port currents, voltages, and powers. This problem is discussed in detail in this manuscript and a generalized renewed modeling approach called "improved GHA" (I-GHA) for a multiport resonant converter is proposed. Another important note is that the dynamic load transient analysis and the corresponding closed-loop controller design process is excluded from this work as the primary focus is only on the steady state operational analysis and categorical/total loss optimization using the proposed nonapproximated circuit equivalence model, which is further carefully benchmarked against other state-of-the-art methods.

After reviewing various MPC topologies, resonant converters, their modulation schemes and modeling approaches, this manuscript has decided to focus on a problem statement, which intends to redefine the modeling approach for a multiport resonant converter. This topology inherits the benefits of a resonant topology, such as ZVS-based soft switching by enabling phase-frequency control of all full bridges. The key contributions and contents of this manuscript are discussed below.

1) A nonapproximated all-harmonics-inclusive methodology for reconstruction of currents, voltages, and power transfer dynamics in a multiport resonant dc–dc converter network that aids in the power loss objective function formulation and hence control variable set optimization under a wide range of operating conditions, followed by model derivation and verification with some test candidates delineated in Sections II–IV.

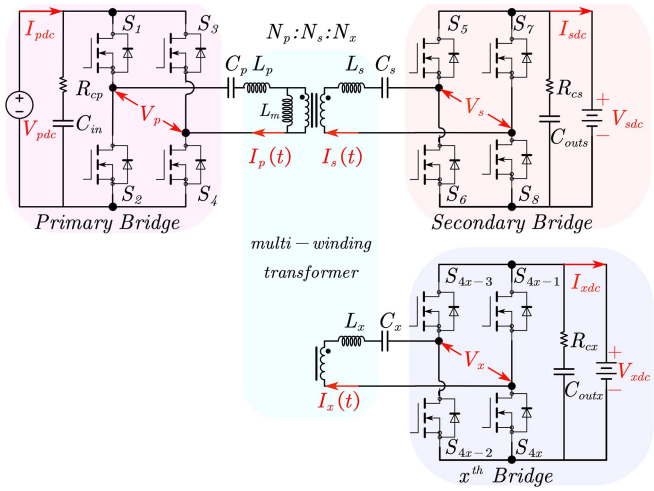

Fig. 1. Generalized three-port C3L3 resonant converter circuit diagram.

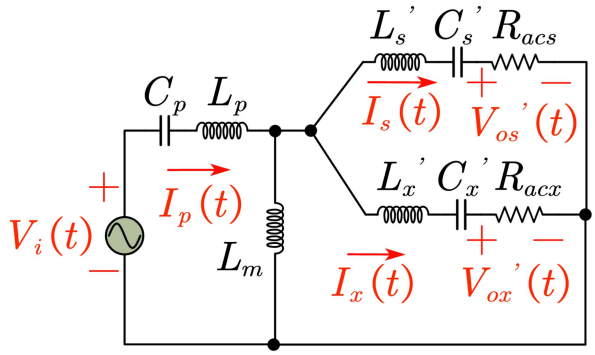

Fig. 2. FHA-based AC equivalent circuit diagram.

2) Formulation of categorical/ total semiconductor loss objective function optimization (specifically, conduction loss and current-frequency product at switching transitions) for power semiconductor devices while semiconductor loss model accounting for ZVS constraints on the inverting-side full-bridge, as outlined in Section III and followed by categorical and total loss optimization in Section IV.
3) Hybrid offline one-cycle optimal control variable set calculation and realization in digital controller platform performed using I-GHA-derived multivariate polynomial regression with reduced order memory complexity, as delineated in Section V. Finally, comprehensive experimental results supporting the concept validation are compiled and discussed in Section VI. Finally, Section VII concludes this article.

II. Nonapproximated Steady-State Network Modeling of Three-Port C3L3 Resonant Converter

A. Modeling Approach Using FHA and GHA Methods

The topology for a conventional bidirectional full-bridge three-port C3L3 resonant converter is presented in Fig. 1. It uses an integrated multiwinding high-frequency power transformer (HFPT), with turns (N_p, N_s, andN_x) and magnetizing inductance L_m, for galvanic isolation and serves as an interface at high-frequency power conversion. Converter ports in addition to primary (p) and secondary (s) are represented by subscript "x" in order to derive a generalized model. However, this work predominantly focuses on a three-port resonant C3L3 converter realization. The transformer is connected to an inverting bridge on the primary side used for converting dc to pulse width and pulse frequency modulated ac and to the rectifying bridges (secondary, xth) for converting reflected ac to dc on respective output ports. Resonant inductors (L_p, L_s, and L_x) are realized through controllable leakage inductance of the HFPT while the resonant capacitor (C_p, C_s, and C_x) values are selected to keep a uniform resonant frequency $F_{\text{res}p} = F_{\text{res}s} = F_{\text{res}x}$ across all active bridges based on formulae $F_{\text{res}p} = \frac{1}{2\pi\sqrt{(L_p.C_p)}}$, $F_{\text{res}s} = \frac{1}{2\pi\sqrt{(L_s.C_s)}}$, and $F_{\text{res}x} = \frac{1}{2\pi\sqrt{(L_x.C_x)}}$, where x $\in (t, q, p, h\ldots)$.

The proposed methodology is extendable to any multiactive-bridge converter comprising any number of full-bridges or half-bridges that are interfaced using their *L*-based and/or *LC*-based resonant tanks coupled by a multiwinding transformer. For any restructuring to the active bridge network (4)–(6) depicting the port voltage generation may be affected by some factor, while other (7)–(30) governing the port current formulation and power loss modeling remain the same.

Some existing state-of-the-art modeling approaches for a three full-bridge-based resonant converter topology based on Fig. 1 are reviewed in this section. Fig. 2 shows the ac equivalent circuit of FHA-based resonant converter circuit analysis. In this modeling approach, square wave outputs of primary, secondary, and tertiary full-bridges are represented as voltage sources (referred to primary) $V_i(t)$, $V'_{os}(t)$ and $V'_{ox}(t)$, respectively, by their fundamental sinusoidal frequency and the higher order harmonics are ignored [30]. As a result, the converter analytical model becomes much simpler, and the equations are much easier to implement in the digital environment of a digital signal processor (DSP). This model is fairly accurate when the switching frequency F_{sw} of the converter is within the vicinity of resonant frequency F_r. Any operation beyond a certain range outside the resonant frequency leads to a much lower accuracy in the port current reconstruction. Inaccurate port current reconstruction leads to inaccurate loss calculation and further leads to incorrect control variable generation that operates the converter in a nonoptimal condition. Typically, for converters with lower value of quality factor (Q) and low gain (G) requirements $0.95 \leq \text{G} \leq 1.05$, F_{sw} is found to be very close to F_r. In such scenarios, FHA is proven to be useful and highly accurate leading to widespread usage within the industry and academia for resonant converter modeling. In FHA, the output port ac equivalent resistance can be calculated as follows:

$$R'_{\text{ac}x} = \frac{V'_{ox}}{I'_{x\text{dc}}} = \frac{\frac{4V'_{x\text{dc}}}{\pi}\sin(2\pi F_{\text{sw}}t)}{\frac{I'_{x\text{dc}}}{\pi}\sin(2\pi F_{\text{sw}}t)} = \frac{8R'_{\text{out}x}}{\pi^2} \quad (1)$$

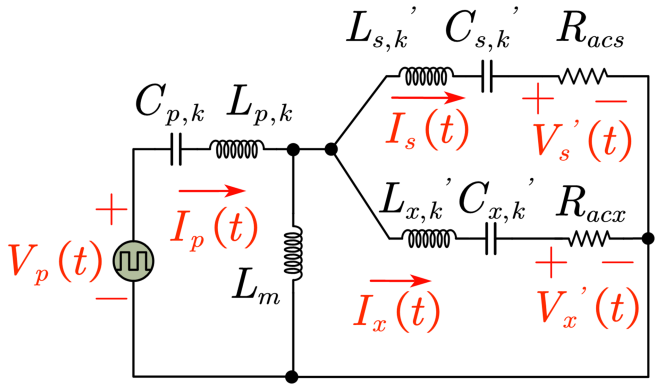

Fig. 3. GHA-based AC equivalent circuit diagram.

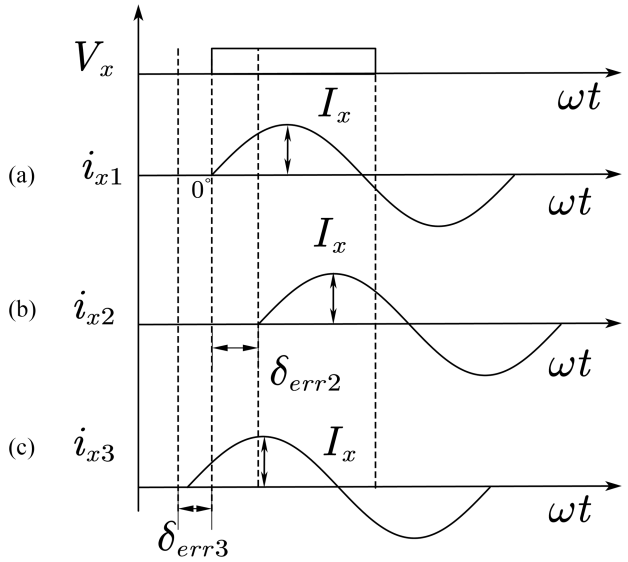

Fig. 4. Zero-crossing xth port voltage-current mismatch waveform for three cases viz. (a) $i_{x1}(\delta_{\text{err}} = 0°)$. (b) $i_{x2}(\delta_{\text{err2}} > 0°)$. (c) $i_{x3}(\delta_{\text{err3}} < 0°)$.

where $R_{\text{out}x}$ is the equivalent dc-load resistance and can be calculated as $R'_{\text{out}x} = \frac{V'_{x\text{dc}}}{I'_{x\text{dc}}}$

1) Drawbacks of FHA: FHA-based modeling demonstrates the issue pertaining to inaccurate phase tracking reported in [7] necessitating a redefined modeling approach. Replacing secondary side diodes with actively controlled devices leads to the requirement for tracking of zero-crossing instant of secondary current, also referred as SR. Port Current i_x flowing through xth bridge can be formulated as: $i_x = I_x.\sin(\delta_{\text{err}}) \approx I_x.\delta_{\text{err}}$; where δ_{err} is the phase error of port current with respect to port voltage due to asynchronized zero-crossing events, as illustrated in Fig. 4. For small angle, δ_{err}, current is directly proportional to phase error. Therefore, total extra loss due to δ_{err} with turn-OFF time t_{off} can be derived as: $P_{\text{turnoff}} = 0.5.V_{\text{dc}}.I_s.F_{\text{sw}}.t_{\text{off}}.\sin(\delta_{\text{err}}) \approx 0.5.V_{\text{dc}}.I_sF_{\text{sw}}.t_{\text{off}}.\delta_{\text{err}}$. From the above equation, it can be concluded that failure to determine the phase angle could lead to incorrect firing of gate signals for secondary devices causing higher turn OFF losses and consequently reducing the overall efficiency of the converter. FHA

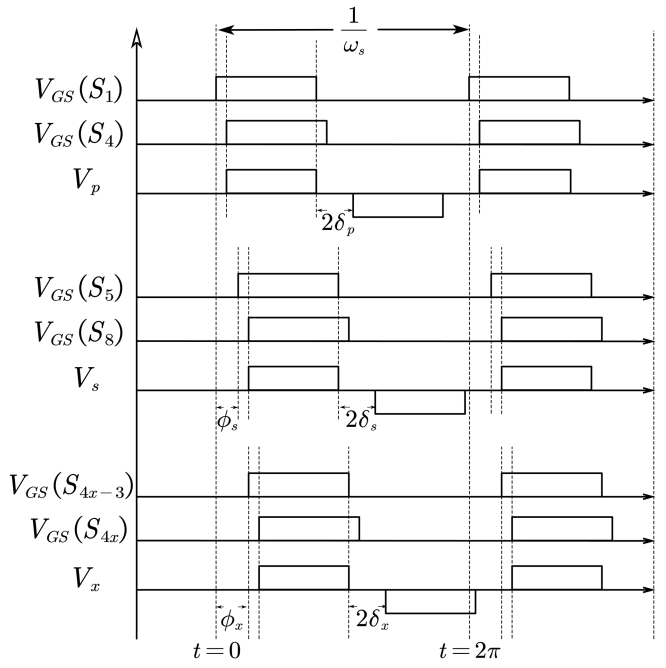

Fig. 5. Relationships between port voltages and corresponding control parameters.

generated port currents led to ≈ 35.5% error in zero-crossing phase angle estimation when compared with the experimentally obtained wave forms compared with GHA [7].

2) Formulation of GHA and I-GHA: As power electronic converter applications have evolved with time, there has been an emerging need for dc–dc converters with wider voltage gain range for a range of applications including EV battery charging. As a result, the need for a better modeling approach was felt, which could replace FHA in port current reconstruction. The authors in [7] and [9] focused on developing GHA, which accounts for higher order switching frequency harmonics in modeling leading to higher port current reconstruction accuracy along with control realization complexity. However, similar to FHA, the output ac equivalent resistance is calculated as a summation of ratios of port voltage to port current for "k" harmonics in GHA

$$R'_{\text{ac}x} = \frac{N_p}{N_x} \sum_{k=1}^{2m+1} \frac{V'_{x\text{rms}}}{k^2 I'_{x\text{rms}}} \approx R'_{\text{out}x}. \tag{2}$$

The next evolutionary step in the advancement of modeling techniques of resonant converter is termed as I-GHA, in which the output impedance could be resistive, capacitive, or inductive for a particular harmonic. Instead of representing the terminal impedance as a resistor, this model establishes a relation between the desired voltage–power combination and the control variables (i.e., frequency and phase shift angles) for a given load while minimizing the total switching network losses. With that, the accuracy of port current rms/peak estimation turns out significantly enhanced, which lets the converter operate under loss-optimal condition with the best thermal performance. The equivalent ac

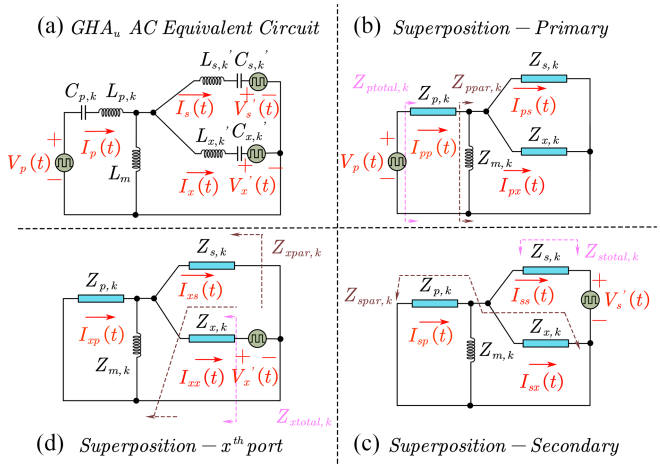

Fig. 6. (a) I-GHA AC equivalent model and (b), (c), and (d) equivalent port circuits post applying superposition at primary, secondary, and xth ports, respectively.

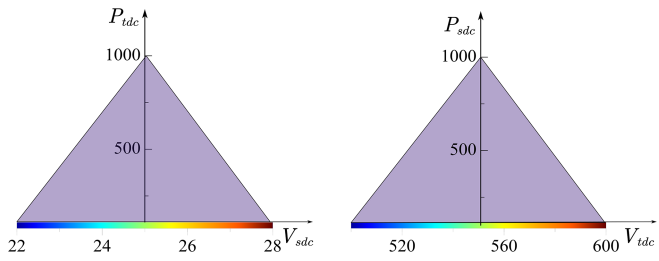

Fig. 7. Output steps desired on secondary and tertiary.

output impedance referred to primary side is defined as follows:

$$R'_{\mathrm{ac}x} = \frac{N_p}{N_x}\frac{\sum_{k=1}^{2m+1} V_{x,k}^2}{P_{xac}}. \tag{3}$$

Figs. 3 and 6(a) delineate the primary referred ac equivalent circuits for GHA and I-GHA, respectively. The voltage sources in both the approaches are delineated as quasi-square wave voltage sources, which can be represented as a summation of k odd order sinusoidal voltage sources ($k \to 1$ to $2m+1; m \in [0, \infty)$), which includes the fundamental and higher order harmonics as formulated below:

$$V_p(t) = \frac{4V_{\mathrm{pdc}}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(2\pi F_{\mathrm{sw}} kt)}{k} \tag{4}$$

$$V'_s(t) = \frac{N_p}{N_s}\frac{4V_{\mathrm{sdc}}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(2\pi F_{\mathrm{sw}} kt - k\phi_s)}{k} \tag{5}$$

$$V'_x(t) = \frac{N_p}{N_x}\frac{4V_{x\mathrm{dc}}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(2\pi F_{\mathrm{sw}} kt - k\phi_x)}{k}. \tag{6}$$

However, the major difference in both these circuits is the exclusion of the output load impedance and inclusion of square wave ac-voltage sources for each of the output ports based on (5) and (6) within the equivalent model based on I-GHA. It is argued that requisite information of load impedance, such as its magnitude and angle, is contained within the formulation of port voltages specifically defined by the control variables, such as $(F_{\mathrm{sw}}, \phi_s, \phi_x)$. The next sections focus on the I-GHA-based analytical model derivation and verification.

B. I-GHA-Based Three-Port C3L3 Model Derivation

In ideal MPC, power can be transferred from one port to any of the other ports and vice-versa. The summation of output dc power is always equal to the summation of input dc power. In addition, for a given port, the ac active power injected to the rectifying/inverting full-bridge is equal to its dc output power since active power is processed when ac current and voltage are in-phase. These objective statements serve as a premise for development of the I-GHA model and its ac equivalent representation is shown in Fig. 6(a). The aim of the following derivation is to obtain the time-domain dynamics of the port currents and subsequently construct the ac active port power formulations.

Together $(F_{\mathrm{sw}}, \phi_s, \phi_x)$, where (ϕ_s, ϕ_x) are the interbridge phase shifts of secondary and xth bridge with respect to the primary port voltage, are the control variable set for this converter. Furthermore, intrabridge phase shifts, such as $(\delta_p, \delta_s,$ and $\delta_x)$ are the additional control variables, which brings the total degrees of control for this converter to 6. However, the full-bridge duty cycle modulation is not considered within the scope of this article as those variables only come into consideration in case of hybrid phase-duty control, especially at lighter loads to extend the soft-switching range [13] and thus can be ignored to reduce the complexity of the model as the objective here is to build a nonapproximated circuit equivalence of a phase-frequency modulated resonant converter. The relationship between the control variables and their port voltages and their impact on the waveform is elucidated in Fig. 5.

With the existence of nonidealities in power devices and other parts of the converter, the loss optimization routine needs to account for precise parametric extraction of semiconductor devices, which can be performed standalone prior to the switching modulation implementation phase for a given power converter. The parameters subject to uncertainties and crucial in loss calculations are ON-state resistance $(R_{\mathrm{ds,on}})$, threshold/plateau voltage $(V_{\mathrm{th}}$ and $V_{pl})$, and device junction capacitances (gate-source C_{gs}, gate-drain C_{gd}, and drain-source C_{ds}). The work in [47] focuses on accurate measurement of dynamic ON-state resistance of GaN power devices under hard and soft switching conditions by double and multiple pulse test, while Rothmund et al. [50] performed calorimetric measurements to estimate $R_{\mathrm{ds,on}}$. Multiple methods in [44] for V_{th} extraction exist two of the popular ones being: 1) extrapolation in the linear region and b) constant current method. Extractions of semiconductor parasitic capacitances can be performed using power device analyzer using the method discussed in [43]. For primary side, $R_{\mathrm{winding},p}$ = lumped winding resistance on primary side transformer; $R_{\mathrm{dson},p}$ = ON-state resistance of primary side semiconductor devices; ESR_p = series equivalent series resistance (ESR) of resonant capacitors on primary side; $R_p = R_{\mathrm{winding},p} + 2 * R_{\mathrm{dson},p} + \mathrm{ESR}_p$. For secondary side,

$R_{\text{winding},s}$ = lumped winding resistance on secondary side transformer; $R_{\text{dson},s}$ = ON-state resistance of secondary side semiconductor devices; ESR_s = series ESR of resonant capacitors on secondary side; $R_s = R_{\text{winding},s} + 2 * R_{\text{dson},s} + \text{ESR}_s$. For xth side, $R_{\text{winding},x}$ = lumped winding resistance on xth side transformer; $R_{\text{dson},x}$ = ON-state resistance of xth side semiconductor devices; ESR_x = series ESR of resonant capacitors on xth side; $R_x = R_{\text{winding},x} + 2 * R_{\text{dson},x} + \text{ESR}_x$.

The resonant port impedance Z_y $(y \in \{p, s, x\})$ and magnetizing impedance Z_m are calculated as follows:

$$Z_{p,k} = R_p + j.2\pi F_{\text{sw}} k L_p - j.\frac{1}{2\pi F_{\text{sw}} k C_p} \tag{7}$$

$$Z_{s,k} = \frac{N_p}{N_s}.\left(R_s + j.2\pi F_{\text{sw}} k L_s - j.\frac{1}{2\pi F_{\text{sw}} k C_s}\right) \tag{8}$$

$$Z_{x,k} = \frac{N_p}{N_x}.\left(R_x + j.2\pi F_{\text{sw}} k L_x - j.\frac{1}{2\pi F_{\text{sw}} k C_x}\right) \tag{9}$$

$$Z_{m,k} = 2\pi F_{\text{sw}} k L_m. \tag{10}$$

For "x" ports, identical number of equivalent circuits need to be formulated. Impedance parameters for those circuits can be constructed as follows: $Z_{\text{ppar},k} = Z_{s,k}||Z_{x,k}||Z_{m,k}$; $Z_{\text{spar},k} = Z_{p,k}||Z_{x,k}||Z_{m,k}$; $Z_{x\text{par},k} = Z_{p,k}||Z_{s,k}||Z_{m,k}$; $Z_{\text{ptotal},k} = Z_{ppar,k} + Z_{p,k}$; $Z_{\text{stotal},k} = Z_{\text{spar},k} + Z_{s,k}$; $Z_{x\text{total},k} = Z_{x\text{par},k} + Z_{x,k}$.

As observed in Fig. 6, due to multiple voltage sources in a linear circuit, Superposition-based port current formulation approach is utilized for obtaining port current equations following the steps below.

Port currents defined in Fig. 6(a) are calculated as cumulative sum of individual currents in "x" loops as shown in Fig. 6(b), (c), (d) as follows:

$$I_p(t) = I_{pp}(t) + I_{ps}(t) + I_{px}(t) \tag{11}$$

$$I_s(t) = \frac{N_p}{N_s}(I_{ss}(t) + I_{ss}(t) + I_{sx}(t)) \tag{12}$$

$$I_x(t) = \frac{N_p}{N_x}(I_{xx}(t) + I_{xp}(t) + I_{xs}(t)). \tag{13}$$

Superposed currents in Fig. 6(b) are calculated as

$$I_{pp}(t) = |V_p|.\sum_{k=1}^{2m+1}\frac{\sin(2\pi F_{\text{sw}} kt - \angle Z_{p\text{total},k})}{k.|Z_{p\text{total},k}|} \tag{14}$$

$$I_{ps}(t) = |V_s'|.\sum_{k=1}^{2m+1}\frac{|Z_{\text{spar},k}|}{|Z_{\text{stotal},k}|}\frac{\sin(2\pi F_{\text{sw}} kt - k\phi_s + \angle Z_{\text{spar},k} - \angle Z_{p,k} - \angle Z_{\text{stotal},k})}{k.(|Z_{p,k}|)} \tag{15}$$

$$I_{px}(t) = |V_t'|.\sum_{k=1}^{2m+1}\frac{|Z_{x\text{par},k}|}{|Z_{x\text{total},k}|}\frac{\sin(2\pi F_{\text{sw}} kt - k\phi_x + \angle Z_{x\text{par},k} - \angle Z_{p,k} - \angle Z_{x\text{total},k})}{k.(|Z_{p,k}|)}. \tag{16}$$

Superposed currents in Fig. 6(c) are calculated as

$$I_{sp}(t) = |V_p|.\sum_{k=1}^{2m+1}\frac{|Z_{\text{ppar},k}|}{|Z_{p\text{total},k}|}\frac{\sin(2\pi F_{\text{sw}} kt + \angle Z_{\text{ppar},k} - \angle Z_{s,k} - \angle Z_{p\text{total},k})}{k.(|Z_{s,k}|)} \tag{17}$$

$$I_{ss}(t) = |V_s'|.\sum_{k=1}^{2m+1}\frac{\sin(2\pi F_{\text{sw}} kt - k\phi_s - \angle Z_{\text{stotal},k})}{k.|Z_{\text{stotal},k}|} \tag{18}$$

$$I_{sx}(t) = |V_t'|.\sum_{k=1}^{2m+1}\frac{|Z_{x\text{par},k}|}{|Z_{x\text{total},k}|}\frac{\sin(2\pi F_{\text{sw}} kt - k\phi_x + \angle Z_{x\text{par},k} - \angle Z_{s,k} - \angle Z_{x\text{total},k})}{k.(|Z_{s,k}|)}. \tag{19}$$

Superposed currents in Fig. 6(d) are calculated as

$$I_{xp}(t) = |V_p|.\sum_{k=1}^{2m+1}\frac{|Z_{\text{ppar},k}|}{|Z_{p\text{total},k}|}\frac{\sin(2\pi F_{\text{sw}} kt + \angle Z_{\text{ppar},k} - \angle Z_{x,k} - \angle Z_{p\text{total},k})}{k.(|Z_{p,k}|)} \tag{20}$$

$$I_{xs}(t) = |V_s'|.\sum_{k=1}^{2m+1}\frac{|Z_{\text{spar},k}|}{|Z_{\text{stotal},k}|}\frac{\sin(2\pi F_{\text{sw}} kt + \angle Z_{\text{spar},k} - \angle Z_{x,k} - \angle Z_{\text{stotal},k})}{k.(|Z_{x,k}|)} \tag{21}$$

$$I_{xx}(t) = |V_t'|.\sum_{k=1}^{2m+1}\frac{\sin(2\pi F_{\text{sw}} kt - \angle Z_{x\text{total},k})}{k.|Z_{x\text{total},k}|}. \tag{22}$$

From (4)–(6) rms voltage and current equation for kth harmonic can be derived as follows:

$$V_{y\text{rms},k} = \frac{4V_{y\text{dc}}}{\pi.k.\sqrt{2}} \tag{23}$$

$$I_{y\text{rms},k} = \frac{|I_{y,k}|}{\sqrt{2}}. \tag{24}$$

The active ac power at each port can be calculated as

$$P_{\text{pac}} = \sum_{k=1}^{2m+1} V_{\text{prms},k}.I_{\text{prms},k}.\cos(-\angle I_{p,k}) \tag{25}$$

$$P_{\text{sac}} = \sum_{k=1}^{2m+1} V_{\text{srms},k}.I_{\text{srms},k}.\cos(k\phi_s - \angle I_{s,k}) \tag{26}$$

$$P_{\text{xac}} = \sum_{k=1}^{2m+1} V_{\text{xrms},k}.I_{\text{xrms},k}.\cos(k\phi_x - \angle I_{x,k}). \tag{27}$$

The summation of active power at all output ports is equal to the input active power assuming there is no power loss within the circuit as indicated in

$$P_{\text{pac}} = P_{\text{sac}} + P_{\text{xac}}. \tag{28}$$

TABLE I
SENSITIVITY ANALYSIS OF CONTROL VARIABLES C FOR PARAMETRIC VARIATION IN N

	$L_p\ (\mu H)$	$L_s\ (\mu H)$	$L_x\ (\mu H)$	$C_p\ (nF)$	$C_s\ (nF)$	$C_x\ (nF)$	$L_m\ (\mu H)$
Value	7.85	16	0.068	13.39	6.67	1650	73.32
Range	7.065–8.635	14.4–17.6	0.061–0.075	12.051–14.729	6.00–7.337	1485–1815	66–80.652
F_{sw}sensitivity	1.03–0.94	1.02–0.96	1.09–0.88	1.04–0.96	1.04–0.95	1.02–0.97	1.06–0.92
ϕ_s sensitivity	1.12–0.87	1.1–0.89	1.12–0.91	1.14–0.92	1.14–0.93	1.11–0.92	1.08–0.93
$\phi_x$sensitivity	1.07–0.91	1.12–0.91	1.15–0.93	1.14–0.90	1.21–0.87	1.19–0.86	1.15–0.86

The dc power sunk at the output ports is labeled as $P_{s\text{dc}}$ and $P_{x\text{dc}}$ for the secondary and xth ports, respectively, and can be equated to the active ac power calculated in (26) and (28)

$$P_{s\text{ac}} = P_{s\text{dc}} = V_{s\text{dc}}.I_{s\text{dc}} \tag{29}$$

$$P_{x\text{ac}} = P_{x\text{dc}} = V_{x\text{dc}}.I_{x\text{dc}}. \tag{30}$$

Solving (25) to (30) analytically can yield the control variables (F_{sw}, ϕ_s, and ϕ_x) required to achieve the requisite values of ($V_{s\text{dc}}$, $V_{x\text{dc}}$, $P_{s\text{dc}}$, and $P_{x\text{dc}}$) based on the voltage and current requirements of the load ports.

The analytical model derived thus far assumed that all the resonant port parameters are nonsusceptible to environmental variations. However, the leakage and magnetizing inductance of the multiwinding transformer in addition to the resonant capacitors on the three-ports do exhibit parametric variations due to their characteristics and observe a change in their resultant values with variations in temperature, operating conditions, core/winding air gaps, and PCB layout. Hence, it becomes quintessential to analyze the effect of these parameter variations with respect to the estimation of control variables C = ($F_{\text{sw}}, \phi_s, \phi_x$) To quantify this change, a sensitivity term S is introduced, which is defined as the relative change in the control variable with respect to relative variation in parameter N

$$S_N^C = P_{sdc} = \frac{\frac{\Delta C}{C}}{\frac{\Delta N}{N}} \tag{31}$$

where N $\in (L_p, L_s, L_x, C_p, C_s, C_x, L_m)$. A sensitivity analysis of each control variable C with respect to parameter N is summed up in this Table I for the total loss optimum control variable set for voltage–power combination (600 V, 28 V, 1000 W, and 1000 W). The parameters in N are varied by a range of 10% and each control variable sensitivity is calculated and tabulated in Table I. For example, for a 5% variation in L_p, the required change in ϕ_s and ϕ_x should be $\approx 4.35\%$ to 5.6% of their nominal values, which if not performed due to unaccounted L_p variation, would result in only 0.244 W of extra power losses and 0.8% total semiconductor loss compromise from the optimal point.

Another noteworthy point is that this analytical model is derived for a general semiconductor technology and is extendable to the converters utilizing different semiconductor materials including GaN and SiC. The fundamental steps i.e., I-GHA-based voltage/current-reconstruction methodology and phase-frequency modulation-based loss optimization process remain the same. The semiconductor parasitic extraction is a critical required step for taking most advantage of the proposed loss optimization routine (see Section IV) and the extracted semiconductor parasitic parameters should be accounted for in the analytical model of the converter. The derived analytical model in this section is required to be substantiated with simulation results in order to determine its accuracy vis-à-vis its predecessors (GHA and FHA), which is delineated in the following sections.

C. Model Definition for Simulation and Analysis

Converter output voltage and power range are shown in Fig. 7 dictated by the state of charge of HV and LV batteries. Three corner conditions 1) ($V_{s\text{dc}}$, $V_{x\text{dc}}$, $P_{s\text{dc}}, P_{x\text{dc}}$) = (600 V, 28 V, 1000 W, 1000 W), 2) ($V_{s\text{dc}}$, $V_{x\text{dc}}$, $P_{s\text{dc}}, P_{x\text{dc}}$) = (500 V, 22 V, 1000 W, 1000 W), and 3) ($V_{s\text{dc}}$, $V_{x\text{dc}}$, $P_{s\text{dc}}, P_{x\text{dc}}$) = (600 V, 22 V, 100 W, 100 W) are chosen as candidates for model verification. The output voltage–power combinations considered are fed as input to the analytical model to obtain the control variables (F_{sw}, ϕ_s, ϕ_x) as the solution set. For a given voltage–power combination, there is a possibility of multiple control variable sets which satisfy (25) to (30). Subsequently, the control variable solution sets generated are fed as input to a simulation model of Fig. 1 mimicking the behavior of the converter in order to obtain simulated port currents and voltages, which are then juxtaposed with the analytically reconstructed port currents and voltages to determine the model's accuracy in terms of magnitude and phase predictions of the waveform. A simulation model based on the circuit defined in Fig. 1 and Table VIII values is constructed in piece-wise linear electrical circuit simulation software due to its higher accuracy and faster speed of implementation of power electronics circuits [25]. For model verification, the port current parameters, such as peak value and instantaneous value, at the switching transition i.e., ($\omega t = \zeta$) predominantly dictate the relevant accuracy comparison—as these two parameters have significant impact on the calculation of conduction and switching loss, majorly contributing to the total semiconductor and transformer winding losses. Accurate estimation of these parameters is critical because the peak current value often determines the switch current rating selection, while the switching instantaneous value determines the turn-OFF losses in the corresponding devices, as demonstrated in Section III. $m = 499$ value, which determines the maximum number of odd harmonics considered for analytical model is chosen in order to provide a tolerable balance of analytical model accuracy and simulation time.

D. I-GHA Model Verification and Its Comparison With FHA and GHA Counterparts

The I-GHA generated port currents are examined against the state-of-the-art techniques i.e., GHA and FHA and

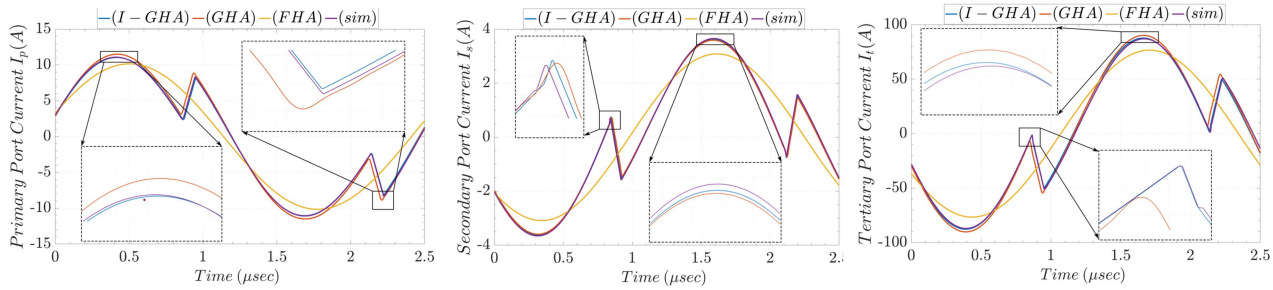

Fig. 8. Comparison of analytically reconstructed port currents $\{I_p, I_s, I_x\}$ from I-GHA, GHA, and FHA with simulation port currents at $\{600\,\text{V}, 28\,\text{V}, 1000\,\text{W}, 1000\,\text{W}\}$ with $\{398\,\text{kHz}, -25.074°, -23.49°\}$

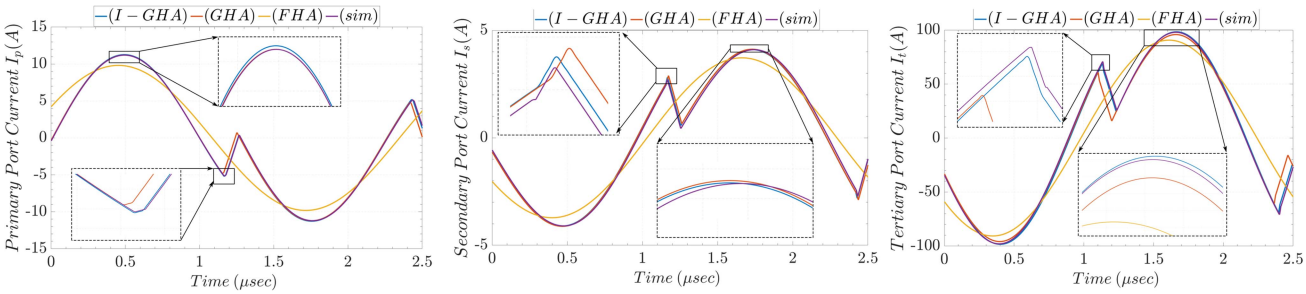

Fig. 9. Comparison of analytically reconstructed port currents $\{I_p, I_s, I_x\}$ from I-GHA, GHA, and FHA with simulation port currents at $\{500\,\text{V}, 22\,\text{V}, 1000\,\text{W}, 1000\,\text{W}\}$ with $\{396\,\text{kHz}, -12.6°, -14°\}$

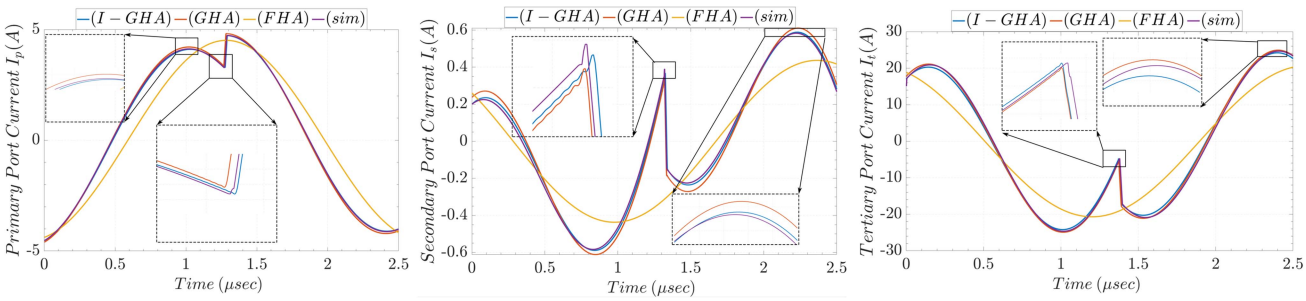

Fig. 10. Comparison of analytically reconstructed port currents $\{I_p, I_s, I_x\}$ from I-GHA, GHA, and FHA with simulation port currents at $\{600\,\text{V}, 22\,\text{V}, 100\,\text{W}, 100\,\text{W}\}$ with $\{360\,\text{kHz}, -2.6°, -2.2°\}$

compared with the simulation obtained currents in Figs. 8–10 at predefined voltage–power levels. Table II sums up the peak, switching instant values for those port currents in addition to the conduction and switching loss of the switching network. The error % (in brackets) is also calculated for conduction and switching loss based on the simulation obtained values. As is observed for almost all the cases, juxtaposing simulation port currents with analytically formulated port currents, I-GHA shows much lower error % when compared with GHA. FHA is not even considered for this comparison as the wave-shape heavily deviates from the simulation current. A higher discrepancy is observed between port current switching instant values estimated by I-GHA and GHA specifically for the tertiary port. A lower value of port impedance on the tertiary side due to lower turns ratio is comparable to the load impedance estimated by GHA causing a huge variation in switching instant value estimation as observed. Although GHA could be acceptable for estimating peak, rms current as the mean error % is still $\approx 5\%$, however, it generates substantial deviation in the estimation of switching instant values. In terms of loss calculation as well, I-GHA exhibits much lower error % compared with GHA for both conduction and switching loss. An important factor to note is that deadtime is not considered during this analysis and hence switching instant current values are directly used for turn-ON and turn-OFF loss calculations in the succeeding section. A detailed semiconductor loss analysis is performed for this converter topology considering the I-GHA modeling approach in the next section followed by a thorough loss optimization process.

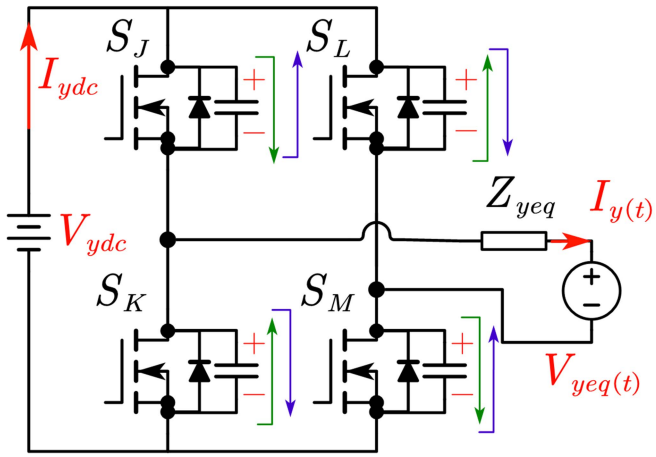

Fig. 11. ZVS investigation using thevenin equivalent circuit (a) for switches (S_L, S_K), current direction shown in green and $V_{yeq}(t) > 0, I_y(t) > 0$ (b) for switches (S_J, S_M), current direction shown in blue and $V_{yeq}(t) < 0, I_y(t) < 0$.

TABLE II
COMPARISON OF RECONSTRUCTED PORT CURRENTS BASED ON I-GHA, GHA, AND SIMULATION VALUES FOR THREE VOLTAGE–POWER COMBINATIONS

600V, 28V, 1kW, 1kW	Simulation	I-GHA	GHA
I_{ppk} (A)	11.08 (0)	11.06 (0.1)	11.49 (3.7)
I_{spk} (A)	3.655 (0)	3.614 (1.1)	3.59 (1.7)
I_{xpk} (A)	87.012 (0)	87.69 (0.7)	90.1678 (3.6)
$I_p(\zeta)$ (A)	8.345 (0)	8.2 (1.7)	8.89 (6.5)
$I_s(\zeta)$ (A)	0.714 (0)	0.74 (3.6)	0.73 (2.2)
$I_x(\zeta)$ (A)	1.14 (0)	1.169 (2.1)	4.77 (104)
P_{cond} (W)	8.9 (0)	8.9 (0)	9.5 (6.8)
P_{switch} (W)	22.7 (0)	22.6 (0.5)	24.7 (8.9)
500V, 22V, 1kW, 1kW	Simulation	I-GHA	GHA
I_{ppk} (A)	11.2 (0)	11.26 (0.5)	11.26 (0.5)
I_{spk} (A)	4.098 (0)	4.10 (0.4)	4.12 (0.5)
I_{xpk} (A)	97.96 (0)	98.366 (0.4)	95.8361 (2.1)
$I_p(\zeta)$ (A)	5.147 (0)	5.2 (1)	4.8 (6.7)
$I_s(\zeta)$ (A)	2.7 (0)	2.81 (4)	2.89 (4)
$I_x(\zeta)$ (A)	70.86 (0)	68.96 (2.6)	61.16 (13.6)
P_{cond} (W)	9.8 (0)	9.8 (0.2)	9.6 (1.5)
P_{switch} (W)	27.1 (0)	27.1 (0.3)	25.5 (5.9)
600V, 28V, 0.1kW, 0.1kW	Simulation	I-GHA	GHA
I_{ppk} (A)	4.124 (0)	4.1 (0.4)	4.21 (2.1)
I_{spk} (A)	0.588 (0)	0.583 (0.8)	0.610 (3.7)
I_{xpk} (A)	24.65 (0)	24.21 (1.7)	24.95 (1.2)
$I_p(\zeta)$ (A)	3.275 (0)	3.272 (0.03)	3.36 (2.5)
$I_s(\zeta)$ (A)	0.39 (0)	0.37 (5.1)	0.34 (12.8)
$I_x(\zeta)$ (A)	4.72 (0)	4.71 (0.2)	5.37 (13.7)
P_{cond} (W)	1.0 (0)	1.01 (1.9)	1.07 (5.8)
P_{switch} (W)	15 (0)	15.6 (3.8)	15.7 (4.67)

III. I-GHA DERIVED SEMICONDUCTOR LOSS MODEL CONSTRUCTION

The semiconductor loss models are derived for a generalized three-port C3L3 resonant converter as follows.

A. I-GHA Enabled Conduction Loss Formulation

Accurate rms current estimation is pertinent for conduction loss calculation. Port rms currents can be formulated based on I-GHA enabled analytical reconstruction of kth harmonic current amplitude as follows:

$$I_{y\text{rms}} = \frac{\sqrt{I_{y,k}^2 + I_{y,k+2}^2 \cdots I_{y,2m+1}^2}}{\sqrt{2}}. \tag{32}$$

Total semiconductor conduction loss is calculated as

$$P_{\text{cond}} = \sum_{y=p}^{t} 2.I_{y,\text{rms}}^2.R_{\text{dson},y} \tag{33}$$

where $R_{\text{dson},y}$ is the device ON-state resistance on the primary (p), secondary (s), and xth bridges, respectively.

B. Switching Loss Formulation Using ZVS Feasibility Evaluation Through Thevenin Equivalence

Switching loss model is developed for conventional three-port C3L3 resonant topology with a target to achieve lowest switch transition losses. The switch loss functions and soft-switching constraints are derived for the entire voltage–power range as follows.

1) Turn-ON Loss Formulation: ZVS turn-ON is achieved by discharging output capacitance C_{oss} of a semiconductor device during turn-ON transition. The three main constraints for achieving ZVS in a three-port C3L3 resonant converter are 1) lagging port current phase with respect to port voltage, 2) adequate minimum dead time in a half-bridge leg, and 3) certain minimum amplitude of magnetizing current. The first constraint is a function of operational control variable set being implemented on the converter and satisfied by operating the converter in the negative slope of gain versus frequency curve, also referred to as the inductive region [29]. Second and third constraints are interrelated and the relationship is explored as follows. An equivalent three-port model is developed to analytically investigate all semiconductor devices at various switching instants within a switching cycle. Similar analysis has been formulated for a two port *CLLC* to obtain the relationship of dead time t_d, magnetizing inductance value L_m, switching frequency F_{sw}, and device output capacitances C_{oss} as [5]: $L_m = \frac{t_d}{8F_{\text{sw}}C\text{oss}}$ where, C_{oss} is the parallel combination of output capacitances of primary and secondary semiconductor devices (referred to primary).

The switch nomenclature used in Fig. 11 corresponds to primary, secondary and xth bridge switches as follows:

$S_J \in \{S_1, S_5, S_{4x-3}\}, S_L \in \{S_3, S_7, S_{4x-1}\}, S_K \in \{S_2, S_6, S_{4x-2}\}, and S_M \in \{S_4, S_8, S_{4x}\}$.

The Thevenin equivalent parameters $V_{\text{yeq}} and\, Z_{\text{yeq}}$ can be calculated for primary port as follows and can be extended to other ports:

$$V_{\text{peq}} = V_s(t)Z_m\frac{[Z_{\text{par}x} - Z_x]}{Z_x[Z_{\text{par}x} + Z_s]} - V_x(t)Z_m\frac{[Z_{\text{par}s} - Z_s]}{Z_s[Z_{\text{par}s} + Z_x]}$$
$$Z_{\text{peq}} = Z_p + (Z_m||Z_s||Z_x) \tag{34}$$

where $Z_{\text{par}p} = (Z_m||Z_p)$; $Z_{\text{par}s} = (Z_m||Z_s)$; $Z_{\text{par}x} = (Z_m||Z_x)$

ZVS criteria for two distinct commutation cases for both the inverting and rectifying modes are explained as follows:

Case I—Inverting side:

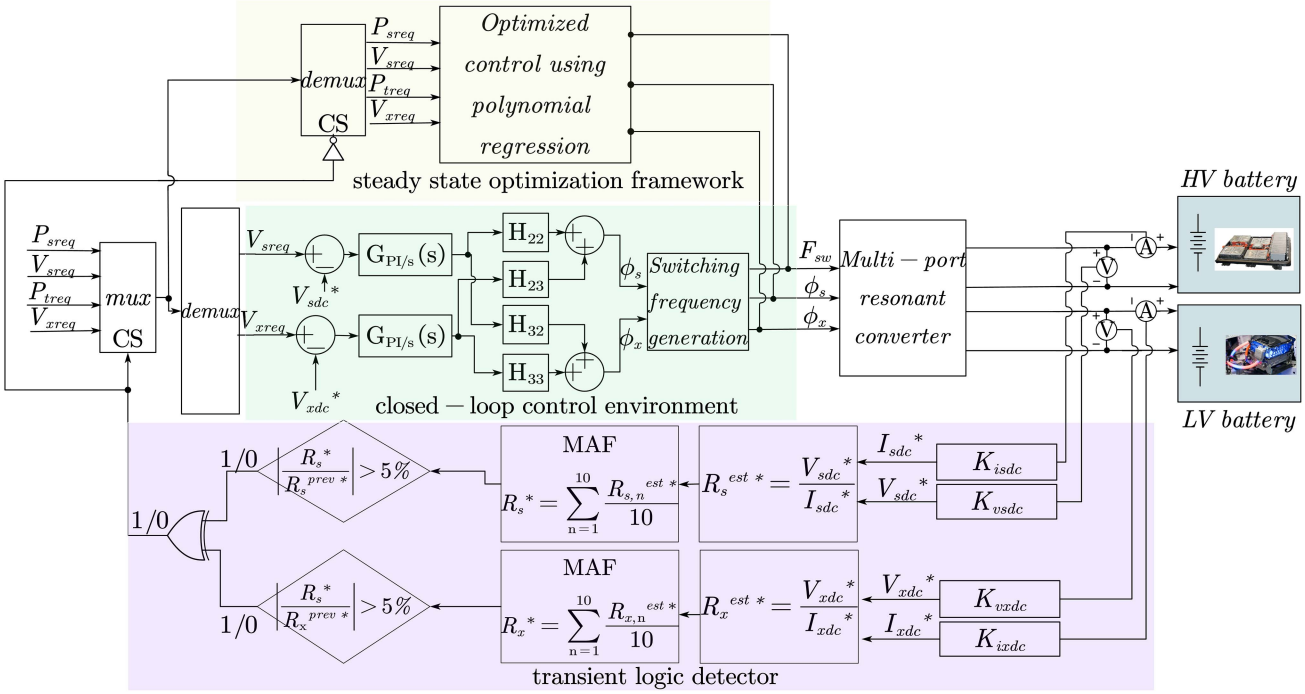

Fig. 12. Transient detector logic based closed loop control and optimization framework for three-port C3L3 resonant converter.

Following the instantaneous circuit structure shown in Fig. 11 and using the turn-ON instant currents for switches $S_L$andS_K at switching instant $(t = \zeta)$

The total energy sunk by the Thevenin port voltage V_{yeq} can be expressed as

$$E_{\text{sunk}} = \int_0^{t_{zvs}} [V_{yeq}.I_{yeq\int}(\zeta) - V_{ydc}.I_{ydc}(\zeta)]dt \tag{35}$$

$$E_{\text{sunk}} = \int_0^{t_{zvs}} [V_{yeq}(-2C_{oss,y}\frac{dV_{ydc}}{dt}) - 0] = 2C_{oss,y}.V_{yeq}.V_{ydc} \tag{36}$$

where t_{zvs} is the time required for completely discharging C_{oss} of semiconductor devices of that port. The total energy in the switch remains constant during commutation interval, which helps formulate necessary constraint $E_{\text{sourced}} \geq E_{\text{sunk}}$ for facilitating ZVS in *Case I* as follows:

$$\frac{1}{2}Z_{yeq}I_{yeq}(\zeta)^2 \geq 2C_{oss,y}.V_{yeq}(\zeta).V_{ydc}. \tag{37}$$

The minimum current $|I_{yeq}| \geq |I_{zvs}|$ required to achieve ZVS on switches S_L and S_K is given by

$$|I_{zvs(L,K)}| \geq 2\frac{\sqrt{C_{oss,y}.V_{yeq}.V_{ydc}}}{\sqrt{Z_{yeq}}}. \tag{38}$$

Similarly, since the port voltage follows half-wave symmetry, the above analysis can be extended to formulate minimum current required to achieve ZVS on switches S_J and S_M as follows:

$$|I_{zvs(J,M)}| \geq 2\frac{\sqrt{-C_{oss,y}.V_{yeq}.V_{ydc}}}{\sqrt{Z_{yeq}}}. \tag{39}$$

TABLE III
MINIMUM VALUE OF I_{zvs} REQUIRED FOR I_y TO ACHIEVE ZVS FOR ALL SEMICONDUCTOR DEVICES ON INVERTING AND RECTIFYING SIDES

Side	Switches	$\lvert I_{zvs}\rvert$	$\angle I_y(\zeta)$
Inverting	S_J, S_M	$\frac{2\sqrt{-C_{oss,y}V_{yeq}V_{ydc}}}{\sqrt{Z_{yeq}}}$	2π
Inverting	S_L, S_K	$\frac{2\sqrt{C_{oss,y}V_{yeq}V_{ydc}}}{\sqrt{Z_{yeq}}}$	π
Rectifying	S_L, S_K	$\frac{2\sqrt{-C_{oss,y}V_{yeq}V_{ydc}}}{\sqrt{Z_{yeq}}}$	$2\pi + \phi_y + \pi$
Rectifying	S_J, S_M	$\frac{2\sqrt{C_{oss,y}V_{yeq}V_{ydc}}}{\sqrt{Z_{yeq}}}$	$2\pi + \phi_y$

Case II—Rectifying side:

Inverting side approach can be extended to rectifying side as well, where the only variations are the current ($I_{yeq}$and I_{ydc}) directions, which are reversed compared with the inverting side and accordingly, the corresponding I_{zvs} equations are derived. The required ZVS criteria for both inverting and rectifying side is summarized in the Table III below.

For $I(\zeta) \geq I_{zvs}$, the turn-ON loss and Output capacitance loss can be considered 0. However, if the criteria are not met, turn-ON loss needs to be accounted for those semiconductors and is formulated as follows:

$$P_{\text{turnon},y} = 2V_{ydc}.(|I_y(\zeta)| - |I_{zvs}|).F_{sw}.t_{ton,y} \tag{40}$$

where

$$t_{on,y} = \frac{Q_{gd}.R_{g,y}}{V_{gs,y} - V_{pl,y}} + R_{g,y}.C_{in,y}.\ln\frac{V_{gs,y} - V_{th,y}}{V_{gs,y} - V_{pl,y}}. \tag{41}$$

Typically, t_{zvs} is used as the marginal value of the deadtime between intraleg semiconductor devices so that the additional

body-diode conduction losses during deadtime period can be minimized. For any reason, if deadtime $t_{\text{dt}} \geq t_{\text{zvs}}$, which is a very small fraction of the switching cycle

$$P_{\text{dead-time},y} = 4V_{f,y}.I_y(\zeta).(t_{\text{dt},y} - t_{\text{zvs},y}).F_{\text{sw}} \tag{42}$$

and should be accounted in semiconductor loss modeling. Equation (42) works with the assumption that $I_y(\zeta)$ remains constant for the entire duration of $(t_{\text{dt},y} - t_{\text{zvs},y})$.

2) Turn-OFF Loss Formulation: The total turn OFF loss for semiconductors in the yth bridge can be calculated as follows:

$$P_{\text{turnoff},y} = 2V_{y\text{dc}}.I_y(\zeta).F_{\text{sw}}.t_{\text{toff},y} \tag{43}$$

where

$$t_{\text{off},y} = \frac{Q_{gd}R_{g,y}}{V_{pl,y}} + R_{g,y}.C_{\text{in},y}.\ln\frac{V_{pl,y}}{V_{th,y}} \tag{44}$$

parameters $(Q_{gd},\ R_g,\ V_{pl},\ C_{\text{in}}, V_{\text{th}}) =$ (gate charge, gate resistance, plateau voltage, input capacitance, threshold voltage) for the corresponding devices can be obtained from detailed semiconductor device characterization following the procedure mentioned in Section II-B.

Other semiconductor losses such as reverse recovery loss $(P_{\text{diode},y} = 2V_{y\text{dc}}.I_{RR,y}.t_{RR,y}.F_{\text{sw}})$, output capacitance loss $(P_{\text{coss},y} = \frac{C_{\text{oss},y}.V_{y\text{dc}}^2.F_{\text{sw}}}{2})$ and gate charge loss $(P_{\text{gate},y} = Q_{g,y}.V_{gs,y}.F_{\text{sw}})$ are independent of load and typically contribute a smaller fraction of the total losses compared with conduction and switching and hence could be ignored for further optimization. However, conduction loss, switching loss, which are dependent on the port current values and consequently on the load power and output voltage are considered for constructing the objective function, discussed in detail in the next section.

IV. Semiconductor Power Loss Optimization

A. Conduction Loss Optimization

Apart from the total semiconductor loss optimization, discrete rms current optimization is critical as relaxing the rms current stress on the devices helps in selection of lower current-rated semiconductor devices, improving the possibility for a cost-effective design. The generalized objective function for conduction loss optimization is formulated in the following as the sum of squares of rms values of the port currents subject to $I_{y,\text{rms}} \geq 0$:

$$F_{\text{cond}}(F_{\text{sw}}, \phi_s, \phi_x) = \sum_{y=p}^{x} I_{y,\text{rms}}^2. \tag{45}$$

B. Current Frequency Product Optimization

Switching instant current $I_y(\zeta)$ for yth bridge plays a significant part in switching loss calculations. Within the equation of switching loss calculation, switching instant current $I(\zeta)$ and F_{sw} are the only two parameters, which vary according to the control variables. It provides an opportunity to fabricate a optimization cost function to minimize $I(\zeta) * F_{\text{sw}}$ product for a given voltage–power combination in order to evaluate the best control variable with the least switching losses. Hence, the current-frequency product optimization is necessitated and is formulated as follows:

$$F_{\text{switch}}(F_{\text{sw}}, \phi_s, \phi_x) = \sum_{y=p}^{x} I_y(\zeta) * F_{\text{sw}}. \tag{46}$$

C. Total Loss Optimization

The loss models derived in the previous section can be used to calculate the total semiconductor loss for this converter and global loss function is defined as follows $F_{\text{total}} = P_{\text{cond}} + P_{\text{switch}} + P_{\text{qrr}} + P_{\text{coss}} + P_{\text{gate}}$. It is imperative to note that for a given voltage–power combination, a single control variable might not necessarily ensure all three cost function minimizations viz. lowest total semiconductor loss, least conduction loss and least switching losses. There is a possibility that one or more control variables satisfy those requirements individually. Hence, it is requisite to formulate these discrete optimization functions, which allow the designer with additional insight during converter design and operation. To emphasize this point further, control variable sets for corner voltage–power conditions are tabulated in Table IV. The control variables tabulated are constrained to achieve the ZVS condition on all three ports in addition to achieving the requisite voltage–power on output ports. The calculated values of loss functions defined above in this section along with total semiconductor loss for each control variable are catalogued, which aid in making significant observations and derive loss trends. The conduction loss function F_{cond} shows a negative slope with an increase in switching frequency, which could be explained by the fact that increasing switching frequency and moving closer to the resonant frequency enables the converter to operate in a comparatively lower input impedance phase angle, thus reducing the portion of reactive power in the total power transferred. For a constant voltage–power condition, control variable with highest switching frequency (below resonant frequency) would demonstrate lowest rms current values. Typically, the current frequency product loss function F_{switch} follows similar trend as F_{cond}, however, it is also impacted by other converter parasitic, such as device output capacitance, deadtime, and transformer inter/intra winding capacitance, hence, it is difficult to predict the trend for all the voltage–power combinations. The total semiconductor loss value function is a sum total of conduction, switching and other semiconductor losses and its value follows the trend by its dominant constituent. Considering the case, $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}})$ = (600 V, 28 V, 750 W, 500 W), F_{switch} follows a parabolic curve with the minima achieved at 392 kHz, $-14.95°$, $-13.68°$, even with a comparative higher value of F_{cond}, it achieves the lowest total semiconductor loss at this control variable. For the case, $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}})$ = (600 V, 28 V, 1 kW, 1 kW), the control variable with the highest switching frequency provides the least value of F_{cond}, F_{switch}, and F_{total}. The least power loss achieved is 32.63 W, while another feasible control variable set executing the same power/voltage conversion results in a power loss of 37.07 W, which illustrates the effectiveness of the blended modulation by offering 13.6% lower total losses. Similar trends are observed for other voltage–power combinations tabulated in Table IV.

TABLE IV
VOLTAGE–POWER CORNER COMBINATIONS WITH THEIR RESPECTIVE CONTROL VARIABLES AND CALCULATED CONDUCTION AND CURRENT-FREQUENCY LOSS FUNCTIONS, TOTAL SEMICONDUCTOR LOSS FUNCTION

Voltage-Power	Control variable sets (F_{sw}, ϕ_s, ϕ_t)	F_{cond}	F_{switch}	$F_{total}(W)$
$600V, 28V,$ $1kW, 1kW$	$\{379kHz, -27.3°, -25.2°\}$, $\{370kHz, -29.3°, -27.3°\}$, $\{364kHz, -30.1°, -27.4°\}$, $\{358kHz, -32.2°, -29.1°\}$	2722, 2757 2773, 2788	4.3e6, 6.11e6 8.2e6, 1.05e7	32.63, 34.08 35.58, 37.07
$600V, 28V,$ $750W, 500W$	$\{396kHz, -14.7°, -13.4°\}$, $\{392kHz, -15°, -13.7°\}$, $\{385kHz, -15.8°, -14.6°\}$, $\{378kHz, -16.3°, -15°\}$,	693, 714 782, 842	3.7e6, 3.6e6 4.2e6, 4.86e6	19.88, 19.62 19.95, 19.61
$550V, 25V,$ $900W, 750W$	$\{380kHz, -20.5°, -13.6°\}$, $\{373kHz, -22.8°, -17.5°\}$, $\{367kHz, -24.4°, -17.8°\}$, $\{362kHz, -25.1°, -18.6°\}$	1505, 1601 1637, 1635	1.37e7, 1.35e7 1.38e7, 1.49e7	26.56, 29.29 29.56, 29.98
$550V, 25V,$ $750W, 250W$	$\{402kHz, -6.5°, -2.9°\}$, $\{396kHz, -7.1°, -2.8°\}$, $\{388kHz, -8.1°, -3.49°\}$ $\{380kHz, -9.3°, -2.9°\}$, $\{374kHz, -10.1°, -5.4°\}$	242 260, 274 264, 281	1.32e7 1.25e7, 1.35e7 1.33e7, 1.35e7	21.21 21.29, 21.219 21.3, 21.33
$525V, 22V,$ $750W, 250W$	$\{406kHz, -5.1°, -2.6°\}$, $\{398kHz, -6°, -3.3°\}$ $\{390kHz, -6.4°, -3.8°\}$, $\{384kHz, -7.6°, -4.6°\}$ $\{382kHz, -8.3°, -6.6°\}$, $\{374kHz, -10°, -8.3°\}$	603, 710 830, 888 822, 756	1.6e7, 1.8e7 1.94e7, 2.0e7 1.95e7, 1.87e7	21.15, 22.12 22.61, 22.87 23.2, 23.05

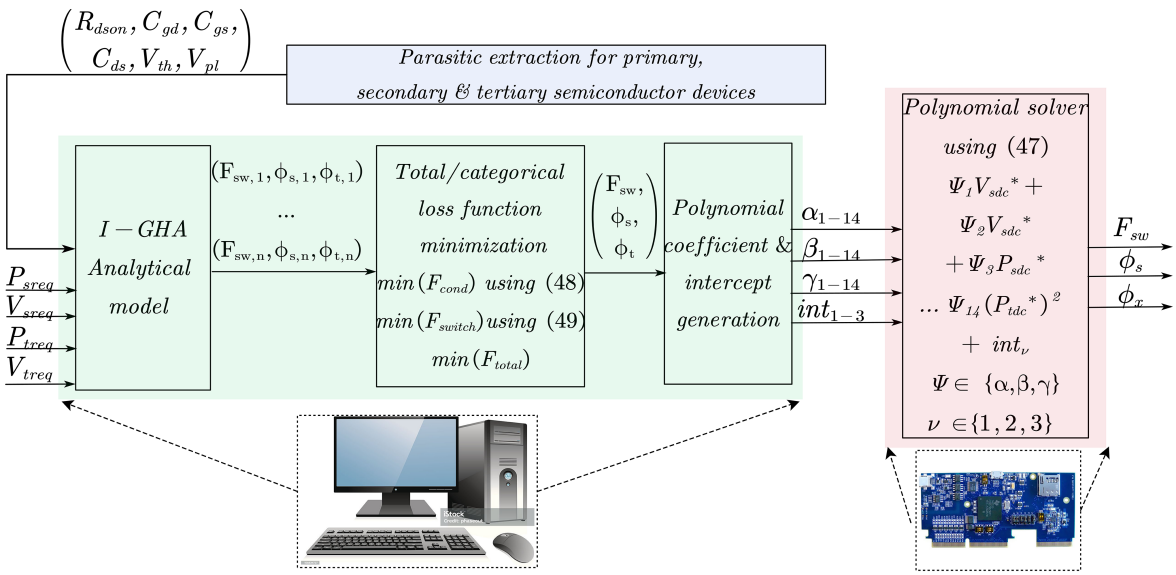

Fig. 13. Hybrid offline–online polynomial regression-based steady-state optimization framework for three-port C3L3 resonant converter.

V. REALIZATION AND IMPLEMENTATION OF OPTIMIZED SWITCHING MODULATION

A. Literature Review of Control Realization

An effort has been made to assess the existing literature related to control (open or closed loop) of a multiport resonant converter. The works in [9], [38], [39], [40], [41], [42], and [19] focused on controlling a three-port resonant converter and the findings are compiled in Table V. As observed from Table IV, multiple control variable sets could feasibly result in a unique voltage–power combination. As part of the optimization routine, the primary objective is to extract the most optimal control variable set, yielding objective function minima and to realize the variables through a hybrid-offline control method. To solve such optimization routines, multidimensional look-up table (LUT) have been historically used and implemented as part of the digital control platform. However, the major bottlenecks with LUT-based approaches [31] are constraints on memory size requirements and increased complexity in the process of recalling a variable set that does not match the entry array. This becomes particularly challenging with exponentially worsening space complexity with an increasing dimension of the array, which is four (comprising the port voltages and powers) in this case and also with the finely spaced array variable entries. Further, to recall and interpolate an entry that does not match the array members, linear interpolation is often used, which is, however, erroneous and time-consuming, thus potentially causing execution of instruction beyond one switching cycle and hence finally leading to signal aliasing issues. In additional, considering higher number of steps for increased output voltage–power resolution i.e., for example, 100 steps each in $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}})$ gives rise to 10^8 optimized control variable sets. This approach if implemented is nonscalable and the 3-D size of the LUT would be extremely large leading to memory allocation challenges in the DSP. Offline calculation of control variables is of a greater usefulness as it allows for higher computational accuracy by accounting for higher number of harmonics. Complimenting all these findings, transient detector logic-based steady-state closed loop control architecture including hybrid offline–online optimization framework is proposed that accounts for calculation of optimal variable sets for all possible voltage–power combinations.

TABLE V
CONTROL TECHNIQUE REVIEW OF EXISTING LITERATURE OF THREE-PORT RESONANT CONVERTER TOPOLOGY

Reference	Topology nomenclature	V_{pdc} /V_{sdc} /V_{xdc} (V)	$P_{out}(kW)$	Control variables	Control technique	Important points
[38]	Three port isolated resonant converter with switch-controlled capacitor	60 /72 /110	1.5	F_{sw}, ϕ_s, ϕ_x	Open loop	Power decoupling, Tank mismatch adjustment, Conduction loss minimization
[19]	Three port series resonant DC-DC	50 /36 /200	0.5	$F_{sw}, \phi_{12}, \phi_{13}$	Closed loop PI	Phase shifts are used for power transfer, Impact of output voltage on control variable is not analytically derived
[39]	Three port bidirectional series resonant converter	90 /90 /90	0.9	$F_{sw}, \delta_1, \delta_2, \delta_3$	First harmonic synchronized pulse width modulation	Power decoupling, ZVS for wide operating range, Power transfer direction changed smoothly, Output voltage is determined by duty ratio
[40]	Series resonance based three port converter	12 /24 /110	0.05	F_{sw}, ϕ	Single phase shift with closed loop control	Hardware decoupling, Maximum Power Point Tracking with autonomous control scheme
[41]	Three port resonant converter topology	400 /46 /10	6	F_{sw}, ϕ_s, ϕ_x	Nested dual phase shift based closed loop control	Wide voltage regulation with ZVS, Real time port decoupling
[42]	Bidirectional multiple port DC-DC transformer topology	390 /48 /12	0.3	F_{sw}	Open loop control	Self and cross load regulation, ZVS/ ZCS based soft-switching
[9]	Three port C3L3 converter	400 /600 /28	2	F_{sw}, ϕ_s, ϕ_x $\delta_p, \delta_s, \delta_x,$	Open loop frequency phase-duty modulation	Optimized conduction/ transformer losses, ZVS/SR based soft-switching for all loading and gain conditions, Algorithm based on global loss objective to reduce computational burden, Additional gain modulation flexibility due to hybrid control
This work	Three port C3L3 resonant converter	400 /600 /28	2	F_{sw}, ϕ_s, ϕ_x	Frequency -phase control	Non-approximated output impedance inclusion, Higher accuracy of port current reconstruction compared to existing state-of-the-art, Hybrid offline-online control architecture abiding one cycle switching limit, Higher precision in control variable generation based on output voltage-

B. Transient Logic Detector-Based Steady-State Closed Loop Control Architecture

In order to address the issue of output voltage regulation on both the ports due to transient variation of port power/voltage, a transient detector logic dependent control loop architecture as shown in Fig. 12 is proposed. During steady state operation, the required values of output power and voltages are fed to the optimized control using polynomial regression block. The detailed version of the block is shown in Fig. 13 and its working is discussed in further section. During output load transients, the control variable set generation after being triggered by transient detector logic is transferred from the steady state optimization framework to the closed loop control based on certain logic steps as defined ahead. The sensed values of output voltage and currents $(V^*_{\text{sdc}}, V^*_{x\text{dc}}, I^*_{\text{sdc}}, I^*_{x\text{dc}})$ are fed back to the DSP using appropriate gain, to estimate instantaneous resistances $R_s^{\text{est}*}$ and $R_x^{\text{est}*}$ at the output ports. In order to minimize the impact of dc output voltage ripple, current ripple, and sensor delays on resistance estimation process, a 10-point moving average filter is employed within the DSP. The moving average window (which in this case is 20 μs) is selected in a way that the resulting low-pass filter action can heavily attenuate the undesired ripple frequency components in the output port voltages, so that the estimation process remains uninterrupted. The ratio of averaged resistance values with the previously stored values ($\frac{R_s^*}{R_s^{\text{prev}*}}$ and $\frac{R_x^*}{R_x^{\text{prev}*}}$) is calculated to determine percentage variation of steady

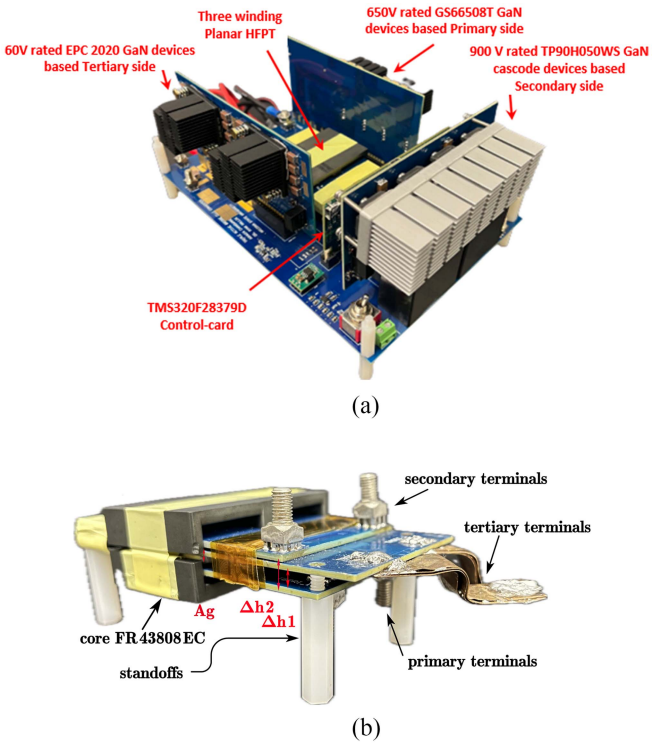

Fig. 14. Hardware realization of three-port resonant converter isometric view (a) converter (b) multiwinding transformer.

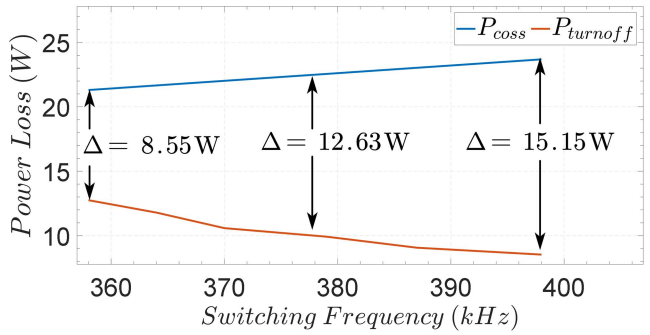

Fig. 15. Variation of total output capacitance loss and total turn-OFF loss for all rectifying bridge semiconductor devices across switching frequency.

state resistances. If the measured variation is found to be above certain margin, which is selected to be 5% in this case based on worst-case voltage ripple for both outputs, the converter switches over to closed loop control environment.

Based on the inputs of required output port dc voltages, an error signal is calculated by comparing the reference value to the sensed value and the error is provided to the PI controllers for each of the ports. Dey and Mallik [37] discussed a systematic derivation of cross coupling term cancelation-based approach for improvement of converter transient dynamics, which is also extendable to the C3L3 converter discussed in this article due to similar structures of active full-bridge network. Similar to TAB converter, the C3L3 demonstrates cross coupling terms ϕ_s and ϕ_x, which can be cancelled using this control loop. The obtained ϕ_s and ϕ_x are provided to the switching frequency generation block, which contains the 3-D contours of ($F_{\rm sw}$, ϕ_s, and ϕ_x) to obtain the required $F_{\rm sw}$ for a specified voltage–power combination. After termination of the transient event, once the relative variations in port resistances is within 5% of tolerance, the DSP shifts back to steady-state optimized control after a delay of 100 ms, which is conservatively selected for the converter output to reach the steady state for a control bandwidth of ≈50 kHz. The fundamental advantage of such a logic-triggered closed loop, which is implemented within the DSP as an interrupt to the main loop, is that the converter majorly operates at the most optimized values of control variables in addition to being robust against output load variations frequently occurring in on-board charging systems. During the load transients window, the possibility of the converter running at nonoptimal control variable set for a given required output voltage and power exists; however, the impact on the continuous converter operational efficiency is minimal due to negligibly narrow transient interval in comparison to steady-state window.

C. Polynomial Regression-Based Control Realization and Implementation

The steady-state optimization framework is implemented on the C3L3 resonant converter is shown in Fig. 13. This control implementation is realized as a combination of offline and online calculations. The optimized control variable sets based on total loss optimization for all corner cases of voltage–power combinations defined in Table IV serve as an input to the function in addition to the converter semiconductor parasitic extracted parameters are fed as an input to a high computation capable offline machine. The converter semiconductor parasitic extraction block is a representative of the methods for parasitic parametric extraction as discussed in [43], [44], [45], and [46], and outputs the values of ($R_{dson}, C_{\rm oss}, C_{iss}, V_{\rm th}, V_{pl}$). The mathematical model developed in this manuscript analytically solves the given equations for the provided inputs of voltage–power combinations to derive all possible control variables as solution sets. For a given voltage–power combination, multiple output solution sets are possible. The mathematical model is followed by an optimization routine subject to constraints to select the most optimum control variable out of multiple sets. Based on the corner conditions of voltage and power range of this converter, a few preselected corner voltage–power combinations are chosen as inputs to the mathematical model to generate the optimum control variable sets for each of the inputs, which were then compiled and tabulated. These voltage–power combinations and their corresponding tabulated optimum control variable sets are loaded in a polynomial regression algorithm to subsequently generate polynomial coefficients and intercepts on a high computation capable machine using least mean square error estimator. Polynomial regression toolbox in MATLAB software could be utilized for handling high number of computations to generate polynomial coefficients and intercepts. Generation of polynomial coefficients and intercept step concludes the offline aspect of this control architecture, which is followed by the online section which involves flashing these polynomial

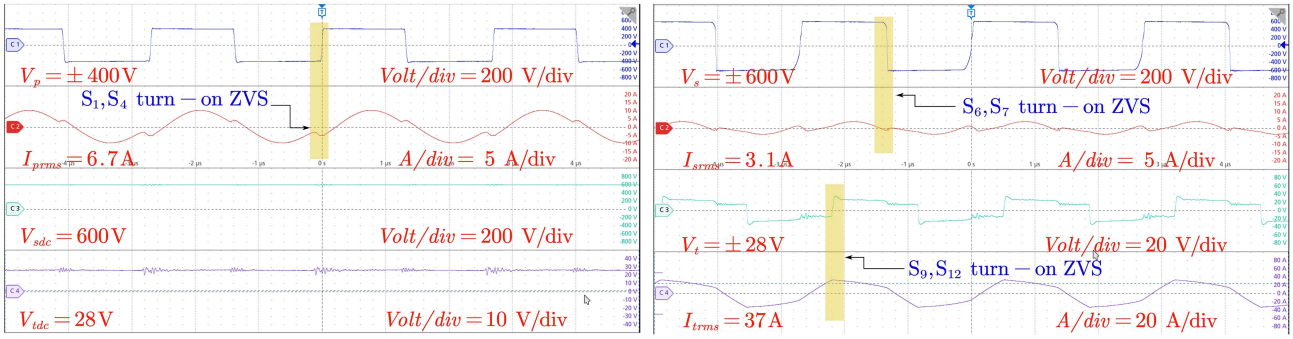

Fig. 16. Experimental Results for ($V_{\mathrm{sdc}} = 600\,\mathrm{V}, V_{x\mathrm{dc}} = 28\,\mathrm{V}, P_{\mathrm{sdc}} = 1000\,\mathrm{W}, P_{x\mathrm{dc}} = 1000\,\mathrm{W}$) at control variable set ($F_{\mathrm{sw}} = 379\,\mathrm{kHz}, \phi_s = -28.9°, \phi_x = -26.3°$).

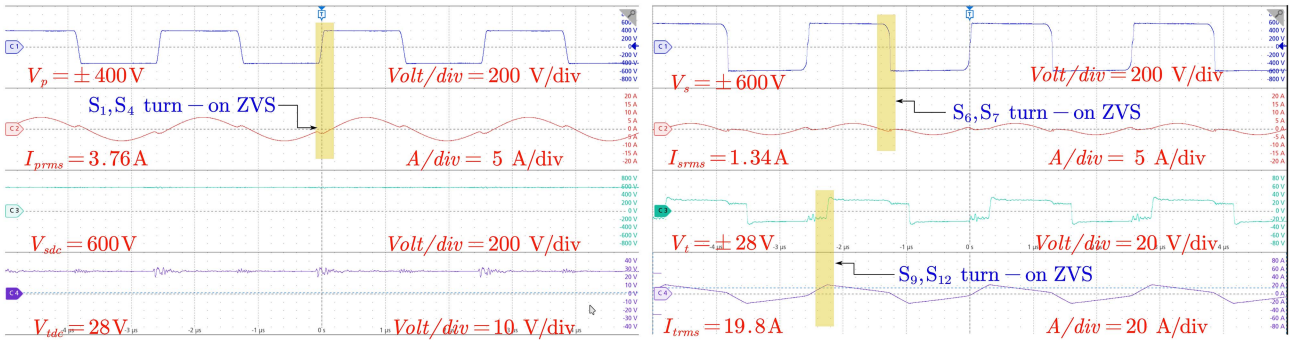

Fig. 17. Experimental Results for ($V_{\mathrm{sdc}} = 600\,\mathrm{V}, V_{x\mathrm{dc}} = 28\,\mathrm{V}, P_{\mathrm{sdc}} = 750\,\mathrm{W}, P_{x\mathrm{dc}} = 500\,\mathrm{W}$) at control variable set ($F_{\mathrm{sw}} = 392\,\mathrm{kHz}, \phi_s = -16.2°, \phi_x = -14.2°$).

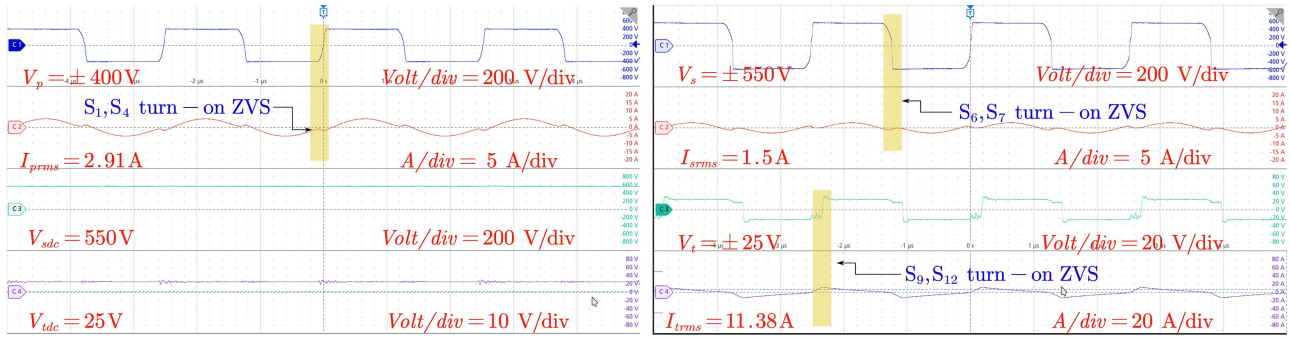

Fig. 18. Experimental Results for ($V_{\mathrm{sdc}} = 550\,\mathrm{V}, V_{x\mathrm{dc}} = 25\,\mathrm{V}, P_{\mathrm{sdc}} = 750\,\mathrm{W}, P_{x\mathrm{dc}} = 250\,\mathrm{W}$) at control variable set ($F_{\mathrm{sw}} = 402\,\mathrm{kHz}, \phi_s = -7.23°, \phi_x = -3.62°$).

coefficients and intercepts for each of three control variables on the ROM memory of the DSP. This computation time directly corelates with the order of the modeled polynomial function. A higher order of polynomial directly relates to a higher model accuracy at the cost of longer program execution time. If the computational time of the duty parameters exceeds the converter switching cycle, the control loop functionality will be updated at a down-sampled rate with respect to the switching rate and the sampling rate of the sensed voltage and current signals that may potentially lead to signal aliasing and loop instability.

For the DSP, calculating control variables through polynomial regression involves a series of implementations of mathematical operations, such as multiplications and additions of the inputs, which are executed using certain instructions. The time utilized for executing these mathematical operations is the cumulative sum of the time required to implement each of these instructions. The total time utilized in execution of these mathematical operations $T_{\mathrm{execute}} \leq T_{\mathrm{sw}}$ (switching period) in order to satisfy the one cycle switching limit. If the execution time exceeds the one switching cycle limit, the control loop functionality will be

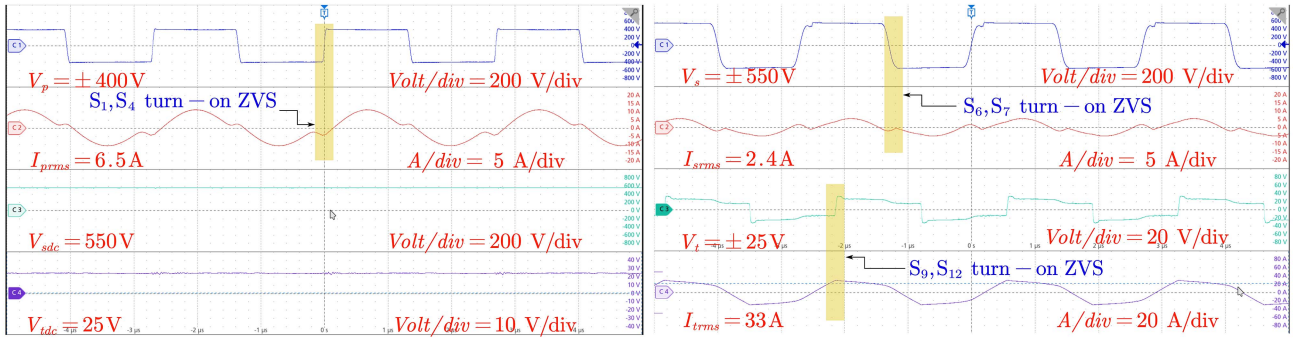

Fig. 19. Experimental Results for ($V_{\text{sdc}} = 550$ V, $V_{x\text{dc}} = 25$ V, $P_{\text{sdc}} = 900$ W, $P_{x\text{dc}} = 750$ W) at control variable set ($F_{\text{sw}} = 380$ kHz, $\phi_s = -21.6°$, $\phi_x = -13.92°$).

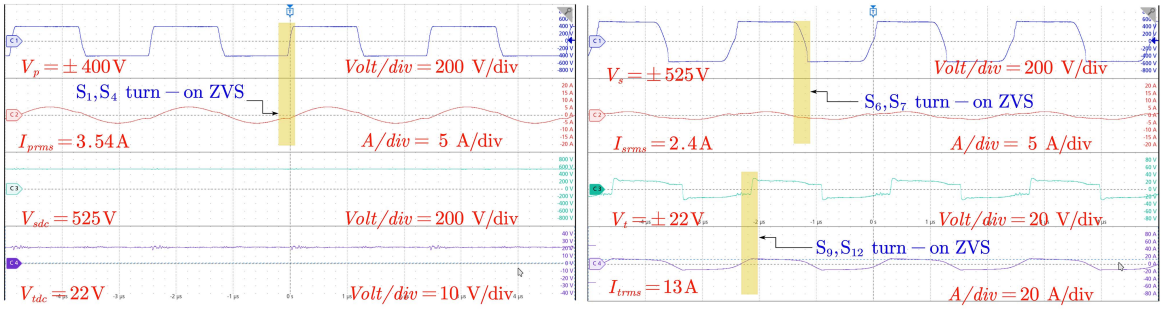

Fig. 20. Experimental Results for ($V_{\text{sdc}} = 525$ V, $V_{x\text{dc}} = 22$ V, $P_{sdc} = 750$ W, $P_{x\text{dc}} = 250$ W) at control variable set ($F_{\text{sw}} = 406$ kHz, $\phi_s = -6.3°$, $\phi_x = -2.9°$).

TABLE VI
COEFFICIENTS FOR POLYNOMIALS OF CONTROL VARIABLES IN POLYNOMIAL REGRESSION BASED OFFLINE CALCULATED CONTROL

F_{sw} coefficients	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}	α_{11}	α_{12}	α_{13}	α_{14}	$int1$
value	0	0	0	0	3.02	-0.0013	0.002	0	0	-0.04266	-0.062	-34.72	0	0	0
ϕ_s coefficients	β_1	β_2	β_3	β_4	β_5	β_6	β_7	β_8	β_9	β_{10}	β_{11}	β_{12}	β_{13}	β_{14}	$int2$
value	0	0	0	0	0.218	-6.67e-7	-2.732e-5	0	0	-0.0002	-0.005	-2.38	0	0	0
ϕ_x coefficients	γ_1	γ_2	γ_3	γ_4	γ_5	γ_6	γ_7	γ_8	γ_9	γ_{10}	γ_{11}	γ_{12}	γ_{13}	γ_{14}	$int3$
value	0	0	0	0	0.2457	-2.96e-7	-4.53e-5	0	0	0.0005	-0.005	-2.6788	0	0	0

updated at a down-sampled rate of the sensed voltage and current that could lead to signal aliasing and loop instability issues. Hence, it becomes a necessity to limit the control execution time within one switching time period. Control card containing IC TMS320F28379D is utilized for control in this application, which follows the reduced instruction set computer (RISC) Instruction Set Architecture (ISA). A second order polynomial implementation ensues 28 multiplications and 14 additions for each of the control variables. Considering three control variables, which brings up the total number of multiplications to 84 and the total number of additions to 42. In converter real-time, the output dc voltage and current sensors on all the dc ports feedback the sensed data to the DSP. The TMS320F28379D IC uses the RISC V ISA, which allows for out of order execution, hence it becomes tedious to estimate the computation time for execution of the polynomial function. However, assuming some deterministic latencies, an approximate computation time for polynomial based on the number of total multiplications and additions for an order of polynomial based on the total number of multiplications and additions can be estimated as given in Table VII. As observed, a polynomial order of degree 2 can be selected for online calculation of control variables for switching frequencies upto 500 kHz. The implemented nature of the polynomial regression equation is shown in (47) and the coefficients and intercepts for some corner conditions are given in Table VI.

TABLE VII
COMPUTATION TIME REQUIRED FOR GENERATION OF CONTROL VARIABLES BASED ON THE ORDER OF THE POLYNOMIAL

Polynomial order	Total multiplication operations	Total addition operations	Computation time by DSP
2	84	42	1.9 μs
3	132	66	3 μs
4	180	90	4.1 μs

$$F_{\text{sw}} = \alpha_1 V_{\text{sdc}} + \alpha_2 V_{x\text{dc}} + \alpha_3 P_{\text{sdc}} + \alpha_4 P_{x\text{dc}}$$

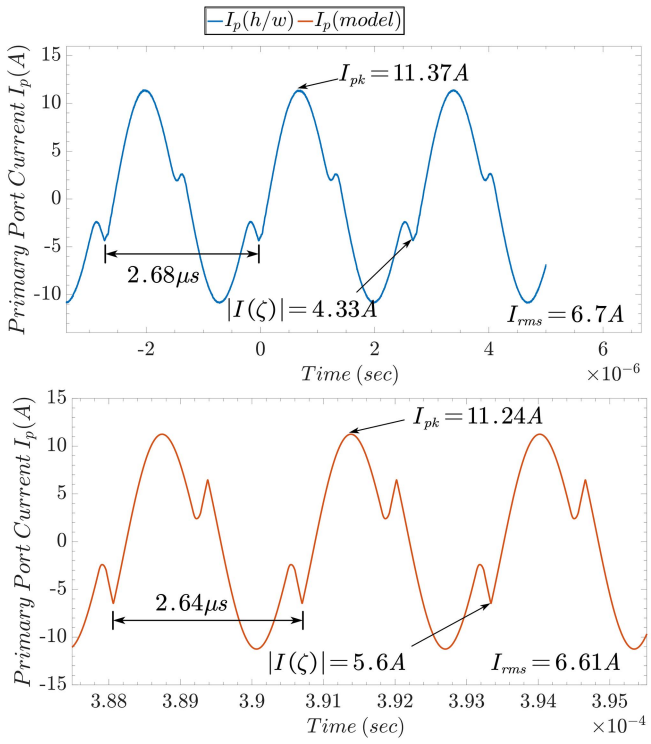

Fig. 21. Hardware I_p versus analytically reconstructed I_p comparison for ($V_{\text{sdc}} = 600\,\text{V}, V_{x\text{dc}} = 28\,\text{V}, P_{\text{sdc}} = 1000\,\text{W}, P_{x\text{dc}} = 1000\,\text{W}$) at control variable set ($F_{\text{sw}} = 379\,\text{kHz}, \phi_s = -27.28°, \phi_x = -25.24°$).

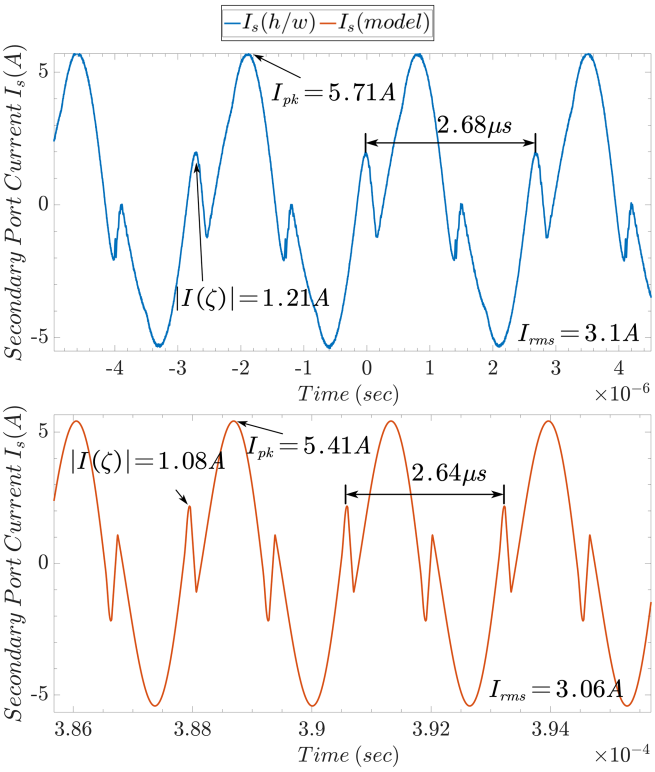

Fig. 22. Hardware I_s versus analytically reconstructed I_s comparison for ($V_{\text{sdc}} = 600\,\text{V}, V_{x\text{dc}} = 28\,\text{V}, P_{\text{sdc}} = 1000\,\text{W}, P_{x\text{dc}} = 1000\,\text{W}$) at control variable set ($F_{\text{sw}} = 379\,\text{kHz}, \phi_s = -27.28°, \phi_x = -25.24°$).

TABLE VIII
DESIGN SPECIFICATIONS FOR THREE-PORT RESONANT C3L3 CONVERTER

Parameters	Values/Part nos.	Units/description/dimensions
V_{pdc}	400	V
V_{sdc} range	500–600	V
V_{xdc} range	22–28	V
$P_{pac}, P_{sac}, P_{xac}$	2k, 1k, 1k	W
$N_p : N_s : N_x$	16:22:1	-
L_p, L_s, L_x	7.85,16,0.068	μH
L_m	73.32	μH
C_p, C_s, C_x	13.39, 6.67, 1650	nF
Primary device	GS66508T	650V, 30A, 50 mΩ
Secondary device	TP90H050WS	900V, 34A, 50 mΩ
Tertiary device	EPC2020	60V, 90A, 1.5 mΩ
Pri gate driver	Si8271	4A, 2.5 kV isolation
Sec gate driver	Si8271	4A, 2.5 kV isolation
Ter gate driver	uP1966E	0.5A, non-isolated
C_{in}	20 μF	2*EZP-V80106LTB
C_{outs}	20 μF	2*EZP-V80106LTB
C_{outx}	66 μF	20*C5750X7R1H335K230KM
Magnetic core	FR45810EC	E58.42*10.54*38.1 mm^3

$$
\begin{aligned}
&+ \alpha_5 V_{\text{sdc}} V_{x\text{dc}} + \alpha_6 P_{x\text{dc}} P_{\text{sdc}} \\
&+ \alpha_7 V_{\text{sdc}} P_{x\text{dc}} + \alpha_8 V_{\text{sdc}} P_{\text{sdc}} \\
&+ \alpha_9 V_{x\text{dc}} P_{\text{sdc}} + \alpha_{10} V_{x\text{dc}} P_{x\text{dc}} + \alpha_{11} V_{\text{sdc}}^2 + \alpha_{12} V_{x\text{dc}}^2 \\
&+ \alpha_{13} P_{\text{sdc}}^2 + \alpha_{14} P_{x\text{dc}}^2 + \text{int}_1
\end{aligned} \tag{47}
$$

where $\alpha_1 - \alpha_{14}$ and int_1 are coefficients for the polynomials and its intercept, respectively. In addition, similar equation can be formulated for other control variables ϕ_s and ϕ_x based on coefficients $\beta_1 - \beta_{14}$ and $\gamma_1 - \gamma_{14}$, respectively.

VI. HARDWARE PROTOTYPING AND EXPERIMENTAL RESULTS

A. Hardware Prototyping

The validation of the analysis and findings presented in the previous sections is performed using a hardware prototype with longitudinal multislot structure for integrating the three full-bridges, as shown in Fig. 14(a) for the design specifications mentioned in Table VIII. The primary side corresponds to a dc link voltage of 400 V nominal, with secondary and tertiary ports corresponding to the HV and LV batteries at 600 and 28 V nominal, respectively. HV battery voltage ranges from 500–600 V whereas LV battery range is within 22–28 V. The gate control signals encoding the phase and frequency parameters are fed to the power stage using TMS320F28379D dual-core digital signal processor. The three-winding leakage-integrated transformer is shown in Fig. 14(b). The primary–tertiary winding gap ($\Delta h1$), primary–secondary winding gap ($\Delta h2$) and core airgap (A_g) are designed to be 3.9, 6.5, and 0.4 mm to synthesize the leakage inductances $L_p = 7.35\,\mu H$, $L_s = 16\,\mu H$, and $L_x = 0.068\,\mu H$ of the multiwinding transformer, respectively.

An iterative approach is executed for converter design based on the design specifications of desired port powers, port voltages, and resonant frequency. First, the transformer turns ratio is selected based on the nominal voltage and gain requirements of the individual ports, which comes to 16:22:1 for (N_p, N_s, and N_x),

respectively. Based on the selected turns' ratio, the optimum ranges of leakage and magnetizing inductance are obtained to satisfy the following soft-switching requirements: 1) ZVS at the primary side (by ensuring an inductive nature of the tank) and 2) minimized turn-OFF instantaneous currents at the secondary and tertiary side. Further, based on the range of the HFPT inductance and corresponding resonant capacitance's, the gain-frequency characteristic is analyzed to check if the gain gradient $\frac{\Delta \text{gain}}{\Delta \text{frequency}}$ adheres to the required voltage regulation corresponding to the least count of realizable phase of PWM signals using the DSP. To ensure appropriate gain gradient, the quality factor (Q) of each port is adjusted by varying the ratios of $\frac{L_x}{L_m}$. The iterative design process follows a back-and-forth scheming until all the design criteria are fulfilled, thus resulting in the optimum selection of the resonant tank parameters $(L_m, L_p, L_s, L_x, C_p, C_s, C_x)$.

The resonant capacitors(C_p, C_s, C_x) are selected with C0G dielectric as they exhibit extremely low ESR values and lower capacitance variation due to temperature and applied voltage. The associated power loss can be calculated as $P_{\text{esr},y} = I^2_{\text{rms},y} * R_{\text{dson},y}$, where $I_{\text{rms},y}$ and $R_{dson,y}$ are the rms value of port current and on state resistance of the yth bridge, respectively. Based on the values of the selected resonant capacitors, the ESR loss is calculated, and it is found that the ESR power loss amounts to only $\approx 10\%$ of the sum of device conduction and winding copper losses in the entire converter and is responsible for only 0.1% efficiency drop at 400–600–28 V operation at 2 kW.

B. Steady-State Experimental Results

Figs. 16–20 show experimental results of the hardware prototype, demonstrating steady-state behavior of $(I_p, I_s, I_x, V_p, V_s, V_t, V_{\text{sdc}}, V_{x\text{dc}})$ waveforms at the following corner conditions:

1) $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}}) = (600\text{V}, 28\,\text{V}, 1000\,\text{W}, 1000\,\text{W})$ at $(F_{\text{sw}}, \phi_s, \phi_x,) = (379\,\text{kHz}, -28.9°, -26.3°)$;
2) $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}}) = (600\,\text{V}, 28\text{V}, 750\text{W}, 500\text{W})$ at $(F_{\text{sw}}, \phi_s, \phi_x,) = (392\,\text{kHz}, -16.2°, -14.2°)$;
3) $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}}) = (550\,\text{V}, 25\text{V}, 750\,\text{W}, 250\,\text{W})$ at $(F_{\text{sw}}, \phi_s, \phi_x,) = (402\,\text{kHz}, -7.23°, -3.62°)$;
4) $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}}) = (550\,\text{V}, 25\,\text{V}, 900\,\text{W}, 750\,\text{W})$ at $(F_{\text{sw}}, \phi_s, \phi_x,) = (380\,\text{kHz}, -21.6°, -13.92°)$
5) $(V_{\text{sdc}}, V_{x\text{dc}}, P_{\text{sdc}}, P_{x\text{dc}}) = (525\,\text{V}, 22\,\text{V}, 750\,\text{W}, 250\,\text{W})$ at $(F_{\text{sw}}, \phi_s, \phi_x,) = (406\,\text{kHz}, -6.3°, -2.9°)$.

In Fig. 16, output power of 1 kW each on secondary and tertiary ports is achieved at 600 and 28 V respectively, all the while maintaining ZVS conditions on all three ports. It can be verified by observing the direction and magnitude of port current with respect to its port voltage. The directions of current probes on all three ac ports are aligned following the convention defined in Fig. 1. As per the convention, a negative current magnitude less than $I_{\text{zvs},p}$ ensures turn-ON ZVS on all the semiconductor devices on the inverting primary bridge while a positive current magnitude greater than $I_{\text{zvs},s}$ and $I_{\text{zvs},t}$ achieves turn-ON ZVS for all devices on rectifying secondary and tertiary bridges, respectively. It can be argued that for one of the output bridges is capable of achieving SR turn-ON/OFF at the cost of output capacitor losses instead of turn-ON ZVS. During SR operation, the semiconductor device encounters almost zero turn-ON and turn-OFF loss, however, the output capacitance loss is still experienced. During ZVS turn-ON, the semiconductor device achieves almost zero turn-ON and output capacitance loss but encounters turn-OFF loss based on the switching instant value of the current. Hence, a selection criterion for operation of rectifying bridge semiconductor devices based on SR or turn-ON ZVS operation is required. This selection criteria can be formulated by comparison of total output capacitance loss versus total turn-OFF loss for all rectifying bridge semiconductor devices, as detailed in the loss formulation section. It is observed from Fig. 15 that turn-OFF losses encountered by semiconductor devices are lower than output capacitance loss for all control variables at $(600\,\text{V}, 28\,\text{V}, 1000\,\text{W}, 1000\,\text{W})$ condition and this trend is continued for other voltage–power levels too. The output capacitance and turn-OFF loss are directly proportional to switching frequency, hence it is expected for both the losses to increase with rise of switching frequency. This trend, however, is bucked for turn-OFF loss as it shows a steady decline, which is due to the fact that the switching instant current value decreases with higher switching frequency for this voltage–power level, which can be observed in the F_{switch} trend in Table IV. Based on the observations in Fig. 15, for a total loss optimized solution, running the converter with turn-ON ZVS instead of SR on the rectifying bridge semiconductor devices turns out to be a preferred solution.

Similar to Fig. 16, in other voltage–power conditions in Figs. 17–20, an effort is made to obtain ZVS turn-ON for all semiconductor devices in all three full-bridges by adjusting the control variables and dead-time.

TABLE IX
CALCULATION OF RMS/AVG FOR VARIOUS VOLTAGE – POWER COMBINATIONS

$(V_{sdc}, V_{xdc}, P_{sdc}, P_{xdc})$	I_{rms} $(I_p/I_s/I_x)$	I_{avgrms} $(I_p/I_s/I_x)$	RMS/AVG $(I_p/I_s/I_x)$
(600V, 28V, 1kW , 1kW)	6.7/3.1/37	4.5/1.5/32.15	1.48/2.1/1.15
(600V, 28V, 0.75kW , 0.5kW)	3.76/1.34/19.8	2.8/1.12/16	1.34/1.19/1.23
(550V, 25V, 0.75kW , 0.25kW)	2.91/1.5/11.38	2.25/1.23/9	1.3/1.21/1.26
(550V, 25V, 0.9kW , 0.75kW)	6.5/2.4/33	3.7/1.47/27	1.75/1.63/1.22
(525V, 22V, 0.75kW , 0.25kW)	3.54/2.4/13	2.25/1.28/10.23	1.57/1.875/1.27

C. Hardware Result Analysis

Figs. 21 and 22 show the comparison of I_p and I_s hardware current waveform with analytically generated currents for similar control variables, respectively. Table X shows the comparison of hardware currents with the I-GHA and GHA generated analytical currents and their error % with respect to the hardware values. The control variables used in the hardware and I-GHA differ due to nonaccounting of certain nonidealities, such as converter deadtime and multiwinding transformer parasitics, however the variation is within 2% for F_{sw} and within 5% for ϕ_s and ϕ_x. Accounting for those nonidealities would complicate the analytical model and could increase the execution time beyond

TABLE X
COMPARISON OF HARDWARE AND I-GHA RECONSTRUCTED PORT CURRENTS FOR CORNER CONDITIONS

600V, 28V, 1kW, 1kW	Hardware	I-GHA	GHA
I_{prms} (A)	6.7 (0)	6.56 (2.08)	6.9 (3)
I_{srms} (A)	3.1 (0)	2.89 (6.45)	2.79 (10)
I_{xrms} (A)	37 (0)	40 (7.5)	42 (13.5)
$I_p(\zeta)$ (A)	5.2 (0)	5.8 (11.53)	6.3 (21.1)
$I_s(\zeta)$ (A)	2.1 (0)	2.4 (12.5)	2.9 (38)
$I_x(\zeta)$ (A)	42 (0)	46 (12.5)	49 (16)
Conduction loss (W)	8.46 (0)	8.65 (2.2)	9.42 (11.8)
Switching loss (W)	24.344 (0)	25.72 (5.6)	27.32 (12.3)
600V, 28V, 0.75kW, 0.5kW	Hardware	I-GHA	GHA
I_{prms} (A)	3.76 (0)	3.66 (2.7)	3.93 (4.5)
I_{srms} (A)	1.34 (0)	1.31 (2.2)	1.49 (11.1)
I_{xrms} (A)	19.8 (0)	19.2 (3)	22 (11.1)
$I_p(\zeta)$ (A)	1.1 (0)	1.45 (31)	1.9 (72)
$I_s(\zeta)$ (A)	0.4 (0)	0.43 (7.5)	0.62 (55)
$I_x(\zeta)$ (A)	22 (0)	26 (18)	28 (27)
Conduction loss (W)	2.45 (0)	2.31 (5.7)	2.83 (15.5)
Switching loss (W)	16.65 (0)	17.5 (6.9)	18.61 (12)
550V, 25V, 0.75kW, 0.25kW	Hardware	I-GHA	GHA
I_{prms} (A)	2.91 (0)	2.89 (1)	3.1 (6.8)
I_{srms} (A)	1.5 (0)	1.52 (1.3)	1.9 (26)
I_{xrms} (A)	11.38 (0)	11.28 (0.8)	11.7 (2.8)
$I_p(\zeta)$ (A)	1.1 (0)	1.6 (45)	1.9 (72)
$I_s(\zeta)$ (A)	0.4 (0)	0.49 (22.5)	0.82 (105)
$I_x(\zeta)$ (A)	16 (0)	18 (12.5)	24.8 (55)
Conduction loss (W)	1.35 (0)	1.37 (1.4)	1.62 (20)
Switching loss (W)	16.3 (0)	17.15 (5.2)	18.4 (12.8)
550V, 25V, 0.9kW, 0.75kW	Hardware	I-GHA	GHA
I_{prms} (A)	6.5 (0)	6.42 (4.6)	6.9 (6.1)
I_{srms} (A)	2.4 (0)	2.37 (1.25)	2.8 (16.67)
I_{xrms} (A)	33 (0)	34 (3)	36 (9)
$I_p(\zeta)$ (A)	4.6 (0)	4.3 (6.5)	5.2 (14.2)
$I_s(\zeta)$ (A)	3.3 (0)	3.8 (15)	4.2 (27)
$I_x(\zeta)$ (A)	24 (0)	27 (12.5)	31 (29.1)
Conduction loss (W)	7.2 (0)	7.23 (0.9)	8.1 (12.5)
Switching loss (W)	23.9 (0)	24.5 (2.5)	26.37 (10.3)
525V, 22V, 0.75kW, 0.25kW	Hardware	I-GHA	GHA
I_{prms} (A)	3.54 (0)	3.45 (2.5)	3.6 (1.6)
I_{srms} (A)	2.4 (0)	2.335 (2)	2.6 (8.3)
I_{xrms} (A)	13 (0)	13.5 (3.8)	14.4 (10.7)
$I_p(\zeta)$ (A)	2 (0)	2.4 (20)	2.91 (45)
$I_s(\zeta)$ (A)	0.6 (0)	0.69 (15)	1.1 (83)
$I_x(\zeta)$ (A)	19 (0)	26 (36.8)	31 (63)
Conduction loss (W)	2.2 (0)	2.12 (3.6)	2.44 (10.9)
Switching loss (W)	17.55 (0)	18.72 (6.7)	20.31 (15.7)

one switching cycle of the DSP. Certain differences are also observed in the predicted control variables from I-GHA and GHA, which could be attributed to the nonapproximated effects of the load impedance in I-GHA, which is the main motivation of this work. FHA is not considered in this comparative analysis as the FHA reconstructed current waveforms massively differ from the hardware experimentally obtained current waveforms, which was also seen in Figs. 8–10. Initial observations show that the error $\%$ in the GHA currents is higher compared with I-GHA currents. The switching instant currents show higher error $\%$ compared with the rms values for the same current, as a result, the switching loss calculation reflects a higher error $\%$ compared with conduction loss values. For the rms values of the three-ports currents for five corner conditions considered, I_p, I_s, and I_x, show a mean variation of 2.5%, 2.65%, and 3.62% compared with the experimental value. Tertiary side peak and rms values show the highest variation due to comparable values of the port impedance and output ac impedance. Hence, the impact of the tertiary parasitic is comparatively higher on the port current estimation especially on the switching instant values. As observed from Table X, the calculated semiconductor loss values exhibit $\approx 4\%$ mean error using I-GHA while the mean error is 13.78% for GHA, which could be directly accounted for by the higher switching instant error $\%$ demonstrated by GHA method. Hence, I-GHA performs better in estimating the hardware converter performance at multiple corner conditions of operation.

Furthermore, in order to understand the trend in rms currents at corner conditions, RMS/AVG is a defined as a metric, which is a ratio of rms to average rms value of the port current. As noted from Table IX, the RMS/AVG value for the primary side current remains within the range of 1.3–1.7, while it shows the highest deviation from base value for the secondary side current and is comparatively lowest for the tertiary side. Since rms/AVG remains above 1 for almost all the cases, it can be inferred that the system is processing reactive power, which leads to converter losses and adds to the cooling burden of the entire system. During the I-GHA model derivation, (29) and (30) equated the dc power sunk in the battery during charging to the ac active power at the ports; however, at that time reactive power was not considered during the entire analytical modeling exercise. For higher gain converters, which necessitate switching frequency operation farther away from the resonant frequency, the converter operates in a higher impedance region contributing to higher reactive power. As a result, high reactive power cannot be escaped for high gain converters; however, using rms current optimization defined in Section IV could lead to reduction in the rms/AVG for all three ports and thus could minimize the circulating reactive power for a given active power transfer. It is also noteworthy that the control variables responsible for the lowest rms values might not always provide the lowest total loss due to the dominance of switching frequency dependent losses.

VII. CONCLUSION

To enhance the accuracy of analytical reconstructed current waveforms of multiport resonant converter, this article elucidates a redefined modeling approach labeled I-GHA, which deviates from the existing state of art techniques, such as GHA and FHA. In addition, semiconductor loss model for three-port resonant converter is derived followed by categorical and total loss optimization analysis by incorporating a blended modulation of switching frequency and interbridge phase shifts. The three-port resonant converter is operated in an steady-state optimization framework with the switching patterns information encoding switching frequency and interbridge phase shifts, implemented on the controller using polynomial regression approach. For concept verification, an all-GaN-based 2 kW C3L3 converter with 490 kHz resonant frequency is developed to operate in a wide-gain operation converting 400 V to (500–600) V and (22–28)V. Various experimental results at five output voltage–power corner conditions are presented to emulate different conditions of battery voltages and charging power at secondary and tertiary ports, respectively. The resulting port currents show a $\leq 3\%$ mean variation with respect to hardware obtained port current for peak and rms values and $\leq 10\%$ mean variation for switching instant values. Although the mean variation in the switching

instant values is higher for certain cases, the overall impact on the total semiconductor loss estimation is $\leq 5\%$, which befalls in an acceptable limit for a multiport resonant converter modeling analysis. This variation is much lower compared to existing state-of-the-art modeling techniques, such as GHA and FHA, which exhibit $\geq 10\%$ total semiconductor loss estimation error.

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Shubham Mungekar (Student Member, IEEE) received the bachelor of science degree in electronics engineering from Mumbai University, Mubai, India, in 2016, and the master of science degree in electrical engineering from The University of Texas at Dallas (UTD), Richardson, TX, USA, in 2020. He is currently working toward the Ph.D. degree in systems engineering with Arizona State University, Tempe, AZ, USA.

He is a Graduate Student Researcher with Arizona State University. He was awarded Master Research Fellowship with Utd in July 2020. He has a cumulative work experience as a Design and Test Engineer for 4 years. His research interests include modeling, control and optimization of high efficiency, high power density dc–dc converters for applications in electric transportation, data centers, space, etc.

Ayan Mallik (Senior Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland (UMD), College Park, MD, USA, 2018 and 2019, respectively.

He is an Assistant Professor with Arizona State University, Tempe, AZ, USA. He is an author/coauthor/co-inventor of more than 90 peer-reviewed publications and four pending/issued U.S. Patents. His research interests include the modeling, control, and multiobjective optimization of complex multiorder power converters, highly efficient and high-density wide bandgap power conversion solutions in the applications of transportation electrification, extreme environment Space, grid-integration of renewables and storage, and among many others.

Dr. Mallik was the recipient of various awards and recognitions, including National Science Foundation CAREER award (2023), IEEE TPEL second place Prize Paper Award (2023), FSE top 5% Faculty Award at ASU (2023), first place in Dean's Doctoral Dissertation award competition at UMD (2019), UMD Invention of the Year award (2018), and third place in Allegheny Region Cleantech University Prize Collegiate Competition (2017) sponsored by the U.S. Department of Energy, and many others.