Achieving Fast Dynamic Response and Output Filter Condition Monitoring in Hybrid PWM Inverters Using a Low-Computational State Trajectory Prediction Algorithm Incorporating With Reduced-Order Switching Surfaces

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***Abstract*—This article presents a novel state trajectory prediction algorithm with reduced-order switching surfaces, designed for H-bridge inverters using hybrid pulsewidth modulation (*h*-PWM). *h*-PWM hybridizes the merits of a unipolar two-level switching scheme (U2SS) and a bipolar three-level switching scheme (B3SS), operating mainly in U2SS while temporarily transitioning to B3SS near the zero-crossing region to resolve the impact of pulse droppings. The algorithm predicts the state trajectory for the entire switching cycle, facilitating fast control and fast dynamic response. By sampling the state variable once at the beginning of each switching cycle, the duty ratios of all switching devices are established for the entire cycle. Since the effective operating frequency under *h*-PWM is twice the switching frequency, the values of the output filter components are minimized, and thus the power density can be increased. Furthermore, the algorithm can indirectly assess the condition of the output filter by adjusting the switching surface based on the comparison of actual and predicted state trajectories, thereby 1) ensuring that the prediction can adapt component variations, 2) identifying aging conditions, and 3) enabling preventive maintenance to avoid unexpected failures. The performance of the algorithm and the output filter parameter estimation technique are evaluated on a 1-kVA prototype.**

***Index Terms*—DC–AC power conversion, hybrid pulsewidth modulation (*h*-PWM), inverters, parameter extraction, trajectory prediction control.**

I. INTRODUCTION

PULSEWIDTH modulation (PWM) is widely used to control the output voltage and frequency of ac waveform in many inverter applications. The basic concept behind PWM involves switching a dc voltage ON and OFF at high frequency to generate a series of pulses. The width of the pulses is typically derived by comparing a modulating signal, usually a sine wave with a frequency equal to the reference output frequency, with a high-frequency carrier signal.

The popular full bridge inverter utilizes either a unipolar switching scheme (USS) or a bipolar switching scheme (BSS). To improve the output spectrum, different PWM schemes have been proposed, such as sinusoidal PWM (SPWM) [1], [2], [3], improved SPWM [4], and PWM with selective harmonic elimination [5], [6]. However, many practical challenges affect the output quality, such as dead time and maximum/minimum pulsewidth. Switching devices require a certain amount of time to turn on or off fully, while narrow gate pulses can result in pulse dropping at the output. Even modulation schemes that can produce a theoretically high-quality output spectrum may introduce undesired harmonics. These considerations are significant for inverters operated at high frequencies.

The ideal output waveform with USS has low switching losses and total harmonic distortion (THD). However, narrow pulses near the zero-voltage region tend to disappear in the actual output waveform due to the inability of the switching device to respond, resulting in increased THD and decreased output quality. Li et al. [7] presented a mathematical model to analyze the relationship among the THD, modulation index, and pulse-dropping duration [8]. In contrast, BSS provides a duty ratio of around 0.5 for pulses near the zero-voltage region, resulting in lower output waveform distortion in this region, but it causes a higher switching loss compared to USS [9].

Apart from steady-state characteristics, PWM inverters also require a fast dynamic response, enabling them to respond quickly to load changes and maintain a stable output. Various fast dynamic control techniques have been proposed to achieve fast transient response recovery on disturbances and periodic distortion. They include deadbeat control [10], [11], [12], state feedback control [13], [14], hysteresis control [15],

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[16], [17], sliding-mode control [18], [19], boundary control [20], and model predictive control [21]. Basic hysteresis control, sliding-mode control, and deadbeat control rely on several control equations, which can lead to some technical challenges. For example, fixed band hysteresis control results in a variable switching frequency with ultra-low and high-frequency components injected into the filters, thus increasing their sizes. A low switching frequency also leads to high ripple current and switching loss [22], [23]. This restriction in turn limits the design of filter components in the converters. To overcome this limitation, additional equations are required to ensure that the output filter is designed under requirements [19], [24].

To address this issue, multiple sliding surfaces are implemented in a high-order equation that can smoothly guide the designed variable. This provides better performance on different load conditions but also requires more boundaries as additional requirements need to be fulfilled [25]. Practically, implementing traditional control laws requires more instruction cache memory per sample, resulting in higher computational power and increased latency.

Due to advancements in semiconductor technology, the operating frequency of the switching devices is continually increasing and is anticipated to reach several MHz in the near future. Besides cost-effectiveness, the controller's hardware and software requirements are becoming increasingly stringent. To satisfy these requirements, several factors must be considered. If the sampling frequency needs to exceed the switching frequency to determine optimal switching instants, very high-speed sampling circuits and signal conditioning circuits (SCCs) are required. The processing speed of the controller will also be required to be exceptionally high. If the sampling frequency is lower than the switching frequency, the system's overall response will be lowered as it will take more than one switching period to determine the state of the switches after sampling. Thus, the optimal approach is to have the sampling frequency synchronized with the switching frequency and the state of the switches is determined immediately after sampling.

State-trajectory control techniques are known for their fast dynamic response as they determine the appropriate duty ratios for each switch. However, traditional state-trajectory control techniques require significant computational resources, fast analog-to-digital conversion, and signal detection. This article aims to develop a state-trajectory control technique for a hybrid PWM (*h*-PWM) scheme that demands fewer computational resources, demonstrated by utilizing MHz switching. The proposed technique performs the sampling at the start of each switching cycle and takes 60 ns to execute the overall sample-to-update process, equivalent to 6% of the switching period under 1 MHz switching. The *h*-PWM hybridizes the merits of U2SS and B3SS [26] for fast control, dynamic response, and low output THD. It doubles the effective operating frequency, minimizes output filter component values, and increases power density. The algorithm also monitors the condition of the output filter by comparing actual and predicted state trajectories, thereby

1) ensuring that the prediction can adapt component variations;
2) identifying aging conditions;
3) enabling preventive maintenance to avoid unexpected failures.

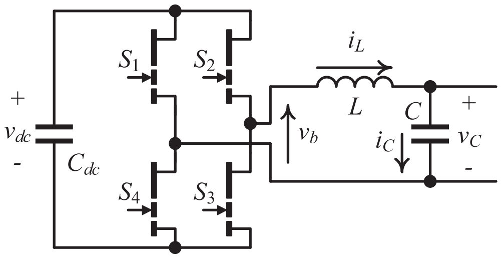


Fig. 1. System architecture of the converter.

TABLE I
HYSTERESIS VALUES FOR PATTERN TRANSITIONS

Hysteresis	From	To	Criterion
Between *P* and *Z*	*Z*	*P*	$\frac{v_{ref}}{v_{dc}} > D_{Z\to P}$
	P	*Z*	$\frac{v_{ref}}{v_{dc}} < D_{P\to Z}$
Between *N* and *Z*	*Z*	*N*	$\frac{v_{ref}}{v_{dc}} < D_{Z\to N}$
	N	*Z*	$\frac{v_{ref}}{v_{dc}} > D_{N\to Z}$

Note: $D_{Z\to P} > D_{P\to Z}$ and $D_{Z\to N} < D_{N\to Z}$

Section II presents the proposed *h*-PWM technique with state-trajectory prediction. Section III presents a comparison with various state trajectory prediction techniques. Section IV describes a technique for extracting the filter component values. The experimental results of a 1-kVA inverter prototype are presented in Section V. Finally, Section VI concludes this article.

II. *H*-PWM WITH STATE-TRAJECTORY PREDICTION

The dc–ac power converter shown in Fig. 1 comprises a full bridge constructed by four switching devices S_1–S_4 and a second-order *LC* output filter. This article proposes an *h*-PWM technique with state-trajectory prediction to dictate the states of all switching devices. Fig. 2 illustrates three patterns, namely *P*, *N*, and *Z*, for the output of the full bridge. The utilization of pattern *P* is used during the positive half cycle of the output, while pattern *N* is used during the negative half cycle. Furthermore, pattern *Z* is used around the zero-crossing region of the output. Variations in the output pattern are dependent on the output reference v_{ref} with hysteresis to regulate the transition from one pattern to another. Table I provides a tabulation of the hysteresis values.

The experimental prototype given in Section V has the following hysteresis values: $D_{Z\to P} = \frac{1}{8}, D_{P\to Z} = \frac{1}{16}, D_{Z\to N} = -\frac{1}{8}$, and $D_{N\to Z} = -\frac{1}{16}$. As depicted in Fig. 2, each output pattern is formed by switching four basic operating modes, namely M1–M4, in a specific sequence. Table II provides the states of the switching devices in all modes.

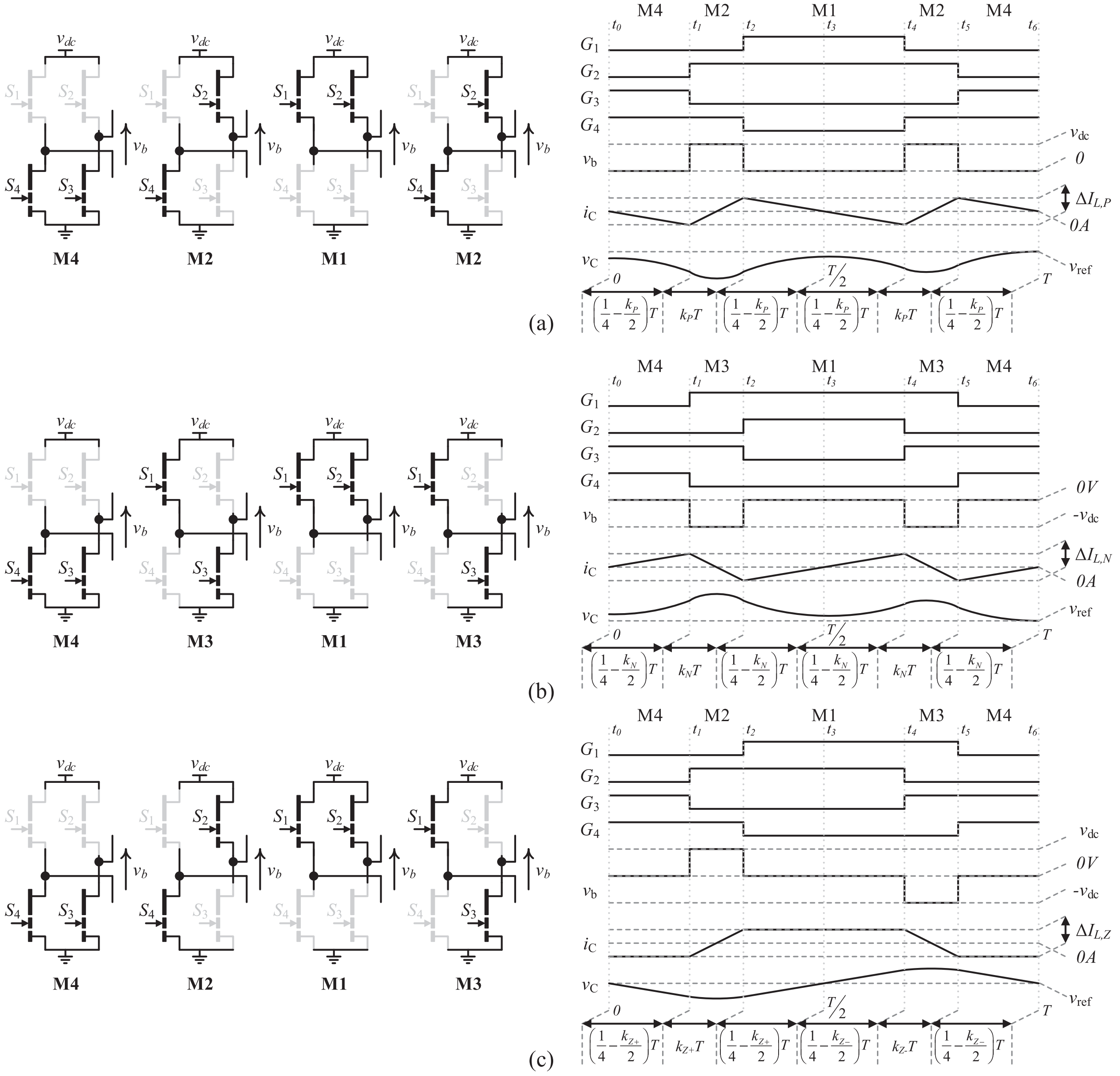


Fig. 2. Switching patterns. (a) *P*. (b) *N*. (c) *Z*.

TABLE II
STATES OF THE SWITCHING DEVICES FOR DIFFERENT MODES

Mode	S_1	S_2	S_3	S_4
M1	ON	ON	OFF	OFF
M2	OFF	ON	OFF	ON
M3	ON	OFF	ON	OFF
M4	OFF	OFF	ON	ON

The waveforms of the gate signals to the four switching devices, $G_1 - G_4$, output voltage of the bridge v_b, output capacitor current i_C, and output capacitor voltage v_C of the three patterns are provided. Six primary time intervals, including $t_0 - t_1\ (t_{01})$, $t_1 - t_2\ (t_{12})$, $t_2 - t_3\ (t_{23})$, $t_3 - t_4\ (t_{34})$, $t_4 - t_5\ (t_{45})$, and $t_5 - t_6\ (t_{56})$, where (•) is the duration of the corresponding interval, can be identified within each switching cycle, resulting from changes in the state of certain switches at t_1, t_2, t_4, and t_5.

A. Estimation of Capacitor Current and Voltage for a Specific Time Interval

The capacitor current and voltage for a specific time interval are estimated. Within the considered time interval, v_b is assumed to be constant. The capacitor current at t_y can be expressed as

$$i_C(t_y) = \left[\frac{v_b(t_x) - v_C(t_x)}{L}\right](t_y - t_x) + i_C(t_x) \qquad (1)$$

TABLE III

PROPERTIES OF PATTERNS *P*, *N*, AND *Z*

Pattern	Duration	t_{01}	t_{12}	t_{23}	t_{34}	t_{45}	t_{56}
P	Mode	M4	M2	M1	M1	M2	M4
	v_b	0	v_{dc}	0	0	v_{dc}	0
N	Mode	M4	M3	M1	M1	M3	M4
	v_b	0	$-v_{dc}$	0	0	$-v_{dc}$	0
Z	Mode	M4	M2	M1	M1	M3	M4
	v_b	0	v_{dc}	0	0	$-v_{dc}$	0

TABLE IV

SUMMARY OF PARAMETERS IN PREDICTING i_C AND v_C USING (1) AND (2) FOR PATTERN *P*

t_x	t_y	$t_{xy} = t_y - t_x$	v_b	Initial values		Predicted values	
				$i_C(t_x)$	$v_C(t_x)$	$i_C(t_y)$	$v_C(t_y)$
t_0	t_1	$t_{01} = (0.25 - 0.5\,k_P)\,T$	0	$i_C(t_0)$	$v_C(t_0)$	$i_C(t_1)$	$v_C(t_1)$
t_1	t_2	$t_{12} = k_P\,T$	v_{dc}	$i_C(t_1)$	$v_C(t_1)$	$i_C(t_2)$	$v_C(t_2)$
t_2	t_3	$t_{23} = (0.25 - 0.5\,k_P)\,T$	0	$i_C(t_2)$	$v_C(t_2)$	$i_C(t_3)$	$v_C(t_3)$
t_3	t_4	$t_{34} = (0.25 - 0.5\,k_P)\,T$	0	$i_C(t_3)$	$v_C(t_3)$	$i_C(t_4)$	$v_C(t_4)$
t_4	t_5	$t_{45} = k_P\,T$	v_{dc}	$i_C(t_4)$	$v_C(t_4)$	$i_C(t_5)$	$v_C(t_5)$
t_5	t_6	$t_{56} = (0.25 - 0.5\,k_P)\,T$	0	$i_C(t_5)$	$v_C(t_5)$	$i_C(t_6)$	$v_C(t_6)$

and the capacitor voltage at t_y can be expressed as

$$v_C(t_y) = \left[\frac{v_b(t_x) - v_C(t_x)}{2\,C\,L}\right](t_y - t_x)^2 + \frac{i_C(t_x)}{C}(t_y - t_x) + v_C(t_x). \tag{2}$$

Equations (1) and (2) depict the capacitor's current and voltage trajectory on the $i_C - v_C$ plane. Detailed proofs of (1) and (2) are given in the appendix.

The operations of patterns *P*, *N*, and *Z* are described below.

1) Pattern P*:* v_b changes five times in one switching cycle, as specified in Table III: 0, $v_{\rm dc}$, 0, $v_{\rm dc}$, and 0. The duration of each level is also provided. The two voltage pulses are symmetrical quarterly at 0.25*T* and 0.75*T*, respectively. Their durations are the same and are determined by predicting v_C to reach $v_{\rm ref}$ after one switching period at *T*. The duty ratio k_P is defined as

$$k_P = \frac{t_{12}}{T} = \frac{t_{45}}{T}. \tag{3}$$

Thus

$$t_{01} = t_{23} = t_{34} = t_{56} = (0.25 - 0.5\,k_P)\,T. \tag{4}$$

Table IV summarizes the parameters used in predicting the values of i_C and v_C after a certain time interval, as described by (1) and (2). By putting the predicted values from a previous time interval as the initial values for the next time interval, the capacitor current and voltage at t_6 can be shown to be

$$i_C(t_6) \approx i_C(t_0)(1) + v_C(t_0)\left(-\frac{T}{L}\right) + v_{\rm dc}(t_0)\left(\frac{2kT}{L}\right) \tag{5}$$

and

$$v_C(t_6) \approx i_C(t_0)\left(\frac{T}{C}\right) + v_C(t_0)\left(1 - \frac{T^2}{2CL}\right) + v_{\rm dc}(t_0)\left(\frac{kT^2}{CL}\right). \tag{6}$$

Let $v_C(t_6) = v_{\rm ref}(t_0)$. The value of k_P is

$$k_P = \left[\left(\frac{CL}{T^2}\right)v_{\rm ref}(t_0) - \left(\frac{L}{T}\right)i_C(t_0) + \left(\frac{1}{2} - \frac{CL}{T^2}\right)v_C(t_0)\right]\frac{1}{v_{\rm dc}(t_0)}. \tag{7}$$

Detailed proofs of (5)–(7) are given in the appendix.

Based on Table I, the minimum value of k_P to switch from pattern *Z* is $\frac{D_{Z\to P}}{2}$ and the minimum value of k_P before changing to pattern *Z* is $\frac{D_{P\to Z}}{2}$.

2) Pattern N*:* v_b also changes five times in one switching cycle, as specified in Table III: 0, $-v_{\rm dc}$, 0, $-v_{\rm dc}$, and 0. The duration of each level is provided. The two voltage pulses are also symmetrical quarterly at 0.25*T* and 0.75*T*, respectively. Their durations are the same and are determined by predicting v_C to reach $v_{\rm ref}$ at *T*. The duty ratio k_N is

$$k_N = \frac{t_{12}}{T} = \frac{t_{45}}{T}. \tag{8}$$

TABLE V
SUMMARY OF PARAMETERS IN PREDICTING i_C AND v_C USING (1) AND (2) FOR PATTERN N

t_x	t_y	$t_{xy} = t_y - t_x$	v_b	Initial values		Predicted values	
				$i_C(t_x)$	$v_C(t_x)$	$i_C(t_y)$	$v_C(t_y)$
t_0	t_1	$t_{01} = (0.25 - 0.5\,k_N)\,T$	0	$i_C(t_0)$	$v_C(t_0)$	$i_C(t_1)$	$v_C(t_1)$
t_1	t_2	$t_{12} = k_N\,T$	$-v_{dc}$	$i_C(t_1)$	$v_C(t_1)$	$i_C(t_2)$	$v_C(t_2)$
t_2	t_3	$t_{23} = (0.25 - 0.5\,k_N)\,T$	0	$i_C(t_2)$	$v_C(t_2)$	$i_C(t_3)$	$v_C(t_3)$
t_3	t_4	$t_{34} = (0.25 - 0.5\,k_N)\,T$	0	$i_C(t_3)$	$v_C(t_3)$	$i_C(t_4)$	$v_C(t_4)$
t_4	t_5	$t_{45} = k_N\,T$	$-v_{dc}$	$i_C(t_4)$	$v_C(t_4)$	$i_C(t_5)$	$v_C(t_5)$
t_5	t_6	$t_{56} = (0.25 - 0.5\,k_N)\,T$	0	$i_C(t_5)$	$v_C(t_5)$	$i_C(t_6)$	$v_C(t_6)$

Thus

$$t_{01} = t_{23} = t_{34} = t_{56} = (0.25 - 0.5\,k_N)T. \tag{9}$$

Table V summarizes the parameters used in predicting the values of i_C and v_C after a certain time interval, as described by (1) and (2). Similar to the pattern P, by putting the predicted values from a previous time interval as the initial values for the next time interval, the capacitor current and voltage at t_6 can be shown to be

$$i_C(t_6) \approx i_C(t_0)(1) + v_C(t_0)\left(-\frac{T}{L}\right) - v_{\mathrm{dc}}(t_0)\left(\frac{2kT}{L}\right) \tag{10}$$

and

$$v_C(t_6) \approx i_C(t_0)\left(\frac{T}{C}\right) + v_C(t_0)\left(1 - \frac{T^2}{2CL}\right) - v_{\mathrm{dc}}(t_0)\left(\frac{kT^2}{CL}\right). \tag{11}$$

Let $v_C(t_6) = v_{\mathrm{ref}}(t_0)$. The value of k_N is

$$k_N = \left[\left(\frac{CL}{T^2}\right) v_{\mathrm{ref}}(t_0) - \left(\frac{L}{T}\right) i_C(t_0) + \left(\frac{1}{2} - \frac{CL}{T^2}\right) v_C(t_0)\right] \frac{-1}{v_{\mathrm{dc}}(t_0)}. \tag{12}$$

Detailed proofs of (10)–(12) are given in the appendix.

Thus, based on Table I, the minimum value of k_N to switch from pattern Z is $\frac{D_{Z\to N}}{2}$ and the minimum value of k_N before changing to pattern Z is $\frac{D_{N\to Z}}{2}$.

3) Pattern Z*:* v_b also changes five times in one switching cycle, as specified in Table III: 0, v_{dc}, 0, $-v_{\mathrm{dc}}$, and 0. The duration of each level is also provided. The two voltage pulses are also symmetrical quarterly at 0.25T and 0.75T, respectively. The average value of v_b equals v_{ref}. Thus

$$k_{Z+} - k_{Z-} = \frac{v_{\mathrm{ref}}}{v_{\mathrm{dc}}} \tag{13}$$

where k_{Z+} is the duty ratio of the voltage pulse when $v_b = v_{\mathrm{dc}}$, and k_{Z-} is the duty ratio of the voltage pulse when $v_b = -v_{\mathrm{dc}}$.

k_{Z+} and k_{Z-} are designed to change oppositely as

$$k_{Z+} = -k_{Z-} + D_{\max} \tag{14}$$

where $D_{\max}$ is the maximum value of k_{Z+} and k_{Z-}.

Upon changing the pattern from P to Z

$$k_{Z+} - k_{Z-} = D_{P\to Z}. \tag{15}$$

Upon changing the pattern from Z to P

$$k_{Z+} - k_{Z-} = D_{Z\to P}. \tag{16}$$

$D_{\max}$ is chosen to cover the operation of the two transitions. Since $D_{Z\to P} > D_{P\to Z}$, the former condition is considered, where $k_{Z-} = 0$. Thus, by using (14) and (16)

$$D_{\max} = D_{Z\to P}. \tag{17}$$

By substituting (17) into (14) and solving (13) and (14) for k_{Z+} and k_{Z-}

$$k_{Z+} = \frac{1}{2}\left(D_{Z\to P} + \frac{v_{\mathrm{ref}}}{v_{\mathrm{dc}}}\right) \tag{18}$$

and

$$k_{Z-} = \frac{1}{2}\left(D_{Z\to P} - \frac{v_{\mathrm{ref}}}{v_{\mathrm{dc}}}\right). \tag{19}$$

Similarly, for the transitions between Z and N

$$k_{Z+} = -\frac{1}{2}\left(D_{Z\to N} - \frac{v_{\mathrm{ref}}}{v_{\mathrm{dc}}}\right) \tag{20}$$

and

$$k_{Z-} = -\frac{1}{2}\left(D_{Z\to N} + \frac{v_{\mathrm{ref}}}{v_{\mathrm{dc}}}\right). \tag{21}$$

Thus, the duration of the time intervals can be shown to be

$$t_{01} = t_{23} = (0.25 - 0.5\,k_{Z+})T \tag{22}$$

$$t_{12} = k_{Z+}T \tag{23}$$

$$t_{34} = t_{56} = (0.25 - 0.5\,k_{Z-})T \tag{24}$$

and

$$t_{45} = k_{Z-}\,T. \tag{25}$$

Table VI summarizes the parameters used in predicting the values of i_C and v_C after a certain time interval, as described by (1) and (2). Again, by putting the predicted values from a previous time interval as the initial values for the next time

TABLE VI
SUMMARY OF PARAMETERS IN PREDICTING i_C AND v_C USING (1) AND (2) FOR PATTERN Z

t_x	t_y	$t_{xy} = t_y - t_x$	v_b	Initial values		Predicted values	
				$i_C(t_x)$	$v_C(t_x)$	$i_C(t_y)$	$v_C(t_y)$
t_0	t_1	$t_{01} = (0.25 - 0.5\,k_{Z+})\,T$	0	$i_C(t_0)$	$v_C(t_0)$	$i_C(t_1)$	$v_C(t_1)$
t_1	t_2	$t_{12} = k_{Z+}\,T$	v_{dc}	$i_C(t_1)$	$v_C(t_1)$	$i_C(t_2)$	$v_C(t_2)$
t_2	t_3	$t_{23} = (0.25 - 0.5\,k_{Z+})\,T$	0	$i_C(t_2)$	$v_C(t_2)$	$i_C(t_3)$	$v_C(t_3)$
t_3	t_4	$t_{34} = (0.25 - 0.5\,k_{Z-})\,T$	0	$i_C(t_3)$	$v_C(t_3)$	$i_C(t_4)$	$v_C(t_4)$
t_4	t_5	$t_{45} = k_{Z-}\,T$	$-v_{dc}$	$i_C(t_4)$	$v_C(t_4)$	$i_C(t_5)$	$v_C(t_5)$
t_5	t_6	$t_{56} = (0.25 - 0.5\,k_{Z-})\,T$	0	$i_C(t_5)$	$v_C(t_5)$	$i_C(t_6)$	$v_C(t_6)$

interval, the capacitor current and voltage at t_6 can be shown to be

$$i_C(t_6) \approx i_C(t_0)(1) + v_C(t_0)\left(-\frac{T}{L}\right) + v_{\text{dc}}(t_0)\left(\frac{2kT}{L} - \frac{T}{8L}\right) \tag{26}$$

and

$$v_C(t_6) \approx i_C(t_0)\left(\frac{T}{C}\right) + v_C(t_0)\left(1 - \frac{T^2}{2CL}\right) + v_{\text{dc}}(t_0)\left(\frac{kT^2}{CL} - \frac{T^2}{32CL}\right). \tag{27}$$

Let $v_C(t_6) = v_{\text{ref}}(t_0)$.

Based on (14), (23), and (25), k_{z+} and k_{z-} are

$$k_{Z+} = \left[\begin{array}{r}\left(\frac{CL}{T^2}\right) v_{\text{ref}}(t_0) - \left(\frac{L}{T}\right) i_C(t_0)\\ + \left(\frac{1}{2} - \frac{CL}{T^2}\right) v_C(t_0)\end{array}\right]\frac{1}{v_{\text{dc}}(t_0)} + \left(\frac{1}{4}\right) D_{\max} \tag{28}$$

and

$$k_{Z-} = \left[\begin{array}{r}\left(\frac{CL}{T^2}\right) v_{\text{ref}}(t_0) - \left(\frac{L}{T}\right) i_C(t_0)\\ + \left(\frac{1}{2} - \frac{CL}{T^2}\right) v_C(t_0)\end{array}\right]\frac{-1}{v_{\text{dc}}(t_0)} + \left(\frac{3}{4}\right) D_{\max}. \tag{29}$$

Detailed proofs of (26)–(29) are given in the appendix.

B. Derivations of Duty Ratios

Based on (7), (12), (28), and (29), the duty ratios are

$$k_P = [\alpha_1\, v_{\text{ref}}(t_0) + \alpha_2\, i_C(t_0) + \alpha_3\, v_C(t_0)]\,(\alpha_4) \tag{30}$$

$$\begin{aligned} k_N &= [\alpha_1\, v_{\text{ref}}(t_0) + \alpha_2\, i_C(t_0) + \alpha_3\, v_C(t_0)]\,(-\alpha_4)\\ &= 0 - k_P \end{aligned} \tag{31}$$

$$\begin{aligned} k_{Z+} &= [\alpha_1\, v_{\text{ref}}(t_0) + \alpha_2\, i_C(t_0) + \alpha_3\, v_C(t_0)]\,(\alpha_4) + \alpha_5\\ &= k_P + \alpha_5 \end{aligned} \tag{32}$$

$$\begin{aligned} k_{Z-} &= [\alpha_1\, v_{\text{ref}}(t_0) + \alpha_2\, i_C(t_0) + \alpha_3\, v_C(t_0)]\,(-\alpha_4) + 3\alpha_5\\ &= 0 - k_P + 3\alpha_5 \end{aligned} \tag{33}$$

where $\alpha_1 = \frac{CL}{{T_{\text{sc}}}^2}$, $\alpha_2 = -\frac{L}{T_{\text{sc}}}$, $\alpha_3 = \frac{1}{2} - \frac{CL}{{T_{\text{sc}}}^2}$, $\alpha_4 = \frac{1}{v_{\text{dc}}(t_0)}$, and $\alpha_5 = \frac{D_{\max}}{4}$.

The duty ratio is a linear combination of v_{ref}, i_C, and v_C forming a switching surface. Fig. 3 shows the block diagram illustrating the overall control mechanism. Fig. 3(a) shows the block diagram of generating the gate signals, $G_1 - G_4$, from the sampled values of v_{dc}, i_c, and v_c. The output voltage reference v_{ref} is internally generated. The control mechanism consists of the following four main parts.

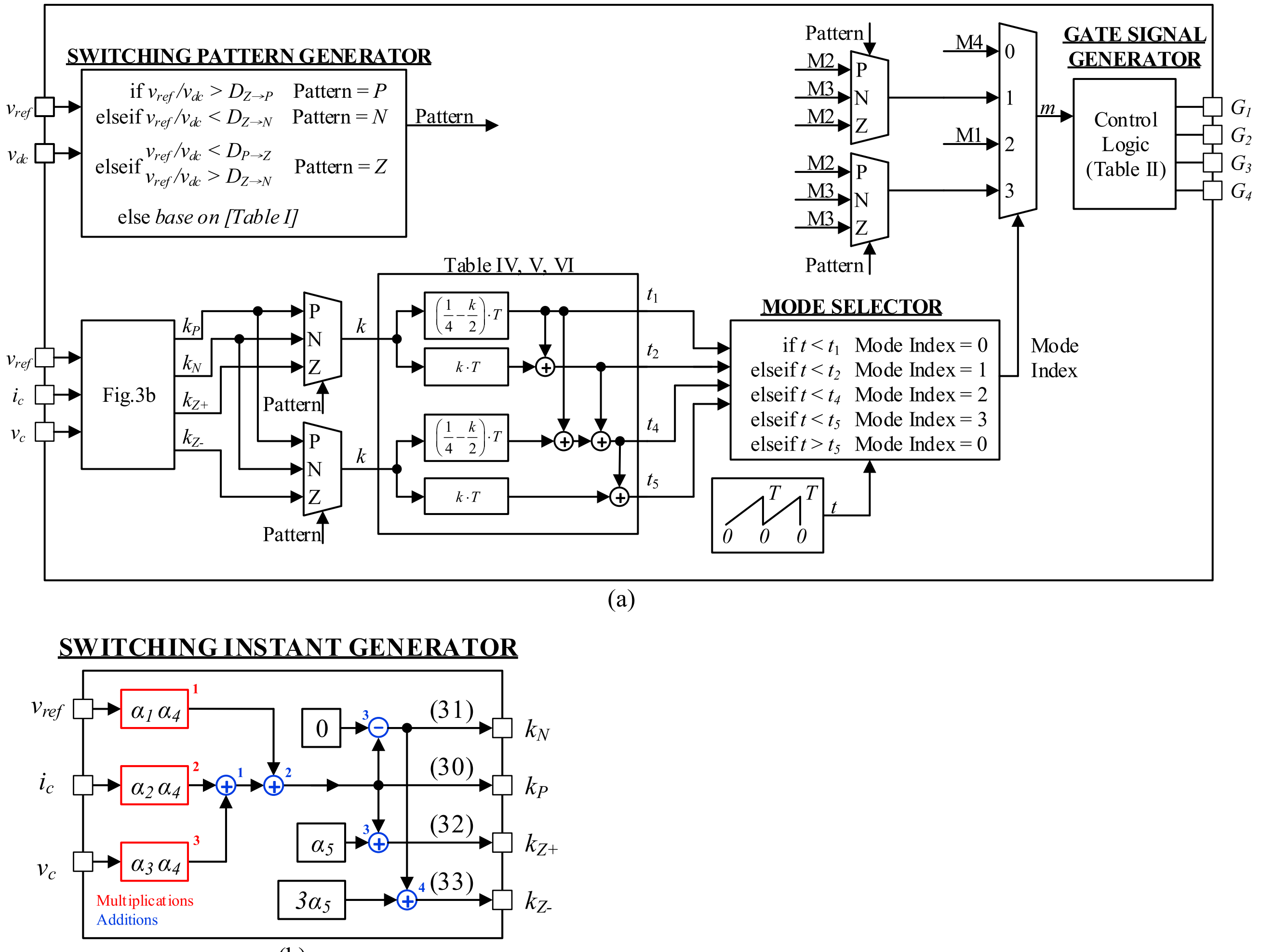
1) The first one is the switching pattern generator. It produces the switching pattern, i.e., pattern *P*, *Z*, and *N*, named as "Pattern," in Fig. 3(a). Based on Table I, the switching pattern is determined by v_{ref} / v_{dc}, and the threshold for changing the switching pattern.
2) The second part is switching instant generator. As shown in Fig. 2, t_1, t_2, t_4, and t_5 are switching instants of each switching pattern. Based on (30)–(33), the duty ratios of the voltage pulses of all switching patterns, i.e., k_P, k_N, k_{z+}, and k_{z-}, are first calculated. Fig. 3(b) shows the realization. Then, based on Tables IV–VI, the switching instants are calculated with the duty ratio of the selected switching pattern *k* as the input.
3) The third part is the mode selector. An internal reference time *t* changing between 0 and *T* is derived from a sawtooth function. It is compared with the values of the switching instants to determine the mode, i.e., M1 – M4, which is indexed by Mode Index.
4) The fourth part is the gate signal generator. Based on Table II, the gate signals to $S_1 - S_4$ are generated with the output of the mode selector *m* as the input to this part.

C. Static Characteristics

The ripple current through *L* and the ripple voltage across *C* in the three patterns are derived. Since the modulation approach for patterns *P* and *N* is similar, the ripple current and ripple voltage are the same and thus their values in pattern *P* are studied only.

1) Pattern P*:* The average output voltage across *C*, i.e., $V_{C,P}$, is

$$V_{C,P} = 2\,k_P\, v_{\text{dc}}. \tag{34}$$



(a)

(b)

Fig. 3. Mechanism of the proposed control method. (a) Generation of gate signals. (b) Generation of the duty ratios of different patterns [requiring three multiplications (red) and four additions (blue)].

Based on (2)

$$\frac{\Delta I_{L,P}}{k_P\, T} = \frac{v_{\mathrm{dc}} - V_{C,P}}{L} \tag{35}$$

where $\Delta I_{L,P}$ is the peak-to-peak ripple current.

By substituting (34) into (35)

$$\Delta I_{L,P} = \frac{(1-2\,k_P)\,k_P\,v_{\mathrm{dc}}\,T}{L}. \tag{36}$$

$\Delta I_{L,P}$ is maximum when $k_P = 0.25$. Its maximum value $\Delta I_{L,P,\max}$ is

$$\Delta I_{L,P,\max} = \frac{v_{\mathrm{dc}}\,T}{8\,L}. \tag{37}$$

The averaging charging current to the capacitor $I_{C,\mathrm{ch},P}$ is

$$I_{C,\mathrm{ch},P} = \frac{(1-2k_p)\,k_p\,T^2\,v_{\mathrm{dc}}}{16\,L}. \tag{38}$$

Thus, the peak-to-peak ripple voltage $\Delta V_{C,P}$ is

$$\Delta V_{C,P} = \frac{(1-2k_p)\,k_p\,T^2\,v_{\mathrm{dc}}}{16\,C\,L}. \tag{39}$$

$\Delta V_{C,P}$ is maximum when $k_P = 0.25$. Its maximum value $\Delta V_{C,P,\,\max}$ is

$$\Delta V_{C,P,\,\max} = \frac{T^2\,v_{\mathrm{dc}}}{128\,C\,L}. \tag{40}$$

2) *Pattern* Z: The average output voltage across C, i.e., $V_{C,Z}$, is

$$V_{C,Z} = (k_{Z+} - k_{Z-})\,v_{\mathrm{dc}}. \tag{41}$$

Based on (2)

$$\begin{aligned}\Delta I_{L,Z} &= \frac{k_{z-}T\,(v_{\mathrm{dc}} + V_{C,Z})}{L} \quad \text{for} \quad k_{z-} > k_{z+}\\ \Delta I_{L,Z} &= \frac{k_{z+}T\,(v_{\mathrm{dc}} - V_{C,Z})}{L} \quad \text{for} \quad k_{z+} > k_{z-}\end{aligned} \tag{42}$$

where $\Delta I_{L,Z}$ is the peak-to-peak ripple current.

By substituting (41) into (42)

$$\Delta I_{L,Z} = \frac{k_{z-}T\,v_{\mathrm{dc}}\,(1 + k_{Z+} - k_{Z-})}{L} \quad \text{for} \quad k_{z-} > k_{z+}$$

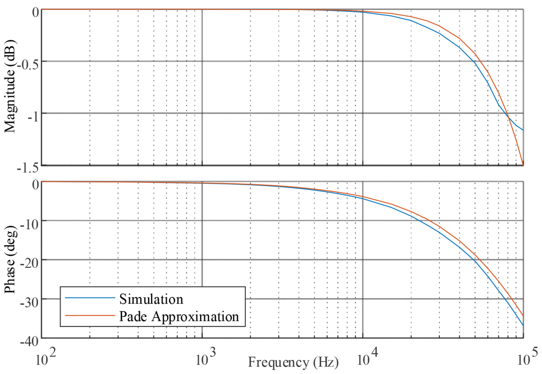


Fig. 4. Transfer characteristics of the entire system.

$$\Delta I_{L,Z} = \frac{k_{z+}\, T\, v_{\mathrm{dc}}\, (1 - k_{Z+} + k_{Z-})}{L} \quad \text{for} \quad k_{z+} > k_{z-}. \tag{43}$$

$\Delta I_{L,Z}$ is maximum when $k_{Z+} - k_{Z-} = \frac{1}{8}$ or $-\frac{1}{8}$. The maximum value $\Delta I_{L,Z,\,\max}$ is

$$\Delta I_{L,Z} = \frac{T\, v_{\mathrm{dc}}}{L} \left(\frac{7}{64}\right). \tag{44}$$

The averaging charging current to the capacitor $I_{C,\mathrm{ch},Z}$ is

$$I_{C,\mathrm{ch},Z} = \frac{T^2\, v_{\mathrm{dc}} \left(k_{z-} - {k_{z-}}^2 + k_{z+} - {k_{z+}}^2\right)}{8\, L}. \tag{45}$$

Thus, the peak-to-peak ripple voltage $\Delta V_{C,Z}$ is

$$\Delta V_{C,Z} = \frac{T^2\, v_{\mathrm{dc}} \left(k_{z-} - {k_{z-}}^2 + k_{z+} - {k_{z+}}^2\right)}{8\, C\, L}. \tag{46}$$

$\Delta V_{C,Z}$ is maximum when $k_{Z+} - k_{Z-} = 0$. Its maximum value $\Delta V_{C,Z,\,\max}$ is

$$\Delta V_{C,Z,\,\max} = \frac{T^2\, v_{\mathrm{dc}}}{C\, L} \left(\frac{15}{1024}\right). \tag{47}$$

D. Transfer Characteristics

Since the value of $v_C(t_6)$ is controlled to be the same as $v_{\mathrm{ref}}(t_0)$, the transfer characteristic of the entire system G can be expressed as

$$G = \frac{V_C\,(s)}{V_{\mathrm{ref}}\,(s)} = e^{-sT}. \tag{48}$$

By applying first-order Padé approximation with a zero-order numerator

$$G\,(s) = \frac{v_C(s)}{v_{\mathrm{ref}}(s)}\Big|_{s=j\omega} = \frac{1}{1+sT}. \tag{49}$$

Fig. 4 shows the simulated transfer characteristics and the approximated characteristics with (49). The parameters used in the analysis are listed in Table VIII. Simulations are performed using PSIM where a sinusoidal signal v_{ref} is injected and the output v_C is obtained at different injection frequencies. At 10 kHz, the gain is reduced by 0.025 dB and the phase shift is 4°. In other words, the proposed control technique can keep tracking tightly. At the *LC* filter's cutoff frequency of 60 kHz, the gain is reduced by 0.7dB and the phase shift is 25° only. It can be observed that the half-power point of the entire system is theoretically higher than the cutoff frequency of the output *LC* filter with the proposed control method.

E. Design of the Values for L *and* C

The cutoff frequency of the output filter is designed to be twice the maximum output frequency $f_{\max}$. That is

$$\frac{1}{2\pi\sqrt{L\,C}} = 2\, f_{\max}. \tag{50}$$

The value of L is designed by considering the peak current in C in a switching cycle as

$$L = \frac{V_{\mathrm{dc}}}{2\, f_{\mathrm{sw}}\, i_{C,pk}} \tag{51}$$

where $i_{C,pk}$ is the peak capacitor current.

By using (50) and (51)

$$C = \frac{f_{\mathrm{sw}}\, i_{C,pk}}{8\,\pi^2\, f_{\max}^2\, V_{\mathrm{dc}}}. \tag{52}$$

A maximum current slew rate is expressed as

$$i_{\mathrm{slew-rate}} = \frac{T\, v_{\mathrm{dc}}}{L}. \tag{53}$$

Based on (53), the maximum voltage slew rate is expressed as follows:

$$v_{\mathrm{slew-rate}} = \frac{T\, i_{\mathrm{slew-rate}}}{2\, C}. \tag{54}$$

III. COMPARISONS

A comparative study of the techniques using state trajectory prediction is conducted. The results are tabulated in Table VII. To track state trajectories and decide on appropriate switching action, the research work in [27], [28], and [29] required a sampling frequency f_{samp} significantly higher than the switching frequency f_{sw}. The techniques described in [27], [28], and [29] require the sampling frequencies to be 75, 185.2, and 25–50 times higher than the switching frequency, respectively. If the designed switching frequency is high, for example, 1 MHz, it poses challenges to implementing the techniques. Furthermore, as the computation is performed after each sampling, it places a demand on the controller's computational speed and resources. Conversely, the sampling frequency required by the proposed technique is the same as the switching frequency. Computational requirements are relatively less stringent. In addition, in terms of the number of mathematical operations, the proposed technique is similar to those presented in [27], [28], and [29]. One potential realization of trajectory prediction relies on an analog approach as described in [30] or a hybrid approach as described in [29], but it is less adaptable and is affected by variations in component tolerance that can impact its operation. Finally, due to the low-frequency operation, the necessary filter components

TABLE VII
COMPARISON OF VARIOUS TRAJECTORY PREDICTION TECHNIQUES

Ref.	[27]	[28]	[29]	[30]	Proposed
Switching frequency (f_{sw})	Variable Avg. 4 kHz	Variable Avg. 27 kHz	Fixed 20–40 kHz	Fixed 15 kHz	Fixed 1 MHz
Effective switching frequency	Avg. 8 kHz	Avg. 27 kHz	20–40 kHz	30 kHz	2 MHz
Sampling frequency (f_{samp})	300 kHz	5 MHz	1 MHz	–	1 MHz
f_{samp} / f_{sw}	75	185.2	25–50	–	1
Modulation	Unipolar	Bipolar	Bipolar	Unipolar	Unipolar + Bipolar
Control method	PS-MC *	PS-MC *	TC-PWM **	TC-PWM **	TC-PWM **
Capacitor voltage sensing (v_C)	YES	YES	YES	YES	YES
Capacitor current sensing (i_C)	YES	YES	NO	YES	YES
Inductor (μH)	7000	680	1500	357	2
Output Capacitor (μF)	4.7	2.2	60	9.4	2
Filter cutoff freq. (kHz)	0.88	4.1	0.53	2.75	79.5
Effective switching freq./ Filter cutoff freq.	9.1	6.5	75.5	10.9	25
Sampling freq./ Filter cutoff freq.	340.9	1219.5	1886.8	-	12.6
Load transient settling time (μs)	3440	66	1200	500	3–9
# of switching actions under load transient*	26	2	48–96	15	6–18
# of mathematical operations before the 1st switching action	Digital: 6 multiplications 3 additions	Digital: 6 multiplications 3 additions	Analog: 1 differentiation 1 multiplication 3 additions Digital: 1 nonlinear function	Analog: 2 multiplications 3 additions	Digital: maximum 3 multiplications 3 additions

*PS-MC: periodic sampling modulation control [31]; ** TC-PWM: triangular carrier PWM control [31]

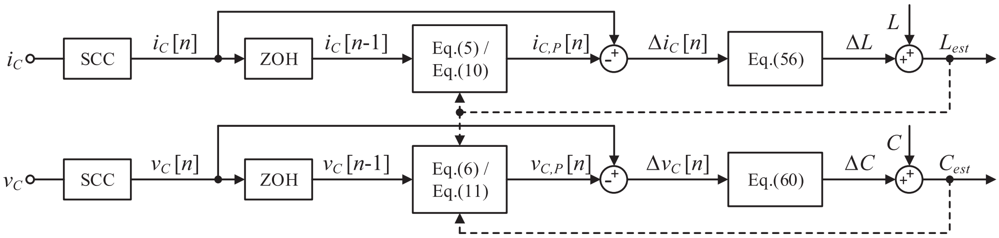


Fig. 5. Output filter estimator.

typically have substantial values, which leads to bulky size and a long settling time in the presence of large-signal disturbances.

IV. EXTRACTION OF FILTER PARAMETERS

Based on the control technique, a filter parameter extraction mechanism is derived. The idea utilizes a feedback mechanism that begins by comparing the predicted and actual values of the capacitor voltage and current after one switching cycle. The difference is then used to estimate filter parameters and subsequently alter the prediction formulas. The ultimate target is to ensure that the predicted values are the same as the actual values. Fig. 5 shows the block diagram.

Equations (5), (10), and (26) are the prediction formulas for i_C in patterns *P*, *N*, and *Z*, respectively. They are functions of *L*. Equations (6), (11), and (27) are the ones for v_C in patterns *P*, *N*, and *Z*, respectively. They are functions of *L* and *C*. Then, the predicted and actual values of i_C are used to determine *L*, whereas the predicted and actual values of v_C are used to determine *C*. The mechanisms are given below.

A. Determination of the Value of L

i_C is sampled by a SCC and a zero-order-hold (ZOH). The sampled values of i_C and v_C, i.e., $i_C(nT)$ and $v_C\ (nT)$, are used to calculate the predicted value of i_C after one switching cycle, i.e., $i_{C,P}((n+1)T)$, with the prediction formulas. Then, the error between $i_{C,P}((n+1)T)$ and the actual value of i_C after one switching cycle, i.e., $i_C((n+1)T)$, is determined. Mathematically

$$\Delta i_C\left((n+1)T\right) = i_C\left((n+1)T\right) - i_{C,P}\left((n+1)T\right) \quad (55)$$

where $\Delta i_C((n+1)T)$ is the estimation error of the (n+1)th cycle.

Δi_C is fed to a proportional-plus-integral (PI) controller. The output of the controller L_{est} gives the estimated value of L. It can be expressed as

$$L_{\text{est}} = K_{P,L}\,\Delta i_C + K_{i,L}\int \Delta i_C\,dt. \quad (56)$$

According to Cohen–Coon PI design method [32], the initial guest values for $K_{P,L}$ and $K_{i,L}$ are

$$K_{P,L} = \frac{\tau}{\tau_{\text{dead}}}\left(1+\frac{\tau_{\text{dead}}}{3\tau}\right) \quad (57)$$

$$K_{i,L} = \frac{K_{P,L}}{\tau_{\text{dead}}}\left(\frac{9\tau+20\tau_{\text{dead}}}{30\tau+3\tau_{\text{dead}}}\right) \quad (58)$$

where the process reaction curve dead time (τ_{dead}) is $\frac{T_{50\text{ Hz}}}{32}$ and the time constant for the response change (τ) is $\frac{T_{50\text{ Hz}}}{64}$. The estimated value of L is then fed to the prediction formulas.

B. Determination of the Value of C

The value of v_C is sampled by an SCC and a ZOH. The sampled values of i_C and v_C, i.e., $i_C(nT)$ and $v_C\ (nT)$, are used to calculate the predicted value of v_C after one switching cycle, i.e., $v_{C,P}((n+1)T)$, with the prediction formulas. Then, the error between $v_{C,P}((n+1)T)$ and the actual value of v_C after one switching cycle, i.e., $v_C((n+1)T)$, is determined. Mathematically

$$\Delta v_C\left((n+1)T\right) = v_C\left((n+1)T\right) - v_{C,P}\left((n+1)T\right) \quad (59)$$

where $\Delta v_C((n+1)T)$ is the estimation error of the $(n+1)$th cycle.

Δv_C is fed to a PI controller. The output of the controller C_{est} gives the estimated value of C. It can be expressed as

$$C_{\text{est}} = K_{P,C}\,\Delta v_C + K_{i,C}\int \Delta v_C\,dt \quad (60)$$

According to Cohen-Coon PI design method [32], the initial guess values for $K_{P,C}$ and $K_{i,C}$ are

$$K_{P,C} = \frac{\tau}{\tau_{\text{dead}}}\left(1+\frac{\tau_{\text{dead}}}{3\tau}\right) \quad (61)$$

$$K_{i,C} = \frac{K_{P,L}}{\tau_{\text{dead}}}\left(\frac{9\tau+20\tau_{\text{dead}}}{30\tau+3\tau_{\text{dead}}}\right) \quad (62)$$

where the process reaction curve dead time (τ_{dead}) is $\frac{T_{50\text{ Hz}}}{32}$ and the time constant for the response change (τ) is $\frac{T_{50\text{ Hz}}}{64}$.

The estimated value of C is then fed to the prediction formulas.

V. EXPERIMENTAL VERIFICATION

A 1-kVA prototype applied to a wideband series harmonic voltage compensator (WSHVC) for enhancing the stability of a 6.5-kVA microgrid has been built. The microgrid consists of three commercial grid-tied solar inverters, one nonlinear load, and a grid simulator with adjustable grid inductance. Detailed descriptions of WSHVC can be found in [33] and [34].

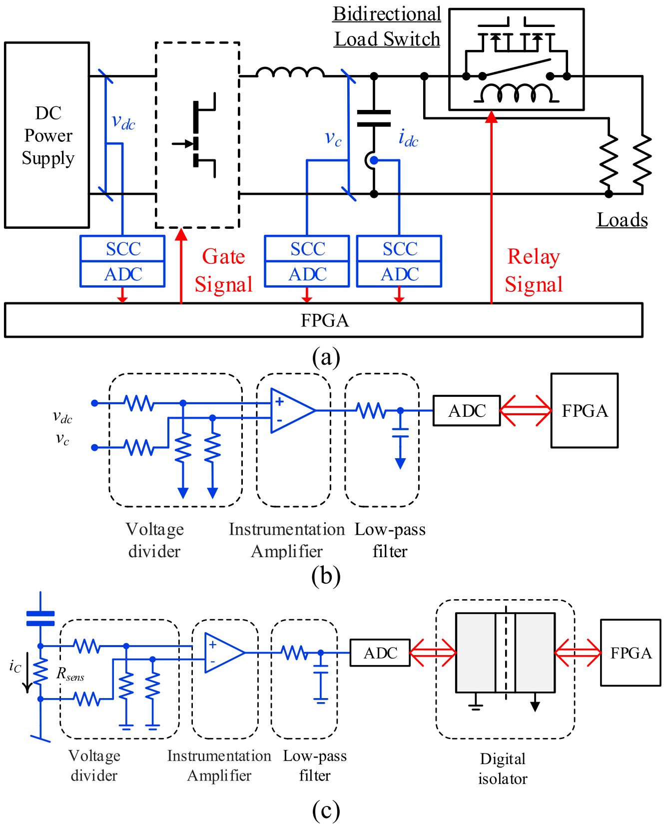


Fig. 6. Prototype inverter. (a) Circuit schematic. (b) SSC for sensing v_{dc} and v_c. (c) SCC for sensing i_c.

TABLE VIII
DESIGN SPECIFICATION AND COMPONENT VALUES OF THE PROTOTYPE

Parameter	Value	Component	Part no.
v_{dc}	50 V	$S_1 - S_4$	GaN Systems GS61008T
Rated output voltage	40 V	L	2 μH
Rated output current	38 A	C	2 μF
Bandwidth	−1 dB @ 75 kHz	Controller	Cyclone V SoC FPGA (5CEFA5)

The test setup for the inverter is shown in Fig. 6(a) and (b) provides details of the SCCs used for sensing voltages v_{dc} and v_c. Fig. 6(c) shows the SCC used for sensing current i_c. The design specification and component values of the prototype inverter are given in Table VIII. The transient response of the inverter is studied by using a bidirectional load switch, which is connected in series with the load. The load can then be controlled to connect with the inverter output.

To implement the control algorithm and generate gate signals for the switching devices, a field-programmable gate array (FPGA) is utilized. The core switching control flowchart is

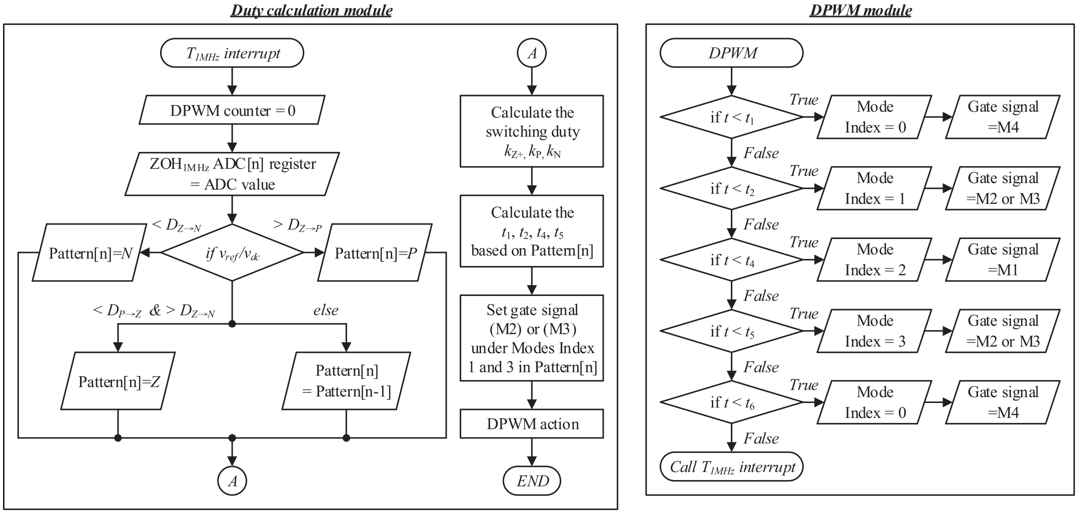


Fig. 7. Flowchart of the proposed control algorithm.

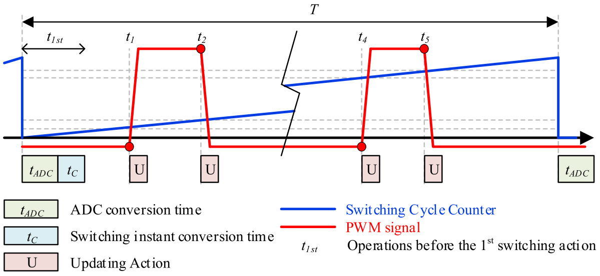


Fig. 8. Illustration of the sample-to-update process.

depicted in Fig. 7. Fig. 3 shows the FPGA's parallel processing signal mechanism and the control equation. At the start of each switching cycle, the PWM timer will trigger the algorithm and reset the counter to zero. Then, the ADC will store the sampled data in the memory registers and the switching pattern will be chosen by referencing v_{ref}. The duty ratios are determined by (30)–(33). By comparing the duty ratios with the counter registers, the gate signals will be updated via the Mode Index at t_1, t_2, t_4, and t_5.

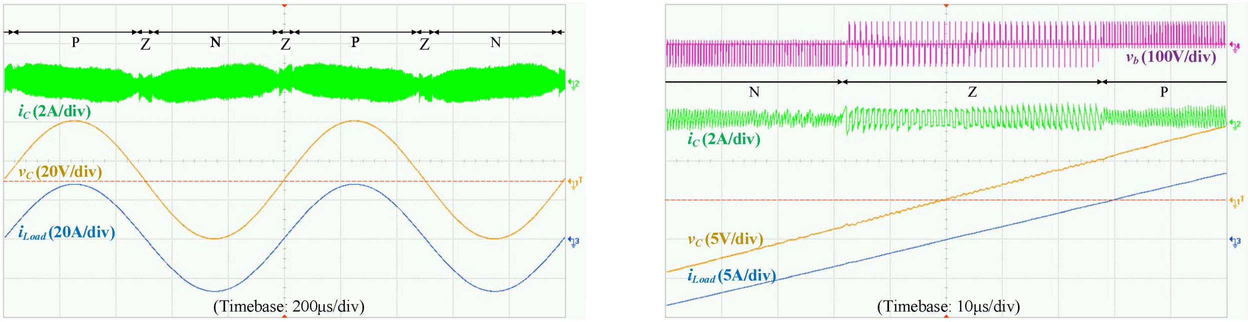
The proposed control algorithm has its sampling frequency being the same as the switching frequency. In other words, it does not require sensing any voltage or current waveforms within a switching cycle. Instead, the sampling function is performed at the beginning of each switching cycle. Afterward, the duty ratios of all switches are computed by the control algorithm given in Fig. 3(b). The sample-to-update process over one switching cycle is shown in Fig. 8. At the start of each switching cycle, the controller takes a time of t_{ADC} to complete analog-to-digital conversion. Then, the algorithm takes a time of t_C to calculate the switching instants of all switches. Thus, the controller will update the switching states of all switches accordingly. The experimental prototype has $t_{\text{ADC}} = 38$ ns and $t_C = 16$ ns. In other words, the earliest updating time t_1, which determines the maximum duration of the first pulse, is limited by the total time, $t_{\text{ADC}} + t_C$.

When implementing traditional control laws, there is a higher demand for instruction cache memory per sample, resulting in increased computational power requirements and latency. As the power converter era is moving towards higher frequencies, reaching into the megahertz range, practical implementation encounters challenges such as computational power limitations of digital controllers, analog-to-digital conversion speed, signal detection limitations, complex control equations, and cost-effectiveness considerations. In contrast, the proposed control technique offers a simplified sample-to-update mechanism, making it well-suited for application in high-frequency power converters. Ten memories, including three for storing constants, three for storing sampled data, and four for storing duty ratios, and three multiplication memories are required. In total, 13 memories are used. The total memory size used is 234 bits (13 × 18 bits). The signal latency is around 54 ns. The algorithm can be easily implemented on many popularly adopted controllers, such as C2000, STM32, and RISC V series processors.

Fig. 9(a) shows the waveforms of the capacitor current i_C, output voltage v_C, and output current i_{Load} when the prototype is connected to a resistive load and the output frequency is set at 1 kHz. Fig. 9(b) shows their waveforms at zero crossing. The transitions from pattern *N* to pattern *Z* and from pattern *Z* to pattern *P* are smooth. The measured THD is 0.35%.

To test the dynamic response of the converter, Fig. 10 shows the corresponding waveforms when the prototype is connected to a resistive load and the output frequency is set at 15 kHz, which is commonly observed in some standards, such as LV148 Automotive Test Standard. The transitions switching among patterns *P*, *Z*, and *N* are identified. Compared with the reference signal, the rise time from 0 V to the peak voltage of 40 V is 9.09 μs.

Fig. 11 shows the waveforms of i_C, v_C, and i_{Load} when the prototype is connected to a resistive load. The reference signal



(a) (b)

Fig. 9. Experimental results with the output frequency of 1 kHz. (a) Overall waveform. (b) Zero-crossing region.

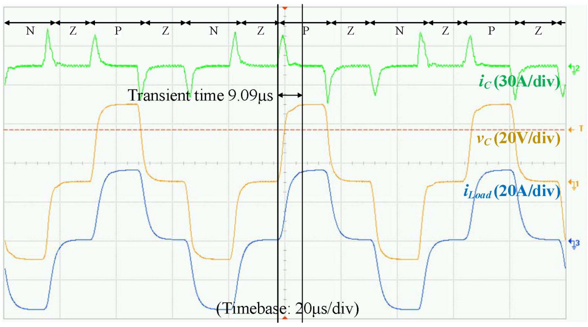


Fig. 10. Experimental results with the output frequency of 15 kHz.

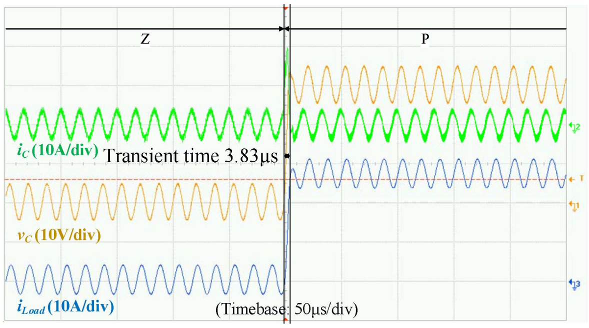


Fig. 11. Experimental results with the output frequency of 60 kHz and voltage step changing.

has its dc value changing from 0 to 30 V and has a 60 kHz, 10 Vpp sinusoidal voltage superimposed onto it. The transitions switching among patterns *P*, *Z*, and *N* are identified. Compared with the reference signal, the rise time from 0 to 30 V is 3.83 μs.

Fig. 12(a) illustrates the key waveforms over five switching cycles upon changing the reference voltage from 0 to 10 V. In Cycle 0, the converter operates in pattern *Z*. The controller determines the duty ratio at the beginning of the cycle. There are mode changes at $t_{1,0}$, $t_{2,0}$, $t_{4,0}$, and $t_{5,0}$. In Cycle 1, v_{ref} is changed from 0 V (OP1) to 10 V (OP2), as shown in Fig. 12(b). The converter operates in pattern *P*. The controller determines the duty ratio at the start of the cycle. The capacitor voltage and current start increasing. There are mode changes at times $t_{1,1}$, $t_{2,1}$, $t_{4,1}$, and $t_{5,1}$. At the start of Cycle 2, the controller calculates the duty ratio and is found to be negative when (30) for pattern *P* is applied. Thus, (31) for pattern *N* is applied. The pattern changes from *P* to *N*. During this cycle, the controller adjusts the duty ratio to increase the capacitor voltage and decrease the capacitor current until it reaches the voltage reference (point X) between $t_{4,2}$ and $t_{5,2}$. There are mode changes at $t_{1,2}$, $t_{2,2}$, $t_{4,2}$, and $t_{5,2}$. In Cycle 3, the controller determines the duty ratio to ensure that the capacitor voltage and current keep the operating point. The capacitor voltage reaches the voltage reference (point Y) again at the end of Cycle 3. There are mode changes at $t_{1,3}$, $t_{2,3}$, $t_{4,3}$, and $t_{5,3}$. Finally, in Cycle 4, the system has reached the steady state operation (OP2). It can be observed from the above illustration that the system can change the operation point within three switching cycles.

Fig. 12(b) shows the trajectory of the transient response, which is in blue color, from OP1 to OP2. The steady-state trajectories are shown in the red line. When $v_b = v_{\text{dc}}$, the family trajectory is represented by green dashed lines, yellow dashed lines represent $v_b = -v_{\text{dc}}$, and blue dashed lines $v_b = 0$ V.

Fig. 12(c) shows the trajectory at OP1, at which the converter is in pattern *Z*. Fig. 12(d) shows the trajectory at OP2, at which the converter is in pattern *P*.

A performance comparison between the proposed control algorithm and the traditional PID control [35]. Fig. 13 shows the outputs of the prototype using both control methods while sweeping the reference frequency from 1 to 28 kHz for testing their frequency responses. The two control algorithms are tested under the same operating conditions with the switching frequency of 1 MHz, input voltage of 50 V, and peak ac output voltage of 35 V. The load resistance is 3 Ω. Fig. 13(a) and (b) shows the results with the proposed method and PID control, respectively. The reference voltage has a sudden change when its frequency is changed from 28 to 1 kHz. With PID control, the output requires 0.25 ms to settle. The steady-state output error also increases with the reference frequency. With the proposed method, the output can keep tracking the reference over the considered frequency range.

In addition, the transient responses of the inverter using the two control methods have been studied. The input voltage is 50 V and the output voltage is 35 V. When the load is changed from 5 Ω (i.e., 7 A) to 2 Ω (i.e., 17.5 A), the results are shown in Fig. 14.

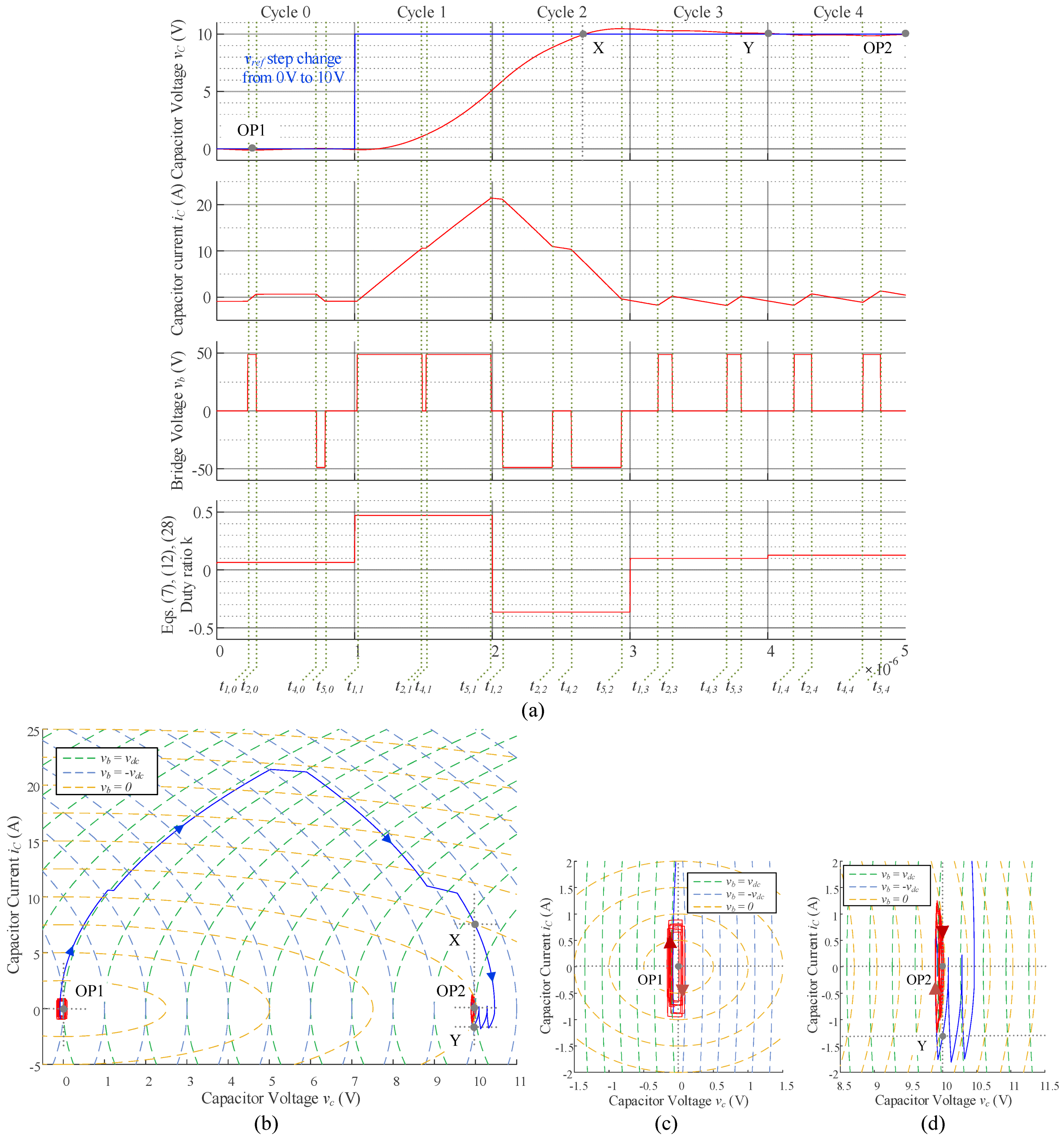


Fig. 12. Simulated switching transients and trajectories upon changing v_{ref} from 0 to 10 V. (a) Key waveforms. (b) Trajectory from OP1 to OP2. (c) Trajectories in pattern *Z*. (d) Trajectories in pattern *P*.

The maximum transient output voltage drop with the proposed method is only 0.5 V (i.e., 1.43%) and that with the PID method is 1.2 V (3.43%). The time required to reach 98% of the steady-state value with the proposed method is negligible, whereas the one using the PID control is 45 μs. Thus, the proposed control method offers a faster transient response.

Fig. 15 shows the block diagram of deriving the duty ratios with the PID control. The number of mathematical operations required in the proposed method [see Fig. 3(b)] involves three multiplications and four additions, which closely aligns with the requirement of the PID control that requires five multiplications and five additions.

The performance of the filter parameter extraction mechanism described in Section IV is evaluated. An experiment using five sets of initial values for the inductor (L) and capacitor (C) to obtain the estimated values and comparing them with the actual

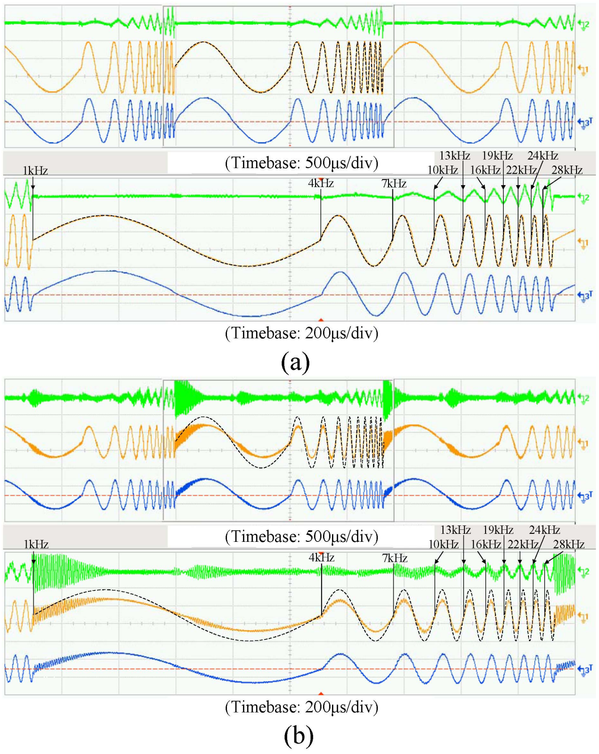


Fig. 13. Frequency response of the inverter with the reference frequency sweeping from 1 to 28 kHz. Black dashed line: v_{ref} (30 V/div), green line: i_C (20 A/div), orange line: v_C (30 V/div), and blue line: i_{Load} (10 A/div). (a) Proposed control. (b) PID control.

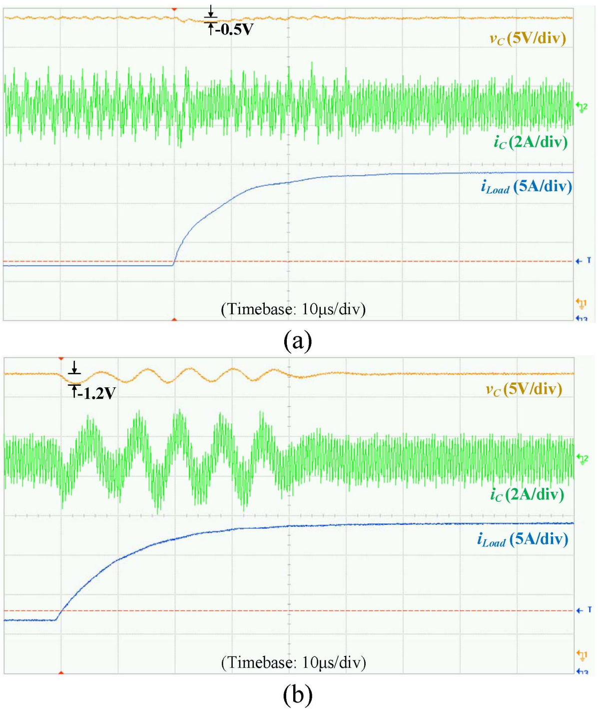


Fig. 14. Transient response under sudden load change from 5 to 2 Ω. (a) Proposed control. (b) PID control.

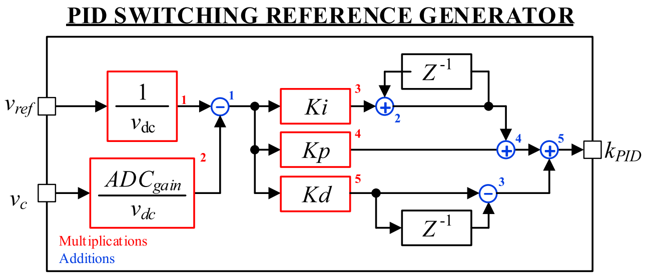


Fig. 15. PID control [requiring five multiplications (red) and five additions (blue)].

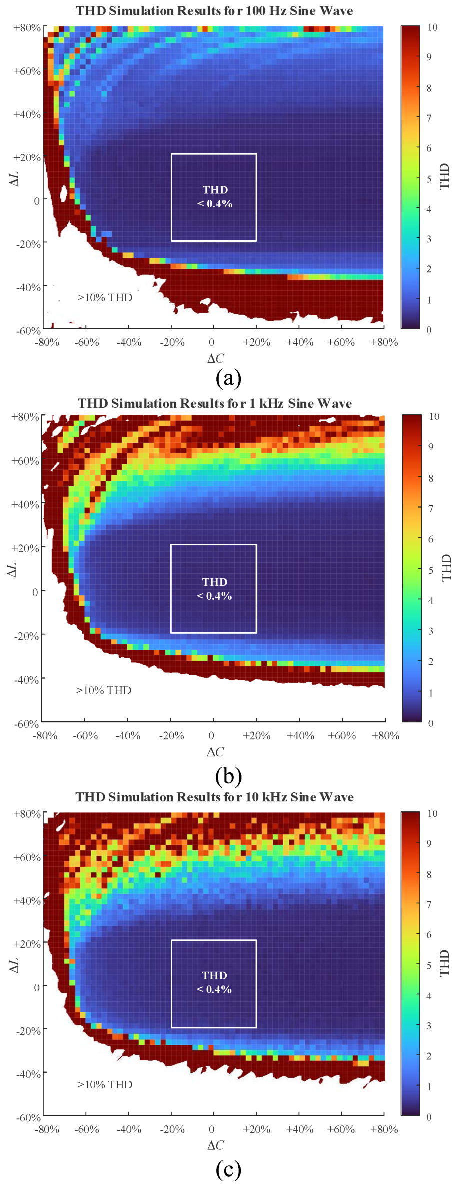


Fig. 16. THD at different reference frequencies while varying the values of L from -60% to $+80\%$ and C from -80% to $+80\%$. (a) At 100 Hz. (b) At 1 kHz. (c) At 10 kHz.

TABLE IX
PERFORMANCE TEST OF THE FILTER PARAMETER EXTRACTION MECHANISM

Component	L					C				
Actual value	2.05 μH					2.19 μF				
Initial value	1.60 μH	1.80 μH	2.00 μH	2.20 μH	2.40 μH	1.80 μF	2.00 μF	2.20 μF	2.40 μF	2.60 μF
Est. value	1.87 μH	1.90 μH	2.12 μH	2.11 μH	2.20 μH	1.85 μF	1.88 μF	1.91 μF	1.96 μF	2.02 μF
Error	−9%	−7%	3%	3%	7%	−15%	−14%	−12%	−10%	−7%
Mean square error	5.44%					11.95%				

values has been conducted. The results are given in Table IX. The mean square errors are found to be 5.44% for *L* and 11.95% for *C*. Although the testing method is different from the one proposed by the reviewer, the experiment described can also evaluate the performance of the parameter extraction algorithm. Further research will be dedicated to improving the estimation accuracy.

The sensitivity of the THD of the inverter output to the values of *L* and *C* has been studied by Monte Carlo analysis. An experiment to investigate the THDs at the reference frequencies of 100 Hz, 1 kHz, and 10 kHz while varying the values of *L* from -60% to $+80\%$ and *C* from -80% to $+80\%$ has been conducted. The results, given in Fig. 16, show the relationship between THD and the variations in *L* and *C*.

Within a $\pm 20\%$ variation in *L* and *C*, the THD remains below 0.4%. Within a $\pm 30\%$ variation in *L* and *C*, the THD remains below 2.1%. Thus, significant changes in the values of *L* and *C* have a minimal impact on the overall distortion of the inverter output.

VI. DISCUSSIONS AND CONCLUSION

The article introduces a state trajectory prediction algorithm for H-bridge inverters, using *h*-PWM. The algorithm predicts state trajectories for the whole switching cycle, enabling fast dynamic control and response. It can also assess the condition of the output filter and identify aging conditions, allowing for preventive maintenance. The algorithm was tested on a 1-kVA inverter prototype with results aligning with theoretical predictions. The following noteworthy points can also be highlighted.

1) The output frequency is twice the frequency of the gate signal, resulting in a smaller output filter being required to reduce output ripple.
2) A well-defined equation is derived to estimate the duty ratios of the switches in all patterns, which can be done with just a few multiplication and addition instructions on the controller.
3) The filter parameter estimation mechanism can estimate the values of *L* and *C* with an error of 10%. Further research will aim to improve the accuracy of this mechanism.

Wideband inverters offer the capability to generate both low- and high-frequency ac outputs, along with a rapid dynamic response. Notably, Lai et al. [33] and [34] discussed WSHVC, which can produce an output frequency range of 100 Hz to 10 kHz using mixed sine signal injection. Furthermore, LV124 and LV148 highlight the Automotive Test Standard, which encompasses frequency ranges from 10 Hz to 30 kHz, including dc step changes. Additionally, compliance with EN61000-4-11 requires the generation of ac voltage dips within microseconds, necessitating the use of wideband inverters.

To achieve a wide frequency range and rapid dynamic response, some specialized converters often utilize linear output regulators, which regulate mixed high-frequency signals. However, this approach necessitates additional power devices and digital signal processing resources, leading to an increase in circuit complexity and a decrease in overall efficiency. The proposed control architecture addresses this challenge by enabling the inverter to exhibit a fast dynamic response using a single stage of power conversion. The architecture requires minimal computational resources, making it well-suited for future controllers that operate with fast-switching devices, such as SiC and GaN devices.

APPENDIX

A. Derivation of (1) and (2)

The capacitor current and voltage for a specific time interval are estimated. Within the considered time interval, v_b is assumed to be constant. Thus

$$\frac{di_L}{dt} = \frac{v_b - v_c}{L} \tag{A1}$$

where i_L is the current through the filter inductor *L*.

Assume that the rate of change of the inductor current is equal to that of the capacitor current

$$\frac{di_C}{dt} \approx \frac{di_L}{dt} - \frac{di_{\text{Load}}}{dt} = \frac{v_b - v_c}{L}. \tag{A2}$$

Consider a time interval $[t_x, t_y]$. The capacitor current at t_y can be expressed as

$$\begin{aligned} \int_{i_C(t_x)}^{i_C(t_y)} di_C &= \int_{t_x}^{t_y} \frac{v_b - v_C}{L}\, dt \\ \Rightarrow \quad i_C\left(t_y\right) &= \left[\frac{v_b\left(t_x\right) - v_C\left(t_x\right)}{L}\right]\left(t_y - t_x\right) + i_C\left(t_x\right). \end{aligned} \tag{A3}$$

As

$$\int_{v_C(t_x)}^{v_C(t_y)} C\, dv_C = \int_{t_x}^{t_y} i_C\, dt. \tag{A4}$$

The capacitor voltage at t_y is obtained by substituting (1) and (2) into (4)

$$\begin{aligned} v_C(t_y) - v_C(t_x) &= \left[{i_C}^2(t_y) - {i_C}^2(t_x)\right] \\ &\quad \times \left[\frac{L}{2\,C\,\left(v_b(t_x) - v_C(t_x)\right)}\right] \\ \Rightarrow \qquad v_C(t_y) &= \left[\frac{v_b\,(t_x) - v_C\,(t_x)}{2\,C\,L}\right](t_y - t_x)^2 \\ &\quad + \frac{i_C\,(t_x)}{C}\,(t_y - t_x) + v_C(t_x). \end{aligned} \tag{A5}$$

Equations (1) and (2) depict the capacitor's current and voltage trajectory on the $i_C - v_C$ plane. The operations of patterns *P*, *N*, and *Z* are described below.

B. Derivation of (5)–(7) and (10)–(12)

The expected capacitor voltage v_C is predicting to reach v_{ref} after one switching period at *T*. Thus, $v_C(t_6)$ equals$v_{\mathrm{ref}}(t_0)$.

$$v_C\,(t_6) = v_{\mathrm{ref}}\,(t_0)\,. \tag{A6}$$

The capacitor voltage and current are measured at t_0. By putting the predicted values from a previous time interval as the initial values for the next time interval, the capacitor voltage and current at t_1 are expressed as

$$i_C\,(t_1) = \left[\frac{v_b\,(t_0) - v_C\,(t_0)}{L}\right](t_1 - t_0) + i_C\,(t_0) \tag{A7}$$

$$\begin{aligned} v_C(t_1) &= \left[\frac{v_b\,(t_0) - v_C\,(t_0)}{2\,C\,L}\right](t_1 - t_0)^2 \\ &\quad + \frac{i_C\,(t_0)}{C}\,(t_1 - t_0) + v_C(t_0). \end{aligned} \tag{A8}$$

At t_2

$$i_C\,(t_2) = \left[\frac{v_b\,(t_1) - v_C\,(t_1)}{L}\right](t_2 - t_1) + i_C\,(t_1) \tag{A9}$$

$$\begin{aligned} v_C(t_2) &= \left[\frac{v_b\,(t_1) - v_C\,(t_1)}{2\,C\,L}\right](t_2 - t_1)^2 \\ &\quad + \frac{i_C\,(t_1)}{C}\,(t_2 - t_1) + v_C(t_1). \end{aligned} \tag{A10}$$

At t_3

$$i_C\,(t_3) = \left[\frac{v_b\,(t_2) - v_C\,(t_2)}{L}\right](t_3 - t_2) + i_C\,(t_2) \tag{A11}$$

$$\begin{aligned} v_C(t_3) &= \left[\frac{v_b\,(t_2) - v_C\,(t_2)}{2\,C\,L}\right](t_3 - t_2)^2 \\ &\quad + \frac{i_C\,(t_2)}{C}\,(t_3 - t_2) + v_C(t_2). \end{aligned} \tag{A12}$$

At t_4

$$i_C\,(t_4) = \left[\frac{v_b\,(t_3) - v_C\,(t_3)}{L}\right](t_4 - t_3) + i_C\,(t_3) \tag{A13}$$

$$\begin{aligned} v_C(t_4) &= \left[\frac{v_b\,(t_3) - v_C\,(t_3)}{2\,C\,L}\right](t_4 - t_3)^2 \\ &\quad + \frac{i_C\,(t_3)}{C}\,(t_4 - t_3) + v_C(t_3). \end{aligned} \tag{A14}$$

At t_5

$$i_C\,(t_5) = \left[\frac{v_b\,(t_4) - v_C\,(t_4)}{L}\right](t_5 - t_4) + i_C\,(t_4) \tag{A15}$$

$$\begin{aligned} v_C(t_5) &= \left[\frac{v_b\,(t_4) - v_C\,(t_4)}{2\,C\,L}\right](t_5 - t_4)^2 \\ &\quad + \frac{i_C\,(t_4)}{C}\,(t_5 - t_4) + v_C(t_4). \end{aligned} \tag{A16}$$

At t_6

$$i_C\,(t_6) = \left[\frac{v_b\,(t_5) - v_C\,(t_5)}{L}\right](t_6 - t_5) + i_C\,(t_5) \tag{A17}$$

$$\begin{aligned} v_C(t_6) &= \left[\frac{v_b\,(t_5) - v_C\,(t_5)}{2\,C\,L}\right](t_6 - t_5)^2 \\ &\quad + \frac{i_C\,(t_5)}{C}\,(t_6 - t_5) + v_C(t_5). \end{aligned} \tag{A18}$$

By substituting (A7)–(A16) into (A17) and (A18)

Thus, the high-order components in (A19) and (A20) shown at the bottom of the next page are smaller than the low-order components. Hence, by substituting zero into the high-order components in (A19) and (A20), we get

In pattern *P*

$$v_b\,(t_1) = v_{\mathrm{dc}} \tag{A21}$$

and the duty ratio is expressed as

$$k = k_P. \tag{A22}$$

By substituting (A21) and (A22) into (A19) and (A20), (5)–(7) can be obtained.

In pattern *N*

$$v_b\,(t_1) = -v_{\mathrm{dc}} \tag{A23}$$

and the duty ratio is expressed as

$$k = k_N. \tag{A24}$$

By substituting (A23) and (A24) into (A19) and (A20), (10)–(12) can be obtained.

C. Derivation of (26)–(29)

The expected capacitor voltage v_C is predicted to reach v_{ref} after one switching period at *T*. Thus, the following equation holds:

$$v_C\,(t_6) = v_{\mathrm{ref}}\,(t_0)\,. \tag{A25}$$

The capacitor voltage and current are measured at t_0. By putting the predicted values from a previous time interval as the initial values for the next time interval, the capacitor voltage and current at t_1 are expressed as

$$i_C\left(t_1\right)=\left[\frac{v_b\left(t_0\right)-v_C\left(t_0\right)}{L}\right]\left(t_1-t_0\right)+i_C\left(t_0\right) \tag{A26}$$

$$\begin{aligned} v_C(t_1)= & \left[\frac{v_b\left(t_0\right)-v_C\left(t_0\right)}{2\ C\ L}\right]\left(t_1-t_0\right)^2 \\ & +\frac{i_C\left(t_0\right)}{C}\left(t_1-t_0\right)+v_C(t_0). \end{aligned} \tag{A27}$$

At t_2

$$i_C\left(t_2\right)=\left[\frac{v_b\left(t_1\right)-v_C\left(t_1\right)}{L}\right]\left(t_2-t_1\right)+i_C\left(t_1\right) \tag{A28}$$

$$\begin{aligned} v_C(t_2)= & \left[\frac{v_b\left(t_1\right)-v_C\left(t_1\right)}{2\ C\ L}\right]\left(t_2-t_1\right)^2 \\ & +\frac{i_C\left(t_1\right)}{C}\left(t_2-t_1\right)+v_C(t_1). \end{aligned} \tag{A29}$$

At t_3

$$i_C\left(t_3\right)=\left[\frac{v_b\left(t_2\right)-v_C\left(t_2\right)}{L}\right]\left(t_3-t_2\right)+i_C\left(t_2\right) \tag{A30}$$

$$\begin{aligned} v_C(t_3)= & \left[\frac{v_b\left(t_2\right)-v_C\left(t_2\right)}{2\ C\ L}\right]\left(t_3-t_2\right)^2 \\ & +\frac{i_C\left(t_2\right)}{C}\left(t_3-t_2\right)+v_C(t_2). \end{aligned} \tag{A31}$$

At t_4

$$i_C\left(t_4\right)=\left[\frac{v_b\left(t_3\right)-v_C\left(t_3\right)}{L}\right]\left(t_4-t_3\right)+i_C\left(t_3\right) \tag{A32}$$

$$v_C(t_4)=\left[\frac{v_b\left(t_3\right)-v_C\left(t_3\right)}{2\ C\ L}\right]\left(t_4-t_3\right)^2$$

$$\begin{aligned} i_C\left(t_6\right)= & \, i_C\left(t_0\right)\left(\underbrace{\begin{array}{l} \frac{k^8T^8}{32C^4L^4}-\frac{k^7T^8}{16C^4L^4}+\frac{3k^6T^8}{64C^4L^4}-\frac{k^5T^8}{64C^4L^4}+\frac{k^4T^8}{512C^4L^4}+\frac{5k^6T^6}{16C^3L^3}-\frac{7k^5T^6}{16C^3L^3}+\frac{11k^4T^6}{64C^3L^3}-\frac{k^2T^6}{128C^3L^3} \\ +\frac{9k^4T^4}{8C^2L^2}-\frac{k^3T^4}{C^2L^2}+\frac{k^2T^4}{16C^2L^2}+\frac{kT^4}{16C^2L^2}+\frac{T^4}{128C^2L^2}+\frac{7k^2T^2}{4CL}-\frac{3kT^2}{4CL}-\frac{5T^2}{16CL} \end{array}}_{\text{high order}}\underbrace{+1}_{\text{low order}}\right) \\ & +v_C\left(t_0\right)\left(\underbrace{\begin{array}{l} \frac{k^9T^9}{128C^4L^5}-\frac{5k^8T^9}{256C^4L^5}+\frac{5k^7T^9}{256C^4L^5}-\frac{5k^6T^9}{512C^4L^5}+\frac{5k^5T^9}{2048C^4L^5}-\frac{k^4T^9}{4096C^4L^5}+\frac{3k^7T^7}{64C^3L^4}-\frac{15k^6T^7}{128C^3L^4} \\ +\frac{25k^5T^7}{256C^3L^4}-\frac{15k^4T^7}{512C^3L^4}+\frac{k^2T^7}{1024C^3L^4}+\frac{3k^5T^5}{32C^2L^3}-\frac{23k^4T^5}{64C^2L^3}+\frac{17k^3T^5}{64C^2L^3}-\frac{k^2T^5}{32C^2L^3}-\frac{5kT^5}{512C^2L^3} \\ -\frac{T^5}{1024C^2L^3}+\frac{k^3T^3}{16CL^2}-\frac{23k^2T^3}{32CL^2}+\frac{19kT^3}{64CL^2}+\frac{11T^3}{128CL^2} \end{array}}_{\text{high order}}\underbrace{-\frac{T}{L}}_{\text{low order}}\right) \\ & +v_b\left(t_1\right)\left(\underbrace{\begin{array}{l} \frac{k^7T^7}{16C^3L^4}-\frac{3k^6T^7}{32C^3L^4}+\frac{3k^5T^7}{64C^3L^4}-\frac{k^4T^7}{128C^3L^4}+\frac{k^5T^5}{2C^2L^3}-\frac{k^4T^5}{2C^2L^3}+\frac{3k^3T^5}{32C^2L^3}+\frac{k^2T^5}{64C^2L^3} \\ +\frac{3k^3T^3}{2CL^2}-\frac{3k^2T^3}{4CL^2}-\frac{kT^3}{8CL^2} \end{array}}_{\text{high order}}\underbrace{+\frac{2kT}{L}}_{\text{low order}}\right). \end{aligned} \tag{A19}$$

$$\begin{aligned} v_C\left(t_6\right)= & \, i_C\left(t_0\right)\left(\underbrace{\begin{array}{l} -\frac{k^9T^9}{128C^5L^4}+\frac{5k^8T^9}{256C^5L^4}-\frac{5k^7T^9}{256C^5L^4}+\frac{5k^6T^9}{512C^5L^4}-\frac{5k^5T^9}{2048C^5L^4}+\frac{k^4T^9}{4096C^5L^4}-\frac{3k^7T^7}{64C^4L^3} \\ +\frac{15k^6T^7}{128C^4L^3}-\frac{25k^5T^7}{256C^4L^3}+\frac{15k^4T^7}{512C^4L^3}-\frac{k^2T^7}{1024C^4L^3}-\frac{3k^5T^5}{32C^3L^2}+\frac{23k^4T^5}{64C^3L^2}-\frac{17k^3T^5}{64C^3L^2} \\ +\frac{k^2T^5}{32C^3L^2}+\frac{5kT^5}{512C^3L^2}+\frac{T^5}{1024C^3L^2}-\frac{k^3T^3}{16C^2L}+\frac{23k^2T^3}{32C^2L}-\frac{19kT^3}{64C^2L}-\frac{11T^3}{128C^2L} \end{array}}_{\text{high order}}\underbrace{+\frac{T}{C}}_{\text{low order}}\right) \\ & +v_C\left(t_0\right)\left(\underbrace{\begin{array}{l} -\frac{k^{10}T^{10}}{512C^5L^5}+\frac{3k^9T^{10}}{512C^5L^5}-\frac{15k^8T^{10}}{2048C^5L^5}+\frac{5k^7T^{10}}{1024C^5L^5}-\frac{15k^6T^{10}}{8192C^5L^5}+\frac{3k^5T^{10}}{8192C^5L^5} \\ -\frac{k^4T^{10}}{32768C^5L^5}-\frac{k^8T^8}{256C^4L^4}+\frac{3k^7T^8}{128C^4L^4}-\frac{9k^6T^8}{256C^4L^4}+\frac{11k^5T^8}{512C^4L^4}-\frac{21k^4T^8}{4096C^4L^4} \\ +\frac{k^2T^8}{8192C^4L^4}-\frac{k^6T^6}{128C^3L^3}+\frac{9k^5T^6}{128C^3L^3}-\frac{63k^4T^6}{512C^3L^3}+\frac{17k^3T^6}{256C^3L^3}-\frac{15k^2T^6}{2048C^3L^3} \\ -\frac{3kT^6}{2048C^3L^3}-\frac{T^6}{8192C^3L^3}+\frac{k^4T^4}{64C^2L^2}+\frac{3k^3T^4}{32C^2L^2}-\frac{29k^2T^4}{128C^2L^2}+\frac{11kT^4}{128C^2L^2}+\frac{17T^4}{1024C^2L^2} \end{array}}_{\text{high order}}\underbrace{-\frac{T^2}{2CL}+1}_{\text{low order}}\right) \\ & +v_b\left(t_1\right)\left(\underbrace{\begin{array}{l} -\frac{k^8T^8}{64C^4L^4}+\frac{k^7T^8}{32C^4L^4}-\frac{3k^6T^8}{128C^4L^4}+\frac{k^5T^8}{128C^4L^4}-\frac{k^4T^8}{1024C^4L^4}-\frac{k^6T^6}{16C^3L^3}+\frac{5k^5T^6}{32C^3L^3} \\ -\frac{13k^4T^6}{128C^3L^3}+\frac{k^3T^6}{64C^3L^3}+\frac{k^2T^6}{512C^3L^3}-\frac{k^4T^4}{8C^2L^2}+\frac{7k^3T^4}{16C^2L^2}-\frac{7k^2T^4}{32C^2L^2}-\frac{kT^4}{64C^2L^2} \end{array}}_{\text{high order}}\underbrace{+\frac{kT^2}{CL}}_{\text{low order}}\right) \end{aligned} \tag{A20}$$

$$+\frac{i_C\left(t_3\right)}{C}\left(t_4-t_3\right)+v_C(t_3). \tag{A33}$$

At t_5

$$i_C\left(t_5\right)=\left[\frac{v_b\left(t_4\right)-v_C\left(t_4\right)}{L}\right]\left(t_5-t_4\right)+i_C\left(t_4\right) \tag{A34}$$

$$\begin{aligned} v_C\left(t_5\right)=&\left[\frac{v_b\left(t_4\right)-v_C\left(t_4\right)}{2CL}\right]\left(t_5-t_4\right)^2\\ &+\frac{i_C\left(t_4\right)}{C}\left(t_5-t_4\right)+v_C\left(t_4\right). \end{aligned} \tag{A35}$$

At t_6

$$i_C\left(t_6\right)=\left[\frac{v_b\left(t_5\right)-v_C\left(t_5\right)}{L}\right]\left(t_6-t_5\right)+i_C\left(t_5\right) \tag{A36}$$

$$\begin{aligned} v_C(t_6)=&\left[\frac{v_b\left(t_5\right)-v_C\left(t_5\right)}{2\,C\,L}\right]\left(t_6-t_5\right)^2\\ &+\frac{i_C\left(t_5\right)}{C}\left(t_6-t_5\right)+v_C(t_5). \end{aligned} \tag{A37}$$

Substituting (A26)–(A35) into (A36) and (A37), the following equations can be obtained:

Thus, the high-order components in (A38) and (A39) shown at the bottom of this page, are smaller than the low-order

$$\begin{aligned} i_C\left(t_6\right)=i_C\left(t_0\right)&\left(\underbrace{\begin{aligned}&-\frac{49k^6T^8}{8192C^4L^4}+\frac{147k^5T^8}{65536C^4L^4}+\frac{441k^4T^8}{524288C^4L^4}-\frac{1127k^3T^8}{4194304C^4L^4}+\frac{147k^2T^8}{8388608C^4L^4}+\frac{k^6T^6}{16C^3L^3}\\ &-\frac{3k^5T^6}{128C^3L^3}-\frac{81k^4T^6}{2048C^3L^3}+\frac{43k^3T^6}{4096C^3L^3}-\frac{671k^2T^6}{262144C^3L^3}+\frac{497kT^6}{2097152C^3L^3}-\frac{147T^6}{4194304C^3L^3}\\ &+\frac{k^4T^4}{2C^2L^2}-\frac{k^3T^4}{8C^2L^2}-\frac{341k^2T^4}{2048C^2L^2}+\frac{357kT^4}{16384C^2L^2}+\frac{181T^4}{16384C^2L^2}+\frac{5k^2T^2}{4CL}-\frac{5kT^2}{32CL}-\frac{89T^2}{256CL}\end{aligned}}_{\text{high order}}\underbrace{+1}_{\text{low order}}\right)\\ +v_C\left(t_0\right)&\left(\underbrace{\begin{aligned}&-\frac{49k^7T^9}{32768C^4L^5}+\frac{343k^6T^9}{262144C^4L^5}-\frac{147k^5T^9}{2097152C^4L^5}-\frac{2891k^4T^9}{16777216C^4L^5}+\frac{637k^3T^9}{16777216C^4L^5}\\ &-\frac{147k^2T^9}{67108864C^4L^5}+\frac{k^7T^7}{64C^3L^4}-\frac{7k^6T^7}{512C^3L^4}-\frac{k^5T^7}{1024C^3L^4}+\frac{741k^4T^7}{65536C^3L^4}-\frac{2145k^3T^7}{1048576C^3L^4}\\ &+\frac{1515k^2T^7}{8388608C^3L^4}-\frac{175kT^7}{8388608C^3L^4}+\frac{147T^7}{33554432C^3L^4}+\frac{k^5T^5}{16C^2L^3}-\frac{41k^4T^5}{256C^2L^3}-\frac{163k^3T^5}{8192C^2L^3}\\ &+\frac{2151k^2T^5}{65536C^2L^3}-\frac{355kT^5}{131072C^2L^3}-\frac{1679T^5}{1048576C^2L^3}+\frac{k^3T^3}{16CL^2}-\frac{37k^2T^3}{64CL^2}-\frac{19kT^3}{1024CL^2}+\frac{861T^3}{8192CL^2}\end{aligned}}_{\text{high order}}\underbrace{-\frac{T}{L}}_{\text{low order}}\right)\\ +v_{\text{dc}}\left(t_0\right)&\left(\underbrace{\begin{aligned}&-\frac{49k^5T^7}{4096C^3L^4}-\frac{49k^4T^7}{32768C^3L^4}+\frac{245k^3T^7}{262144C^3L^4}-\frac{147k^2T^7}{2097152C^3L^4}+\frac{k^5T^5}{8C^2L^3}+\frac{k^4T^5}{64C^2L^3}\\ &-\frac{97k^3T^5}{2048C^2L^3}+\frac{201k^2T^5}{16384C^2L^3}+\frac{21kT^5}{32768C^2L^3}+\frac{k^3T^3}{CL^2}-\frac{23kT^3}{128CL^2}+\frac{3T^3}{2048CL^2}\end{aligned}}_{\text{high order}}\underbrace{+\frac{2kT}{L}-\frac{T}{8L}}_{\text{low order}}\right) \end{aligned} \tag{A38}$$

$$\begin{aligned} v_C\left(t_6\right)=i_C\left(t_0\right)&\left(\underbrace{\begin{aligned}&-\frac{49k^7T^9}{32768C^5L^4}+\frac{441k^5T^9}{1048576C^5L^4}+\frac{49k^4T^9}{4194304C^5L^4}-\frac{2793k^3T^9}{134217728C^5L^4}+\frac{441k^2T^9}{268435456C^5L^4}\\ &+\frac{k^7T^7}{64C^4L^3}-\frac{25k^5T^7}{4096C^4L^3}-\frac{561k^4T^7}{65536C^4L^3}+\frac{3203k^3T^7}{1048576C^4L^3}-\frac{869k^2T^7}{2097152C^4L^3}\\ &+\frac{903kT^7}{67108864C^4L^3}-\frac{441T^7}{134217728C^4L^3}+\frac{k^5T^5}{16C^3L^2}+\frac{31k^4T^5}{256C^3L^2}-\frac{739k^3T^5}{8192C^3L^2}-\frac{379k^2T^5}{32768C^3L^2}\\ &+\frac{1777kT^5}{524288C^3L^2}+\frac{197T^5}{131072C^3L^2}+\frac{k^3T^3}{16C^2L}+\frac{71k^2T^3}{128C^2L}-\frac{41kT^3}{256C^2L}-\frac{769T^3}{8192C^2L}\end{aligned}}_{\text{high order}}\underbrace{+\frac{T}{C}}_{\text{low order}}\right)\\ +v_C\left(t_0\right)&\left(\underbrace{\begin{aligned}&-\frac{49k^8T^{10}}{131072C^5L^5}+\frac{49k^7T^{10}}{262144C^5L^5}+\frac{441k^6T^{10}}{4194304C^5L^5}-\frac{833k^5T^{10}}{16777216C^5L^5}-\frac{3577k^4T^{10}}{536870912C^5L^5}\\ &+\frac{1617k^3T^{10}}{536870912C^5L^5}-\frac{441k^2T^{10}}{2147483648C^5L^5}+\frac{k^8T^8}{256C^4L^4}-\frac{k^7T^8}{512C^4L^4}-\frac{k^6T^8}{32768C^4L^4}\\ &+\frac{31k^5T^8}{262144C^4L^4}+\frac{9063k^4T^8}{4194304C^4L^4}-\frac{2281k^3T^8}{4194304C^4L^4}+\frac{10985k^2T^8}{268435456C^4L^4}\\ &-\frac{231kT^8}{268435456C^4L^4}+\frac{441T^8}{1073741824C^4L^4}-\frac{1585k^4T^6}{32768C^3L^3}-\frac{623kT^6}{1048576C^3L^3}\\ &-\frac{6997T^6}{33554432C^3L^3}+\frac{k^4T^4}{64C^2L^2}-\frac{k^3T^4}{256C^2L^2}-\frac{691k^2T^4}{4096C^2L^2}+\frac{173kT^4}{8192C^2L^2}+\frac{5361T^4}{262144C^2L^2}\end{aligned}}_{\text{high order}}\underbrace{+1-\frac{T^2}{2CL}}_{\text{low order}}\right)\\ +v_{\text{dc}}\left(t_0\right)&\left(\underbrace{\begin{aligned}&-\frac{49k^6T^8}{16384C^4L^4}-\frac{49k^5T^8}{32768C^4L^4}+\frac{49k^4T^8}{524288C^4L^4}+\frac{147k^3T^8}{2097152C^4L^4}-\frac{441k^2T^8}{67108864C^4L^4}\\ &+\frac{k^6T^6}{32C^3L^3}+\frac{k^5T^6}{64C^3L^3}+\frac{13k^4T^6}{8192C^3L^3}-\frac{339k^3T^6}{32768C^3L^3}+\frac{1177k^2T^6}{524288C^3L^3}\\ &+\frac{63kT^6}{1048576C^3L^3}+\frac{k^4T^4}{8C^2L^2}+\frac{31k^3T^4}{128C^2L^2}-\frac{35k^2T^4}{512C^2L^2}-\frac{205kT^4}{8192C^2L^2}+\frac{9T^4}{65536C^2L^2}\end{aligned}}_{\text{high order}}\underbrace{+\frac{kT^2}{CL}-\frac{T^2}{32CL}}_{\text{low order}}\right). \end{aligned} \tag{A39}$$

components. Hence, by substituting zero into the high-order components in (A38) and (A39), (26)–(27) can be obtained.

In pattern Z, the duty ratio is expressed as

$$k = k_{Z+}. \tag{A40}$$

By substituting (A40) into (A39), (28)–(29) can be obtained.

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