A Switching Oscillation Suppression Method With Clamping Function and Quantitative Design for SiC MOSFETs

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***Abstract*—SiC MOSFETs offer significant benefits for power electronics applications due to their material properties, including increased switching speeds, reduced switching losses, and improved power density. However, these benefits can also result in severe switching oscillation and electromagnetic interference in SiC MOSFETs, which can cause device breakdown or damage. In this article, an oscillation suppression method with clamping function and quantitative design is presented, which not only effectively clamps the drain-source voltage overshoot but also does not reduce the switching speed and increase the switching loss. First, the clamping circuit based on a double-pulse circuit is proposed and its operating principle is described. Then, in order to achieve full suppression of oscillation below the clamping capacitor voltage, the high-frequency equivalent circuit in the oscillation stage is derived and the snubber parameters are further quantitatively designed. Finally, an experimental platform is developed to verify the effectiveness of the proposed method. The experimental results show that the proposed method can effectively clamp the overshoot and suppress the switching oscillations, which will significantly improve the device application reliability.**

***Index Terms*—Clamping circuit, silicon carbide (SiC) MOSFET, snubber circuit, switching oscillation.**

I. Introduction

WIDE bandgap devices such as silicon carbide (SiC) devices are being considered as a promising device for power electronic conversion due to their excellent properties. Compared with silicon-based devices, SiC MOSFETs offer faster switching speeds, lower on-state resistance, and higher operation temperatures, which makes them widely used in electric vehicles, photovoltaic power generation, and smart grids [1], [2], [3]. However, the fast switching speed characteristic of SiC MOSFETs can cause turn-OFF voltage overshoot and oscillation problems, which will lead to serious electromagnetic interference issues and even device damage. The switching oscillation of the SiC MOSFETs is generated by the resonance of the device's parasitic capacitance with the power circuit's parasitic inductance during the turn-OFF transient. Combined with the large *dv/dt* and *di/dt* of SiC MOSFETs, the turn-OFF voltage overshoot will be even more severe [4], [5], [6]. Thus, the advanced techniques are expected to overcome switching oscillations.

Recently, many methods have been proposed to suppress the switching oscillations of SiC MOSFETs, which mainly include optimizing the printed circuit board (PCB) layout [7], [8], [9], using active gate driver (AGD) [10], [11], [12], [13], [14], [15], [16], [17], adding snubber or damping methods [18], [19], [20], [21], [22], [23], [24], [25], etc. Optimizing the PCB layout to reduce parasitic inductance is an effective method to reduce switching oscillations. However, due to device package limitations and PCB layout limitations in practice, it is very difficult to reduce these stray parameters.

The AGD design is also a good way to optimize switching transients and mitigate switching oscillations, which can improve device performance by controlling gate resistance, gate current, and gate voltage. Increasing the gate resistance to reduce the slew rate of *dv/dt* and *di/dt* is one of the simplest ways to mitigate switching oscillations, but this method usually slows down the switching speed of the device and increases switching losses [10], [11]. In [12], an AGD technique with variable gate resistance is proposed to minimize detrimental effects of parasitic inductance in layout. The voltage overshoot can be reduced to 10% of the dc-bus voltage. A quasi-zero switching technique for SiC MOSFETs by dynamically controlling the gate current is proposed in [15]. This AGD enables the coexistence of parasitic inductance in the inverter layout and load parasitic capacitance while reducing voltage overshoot and switching losses. In [16], the advantages of current source gate drivers are discussed, and the sensitivity of the parasitic and device parameters to the proposed method is explored. On this basis, a

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switched current source based AGD is designed and tested. In [17], a novel AGD with a multilevel gate driver of high-power SiC MOSFETs is presented. The proposed AGD can not only suppress the oscillation of the voltage but also attenuate the oscillation of the current induced by high switching speed and parasitic elements. Although the above-mentioned AGD method can suppress the switching oscillation of the device, its driver circuit and control method are relatively complex, which bring difficulties for practical application.

Adding appropriate damping or snubber to the circuit can also suppress the switching oscillations, such as adding ferrite beads or *RC* snubbers [2]. Inserting ferrite beads into the power circuit to suppress the turn-OFF oscillation of SiC MOSFETs is also a common method. Although this method is simple, it slightly increases the switching losses and has limited oscillation suppression effect [18], [19]. Adding the *RC* snubber to suppress switching oscillations is also a widely used method. In [20] and [21], the second-order design is used to roughly estimate the *RC* snubber parameters, and only a limited suppression effect can be obtained due to its simplification in the analysis. In [22] and [23], the third-order design technique for *RC* snubber circuits for the half-bridge configuration and the flyback converter has already been developed. In that technique, the characteristic equations of the high-frequency equivalent circuits are analyzed by using the root locus method. Furthermore, the higher-order *RC* design approach has been proposed to suppress false triggering oscillation of the gate-source voltage and sustained oscillation of the drain-source voltage [24], [25]. Although these *RC* snubber design methods can effectively suppress switching oscillations and are easy to implement, they will more or less increase switching losses. In addition to the above-mentioned methods, there is also a study to suppress the switching oscillations of SiC MOSFETs by using a clamping circuit [26]. However, the proposed clamping circuit requires additional inductor and the switching oscillations under clamping capacitor voltage cannot be suppressed. Based on the above-mentioned analysis, it can be summarized that the existing switching oscillation suppression methods mainly have the problems of complex driver design, limited suppression effect, and increased switching losses.

In this article, an oscillation suppression circuit with clamping function and quantitative design for SiC MOSFETs is proposed to suppress drain-source voltage overshoot, which can be applied to other bridge circuits such as buck/boost converters. The proposed method has the following advantages.

1) The proposed suppression method can effectively suppress the overshoot and oscillation of the drain-source voltage when the circuit parameters change.
2) The proposed oscillation suppression method mainly uses passive devices, which makes the circuit design relatively simple.
3) The proposed method does not require the addition of additional inductors and does not slow down the switching speed or increase the switching losses.

The rest of this article is organized as follows. In Section II, the clamping function and operation principle of the proposed method based on the double-pulse circuit is established. Section III presents the analysis and quantitative design of passive snubber parameter of the proposed method. In Section IV, experimental platforms are built to validate theoretical analysis. Finally, Section V concludes this article.

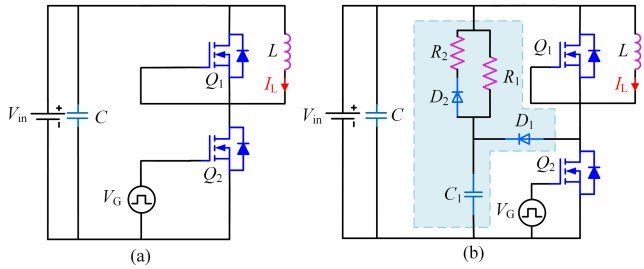

Fig. 1. (a) Schematic diagram of double-pulse circuit. (b) Proposed switching oscillation suppression method.

II. Clamping Function of the Proposed Oscillation Suppression Circuit and Its Operating Principle

The double-pulse circuit is taken as an example to study the switching oscillation suppression, as shown in Fig. 1(a). Q_1 is the inactive device, Q_2 is the active device and also the device under test. The current commutation occurs after Q_2 is turned OFF. The parasitic inductor of power circuit resonates with the parasitic capacitor of Q_2, thus causing switching oscillations. Fig. 1(b) shows the proposed switching oscillation suppression method with clamping function. It can be seen that the proposed method does not require additional controls in the driver and uses mainly passive components, including diodes D_1 and D_2, resistors R_1 and R_2, and capacitor C_1, which makes the oscillation suppression circuit very simple and cost effective.

A. Basic Operating Principle

1) Start-Up Process: When the power circuit is energized, the dc-bus voltage rises and the input voltage V_{in} charges capacitor C_1 through resistor R_1. It should be noted that the value of R_1 should be large enough to prevent it from participating in the circuit activity after the start-up process. Furthermore, this value is much larger than R_2.

2) Turn-off Process: Fig. 2 shows the basic operating principle of the proposed oscillation suppression circuit during the turn-OFF process, which can be divided into four stages. And the typical waveforms of the proposed method are shown in Fig. 3.

Stage 1 [$t_0 - t_1$; See Fig. 2(a)]: When the drive voltage of the device is under test Q_2 changes from high level to low level, and Q_2 is turned OFF. At this time, the voltage of capacitor C_1 remains constant and is equal to the input voltage V_{in}. During this period, the cathode voltage of diode D_1 is higher than the anode voltage, and the diode is reversely blocked. This process ends until the drive voltage drops to $V_{th} + I_L/g_m$. Here, V_{th}, g_m, and I_L represent threshold voltage of the device, transconductance, and load current, respectively.

Stage 2 [$t_1 - t_2$; See Fig. 2(b)]: Under the action of the drive circuit, the drain-source voltage v_{ds} of Q_2 rises gradually. At this time, the voltage across C_1 is still equal to the input voltage V_{in}, and the cathode voltage of diode D_1 is still higher than the

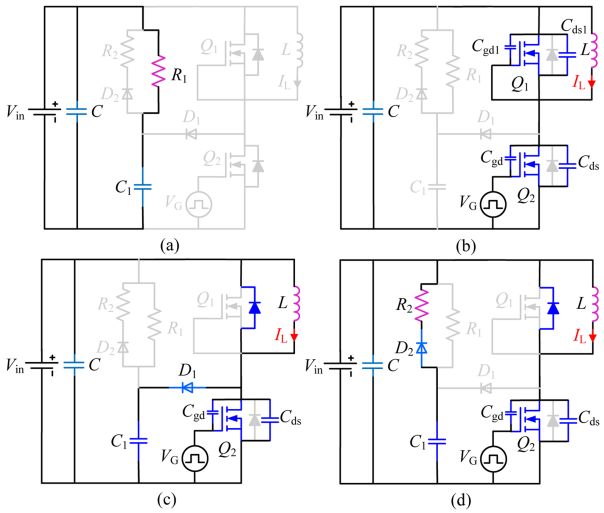

Fig. 2. Operation principle for each stage.

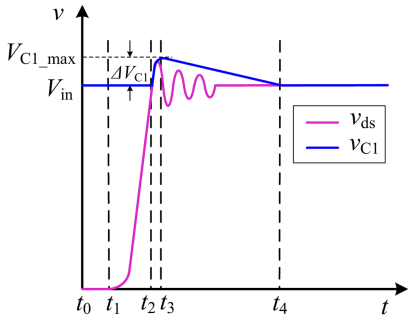

Fig. 3. Typical waveforms of the proposed clamping circuit.

anode voltage. Therefore, the diode D_1 is still reversely blocked until the drain-source voltage v_{ds} reaches the sum of v_{C1} and the voltage drop V_{D1} of diode D_1. Compared with the input voltage V_{in}, the voltage drop V_{D1} of diode D_1 is relatively small, which can be ignored for simplified analysis.

Stage 3 [t_2-t_3; See Fig. 2(c)]: When the drain-source voltage v_{ds} of Q_2 reaches the input voltage V_{in}, v_{ds} will continue to rise and oscillate due to the resonance of the power circuit parasitic inductance with the parasitic capacitance of the device Q_2. At this time, the anode voltage of diode D_1 is higher than the cathode voltage, diode D_1 will conduct forward and capacitor C_1 begins to clamp v_{ds}, which will suppress the overshoot and oscillation of v_{ds}. At this stage, the capacitor C_1 is in parallel with the drain-source capacitance C_{ds} of the Q_2. When the overshoot of v_{ds} charges the capacitor C_1, the clamping current i_{C1} will be generated, which will reduce the current flowing through the drain-source capacitance C_{ds} of Q_2. Usually, the capacitance C_1 is much larger than C_{ds}, the larger C_1 is, the more drain current flows to C_1, and the better the clamping effect.

Stage 4 [t_3-t_4; See Fig. 2(d)]: After the device Q_2 is fully turned OFF, the drain-source voltage v_{ds} of Q_2 drops to V_{in}. Since the clamping capacitor C_1 almost takes all the overshoot and oscillation energy, the voltage across the capacitor C_1 will be higher than the input voltage V_{in}, which will reach $V_{C1\cdot max}$, as shown in Fig. 3. At this time, the cathode voltage of diode D_1

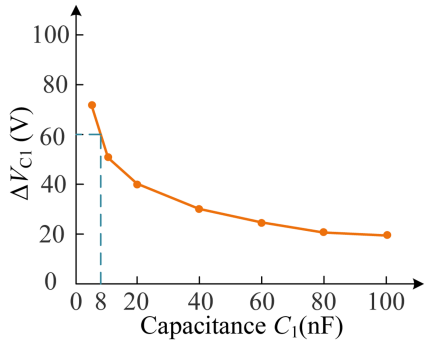

Fig. 4. Relationship between ΔV_{C1} and C_1.

will be higher than the anode voltage, which causes the diode to be blocked reversely. Since the resistance R_1 is much larger than R_2, the energy stored in C_1 will be released to the dc-bus side mainly through diode D_2 and resistor R_2, which will not affect the switching transient of the device. In this stage, the voltage of capacitor C_1 will gradually drop from $V_{C1\cdot max}$ and it can be seen that the switching oscillations under the clamping capacitor voltage cannot be suppressed. When v_{C1} drops to V_{in}, this period will end.

3) Turn-on Process: When Q_2 is turned ON, the drain-source voltage of Q_2 drops from the input voltage V_{in}, which will be lower than the voltage V_{in} of capacitor C_1. At this time, diode D_1 is always reversely blocked. Therefore, the proposed oscillation suppression method has no effect on the performance of the device during the turn-ON process.

B. Parameter Design

1) Capacitors C_1: The overshoot of drain-source voltage v_{ds} of Q_2 will be absorbed by the capacitor C_1 during the turn-OFF process, and the magnitude of the capacitor determines the maximum voltage of v_{C1}. In Fig. 3, ΔV_{C1} represents the difference between the maximum voltage of capacitor C_1 and the input voltage V_{in}, which determines the value at which the overshoot voltage of v_{ds} is finally clamped. Generally speaking, the larger C_1 is, the more current flows through C_1 when oscillation occurs, and the smaller ΔV_{C1} is the better the overshoot suppression effect. Fig. 4 illustrates the relationship between ΔV_{C1} and capacitance C_1. In order to clamp the voltage spikes of v_{ds} well, we set the value of ΔV_{C1} less than 60 V and C_1 should be greater than 8 nF according to Fig. 4. In addition, according to Fig. 2(d), the energy stored in C_1 needs to be released to the dc-bus side through R_2 within one switching cycle, and a large C_1 will cause a long discharge time.

2) Resistors R_1 and R_2: As mentioned earlier, the resistor R_1 should be relatively large to prevent it from participating in the circuit activity after the start-up process. The maximum ΔV_{C1} is designed to be 60 V; thus, the maximum voltage across R_1 is 60 V.

$$i_1 = \Delta V_{C1}/R_1. \tag{1}$$

Here, $i_1 < 20$ mA is set, so we can get $R_1 > 3$ kΩ.

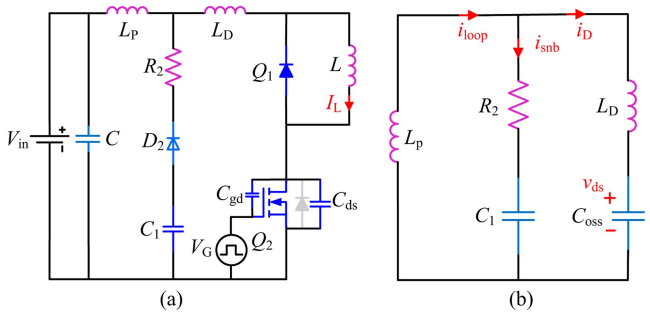

Fig. 5. (a) Circuit diagram of Fig. 2(d) after considering the parasitic parameters of the circuit. (b) Simplified high-frequency equivalent circuit diagram.

Since R_1 is much larger than R_2, the energy stored on C_1 is released to the dc-bus side mainly through D_2 and R_2. The discharge time t_{dis} is the time for the voltage v_{C1} on C_1 to drop from $V_{C1\cdot max}$ to the input voltage V_{in}, which is mainly determined by the time constant τ of C_1 and R_2. A large R_2 will have a large RC time constant τ, which will not ensure that the energy stored in C_1 is fully released within one switching cycle. In order for the stored energy to be fully released, a time constant τ of 5 times is usually set.

$$t_1 = 5 \times C_1 \times R_2. \tag{2}$$

Here, we set the release time $t_1 < 2\ \mu s$, so $R_2 < 50\ \Omega$ can be obtained.

III. Analysis and Quantitative Design of Passive Snubber Parameter of the Proposed Method

A. Establishment and Derivation of Circuit Models

In Section II, the proposed method achieves the clamping suppression of switching overshoot for the SiC MOSFET. However, the above-mentioned design mainly reduces the oscillation spike and does not fully suppress the switching oscillation from t_3 to t_4, as shown in Fig. 3. In order to fully suppress this switching oscillation, this section will further quantify the parameters R_2 and C_1. During the switching oscillation stage (stage 4 in Fig. 3), the equivalent circuit is shown in Fig. 2(d), which can be seen as adding an RC snubber circuit across the dc-bus side. After considering the circuit parasitic parameters, Fig. 2(d) can be replaced by Fig. 5(a).

In order to obtain the high-frequency equivalent circuit diagram of Fig. 5(a), the following assumptions are made.

1) Due to the large inductance of the load inductor L, its high-frequency impedance is much larger than impedance of other parasitic parameters. Therefore, the load inductor can be considered as an open circuit.
2) The decoupling capacitor C can be regarded as a shorted circuit due to its large capacitance, and its high frequency impedance is much smaller than impedance of other parasitic parameters.
3) Q_1 is equivalent to a diode at this time and the inductor current I_L flows through this body diode, the voltage drops of both Q_1 and diode D_2 can be ignored.

TABLE I
Definitions of the Symbols

Symbol	Description
L_P	Parasitic inductance of busbars
L_D	Parasitic inductance between upper and lower device
C_{oss}	Output capacitance of Q_2
i_D	Output capacitance current of Q_2
i_{loop}	Current of busbar
i_{snb}	Current of snubber circuit

4) When the switching oscillation occurs, the device Q_2 is completely turned OFF. Therefore, device Q_2 can be equivalent to the output capacitor C_{oss} at this time.

Based on the above-mentioned assumptions, the simplified high-frequency equivalent circuit diagram is shown in Fig. 5(b), and the definitions of the main symbols in Fig. 5(b) are shown in Table I.

According to KCL and KVL, the following equations can be obtained from Fig. 5(b):

$$i_{loop} = i_{snb} + i_D \tag{3}$$

$$C_{oss}\frac{dv_{ds}}{dt} = i_D \tag{4}$$

$$L_p\frac{di_{loop}}{dt} + i_{snb}R_2 + \frac{1}{C_1}\int i_{snb}dt = 0 \tag{5}$$

$$L_p\frac{di_{loop}}{dt} + L_D\frac{di_D}{dt} + v_{ds} = 0. \tag{6}$$

The values of R_2 and C_1 are determined to suppress the switching oscillation of v_{ds}. Therefore, we perform the Laplace transform on the above-mentioned equations and the s-domain equation of v_{ds} is deduced out. The initial condition of the above-mentioned variable is $i_{loop}(0) = i_D(0) = I_0$, $i_{snb}(0) = 0$, $v_{ds}(0) = 0$. The following equations can be obtained from (3) to (6):

$$i_{loop}(s) = i_{snb}(s) + i_D(s) \tag{7}$$

$$i_D(s) = sC_{oss}v_{ds}(s) \tag{8}$$

$$L_p(si_{loop}(s) - I_0) + i_{snb}(s)R_2 + \frac{1}{sC_1}i_{snb}(s) = 0 \tag{9}$$

$$L_p(si_{loop}(s) - I_0) + L_D(si_D(s) - I_0) + v_{ds}(s) = 0 \tag{10}$$

where $i_{loop}(s)$, $i_D(s)$, $i_{snb}(s)$, and $v_{ds}(s)$ are defined as the Laplace transform of $i_{loop}(t)$, $i_D(t)$, $i_{snb}(t)$, and $v_{ds}(t)$, respectively.

According to (7)–(10), the following expression of v_{ds} is then derived as follows:

$$v_{ds}(s) = \frac{N(s)}{M(s)} = \frac{a_0s^2 + a_1s + a_2}{b_0s^4 + b_1s^3 + b_2s^2 + b_3s + b_4} \tag{11}$$

where b_i ($i = 0, 1, 2, 3, 4$) and a_j ($j = 0, 1, 2$) are coefficients listed in the Appendix. It can be seen that this is a fourth-order system.

B. Quantitative Design of Passive Snubber Parameters

Based on the above-mentioned analysis, the RC parameter values can be derived as s-domain functions according to (11).

TABLE II
KEY CIRCUIT PARAMETERS

Symbol	Values
L_P	62 nH
L_D	15.8 nH
C_{oss}	0.1 nF

In order to suppress the switching oscillations of v_{ds}, we need to study the characteristic equation $M(s) = 0$ of v_{ds}. When all the solutions of the characteristic equation $M(s) = 0$ are negative real numbers, the damping ratio is 1 and v_{ds} has no oscillating term, then the switching oscillations can be fully suppressed. When $M(s)$ is a third-order polynomial, the three solutions are either real numbers or a combination of a real number and two complex conjugate solutions. Thus, R_2 and C_1 determined by simultaneously solving for $dM(s)/ds = 0$ and $M(s) = 0$ can guarantee to have no oscillation terms [27]. However, it cannot guarantee that all solutions of the characteristic equation above third order are negative real numbers [22].

This article uses the root locus method to design the snubber parameters R_2 and C_1. Considering C_1 as a variable, we rearrange (11) as follows:

$$M(s) = P + C_1 Q = 0. \tag{12}$$

Transforming (12) into the following form:

$$M_1(s) = 1 + \frac{C_1 Q}{P} = 0 \tag{13}$$

where the coefficients Q and P are shown in the Appendix.

By changing the value of the capacitance C_1 from zero to infinity according to C_1Q/P, the root locus of the characteristic equation $M(s) = 0$ can be obtained. Some important circuit parameters are shown in Table II, which are obtained based on the parameters of our experimental platform. The inductances mainly include device parasitic inductance and PCB parasitic inductance, which are mainly obtained through the LTspice model of the device and ANSYS Q3D software, respectively. The device parasitic capacitance is mainly obtained through the device datasheet.

Fig. 6 shows the root locus diagram of the characteristic equation $M(s) = 0$ when R_2 is equal to 5 Ω. It can be seen that the characteristic equation $M(s) = 0$ is a fourth-order polynomial and that there exist four poles, that is, four solutions. When the *RC* snubber circuit is added, the root locus of the characteristic equation moves towards the left half plane of s, that switching oscillation tends to be suppressed. As mentioned earlier, it is difficult to satisfy that all solutions are real when the order of the equation is greater than three. When C_1 changes from 0 to infinity, the characteristic equation $M(s) = 0$ has two equal real solutions at the location of the breakaway point and a pair of complex conjugate solutions. And p_{r1}, p_{r1}^* are much closer to the imaginary axis than p_{r2}, p_{r2}^*, therefore, p_{r1}, p_{r1}^* are the two dominant poles. In practical engineering, when the other poles are three to six times farther away from the imaginary axis than the dominant pole, its effect on the system performance

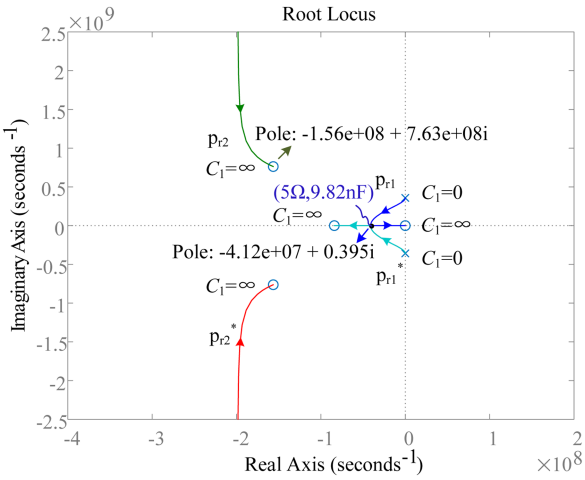

Fig. 6. Root locus diagram of $M(s) = 0$ for parameter C_1 ($R_2 = 5$ Ω).

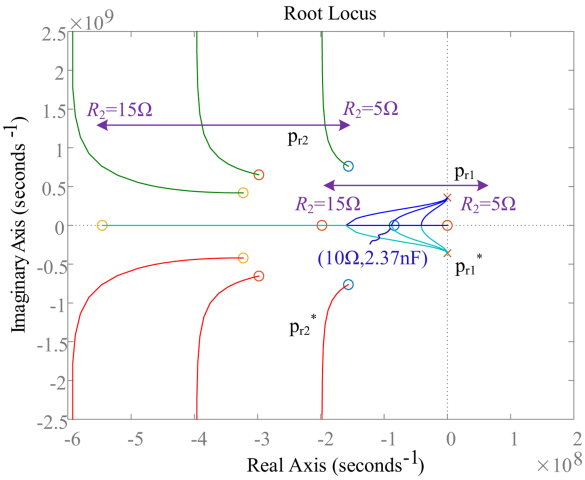

Fig. 7. Root locus diagram of $M(s) = 0$ for parameter C_1 (R_2 changes from 5 to 15 Ω).

can be ignored according to automatic control theory [28]. It can be seen from Fig. 6 that the distance between the poles p_{r1} and p_{r2} satisfies the above-mentioned condition, thus the effect of p_{r2} and p_{r2}^* on the system performance can be neglected. Accordingly, we only need to make the damping ratio of p_{r1} and p_{r1}^* as large as possible to achieve good oscillation suppression. When $R_2 = 5$ Ω, if C_1>9.82 nF, p_{r1}, p_{r1}^* are negative real numbers and the damping ratio is 1, and switching oscillations will be fully suppressed.

Fig. 7 illustrates the root locus diagram of the characteristic equation $M(s) = 0$ when R_2 changes from 5 to 15 Ω. It can be seen that as C_1 varies from 0 to infinity, the poles p_{r2} and p_{r2}^* are always nondominant and their effect on the system performance is negligible. Therefore, we still only need to design the damping ratio of poles p_{r1} and p_{r1}^* to achieve good oscillation suppression. The dominant poles p_{r1} and p_{r1}^* are always at the breakaway point that satisfies the two negative real numbers according to Fig. 7. Taking R_2 equal to 10 Ω as an example, when $C_1 >$ 2.37 nF, then the damping ratio is 1 and the switching oscillation can be fully suppressed.

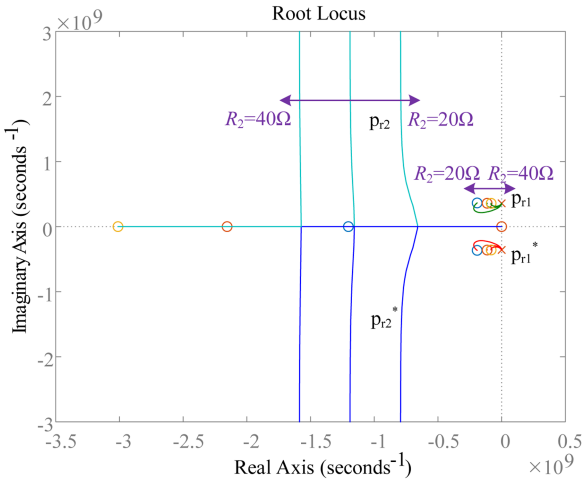

Fig. 8. Root locus diagram of $M(s) = 0$ for parameter C_1 (R_2 changes from 20 to 40 Ω).

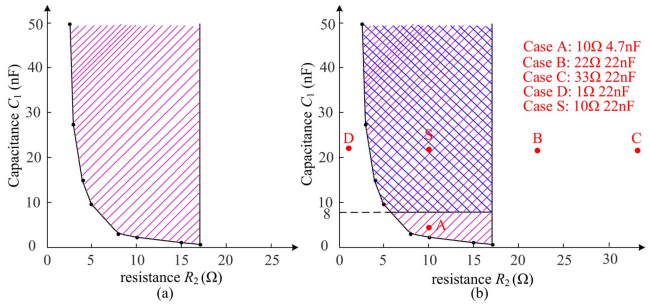

Fig. 9. R_2-C_1 region where the switching oscillation is considered to be fully suppressed. (a) Full suppression region without clamping design range. (b) Full suppression region with clamping design range.

When R_2 changes from 20 to 40 Ω, the root locus diagram of the characteristic equation $M(s) = 0$ is shown in Fig. 8. It can be seen that p_{r1} and p_{r1}^* are still the dominant poles. When C_1 changes from 0 to infinity, although there are negative real solutions for p_{r2} and p_{r2}^* at the breakaway point, the dominant poles p_{r1} and p_{r1}^* always have oscillation terms. Therefore, the switching oscillation cannot be fully suppressed and these design values need to be excluded.

Based on the above-mentioned analytical method, we can also obtain the range of C_1 values at other R_2 values. The R_2-C_1 design region that can fully suppress switching oscillation is shown in Fig. 9(a). In Section II, according to the parametric design of the clamping circuit, R_2<50 Ω and C_1>8 nF are obtained. Combined with the full suppression region of Fig. 9(a), the final R_2-C_1 design region is shown in the overlapping region of Fig. 9(b).

IV. Experimental Verification

To validate the effectiveness of the proposed method, a double-pulse experimental platform is built, as shown in Fig. 10(a), and the comprehensive comparisons are made. The main parameters of the experimental platform are shown in Table III. The SiC MOSFET device is the C2M0080120D manufactured by CREE. D_1 and D_2 are selected as SiC Schottky

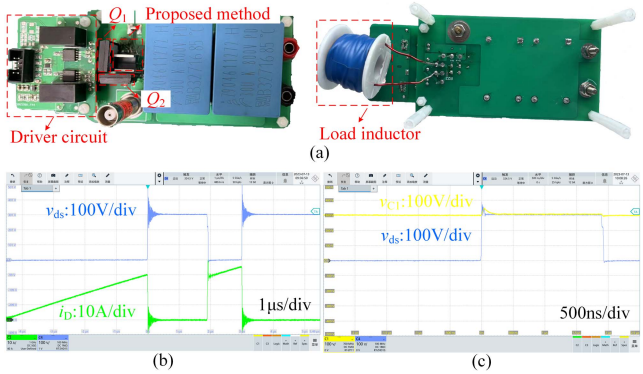

Fig. 10. (a) Experimental platform (front and back). (b) Double-pulse waveforms under the normal situations. (c) Experimental waveforms of v_{ds} and v_{C1} using the proposed method.

TABLE III
Prototype Parameters

Symbol	Values
Input voltage V_{in}	300 V
Inductor current I_L	30 A
Driver resistor R_G	10 Ω
Driver voltage V_G	20 V/−5 V
Start-up resistor R_1	3.9 kΩ

barrier diode (SBD) C4D10120A and Si fast recovery diode (FRD) IDP30E120, respectively, to explore their influence on the oscillation suppression effect. In order to measure the switching current accurately, a coaxial current shunt (named SSDN-10) manufactured by T&M Research Products, Inc., is adopted, which has a bandwidth of 2 GHz. The oscilloscope is MXO44 with a bandwidth of 1 GHz. Fig. 10(b) shows the double-pulse waveforms under normal situations, and the waveforms of the drain-source voltage v_{ds} and the clamping capacitor voltage v_{C1} after applying the proposed method in this article are shown in Fig. 10(c). It can be seen that the proposed clamping method can effectively suppress the switching oscillation.

To further verify the effect of oscillation suppression in the R_2-C_1 quantitative design region, values within and outside the R_2-C_1 design region are examined. In the R_2-C_1 design region, R_2 and C_1 are chosen to be 10 Ω and 22 nF, respectively, which is case S in Fig. 9(b). The R_2-C_1 values selected outside the design region are also shown in Fig. 9(b), which mainly include case A (10 Ω, 4.7 nF), case B (22 Ω, 22 nF), case C (33 Ω, 22 nF), and case D (1 Ω, 22 nF).

Fig. 11 shows the comparison of experimental results using SiC SBD within and outside the R_2-C_1 design region, where v_{C1} is the experimental waveform measured at case S. It can be seen that the switching oscillation spike of SiC MOSFET in normal situations is close to 500 V. When the proposed clamping method is adopted, the switching oscillation spike is significantly reduced, which proves the effectiveness of the proposed method. In stage 4, it can be seen that cases A, B, and C have a larger oscillation amplitude compared with case S. For case D, it will appear the low frequency resonance, that will have longer oscillation time. As a result, the oscillation suppression is not as effective as in the design region.

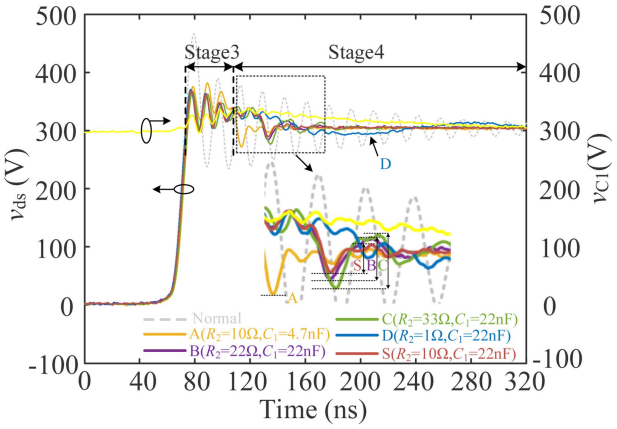

Fig. 11. Comparison of experimental results using SiC SBD within and outside the R_2-C_1 design region.

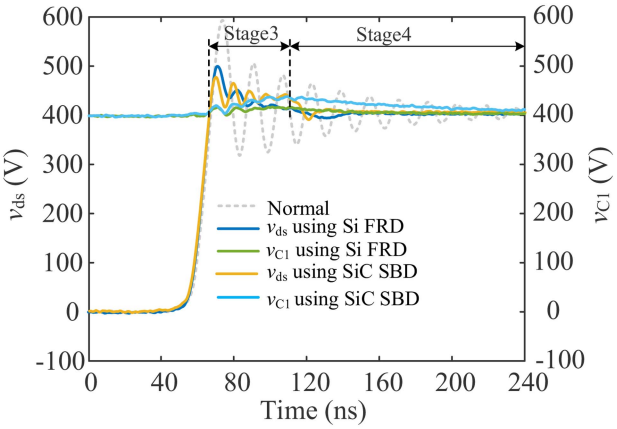

Fig. 12. Experimental waveform comparisons for the normal situation and the proposed method (using Si FRD and SiC SBD, respectively).

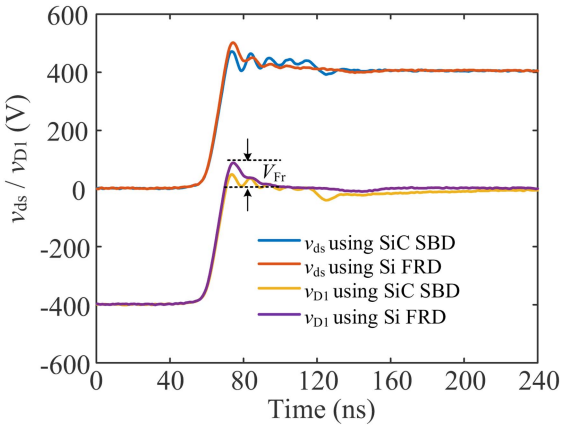

Fig. 13. Experimental waveforms of v_{ds} and v_{D1} using SiC SBD and Si FRD, respectively.

It is worth noting that after v_{ds} rises to the input voltage V_{in}, v_{ds} should rise smoothly with the clamping capacitor voltage v_{C1} in the process of continuing to rise to $V_{C1\cdot max}$ according to Fig. 3. However, in practice, v_{ds} occurs slight oscillation when v_{C1} rises from V_{in} to $V_{C1\cdot max}$, as shown in stage 3 of Fig. 11. In order to explore the cause of this oscillation, we also choose 1200 V Si FRD IDP30E120 to carry out the related experimental investigation. Fig. 12 shows the experimental waveform comparisons for the normal situation and the proposed method (using Si FRD and SiC SBD, respectively). It can be seen that compared with the normal situation, v_{ds} oscillation spikes using Si FRD are slightly higher than that of SiC SBD, but it still has a good oscillation suppression effect. In stage 3, D_1 starts to conduct when v_{ds} rises to the input voltage V_{in}. Due to the diode lead inductance and dynamic on-state resistance, D_1 will have a forward recovery process, that will result in a large forward bias voltage V_{Fr} and it is much larger than the forward conduction voltage drops, as shown in Fig. 13 [29], [30]. As a result, v_{ds} will exceed the clamping capacitor voltage v_{C1} in stage 3. Since SiC SBD has a faster forward recovery process compared with Si FRD, its forward bias voltage V_{Fr} is usually smaller, resulting in a smaller voltage spike in v_{ds} of Q_2, as shown in Fig. 13. Accordingly, the fast forward recovery process of the SiC SBD will also cause the overshoot of v_{ds} to charge C_1 more, that will make $v_{C1\cdot max}$ larger compared with Si FRD, as shown in Fig. 12. In addition, v_{ds} will also oscillate slightly in stage 3 due to the lead inductance of diode D_1. Although v_{ds} oscillation spikes using Si FRD are slightly higher than that of SiC SBD, it still has a good oscillation suppression effect. Therefore, we recommend the selection of Si FRD as clamping diodes from the cost-saving perspective. Furthermore, although different types of diodes have different forward recovery characteristics, which may cause a slight difference in the final oscillation suppression effect, it still has a good oscillation suppression effect. The large forward bias voltage V_{Fr} of the diode may cause a slightly larger oscillation spike in v_{ds}, as shown in Fig. 13. Therefore, in practical engineering, in order to obtain the better oscillation suppression effect, a diode with a small forward bias voltage V_{Fr} can be selected while considering the cost.

Fig. 14 shows the experimental waveform comparisons among the proposed oscillation suppression method, the *RC* method, and the normal situation when the gate resistance R_G is 10 Ω and the load current I_L is 30 A. It can be seen that when the input voltage changes from 400 to 800 V, the proposed method still enables the switching oscillation spikes to be reduced significantly compared with the normal situation. In addition, compared with the conventional *RC* design method, when the *RC* is designed quantitatively, although the switching oscillations of the device can be fully suppressed, the oscillation spikes are not reduced much compared with the normal situation. The proposed method effectively reduces the switching oscillation spikes of the device compared with the normal method and the *RC* method according to Fig. 14. And the proposed method does not affect the turn-ON and turn-OFF speeds of the device, which will not increase the switching loss of the device.

Fig. 15 shows the experimental waveform comparisons between the proposed oscillation suppression method and the normal situation when the input voltage V_{in} is 300 V and the load current I_L is 30 A. It can be seen that the higher the gate resistance, the smaller the switching oscillation spike. Although

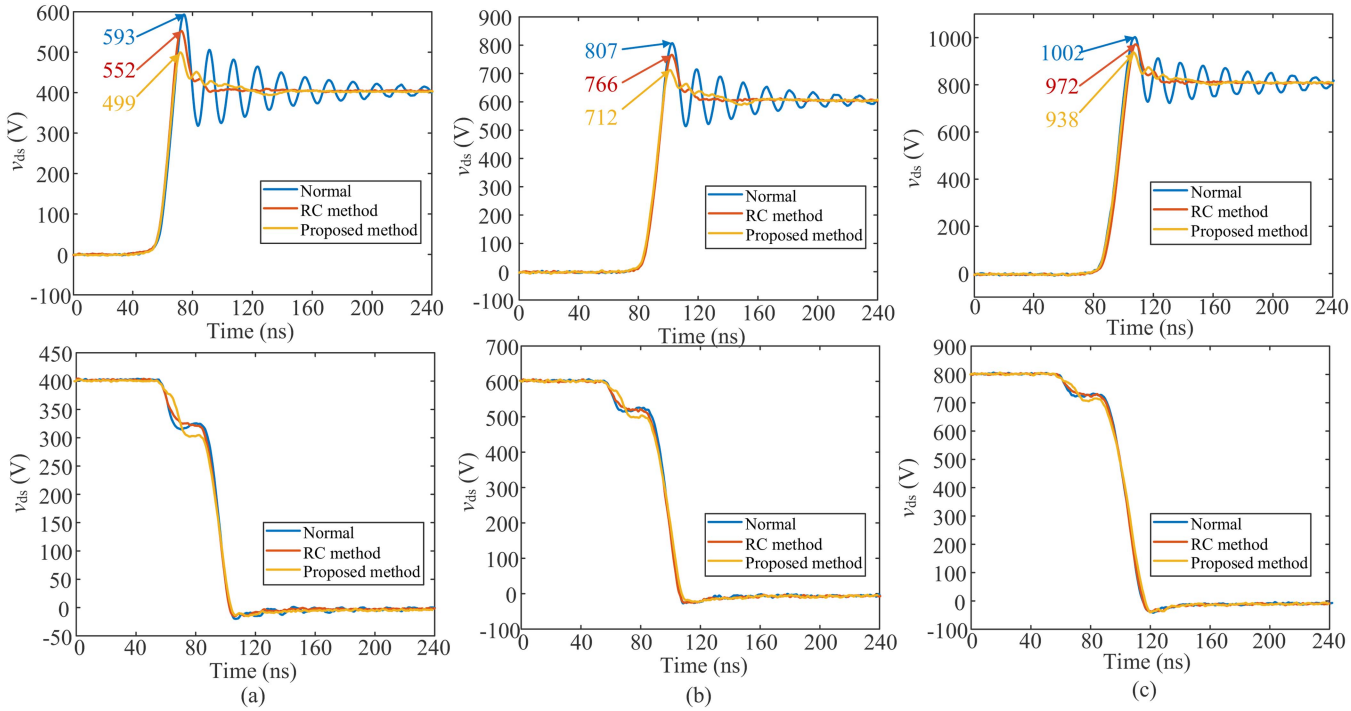

Fig. 14. Experimental waveform comparisons among the proposed method, the *RC* method, and the normal situation ($I_{\mathrm{L}} = 30$ A, $R_{\mathrm{G}} = 10\ \Omega$). (a) $V_{\mathrm{in}} = 400$ V. (b) $V_{\mathrm{in}} = 600$ V. (c) $V_{\mathrm{in}} = 800$ V. (Figures above are turn-OFF processes and figures below are turn-ON processes.).

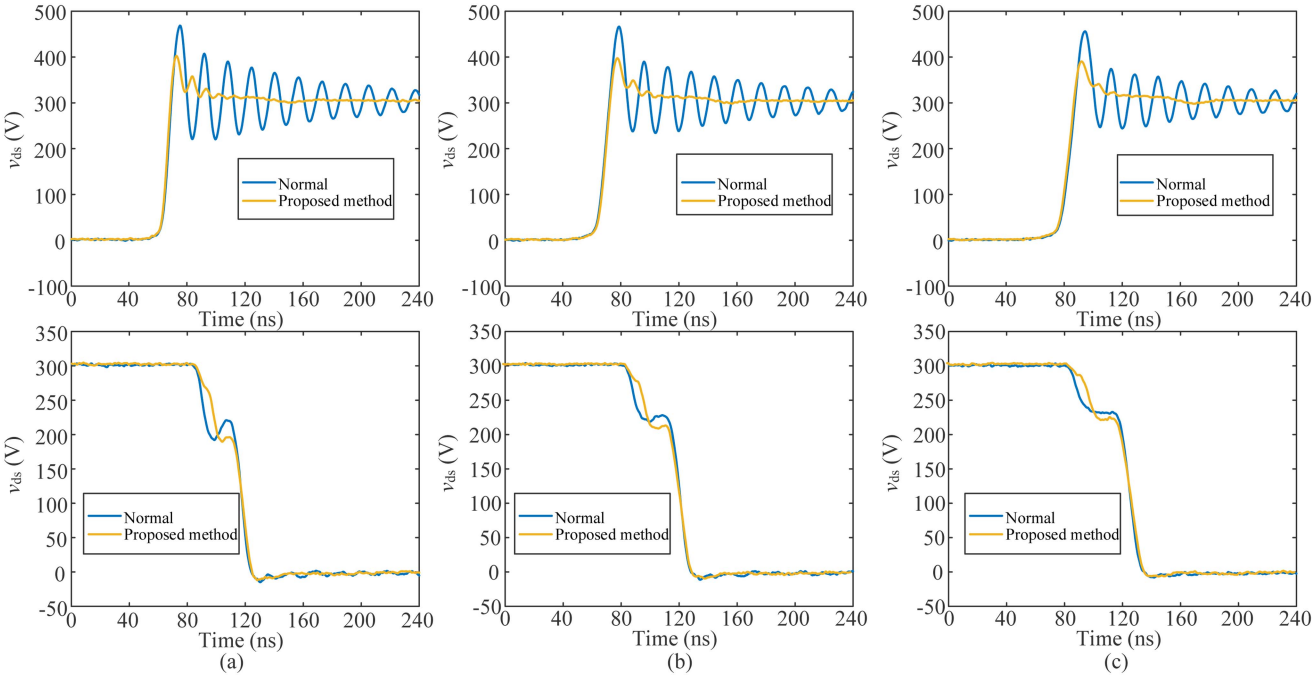

Fig. 15. Experimental waveform comparisons between the proposed method and the normal situation ($I_{\mathrm{L}} = 30$ A, $V_{\mathrm{in}} = 300$ V). (a) $R_{\mathrm{G}} = 5\ \Omega$. (b) $R_{\mathrm{G}} = 10\ \Omega$. (c) $R_{\mathrm{G}} = 15\ \Omega$. (Figures above are turn-OFF processes and figures below are turn-ON processes.).

$v_{\rm ds}$ will have a slight oscillation due to the forward recovery process and the lead inductance of the diode D_1 when $v_{\rm C1}$ rises from $V_{\rm in}$ to $V_{\rm C1\cdot max}$, the proposed method still has good oscillation suppression effect on the switching oscillation. And the switching oscillation can also be fully suppressed in stage 4. In addition, the proposed method also has no obvious effect on the turn-ON and turn-OFF speeds of the device according to Fig. 15. Accordingly, the experimental results effectively support our theoretical design, which proves the good practicability of the proposed method.

V. Conclusion

In this article, a suppression method with clamping function and quantitative design is proposed to suppress the switching oscillations of SiC MOSFETs. Based on the primary design of the clamping circuit parameters, the value ranges of the relevant parameters are further quantitatively analyzed according to the high-frequency equivalent circuit of the switching oscillation, and better oscillation suppression effects are obtained. The theoretical analysis is verified by the experimental platform, which predicts a significant improvement on switching characteristics and system performance. The proposed method can be applied to other bridge circuits such as buck/boost converters and has the following features.

1) During the device switching transient, the proposed method not only can well clamp the drain-source voltage overshoot during the device turn-OFF period, but also does not affect the turn-ON and turn-OFF speed of the device and will not increase the switching loss.
2) The proposed method mainly uses passive devices, such as diodes, resistors, and capacitors, which makes the design method very simple and easy to implement.
3) The switching oscillation under clamping capacitor voltages cannot be suppressed by conventional clamping suppression methods, the proposed design method can always effectively suppress this oscillation when the circuit parameters such as the input voltage or the gate resistance change. In addition, this method has smaller oscillation spikes compared with the *RC* method.

Appendix

The coefficients in (11) are shown in the following:

$$\begin{aligned}
a_0 &= C_1 L_D L_p I_0 \\
a_1 &= C_1 L_D R_2 I_0 + C_1 L_p R_2 I_0 \\
a_2 &= L_D I_0 + L_p I_0 \\
b_0 &= C_{oss} C_1 L_D L_p \\
b_1 &= C_{oss} C_1 L_D R_2 + C_{oss} C_1 L_p R_2 \\
b_2 &= C_{oss} L_D + C_{oss} L_p + C_1 L_p \\
b_3 &= C_1 R_2 \\
b_4 &= 1.
\end{aligned}$$

The coefficients in (12) and (13) are shown in the following:

$$\begin{aligned}
Q &= C_{oss} L_D L_p s^4 + \left(C_{oss} L_D R_2 + C_{oss} L_p R_2\right) s^3 \\
&\quad + L_p s^2 + R_2 s \\
P &= (C_{oss} L_D + C_{oss} L_p) s^2 + 1.
\end{aligned}$$

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