Letters

A Novel Single Isolation Channel Gate Driver With Bidirectional-Signal and Forward-Power Transmission

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***Abstract*—Conventional isolated gate drivers adopt separate isolation channels for gate driver signal and isolated power supply, which suffers from large signal delays, large size, and high cost at medium-voltage (MV) and high-voltage (HV) applications. Gate drivers with single isolation channel were proposed but suffered from gate driver power instability and limited duty-cycle range. A novel compact single isolation channel with bidirectional-signal and forward-power transmission gate driver is proposed in this letter. Gate driver signal is modulated by pulse edge modulation and transmitted through flyback converter with time-division multiplexing. Feedback signal is modulated by amplitude modulation and demodulated based upon the voltage proportional relationship between primary and secondary sides of a flyback transformer. 3D vertical packaging is adopted with an overall size of 20 mm×17 mm×16 mm. The proposed gate driver achieves max. driving current of 13.8 A and can drive silicon carbide devices with max. d*v*/d*t* of 154 V/ns. It can support max. gate driver signal frequency of 100 kHz with duty cycle ranging from 7.5% to 92.5%. Feedback signal transmission is also demonstrated by the desaturation circuit.**

***Index Terms*—Bidirectional-signal transmission, flyback converter, signal-power cotransmission, single isolation channel, time-division multiplexing (TDM).**

I. Introduction

BREAKTHROUGHS in voltage withstand capabilities of next-gen wide-bandgap power devices has significantly improved the volume, efficiency, and cost-effectiveness of medium to high-voltage (MV/HV) converter systems, including solid-state transformers, MV drives, and smart grid-tie systems [1]. The demanding operational conditions characterized by HV stress and high d*v*/d*t* impose stringent requirements on isolated gate driver (GD) design [2], [3].

Conventional isolated GDs adopt separate power and signal isolation transmission unit. While digital isolators are employed for signal isolation transmission at low-voltage levels, MV/HV applications typically require optical fiber or opto-couplers, with limitations of high signal delay, elevated costs, and reduced reliability. Integrating signal and power transmission in a single isolation channel will enhance integration degree, reliability, and reduced costs for MV/HV applications [4]. It will also promote the feasibility of integrating GDs into power modules.

State-of-the-art approaches for signal-power integrated transmission directly transmitted GD signal as pulsewidth modulation (PWM) signal for isolated gate driver power supply (GDPS) [5]. The system architecture is simple, yet the frequency and duty-cycle range of the GD signal is limited. The authors in [6] and [7] extracted the edges of the GD signal to transmit both signal and power through a single pulse transformer. However, the output voltage of GDPS declines gradually due to the leakage current, and is also impossible to achieve full duty cycle. High-frequency carriers were further employed to modulate the GD signal by ON-OFF keying modulation. Nguyen et al. [8] utilized a 500-kHz high-frequency carrier to achieve 0–200 kHz GD signal with 0%–100% duty-cycle range. But at low duty cycles, power transmission of GDPS was insufficient, failed to ensure power stability at the secondary circuit, especially during the power-up of protective circuits. To ensure stable GD power across the entire duty-cycle range, the authors in [9] and [10] employed two complementary high-frequency carriers and transmitted modulated GD signals through two paralleled isolation transformers, which were deviated from original integrated design intention. Therefore, the state-of-the-art approaches have the limitations of GD power instability and limited duty-cycle range of GD signals. The transmission of feedback signal transmission is almost neglected, which is essential for protection and monitoring.

To overcome these problems, a new single isolation channel GD based on time-division multiplexing is proposed. GD signals and GD power are allocated for different time slots of a single PWM cycle in one transmission channel. Feedback signal is modulated by amplitude modulation and demodulated based upon the voltage proportional relationship between primary and secondary sides of the flyback transformer. The proposed novel approach ensures stable GD power delivery with GD signals of full duty cycle. Feedback signals for protection and monitoring are also included.

Manuscript received 20 December 2023; revised 20 January 2024; accepted 7 February 2024. Date of publication 22 February 2024; date of current version 19 April 2024. This work was supported by the National Natural Science Foundation of China under Grant 52277178. *(Corresponding author: Han Peng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3368665.

Digital Object Identifier 10.1109/TPEL.2024.3368665

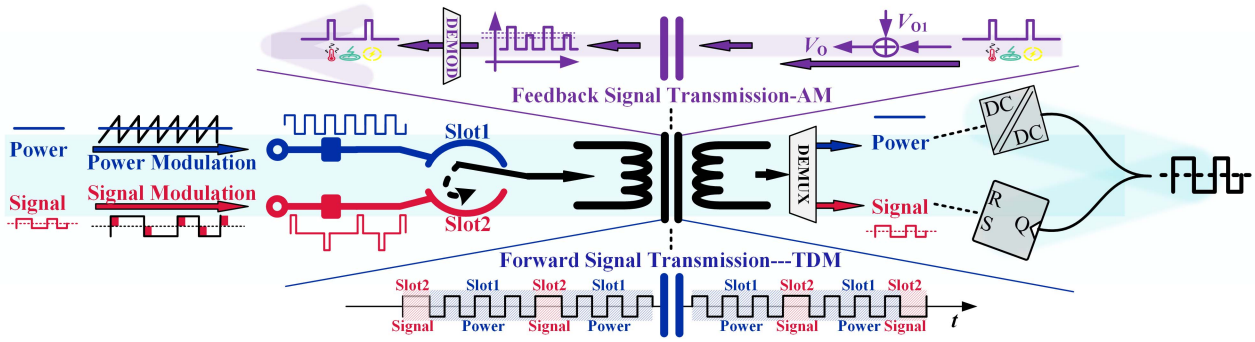

Fig. 1. Bidirectional-signal and forward-power integrated transmission based on TDM.

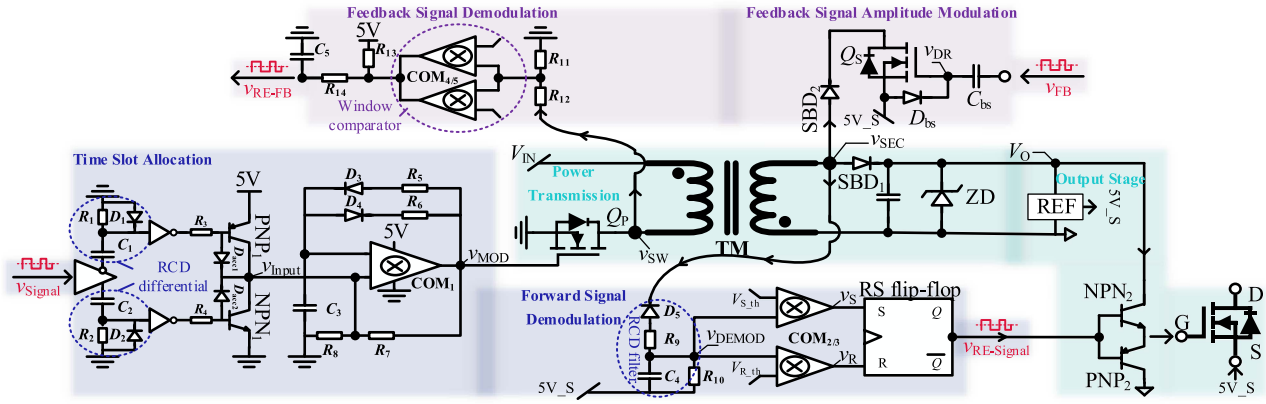

Fig. 2. Detailed schematic for bidirectional-signal and forward-power integrated transmission.

II. Operation Principle and Circuit Description

A. Proposed Cotransmission Approach With Time-Division Multiplexing (TDM)

This letter adopts TDM to divide the entire switching period of the GD signal into two nonoverlapping time slots. A GD signal is transmitted in the signal transmission slot and the GD power is transmitted in the power transmission slot. Within their respective slots, power and signal exclusively occupy channels for the transmission. This method ensures stable power supply transmission with varying duty cycles of GD signal. As depicted in Fig. 1, the GD signal is edge-extracted and combined with the PWM signal of GDPS by the time-sequential superimposition method. On the secondary side, amplitude demodulation is utilized to rectify the GD power and reconstruct the GD signal. A push–pull stage is adopted to further amplify the reconstructed GD signal.

To transmit the protection signals from the power side [e.g., overheat, overvoltage, overcurrent (OC)] to the control side, amplitude modulation is employed, also depicted in Fig. 1. The output voltage at the secondary side of the flyback (V_O) is modulated by adding instantaneous amplitude of the feedback signal. On the signal side, demodulation is achieved by the window comparison of Q_P's drain–source voltage v_{SW} to restore the protection signal.

B. Circuit Schematics

Forward transmission: On the signal side, the channel time slot is allocated to the gate drive signal when the edge pulse arrives through the time slot allocation circuit. As shown in Fig. 3(a), at t_0, the rising edge triggers transistor NPN_1 via the RCD differential circuit, pulling the square wave generator input v_{Input} to zero, where diodes D_{acc1} and D_{acc2} are employed to facilitate transistors to turn ON. The output signal, namely, the modulated signal v_{MOD}, is clamped to zero accordingly. The clamping duration T_{clamp}, dictated by the *RC* parameters in the RCD differential circuit, must exceed the low-level pulsewidth of the square wave for the effective demodulation on the power side. The flyback converter is employed for GDPS, and Q_P is turned OFF due to the low level of its gate voltage v_{MOD}. Therefore, Q_P's drain–source voltage v_{SW} and transformer secondary voltage v_{SEC} are keeping at the high level. v_{SEC} generates a stable 20 V voltage using a Schottky diode (SBD_1), a Zener diode (ZD), and a regulating capacitor. GD supply voltages (+15 V/-5 V) are generated through nonisolated voltage regulator. The GD signal is demodulated through the forward signal demodulation circuit, including an RCD filter, a voltage comparator, and a RS flip-flop. In this signal transmission slot, the demodulated voltage (vDEMOD) is produced from RCD filter, triggering a set signal of RS flip-flop through voltage comparison. At t_1, the RS flip-flop outputs the recovery signal $v_{RE\text{-}Signal}$ for the rising edge of the GD signal. Similarly, when the GD signal's falling edge is triggered at t_2, the RCD differentiation circuit turns ON PNP_1 transistor, generating a controllable low-level pulse T_{clamp} and clamping v_{MOD} to the

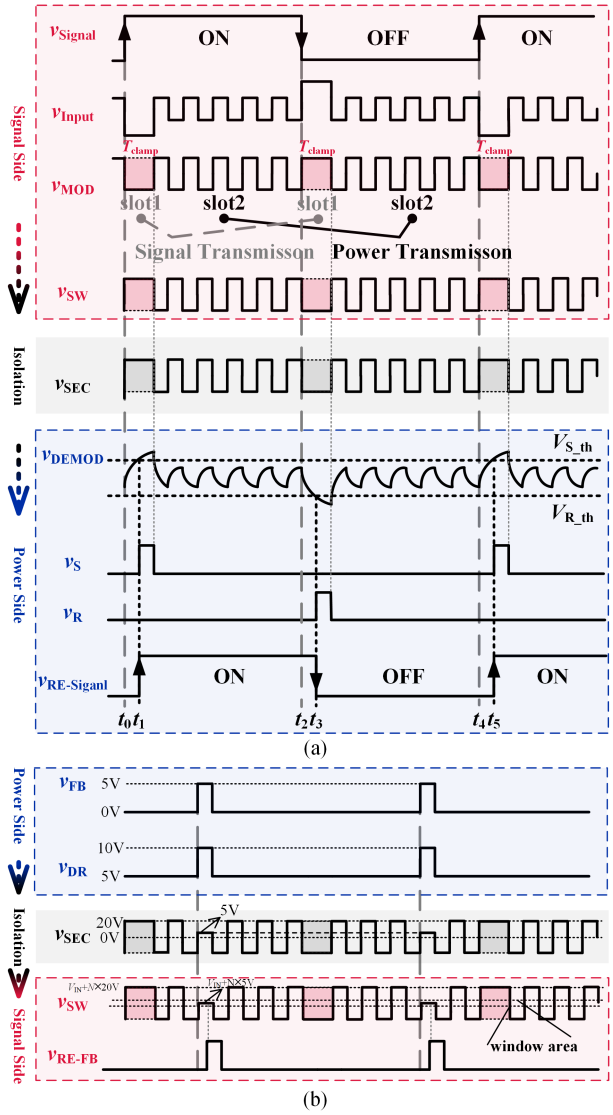

Fig. 3. Key waveforms: (a) forward and (b) backward transmission.

the demodulated voltage v_{DEMOD} triggers the reset signal of RS flip-flop. At t_3, the recovery signal $v_{\mathrm{RE\text{-}Signal}}$ changes from high to low, successfully recovering the falling edge pulse.

When edge pulses of GD signals are not triggered, the time slot is allocated to power control. The RCD differential circuit remains inactive. The recovery signal $v_{\mathrm{RE\text{-}Signal}}$ maintains a constant state.

The GD signal transmission utilizes a negligible fraction of the gate drive PWM switching cycle. A uniform design of pulses width triggered by rising/falling edges will compensate between transformer positive and negative voltages, ensuring a balanced volt–second product at the transformer. Therefore, GD signal transmission has no effect on drive power transmission, keeping stable power and voltage output throughout the entire duty-cycle range.

Reverse transmission: The reverse signal amplitude modulation circuit comprises a diode SBD_1, a switch Q_{S}, and a bootstrap driver circuit composed of capacitor C_{bs} and diode D_{bs}. Utilizing the proportional relationship between the flyback transformer's primary and secondary voltages, reverse signal transmission is achieved through amplitude modulation of the output voltage. When a feedback signal is triggered, an amplitude modulation is applied to the output voltage (V_{O}) controlled by the amplitude of the feedback signal. After transmitting across flyback transformer, v_{SW} is sampled and demodulated through a window comparison. As depicted in Fig. 3(b), the bootstrap driver circuit activates Q_{S}, clamping flyback output voltage (V_{O}) at 5V. On the signal side, v_{SW} is clamped at

$$\boldsymbol{v_{\mathrm{SW}}} = V_{\mathrm{IN}} + V_{\mathrm{O}} \times N \tag{1}$$

where N denotes primary-to-secondary turns ratio. Signal recovery for v_{SW} is accomplished using a resistance voltage divider and a window comparator. Different output clamping voltages can be applied to transmit different feedback signals.

C. GD Signal Duty-Cycle Range Analysis

The range of the duty cycle of the GD signal is influenced by the modulation method. As shown in Fig. 3(a), short pulse with a duration of T_{clamp} is applied to modulate the GD signal, and T_{clamp} should be more than half of the switching period of the GDPS PWM. Duty cycle of the GD signal should follow

$$\begin{cases} T_{\mathrm{clamp}} = \frac{m}{f_{\mathrm{GDPS}}}, m > 0.5 \\ \frac{m}{f_{\mathrm{GDPS}}} \le \frac{D}{f_{\mathrm{GD}}} \mathbf{and} \frac{m}{f_{\mathrm{GDPS}}} \le \frac{(1-D)}{f_{\mathrm{GD}}} \end{cases} \tag{2}$$

where f_{GD} represents the switching frequency of the GD signal, f_{GDPS} represents the switching frequency of the GDPS PWM, and m is the ratio between T_{clamp} and the switching period of the GDPS PWM. According to (2), duty cycle and frequency of the GD signal should follow

$$\begin{cases} \frac{m f_{\mathrm{GD}}}{f_{\mathrm{GDPS}}} \times 100\% \le D \le 1 - \frac{m f_{\mathrm{GD}}}{f_{\mathrm{GDPS}}} \times 100\% \\ f_{\mathrm{GD}} \le \min\left\{ \frac{D f_{\mathrm{GDPS}}}{m}, \frac{(1-D) f_{\mathrm{GDPS}}}{m} \right\}. \end{cases} \tag{3}$$

The minimum duty cycle is determined by T_{clamp} and f_{GD}. And the maximum f_{GD} should be less than $1/(2\times T_{\mathrm{clamp}})$. In this letter, $T_{\mathrm{clamp}} = 0.75/f_{\mathrm{GDPS}}$ ($m = 0.75$) with $f_{\mathrm{GDPS}} = 10 f_{\mathrm{GD}}$, and the duty-cycle range of GD signal is [7.5%, 92.5%]. Due to the time-division transmission of both signal and power, proposed GD can operate reliably under a duty cycle of 0% and 100%, respectively. Therefore, achievable PWM duty-cycle range is $\{0\%\} \cup [7.5\%, 92.5\%] \cup \{100\%\}$.

III. Prototype Design and Experimental Verification

A. Prototype Design

The critical parameters of the single isolation channel GD designed in this letter are detailed in Table I. Employing the compact planar E-core (model: PLT14/5/1.5/S, core material: 3F46), the transformer TM is configured with winding turns ratio of 7:7. Design specifications for the transformer and GD are outlined in Table II. The coupling capacitance (C_{cp}) of the transformer is 5.6 pF and the magnetizing inductance (L_{m}) is 129 μH. 3D-stacked packaging is utilized by sequentially housing the primary circuit, transformer, and secondary circuit,

TABLE I
KEY DEVICES PARAMETERS

Parameter	Value	Parameter	Value
Q_P, Q_S	IRLML2060TRPBF	COM_1	TLV3601
$COM_{2/3}$	TLV3602	$COM_{4/5}$	MCP6567-E_MS
NPN_1, PNP_1	PUMZ1,115	SBD_1, SBD_2	RB021VAM90
ZD	SZ1SMA5932BT3G	RS flip-flop	SN74LVC2G02
REF	TPSM84209	NPN_2, PNP_2	UCC27614

TABLE II
PROTOTYPE KEY PARAMETERS

Parameter	Value	Parameter	Value
L_m	129 μF	V_{IN}	25 V
C_{cp}	5.6 pF	P_O	1.5 W
Frequency	1 MHz	η	50.6%

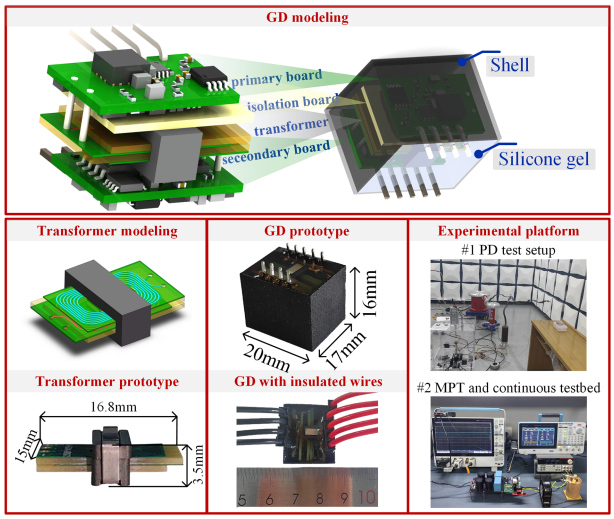

Fig. 4. GD prototype and experimental platform in the laboratory.

as shown in Fig. 4. The electric potential of transformer core is connected to the ground of secondary circuit. And an isolation board is inserted to realize voltage isolation between the signal board and the transformer core. To mitigate surface flashover and eliminate creeping discharge, the driver is potted with silicone gel. With the dimension of 20 mm $\times$17 mm $\times$ 16mm, it is just 38% of the size of current commercially products [12]. Partial discharge (PD) test confirms that the GD transformer meets the insulation requirement with a PD inception voltage (PDIV) of 5 kVrms under 50-Hz ac voltage excitation.

B. Forward Transmission Function Verification

Given $R_5 = 6.8$ kΩ, $R_6 = 8.2$ kΩ, $C_3 = 62$ pF, and $R_{7/8} =$ 1kΩ, GDPS PWM frequency of the flyback converter is set to 1 MHz with duty cycle of 45%, as depicted in Fig. 5. T_{clamp} is 750 ns with $R_1 = 10$kΩ, $R_2 = 8.2$kΩ, and $C_{1/2} = 24$ pF. At an output power of 1.5W, the converter achieves an efficiency of 50.6%. Fig. 5 illustrates the modulation, transmission, and demodulation process with GD signal frequency of 100 kHz. Upon the arrival of the GD signal edges, the demodulation

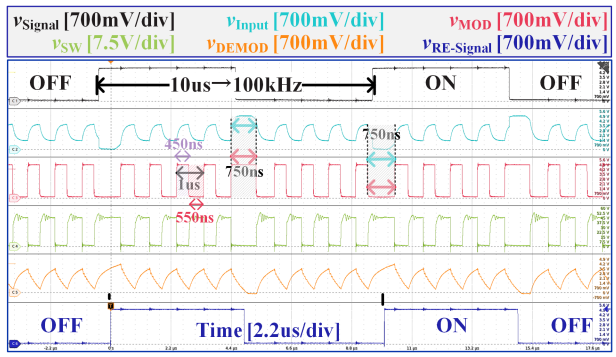

Fig. 5. Critical waveforms in the forward transmission.

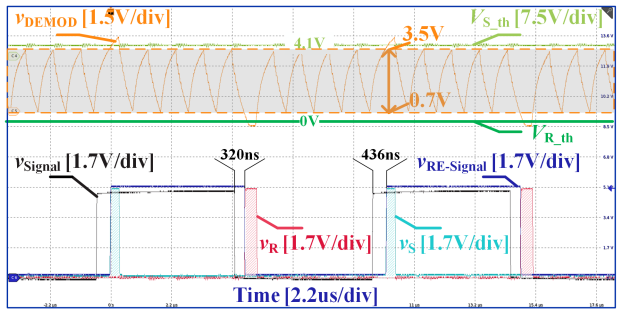

Fig. 6. Specific forward demodulation process waveforms.

voltage v_{DEMOD} triggers set or reset signals of the RS flip-flop. GD signals are successfully restored with a rising edge delay of 436 ns and a falling edge delay of 320 ns. The GD output exhibits a peak sourcing current of 13.8 A and a sink current of 13 A.

Fig. 7(a)–(f) shows GD operating waveform at $D = 0\%$, 7.5%, 30%, 60%, 92.5%, and 100%, respectively, with GD signal frequency of 100 kHz. Small amount of signal distortion exists due to the asynchronous GDPS PWM and GD signal. GD output voltage v_{gs} is generated with desired timing and magnitudes (+15V/−5V). It is demonstrated that proposed GD achieves signal-power integrated transmission within almost full duty-cycle range.

The multiple pulse test (MPT) is conducted on a 1.2-kV SiC MOSFET (C3M0040120K, upper switch) to examine its switching performance with proposed GD, as shown in Fig. 8(a). With a bus voltage V_{BUS} of 600 V, load current of 50 A, and driving resistance of 3 Ω, as illustrated in Fig. 9, the proposed GD achieves di/dt and dv/dt of 5.4 A/ns and 154 V/ns, respectively.

A continuous test is also conducted to validate the robustness of the proposed GD under dynamic switching conditions, as shown in Fig. 8(b). Continuous switching with proposed GD at V_{BUS} of 600V and load currents of $\pm$12 Apk is shown in Fig. 10. Common mode current in upper GD reaches 228 mA at the rising dv/dt of 42 V/ns, and $-$270 mA at the falling dv/dt of 50 V/ns. C_{cp} of the proposed GD is estimated to be approximately 5.4 pF. It can be shown that the proposed GD exhibits robust noise immunity without false-triggered and missed pulses.

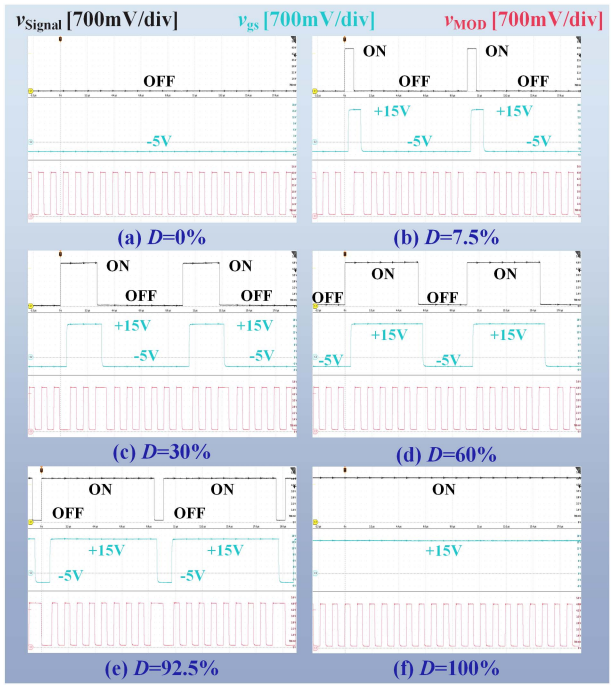

Fig. 7. GD operating waveforms at different duty cycles. (a) D=0%. (b) D=7.5%. (c) D=30%. (d) D=60%. (e) D=92.5%. (f) D=100%.

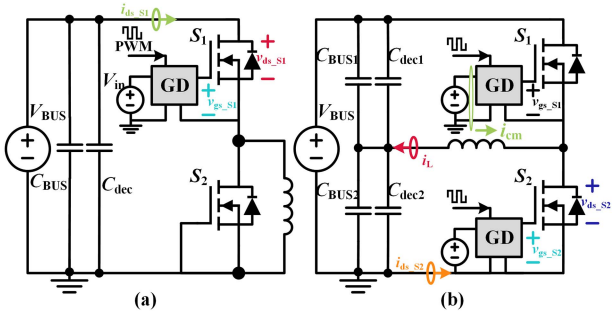

Fig. 8. Working schematic of test setup. (a) MPT. (b). Continuous test.

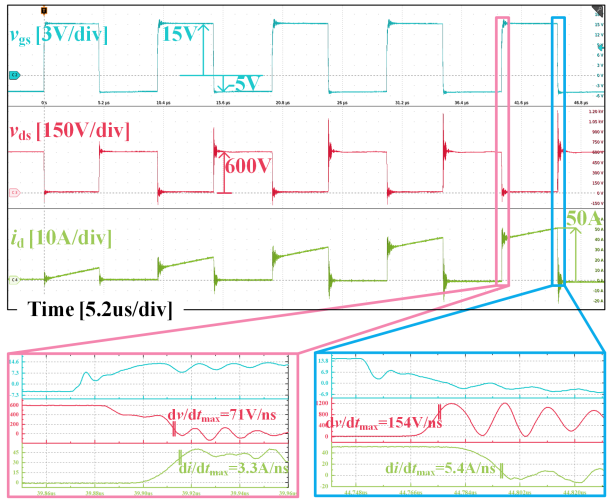

Fig. 9. MPT results at max load current of 50 A.

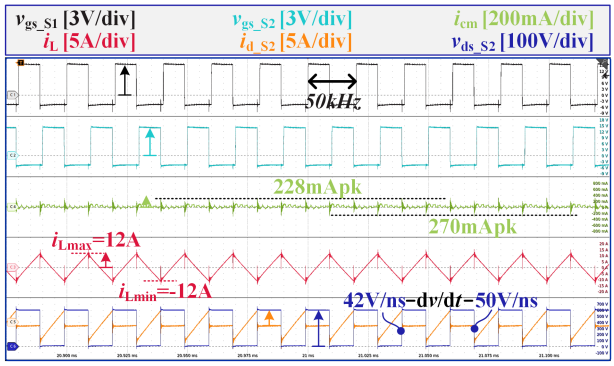

Fig. 10. Continuous testing results at load current of ±12 Apk.

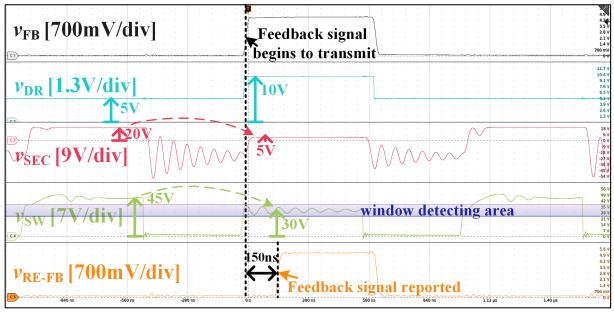

Fig. 11. Specific waveforms of feedback signal transmission process.

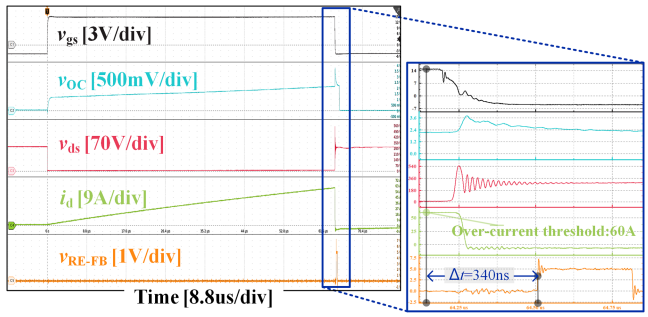

Fig. 12. Experimental waveforms of DESAT protection.

C. Reverse Transmission Function Verification

Fig. 11 shows the process of feedback signal transmission, where a fault signal v_{FB} is intentionally applied by adding pulses on the detecting pin at the GD secondary side. v_{FB} is modulated through amplitude modulation. After v_{DR} increases to 10 V through bootstrap, the flyback output voltage V_O is clamped to 5 V. And the turn-OFF voltage of Q_P is clamped to 30 V ($V_{IN}+N\times V_O$), which can be detected by the window comparator. Therefore, $v_{RE\text{-}FB}$ is successfully recovered with the time delay of 150 ns.

The Desaturation (DESAT) protection is utilized to assess the reverse transmission functionality, as depicted in Fig. 12. An OC fault is tested. OC protection voltage v_{OC} reaches the predefined threshold and activating the DESAT protection when SiC MOSFET's current exceeds 60 A. Then, on the power loop

side, the protective circuit swiftly responds and SiC MOSFET v_{gs} is clamped to -5 V. When the device is turned OFF, the feedback signal begins to transmit. Transmission delay of the OC protection is measured at 340 ns.

IV. Conclusion

This letter proposes a novel single isolation channel GD with a bidirectional-signal and forward-power co-transmission, significantly reducing dimensions and costs. Utilizing a flyback converter as the isolated channel, a single-channel transmission method is established based on a time-division multiplexing technology. GD signals and power are decoupled in time domain to ensure stable power transmission across the entire duty-cycle range of the GD signal. Based upon the proportional relationship of transformer primary and secondary voltages, the reverse transmission of signal is realized by amplitude modulation. Assembled in a 3D-stacked configuration, the proposed GD achieves ultra-high power density (20 mm$\times$17 mm$\times$16 mm) and the GD transformer meets PDIV of 5 kVrms. GD efficiency is 50.6% with output power of 1.5 W and maximum output drive current of 13.8 A. It can support max. GD signal frequency of 100 kHz with duty cycle ranging from 7.5% to 92.5%. Experimental results have verified the driving robustness of GD for SiC MOSFETs.

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