A Fully Integrated Sequential Synchronized Switch Harvesting on Capacitors Rectifier Based on Split-Electrode for Piezoelectric Energy Harvesting

Xinling Yue, *Graduate Student Member, IEEE*, Jiarui Mo, *Student Member, IEEE*,
Zhiyuan Chen, *Member, IEEE*, Sten Vollebregt, *Senior Member, IEEE*, Guoqi Zhang, *Fellow, IEEE*,
and Sijun Du, *Senior Member, IEEE*

***Abstract*—Synchronized rectifiers offer promising solutions for piezoelectric energy harvesting; however, achieving the promised energy extraction performance necessitates using either a bulky inductor or multiple large capacitors, which cannot be on-chip integrated and increase the system form factor. This article introduces a fully integrated sequenced synchronized switch harvesting on capacitors (3SHC) rectifier. The input piezoelectric transducer (PT) uses microelectromechanical system technology. The cantilever is equally split into multiple strongly coupled subcantilevers, with each cantilever treated as an individual PT connected to the proposed rectifier. The 3SHC rectifier cyclically operates multiple times to synchronously flip the voltage of each cantilever sequentially. With the proposed design, all the flying capacitors only need to match the capacitance of each subcantilever; hence, they can be fully integrated on-chip. The design is fabricated using standard 0.18 μm CMOS technology. Measurement results show that the proposed 3SHC rectifier attains an 80% voltage flip efficiency and achieves a 730% power enhancement compared to a full-bridge rectifier.**

***Index Terms*—Bias-flip, fully integrated, microelectromechanical systems (MEMS), piezoelectric energy harvesting (EH), rectifiers, split-electrode, synchronized switch harvesting on capacitors (SSHC).**

I. INTRODUCTION

As THE Internet of everything (IoE) expands, wireless sensors play a pivotal role in bridging the physical world with the Internet. In pursuit of creating self-sustained low-power devices, there has been growing research interest in energy harvesting (EH) solutions, which involve harvesting energy from external sources, such as solar, thermal, wind, and kinetic energy, to power low-power electronics [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. Kinetic energy, in particular, shows a remarkable power density ranging from 10 to 500 μWcm^{-2}. Typically, kinetic energy is converted into electrical energy using a piezoelectric transducer (PT). As the output of the PT is ac energy, it requires an ac–dc rectifier to extract and store the harvested energy [14], [15], [16], [17], [18], [19], [20], [21].

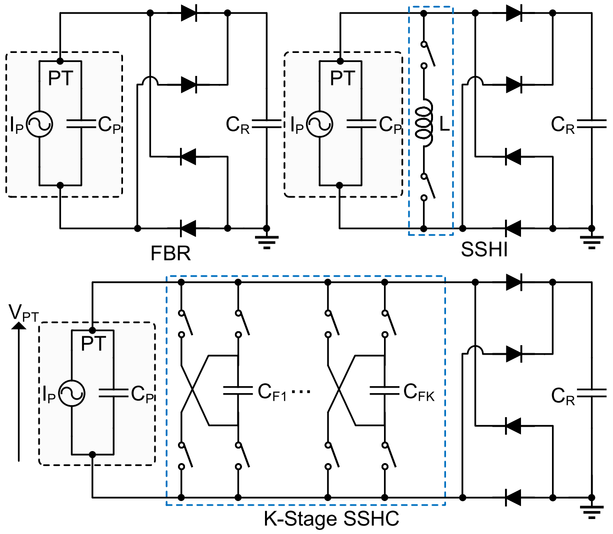

Fig. 1. Conventional rectifiers for piezoelectric EH.

The most typical ac–dc rectifier is a full bridge rectifier (FBR). As shown in the top left of Fig. 1, a PT is modeled as an ac current source, I_P, in parallel with a capacitor, C_P, when the PT is excited at its resonance frequency. An FBR employs four passive diodes and does not require any active components, but the output power efficiency of an FBR is low since the PT voltage flipping (from positive to negative or vice versa) at each zero-crossing moment of I_P consumes the PT-generated charge, resulting in significant energy loss. The passive diodes' high forward voltage drop also introduces extra energy loss.

Some active rectifiers have been developed to reduce the wasted energy due to voltage flipping. The synchronized switch harvesting on the inductor (SSHI) rectifier employs an inductor to flip the PT voltage synchronously by forming an RLC oscillation loop. However, using an inductor makes the system bulky and expensive [15], [22], [23], [24]. An alternative approach, synchronized switch harvesting on capacitors (SSHC) rectifier, was proposed to address this issue. Instead of an inductor, it uses several capacitors to flip the PT voltage [25], [26], [27], [28]. Nevertheless, a challenge arises when dealing with PTs

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Manuscript received 26 December 2023; revised 2 February 2024; accepted 21 February 2024. Date of publication 26 February 2024; date of current version 19 April 2024. Recommended for publication by Associate Editor J. Acero. *(Corresponding author: Sijun Du.)*

Xinling Yue, Jiarui Mo, Sten Vollebregt, Guoqi Zhang, and Sijun Du are with the Department of Microelectronics, Delft University of Technology, 2628CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

Zhiyuan Chen is with the State-Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3369728.

Digital Object Identifier 10.1109/TPEL.2024.3369728

with larger internal capacitors (C_P). Since the flying capacitors (C_{FK}) ideally need to be equal or larger than C_P for good voltage flipping performance, integrating these flying capacitors into a chip becomes very impractical, since C_P is typically in the nano-Farad range.

A fully integrated technique, proposed in [17] and [29], seeks to overcome this challenge by employing PTs with small C_P in the pico-Farad range. However, these approaches limit their application to ultrasonic energy receivers and are impractical when C_P exceeds the nano-Farad range, which is very common in kinetic energy harvesters. Li et al.[26] necessitates the use of four PTs as inputs, employing them as a large flying capacitor during the flipping process. This approach involves sharing of charge among the four PTs in different phases, obviating the need for dedicated flying capacitors. However, while this design choice is effective, it poses challenges for system miniaturization, as the required large PT array dominates the system volume. To deal with PTs with only one larger C_P, Du et al. [30] presented the split-electrode SSHC (SE-SSHC) technique. This method achieves full integration by partitioning a microelectromechanical system (MEMS) PT into multiple sections and connecting them in series during flipping, reducing the effective PT capacitance that interfaces with the circuit. However, this approach imposes high voltage stress on the switches with summed-up voltage when the PT sections are connected in series. The series-connected PT generates a high voltage resulting in a large leakage current since during the flipping moment, the parasitic resistors and capacitors connected to PT voltage are charged to the series-connected high voltage, reducing the flipping efficiency, and necessitating the use of non-standard high-voltage (HV) CMOS transistors. HV transistors occupy a significantly larger layout area due to isolated rings between the substrate and active areas. They exhibit around 4× larger on-resistance than standard CMOS transistors, leading to longer pulse widths during charging sharing and increased power dissipation. Moreover, HV transistors typically present higher parasitic resistance and capacitors. In [30], the high PT voltage results in the charge and discharge of parasitic capacitors, leading to elevated power consumption–a significant concern in EH systems, where power efficiency is paramount. In addition, they require complex drivers, such as bootstrap circuits, contributing to increased circuit complexity.

This article introduces a sequential synchronized switch harvesting on capacitors (3SHC) rectifier, which implements fully integrated flying capacitors to flip voltage across an nF-ranged PT. The PT was made by an in-house MEMS process with split electrodes. During flipping, the shared on-chip flying capacitors flip the sub-PT sequentially rather than connecting them in series. This ensures no high voltage stress on the switches, making using standard CMOS devices only possible. This technique avoids the issues caused by using HV transistors in [30], resulting in no HV points and improved flipping efficiency and output power efficiency. The rest of this article is structured as follows. Section II introduces the analysis of the proposed 3SHC rectifier. The system architecture and the circuit implementation are presented in Section III. Measurement results are shown in Section IV. Finally, Section V concludes this article.

II. ANALYSIS OF THE PROPOSED 3SHC RECTIFIER

A. System Topology

Fig. 2 illustrates the proposed 3SHC rectifier topology and its corresponding flipping phases. As shown on the left, to achieve full integration, the monolithic top and bottom electrode layers of the MEMS PT are subdivided into eight equal regions, effectively reducing the intrinsic capacitor (C_P) by 8× in each area and enabling seamless rectification. With the same tip mass, the eight regions (named PT_1 to PT_8, respectively) are mechanically strongly coupled, allowing them to generate output voltage with almost the same amplitude, frequency, and phase. Further increasing the number of split pieces would lead to smaller on-chip capacitors. However, this approach necessitates space gaps between neighboring PTs (smaller effective PT area), dead time between adjacent flipping phases (longer time required for converting all the sub-PTs), increased switching losses due to more switching phases, etc. Upon consideration of these influencing factors, this article advocates for the adoption of eight split electrodes. This choice strikes a balance, enabling fully on-chip integration without excessive energy loss.

On the right, the eight sub-PTs are connected to the 8-stage 3SHC rectifier. When all eight split MEMS PTs are in the EH state, they are connected in parallel to the FBR by simultaneously activating switches S_1 through S_8. As the current I_P crosses zero, the PT voltage needs to be flipped. To do so, each sub-PT is sequentially connected to the 8-stage 3SHC rectifier by turning on the switches S_1 through S_8 sequentially and nonoverlapping. The rectifier has eight flying capacitors, denoted as C_{F1-8}, for sub-PT voltage flipping. Since only one sub-PT is connected to the rectifier at a time, the required capacitance for the flying capacitors only needs to match that of one sub-PT, not the whole PT. In this case, the required flying capacitance is reduced by eight times. The flipping phases are also shown in the figure. Initially, S_1 is activated to link C_{P1} to eight flying capacitors, C_{F1-8}. After the voltage across C_{P1} is flipped, S_2 is turned ON to connect C_{P2} to C_{F1-8} for flipping. This procedure continues until the voltage across the PT_8 is flipped. The fully integrated 8-stage SSHC rectifier is shared among the eight sub-PTs and is used eight times.

Fig. 3 depicts the waveform of the 8 V_{PT} signals along with their corresponding control signals during the flipping period. To facilitate the sequential voltage flipping of sub-PTs, switches S_1 to S_8 are turned ON one by one during each sub-PT flipping moment, resulting in the sequential flipping of sub-PT voltages, namely, V_{PT1} to V_{PT8}. The zoomed-in figure on the right provides a detailed view of the sub-flipping process. During flipping phases, the energy within each sub-PT is initially transferred into the flying capacitors, C_{F1-8}, by activating switches Φ_{p1} to Φ_{p8}. Subsequently, any remaining charge is cleared by enabling Φ_0. Finally, switches Φ_{n8} to Φ_{n1} are sequentially closed to transfer the charge from C_{F8-1} back to the sub-PT. The switching modes of the 8-stage 3SHC rectifier and the waveform when flipping the last sub-PT (V_{PT8}) are illustrated at the bottom of Fig. 3. When V_{PT8} is flipped from negative to positive, the charge in C_{P8} is initially transferred into C_{F1} by turning ON Φ_{p1} and subsequently propagated through C_{F8} by Φ_{p8}, ultimately

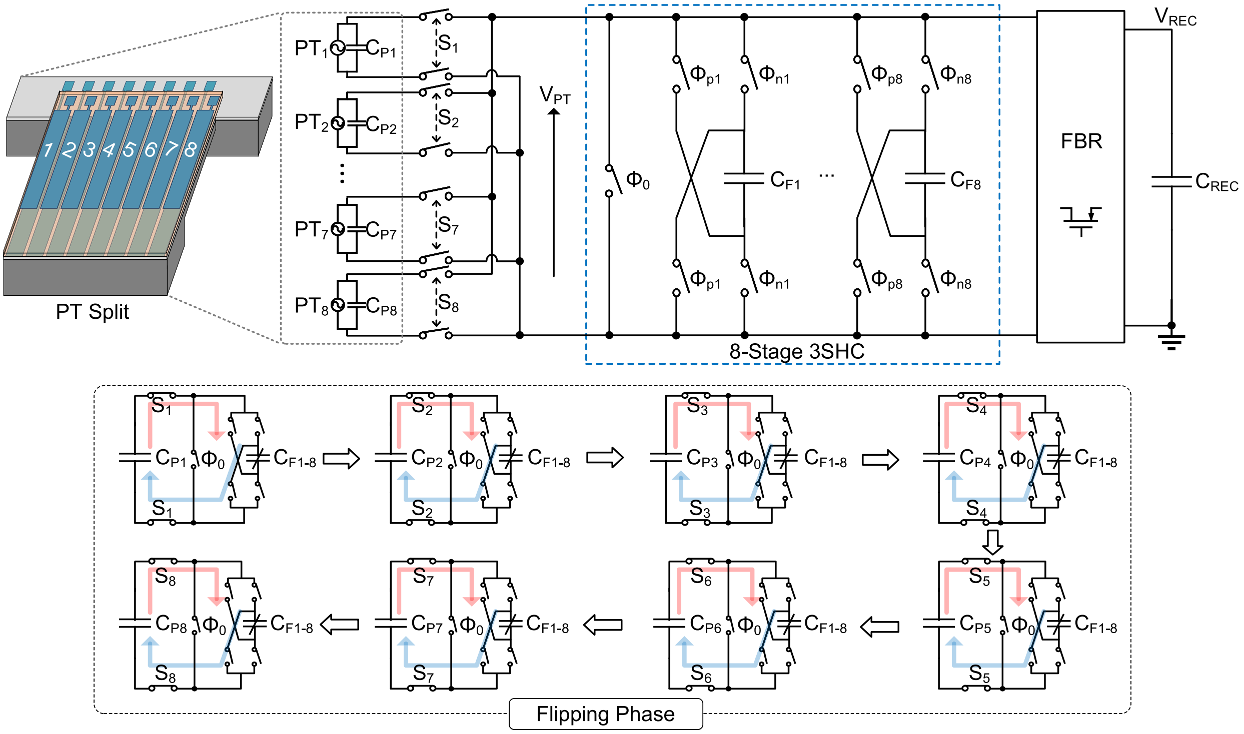


Fig. 2. Proposed 3SHC rectifier topology and flipping phase.

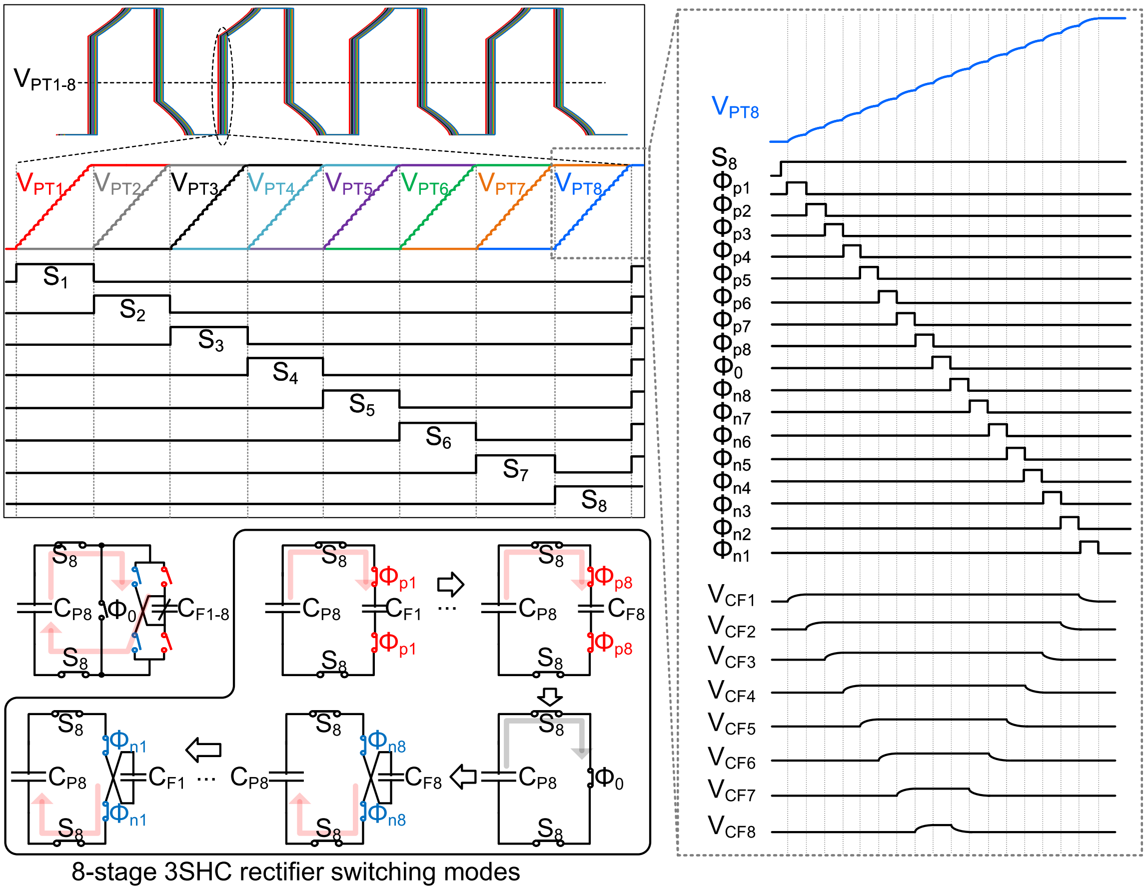


Fig. 3. Waveform of split sub-PT voltage and corresponding 3SHC rectifier switching modes.

returning to C_{F1} by Φ_{n1} in line with the configuration displayed in Fig. 2. The voltage across each flying capacitor $V_{CF1} - V_{CF8}$ is shown on the right. The voltages $V_{CF1} - V_{CF8}$ keep the same before and after flipping, which indicates that the voltage of the flying capacitors for flipping the 8 PTs would not be affected by the repeated sharing process.

B. *Theoretical Analysis*

A theoretical analysis of the flipping moment ensures that the proposed 3SHC rectifier has sufficient time to flip sequentially. The flipping process of the first sub-PT is taken as an example. To simplify the calculation, we assume that the intrinsic sub-PT and the flying capacitance are equal for the theoretical analysis. When C_{P1} is connected to C_{F1}, and assuming that the initial charge in C_{P1} is q_0; the charge flowing into C_{F1} is q; the initial charge in C_{F1} is zero for exploring the longest charge sharing time; there exists a relationship

$$\frac{q_0 - q}{C_{P1}} - \frac{q}{C_{P1}} - i \times R = 0 \tag{1}$$

where i is the current released from C_{P1} to C_{F1} and R is the total resistance of the loop. Equation (1) can be simplified as

$$q_0 - 2q = i \times R \times C_{P1}. \tag{2}$$

Due to $i = \frac{dq}{dt}$ in *RC* loop, the (2) can be expressed by

$$\frac{dq}{dt} \times R \times C_{P1} = q_0 - 2q. \tag{3}$$

The (3) can also be written as

$$\frac{dq}{q_0 - 2q} = \frac{dt}{R \times C_{P1}}. \tag{4}$$

Integrate (4), the following equation derivatives:

$$\int_0^q \frac{dq}{q_0 - 2q} = \int_0^t \frac{dt}{R \times C_{P1}}. \tag{5}$$

Further, we have

$$-\frac{1}{2}\ln[q_0 - 2q]|_0^q = \frac{t}{R \times C_{P1}} \tag{6}$$

$$\rightarrow ln\left(\frac{q_0 - 2q}{q_0}\right) = \frac{-2t}{R \times C_{P1}}. \tag{7}$$

Equation (7) can be simplified as

$$q_0 - 2q = q_0 \times e^{\frac{-2t}{R \times C_{P1}}}. \tag{8}$$

Finally, the relation between the q and the time t is expressed by the following equation:

$$q = \frac{1}{2} \times q_0 \left(1 - e^{-\frac{2t}{R \times C_{P1}}}\right). \tag{9}$$

Substituting (2) into (9), the relationship between the current i and time t can be written as

$$i = \frac{q_0 \times e^{-\frac{2t}{R \times C_{P1}}}}{R \times C_{P1}} = \frac{V_{\mathrm{PT}} \times e^{\frac{-2t}{R \times C_{P1}}}}{R}. \tag{10}$$

Equation (10) illustrates the relationship between the current flowing through the *RC* loop and time, with its corresponding plot in Fig. 4. This current is influenced by several factors, including the voltage across the PT, denoted as V_{PT}, the loop resistance, R, and the intrinsic PT capacitance, C_{P1}. A higher resistance value leads to a longer charge release time. In our design, the total simulated resistance in the *RC* loop is approximate $10\,\Omega$, and the measured intrinsic capacitance is 300 pF. Fig. 4 depicts three cases where V_{PT} is set to 3 V, 4 V, and 5 V. It is evident from the graph that a higher V_{PT} results in a longer charge release time. Specifically, when V_{PT} is 5 V, the longest charge release time is 7 ns. Considering the 8-stage flipping process, the total flipping time for a single sub-PT is calculated as $7\,\mathrm{ns} \times 8 = 56\,\mathrm{ns}$. When all eight split-electrodes are flipped in sequence, sharing the identical flying capacitors, and without accounting for any time delay between each sub-PT, the total flipping time can be calculated as $56\,\mathrm{ns} \times 8 = 448\,\mathrm{ns}$.

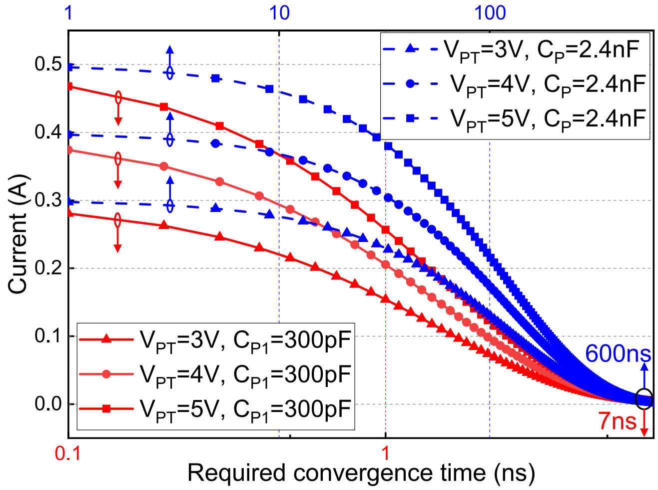


Fig. 4. Current plot of proposed 3SHC and typical rectifiers versus the time in the RLC loop.

However, when the PT is a monolithic electrode, considering the same flipping efficiency, the on-chip capacitance would be 8 × larger than the proposed design. Considering that the intrinsic capacitance of the PT would be 2.4 nF, this requires at least $8 \times 2.4 = 19.2\,\mathrm{nF}$ as the flying capacitance, which is impractical to integrate them on the chip. On the other hand, when the C_P is 2.4 nF, the flowing current of the typical SSHC rectifier versus the time is also shown in Fig. 4, top axis. It shows that the required time for one-stage flipping is about 600 ns. Considering the 8-stage bias-flip process, the total required flipping time would be $600\,\mathrm{ns} \times 8 = 4.8\,\mu\mathrm{s}$, which is much larger than the required flipping time of the proposed rectifier. Therefore, the flipping period of the proposed design would not occupy too much time and is even shorter than the flipping time of a typical SSHC rectifier due to smaller intrinsic capacitance.

III. System Architecture and Circuit Implementation

A. *System Architecture*

Fig. 5 provides an overview of the proposed system architecture for the fully integrated 3SHC rectifier. The input section comprises 8 sub-PTs, PT_1 to PT_8, while the bias-flip

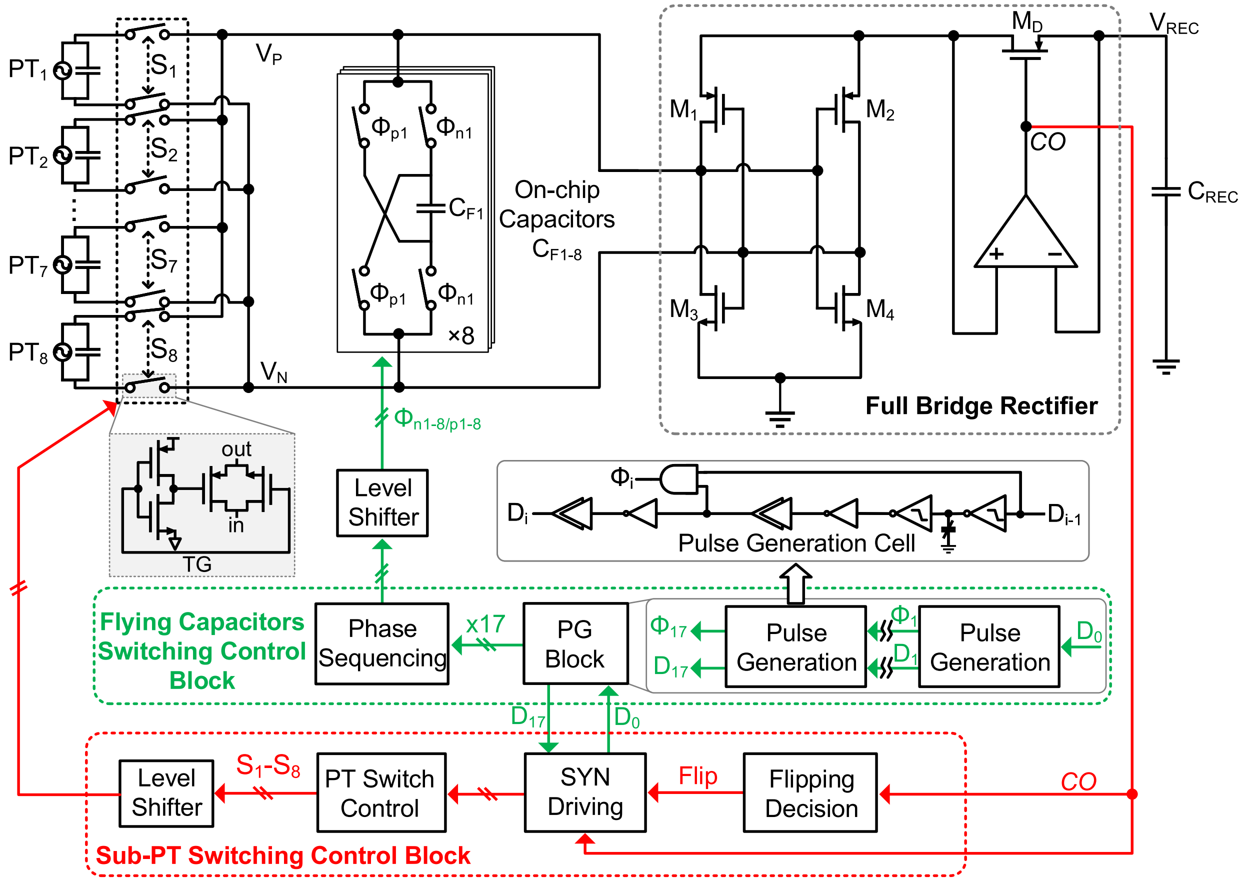


Fig. 5. System architecture of the proposed 3SHC rectifier.

rectifier incorporates eight on-chip flying capacitors, C_{F1} to C_{F8}. The system includes three main blocks: a FBR block, a flying capacitors switching block, and a sub-PT switching control block. The bottom block illustrates the generation of switching control signals, namely, S_1 to S_8, responsible for controlling the connections to the sub-PTs. The “cut-off” signal, denoted as CO and generated by the comparator of the active diode, is initially directed to a flip decision block, indicating the initiation of the flipping process. A synchronized flip signal is then forwarded to the SYN driving block, which in turn drives the PT switching control block to generate S_1 to S_8, controlling the PT switches after level shifters as displayed on the left side of Fig. 5.

Simultaneously, the SYN driving block generates a synchronized signal, D_0, to drive the pulse generation (PG) block, as shown in the middle pathway. The PG block generates 17 pulses sequenced by the phase sequencing block. After passing through the level shifters, these pulses control the 17 switches, namely, Φ_{n1-n8} and Φ_{p1-p8}, within the bias-flip rectifier. The final synchronized signal, D_{17}, is recognized as the indication of the end of the flipping process and is relayed to the PT switching control block. At this point, when D_{17} is generated, all eight sub-PTs are reconnected in parallel, signaling the system’s transition to the EH state.

B. Flipping Decision Generation of sub-PT Electrodes

Fig. 6 shows the circuit implementation details of the flipping decision block, SYN driving block, and PT switch control block as shown in the bottom of Fig. 5. The CO generated by the comparator of the active in Fig. 5 is fed to the flipping decision block firstly to decide the flipping starting moment. When the CO generates a rising edge, the PT flipping moment is coming. Then, the a_0 to a_2 is caused by the counter in the bottom PT switch control block. The c_0 to c_2 represent PT-split numbers, where the maximum configured number is 8. The a_0 to a_2 combined with c_0 to c_2 are used to decide which sub-PT is flipped. When the first flip control signal is triggered, it is fed to the SYN driving block to generate the synchronized signal D_0 to start the first PG block as shown in the middle of Fig. 6. Where the input D_{17} is generated by the last PG block, indicating the ending moment of flipping. By using the 3-bit counter and 3–8 decoder, the PT switch block generates the final switch driving signals S_1 to S_8 to decide, which connects the corresponding sub-PT to the shared eight flying capacitors for each sub-PT voltage flipping.

C. Pulse Sequencing

Fig. 7 illustrates the pulse sequencing cell and the generation of the PT polarity indicating signal, PN. Given the varying

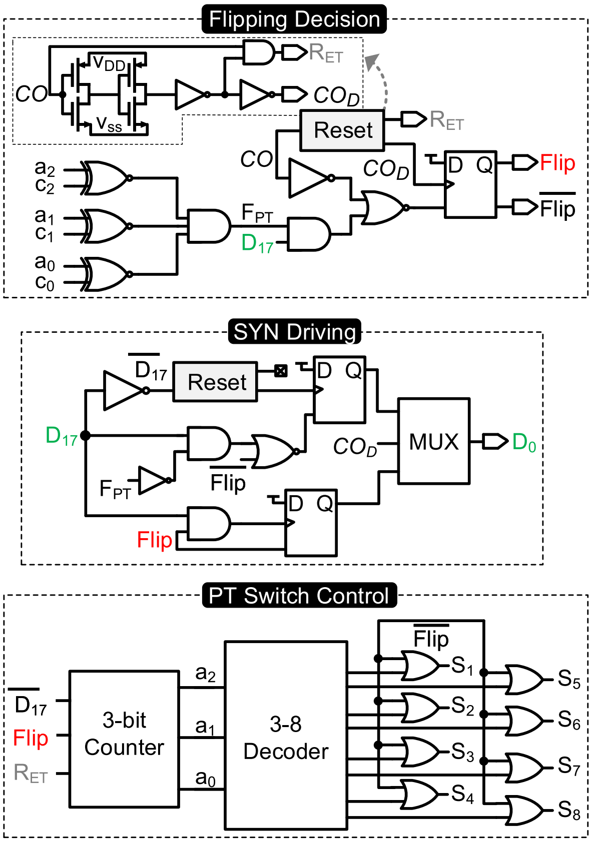


Fig. 6. Circuit implementation details of the flip decision, SYN drive, and PT switch control blocks.

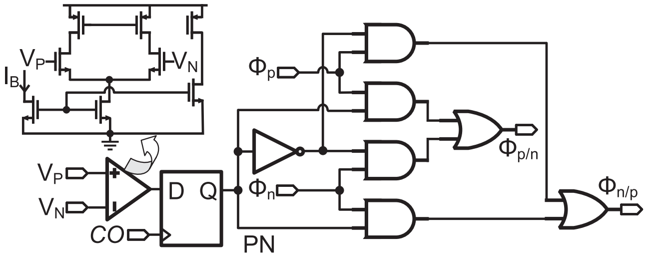


Fig. 7. Pulse sequencing cell and PT polarity signal, PN, generation.

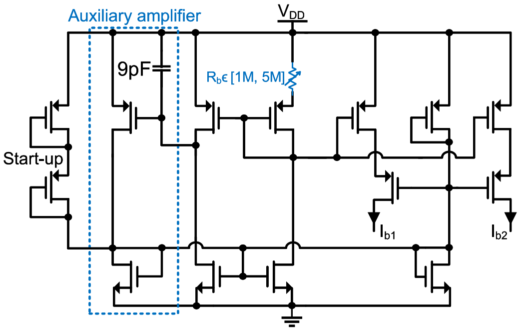


Fig. 8. Constant gm current source for biasing current generation.

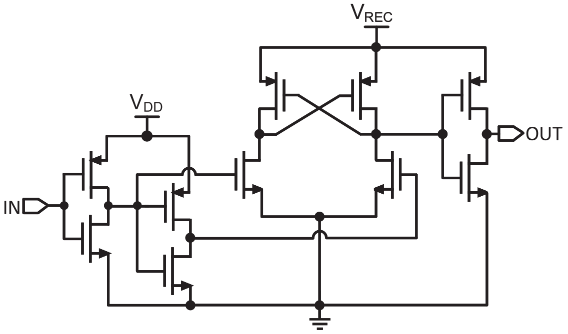
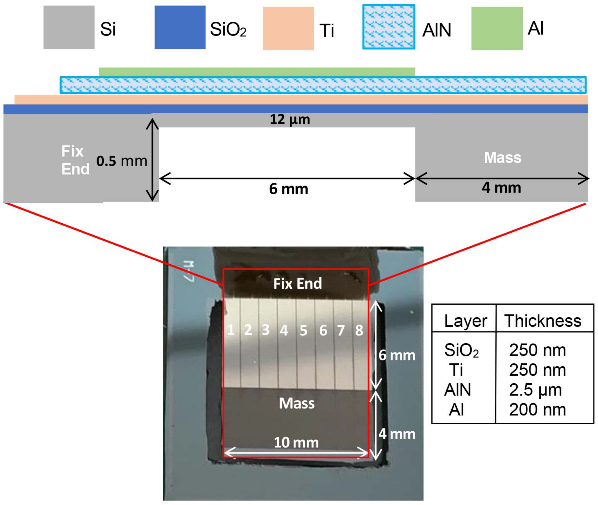


Fig. 9. System level shifter for driving switches.



Layer	Thickness
SiO_2	250 nm
Ti	250 nm
AlN	2.5 µm
Al	200 nm

Fig. 10. Side section and zoomed-in photograph of the fabricated split-electrode MEMS PT.

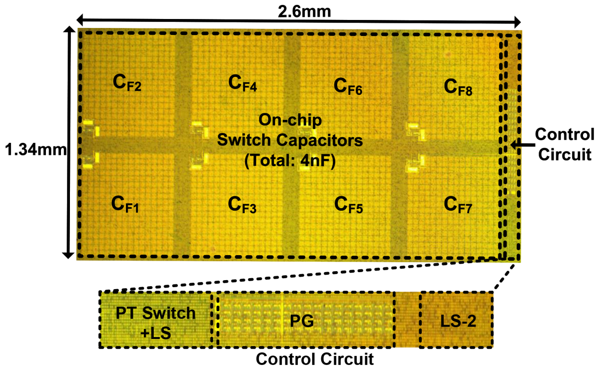


Fig. 11. Chip micrograph.

polarity of the PT, it is crucial to detect PN polarity to determine the activation of switches Φ_p or Φ_n. A high PN signal signifies that V_{PT} is positive, while a low PN signal indicates the opposite. The PN signal is generated using a differential pair, as depicted on the left side of Fig. 7. Within the pulse sequencing block, there are nine digital pulse sequencing cells for Φ_{p1-8} and Φ_{n1-8}, where each digital pulse sequencing cell is shown on the right side of Fig. 7.

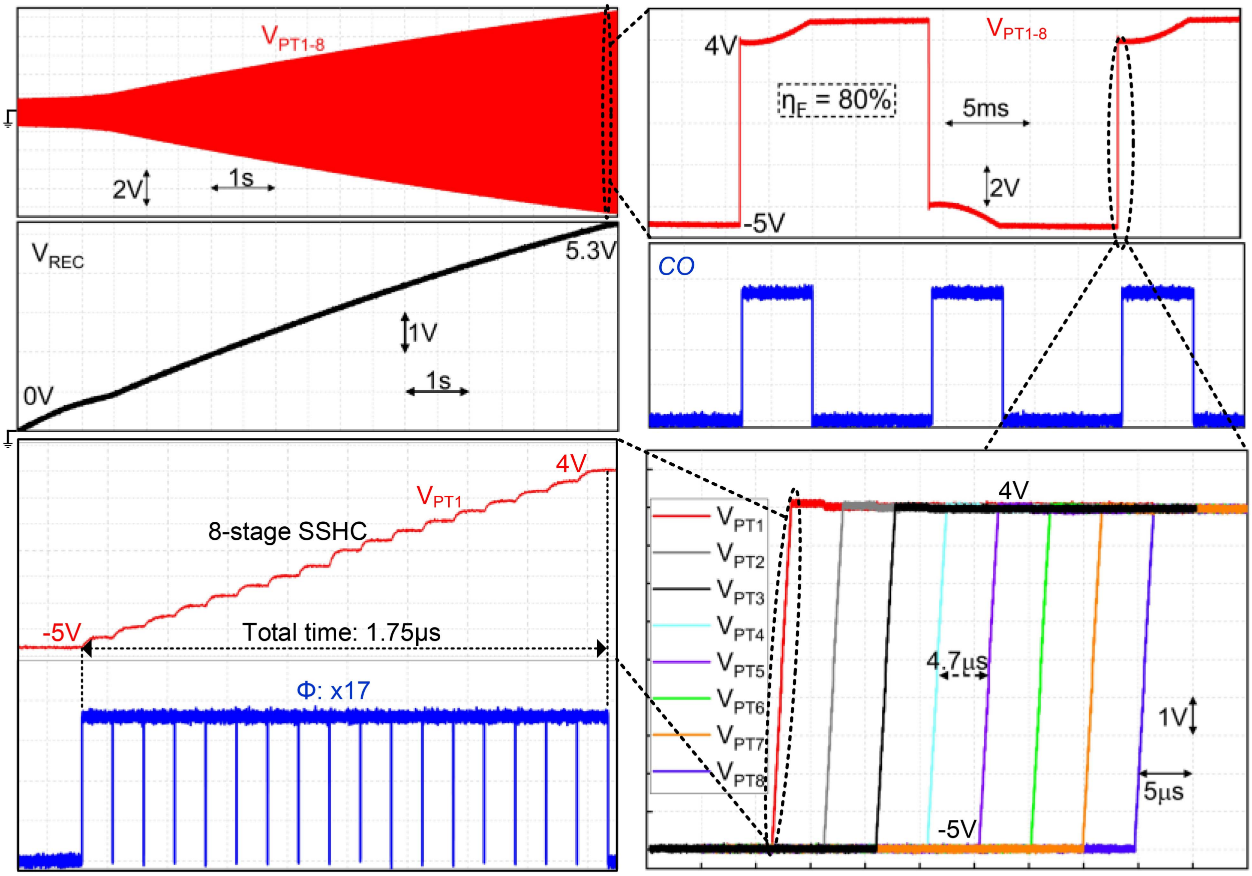


Fig. 12. Measured waveform of the voltage across each sub-PT from startup and measured transient rectified voltage (top-left); zoomed-in PT voltage and CO signal (top-right); zoomed-in eight sub-PT voltage during the flipping moment (bottom-right) and the 17 switching control phases of the 3SHC rectifier (bottom-left).

D. Biasing Current Generation

Fig. 8 showcases using an on-chip constant-gm bias circuit to generate the necessary biasing currents. The primary objective of the constant-gm bias circuit is to provide a consistent biasing current despite process variations and changes in operating conditions. To accomplish this, the biasing resistor R has been designed with tunability, ranging from $1\ \mathrm{M}$ to $5\ \mathrm{M}$ in increments of $1\ \mathrm{M}$. This allows for precise adjustment of R to maintain the desired biasing current level, effectively mitigating the impact of process variations. Furthermore, an auxiliary amplifier has been integrated into the biasing circuit to enhance the power supply rejection ratio. This addition makes the biasing circuit less susceptible to fluctuations in the power supply voltage, ultimately improving the stability of the generated biasing currents. The measured induced biasing current is around $7.5\ \mathrm{nA}$.

E. Level Shifters

To fully turn ON or turn OFFthe switches, a level shifter is typically required, as shown in Fig. 9. The level shifter enables the control of switches or components to operate at different voltage levels. The EH system involves two voltage sources: V_{DD}, a lower voltage for powering low-voltage transistors, and V_{REC}, the highest voltage generated by a rectifier. A level shifter is employed to bridge this voltage gap. Its purpose is to take the control signal from V_{DD} and adjust it to a higher voltage level compatible with components powered by V_{REC} to control the switches effectively.

IV. MEASURED RESULTS ANALYSIS

The fabrication of the front-end split-electrode MEMS PT was carried out in our in-house Else Kooi Laboratory cleanroom. The MEMS PT consists of a Si-based single-clamped beam with a mass attached to the free end to amplify the vibration. On top of the cantilever, the Aluminum Nitride (AlN), the piezoelectric layer, is applied to convert the energy from the mechanical to the electrical domain. Two electrodes, Titanium (Ti) and Aluminum (Al) are placed on both sides of the piezoelectric layer to conduct current as shown in Fig. 10. The MEMS split-PT was mounted on a PCB, which vibrates with the shaker. The eight paired outputs of the MEMS PT are connected to the PCB through wire bonding. Each sub-capacitance unit in this MEMS device measures approximately $300\ \mathrm{pF}$. The measured resonant frequency of this MEMS device is around $46\ \mathrm{Hz}$.

The proposed 3SHC rectifier was fabricated in a 180-nm BCD process. In Fig. 11, the on-chip flying capacitors, denoted as C_{F1} through C_{F8}, collectively contribute to a total capacitance of $4\ \mathrm{nF}$. Each flying capacitor has a capacitance of $500\ \mathrm{pF}$. The chip occupies an active area of $3.484\ \mathrm{mm}^2$.

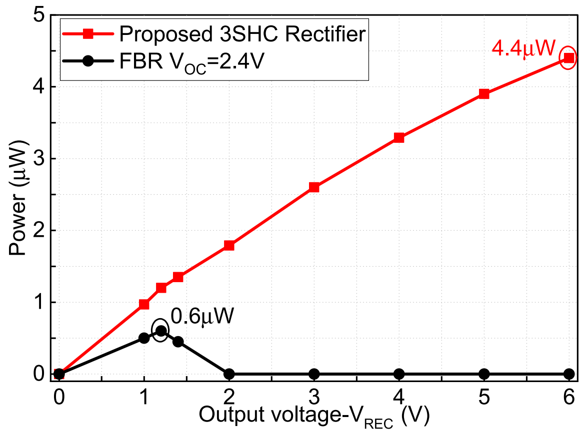


Fig. 13. Measured output power of 3SHC and FBR versus different rectified voltages.

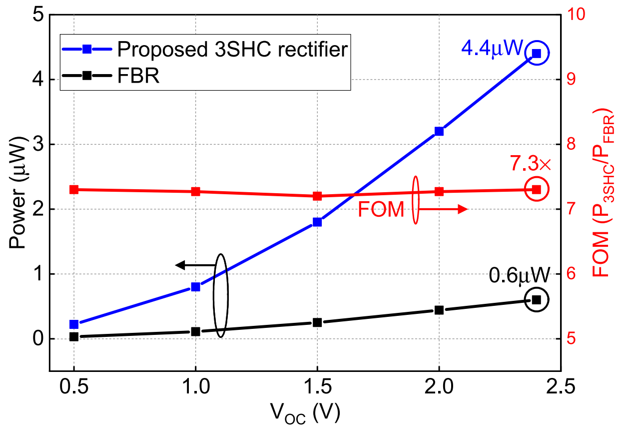


Fig. 14. Measured output power and FOM comparison of 3SHC and FBR versus different open circuit voltages.

Fig. 12 displays the measured voltage across each sub-PT. The top-left sub-figure shows the PT voltage and the rectified output voltage, ranging from 0 V to 5.3 V. On the top right, a zoomed-in view of the PT voltages, $V_{\mathrm{PT}1-8}$, is shown, which varies between -5 V and 4 V, signifying an 80% voltage flipping efficiency, $\eta_F = \frac{FlippedVoltage}{RectifiedVoltage}$. This indicates that the proposed 3SHC rectifier, based on the split-electrode design, does not subject the system to high voltage stress, resulting in a high flipping efficiency. In comparison, a similar SSHC rectifier reported in [30] achieved a 71% flipping efficiency, mainly due to thick oxide transistors, which introduced high-voltage stress and more considerable parasitic losses. The rectifier cut-off (CO) signal is also presented. When CO generates a rising edge, the PT voltage flips. The flipping moment occurs too rapidly to be observed in this figure, so a zoomed-in version of 8 sub-PT voltage during flipping, V_{PT1-8}, is provided at the bottom right. The voltage across each sub-PT is flipped sequentially, with a time interval of approximately 4.7 μs. The first sub-PT flipping moment is highlighted in the bottom left. It comprises 17 pulses, and the total measured flipping time is about 1.75 μs, which is longer than the theoretical analysis due to parasitic resistance and capacitance. However, this short time can be almost ignored compared with the half vibration cycle 10.87 ms. These 17 pulses are generated repeatedly eight times for each of the eight split electrodes.

Fig. 13 shows the measured output power over a range of the rectified output voltage, V_{REC}. The proposed 3SHC rectifier achieves 4.4 μW of output power at $V_{\mathrm{REC}} = 6$ V when the open circuit voltage from the fabricated MEMS PT, V_{OC}, is 2.4 V. In comparison, the conventional FBR circuit only yields 0.6 μW. This demonstrates a 7.3× power enhancement achieved by the proposed 3SHC rectifier.

The output power of the proposed 3SHC and FBR rectifiers with different open circuit voltage V_{OC} are measured and shown in Fig. 14. When the V_{OC} varies from 0.5 V to 2.4 V, the maximum output power of the proposed 3SHC rectifier is up to 4.4 µW while FBR has only 0.6 µW output power. Fig. 14 also shows the figure of merit (FOM) of the power comparison on the right axis. It offers a 7.3× power enhancement compared with the FBR, which is the same result illustrated in Fig. 13. Fig. 15 shows the measured open circuit voltage of the MEMS PT versus the excitation frequency. It shows that the natural frequency of the in-house fabricated MEMS PT is 46 Hz.

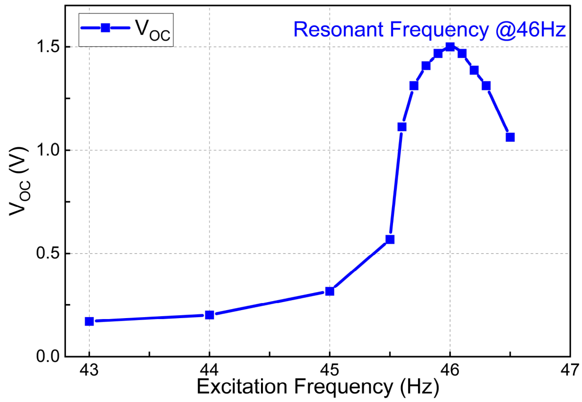


Fig. 15. Measured output open circuit voltage versus varying frequency.

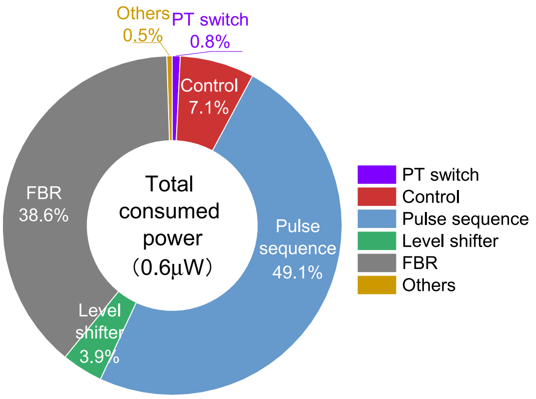


Fig. 16. System total power consumption analysis.

Fig. 16 presents the power consumption breakdown of the system. The total power consumption during the steady operation

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUS WORK

	JSSC'17 [25]	JSSC'19 [30]	TPE'21 [31]	TPE'22 [6]	TPE'22 [32]	TPE'23 [2]	JSSC'23 [26]	**This work**
Technology	180 nm	180 nm	Discrete	Discrete	Discrete	Discrete	180 nm	180 nm
Technique	SSHC	SE-SSHC	SSDCI	FBR	SSHI	SECE	SPDC	**3SHC**
C_P (nF)	45	1.94	100	N/R	170*	130	88	**2.4**
Frequency (Hz)	92	219	22	153	77.5	46	100	**46**
Inductor	No	No	Yes	No	Yes	Yes	No	**No**
V_{OC}(V)	2.5	2.5	N/R	0.4-15	3.9-5.8	15*	1-2	**2.4**
Chip Area (mm^2)	2.9	3.9	Discrete	Discrete	Discrete	Discrete	0.7	**3.49**
Power Consumption	1.7μW	2.9μ W	2-6μW	12-22μW	N/R	341.6mW*	3μW	**0.6μW**
Fully Integrated	No	Yes	No	No	No	No	Yes	**Yes**
Flipping Efficiency-η_F	80%	71%	No	No	66%*	No	80%	**80%**
P_{IC}/P_{FBR}	270%	210%-520%	300%	100%	322%	212%	278%-488%	**730%**

*: Estimated, N/R: Not reported.

is around $0.6\ \mu$W. Notably, the pulse sequence and FBR blocks account for most of the power consumption, with 49.1% and 38.6%, respectively. Both incorporate comparators, pivotal in PT polarity detection and current zero-crossing moment detection. Subsequently, the logic control and level shifter blocks consume 7.1% and 3.9%, respectively, of the total power consumption. It's worth noting that since the proposed design can be implemented using standard CMOS technology, the output PT voltage is at least 4× lower than in [30] the leakage current is significantly lower.

Table I provides a comprehensive comparative analysis of the proposed 3SHC rectifier compared to state-of-the-art designs. What sets our work apart is its full integration capability without requiring external inductors or off-chip flying capacitors. Leveraging the advantages of standard CMOS technology for chip fabrication, our design achieves the distinction of exhibiting the lowest power consumption among the solutions listed. The utilization of standard CMOS, as opposed to HV CMOS, not only ensures efficient integration but also brings about benefits such as reduced layout area, lower on-resistance, and simplified circuitry, contributing to overall improved performance and cost-effectiveness.

V. CONCLUSION

This article proposes a fully integrated 3SHC rectifier. This design sequentially connects an in-house fabricated 8-split-electrode PT to a shared fully on-chip 8-stage SSHC rectifier, effectively flipping each sub-PT's voltage with small capacitors. Notably, this approach eliminates the need for high-voltage transistors since the PTs are scanned in parallel rather than series. The proposed 3SHC rectifier can be realized using standard CMOS transistors, resulting in 80% flipping efficiency and 730% power extraction enhancement. In future works, the authors aim to explore the development of a fully integrated SSHC rectifier specifically designed to address the challenge posed by the large intrinsic capacitance of a standard PT. The focus will be devising a solution to efficiently flip the large intrinsic capacitance, contributing to advancing EH technologies.

ACKNOWLEDGMENT

The authors would like to thanks Europractice for support in MPW and design tools, and Zu-Yao Chang from TU Delft for his valuable technical support.

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Xinling Yue (Graduate Student Member, IEEE) currently working toward the Ph.D. degree in microelectronics with Electronic Instrumentation Laboratory, Delft University of Technology, Delft, the Netherland.

She joined the Electronic Instrumentation Laboratory, Delft University of Technology, the Netherlands in 2020. Her current research interests are energy-efficient power management integrated circuits and systems, which include energy harvesting, ac/dc rectifiers, dc/dc converters, and maximum power point tracking techniques.

Ms Yue was a recipient of the the Best Student Paper Award at 2022 IEEE International Conference on Electronics Circuits and Systems (ICECS), Student Travel Grant Awards in 2022 IEEE International Symposium on Circuits and Systems (ISCAS) and 2023 International Solid-State Circuits Conference (ISSCC), 2023-2024 Solid-State Circuits Society (SSCS) Predoctoral Achievement Award.

Jiarui Mo (Student Member, IEEE) received the B.Sc. degree in measuring and testing technology and instruments from Chongqing University, Chongqing, China, in 2017, and the MSc. degree in microelectronics from Delft University of Technology, Delft, The Netherlands, in 2019. He is currently working toward the Ph.D. degree with the Department of Electronic Components, Technology and Materials (ECTM), Delft University of Technology, Delft, The Netherland.

In 2020, he worked with Prof. Zandbergen’s research group as a MEMS engineer in Faculty of Applied Physics of Delft University of Technology. His main research topics are harsh environment sensing and monolithic integration of SiC devices. Additionally, he is also interested in piezoelectric device development. This project is funded by the European Consortium project “Intelligent Reliability 4.0.”

Zhiyuan Chen (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Macau (UM), Macao, China, in 2011, 2013, and 2018, respectively.

Since 2018, he has been with the School of Microelectronics, Fudan University, Shanghai, China, where he is currently an Associate Professor. His research interests include ultra-low power management systems, solar and piezoelectric energy harvesting (EH) systems.

Dr. Chen is a member of the Technical Committee of Power and Energy Circuits and Systems in IEEE Circuits and Systems Society and has been the Review Committee Member of the IEEE International Symposium on Circuits and Systems since 2021. He was a recipient of the Macau Science and Technology Development Fund (FDCT) Postgraduates Award and Shanghai Super Postdoctoral Award.

Sten Vollebregt (Senior Member, IEEE) received the B.Sc. and M.Sc. (cum laude) degrees in electrical engineering from Delft University of Technology, Delft, The Netherland, in 2006 and 2009, respectively.

For his master thesis, he investigated the growth of carbon nanotubes with NanoLab, Newton, MA, USA and AIXTRON, Cambridge, U.K. In 2014, he completed his Ph.D. thesis in the Microelectronics Department of the Delft University of Technology on the low-temperature high-density growth of carbon nanotubes for application as vertical interconnects in 3-D monolithic integrated circuits. After obtaining his Ph.D., he held a post-doc position on the waferscale integration of graphene for sensing applications together with the faculty of Mechanical Engineering and several industrial partners. During this research, he developed a unique transfer-free wafer-scale CVD graphene process. Since 2017, he has been an Assistant Professor with the Laboratory of Electronic Components, Technology and Materials of the Delft University of Technology, where his research focuses on the integration of emerging electronic materials into semiconductor technology for sensing applications. His research interests are (carbonbased) nanomaterials, 3-D monolithic integration, wide-bandgap semiconductors, and (harsh) environmental sensors.

Guoqi Zhang (Fellow, IEEE) received the Ph.D. degree in stability of composite structure from Delft University of Technology, Delft, the Netherlands, in 1993.

His research interest covers multilevel heterogeneous system integration and packaging; wide band gap semiconductors sensors and components; multiphysics and multiscale modeling of micro/nanoelectronics; digital twin for mission critical multifunctional electronics components and systems.

He authored/co-authored more than 400 scientific publications; serves as deputy Director of European Center for Micro- and Nanoreliability (EUCEMAN); co-chair of Advisory Board of International Solid State Lighting Alliance (ISA); secretary general of ITRW (International Technology Roadmap of Wide bandgap Semiconductors). He has worked for NXP Semiconductors as Senior Director of Technology Strategy until 2009, Philips Research Fellow until May 2013.

Dr. Zhang is IEEE Fellow, chair Professor for "Micro/Nanoelectronics System Integration and Reliability" of Delft University of Technology.

Sijun Du (Senior Member, IEEE) received a First Class in B.Eng. degree in electrical engineering from University Pierre and Marie Curie (UPMC), Paris, France, in 2011, and a Distinction in M.Sc. degree in electrical and electronics engineering from Imperial College, London, U.K., in 2012. He started his Ph.D. research in 2014 and received the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in 2018.

He worked with the Laboratoire d'Informatique de Paris 6 (LIP6), University Pierre and Marie Curie, Paris, France, and then worked as a digital IC engineer in Shanghai, China, between 2012 and 2014. He was a summer engineer intern at Qualcomm Technology Inc., San Diego, CA, USA, in 2016. He was a visiting scholar with the Department of Microelectronics, Fudan University, Shanghai, China, in 2018. He was a postdoctoral Researcher with the Berkeley Wireless Research Center (BWRC), Department of Electrical Engineering and Computer Sciences (EECS), University of California, Berkeley, CA, USA between 2018 and 2020. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, where he is currently an Assistant Professor. His current research is focused on energy-efficient integrated circuits and systems, including power management integrated circuits (PMIC), energy harvesting, wireless power transfer, and dc/dc converters used in Internet-of-Things (IoT) wireless sensors, wearable electronics, biomedical devices, and microrobots.

Dr. Du was a recipient of the Dutch Research Council (NWO) Talent Program-VENI grant in the 2021 round. He was a co-recipient of the Best Student Paper Award in IEEE ICECS 2022. He is a technical committee member of the IEEE Power Electronics Society (PELS) and IEEE Circuits and Systems Society (CASS). He has been a committee member of the IEEE ISSCC Student Research Preview (SRP) since 2023.