Protecting SiC JFET From Gate Overstress in GaN/SiC Cascode Device Without Compromising Switching Performance

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***Abstract*—The GaN/SiC cascode device featuring a low-voltage (LV) enhancement-mode (E-mode) GaN high-electron-mobility transistors (HEMT) and a high-voltage (HV) SiC JFET has the unique capability of delivering thermally stable threshold voltage, avalanche capability, zero reverse recovery charge ($Q_{\rm rr}$), and fast switching speed simultaneously. However, the lack of avalanche capability in the LV GaN HEMT presents a challenging issue, namely the negative gate overstress of the HV SiC JFET during the switching process, which raises reliability concerns. A clamping unit based on a Si Zener diode can provide gate protection for JFET but inevitably increases the switching loss significantly due to the reverse-recovery process of the Si Zener diode. This article presents a new gate protection design based on a Si bi-directional Zener diode that can clamp the gate voltage of JFET without introducing the reverse-recovery process. Therefore, the gate of JFET can be protected while the switching performance of the cascode device is not compromised, as verified by the experiment results.**

***Index Terms*—Cascode, enhancement-mode (E-Mode), gallium nitride (GaN) high-electron-mobility transistors (HEMTs), gate protection, reverse recovery, silicon carbide (SiC) JFET, switching loss.**

I. Introduction

POWER devices based on wide-bandgap (WBG) semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC), are suitable for the next-generation high-efficiency and high-power-density converters, mainly owing to their superior properties than the Si-based counterparts, such as higher operation temperature, faster switching speed, and lower specific ON-resistance [1], [2].

SiC-based power devices such as SiC MOSFETs and SiC JFETs have been intensively developed, targeting at applications of high voltage levels (i.e., 650 V and above) [3], [4]. For SiC MOSFETs, the high trap density at the SiO_2/SiC interface of the gate oxide reduces the channel mobility significantly, thus increasing the channel resistance and conduction loss [5]. SiC JFET does not suffer from the high channel resistance issue, but its depletion-mode (D-mode) gate control is not desired in power electronics applications that demand fail-safe operation [6], [7]. Combining a low-voltage (LV) enhancement-mode (E-mode) Si MOSFET with a high-voltage (HV) D-mode SiC JFET in a cascode Si/SiC configuration can realize an HV E-mode power device with low conduction loss [see Fig. 1(a)] [8], [9]. The cascode Si/SiC devices are already commercially available at voltage levels of 650 V and 1.2 kV [10].

Meanwhile, GaN E-mode high-electron-mobility transistors (HEMTs) have been widely available and commercialized with products at both low- and medium-voltage levels ranging from 15 to 650 V [2], [11], [12]. Recently, a new HV GaN/SiC cascode device combining the merits of an LV E-mode GaN HEMT and an HV D-mode SiC JFET has been proposed [6], [13], [14], [see Fig. 1(b)]. Compared with the cascode Si/SiC device, the LV Si MOSFET is replaced by an LV GaN HEMT, which brings the benefits of faster switching speed, thermally stable threshold voltage ($V_{\rm TH}$), and most importantly, zero reverse-recovery charge ($Q_{\rm rr}$).

However, replacing the LV Si MOSFET with an LV GaN HEMT may lead to a challenging issue, namely the gate overstress of HV SiC JFET during the switching process [6], [13], [15]. Due to the lack of avalanche capability in the LV GaN HEMT, the drain-source voltage of GaN HEMT ($V_{\rm DS\text{-}GaN}$) cannot be clamped during the switching process. As a result, the gate of the HV SiC JFET could be overstressed because the gate-source voltage of SiC JFET ($V_{\rm GS\text{-}SiC}$) is the same as $V_{\rm DS\text{-}GaN}$ [16], [17]. In comparison, the JFET's gate in the cascode Si/SiC device is protected against overstress, as the $V_{\rm GS\text{-}SiC}$ can be clamped by the LV Si MOSFET with avalanche capability [18], [19], [20].

To protect the gate of HV SiC JFET in GaN/SiC cascode device, a flip-chip co-packaging structure [13], [15] has been proposed to reduce the parasitic interconnection inductance between the SiC JFET and GaN HEMT to suppress the oscillation and also decrease the magnitude of $V_{\rm DS\text{-}GaN}$ during the switching process. In addition, in-depth analysis of the GaN/SiC cascode device's switching process reveals that the internal gate resistance of the high-voltage SiC JFET and can also lead to

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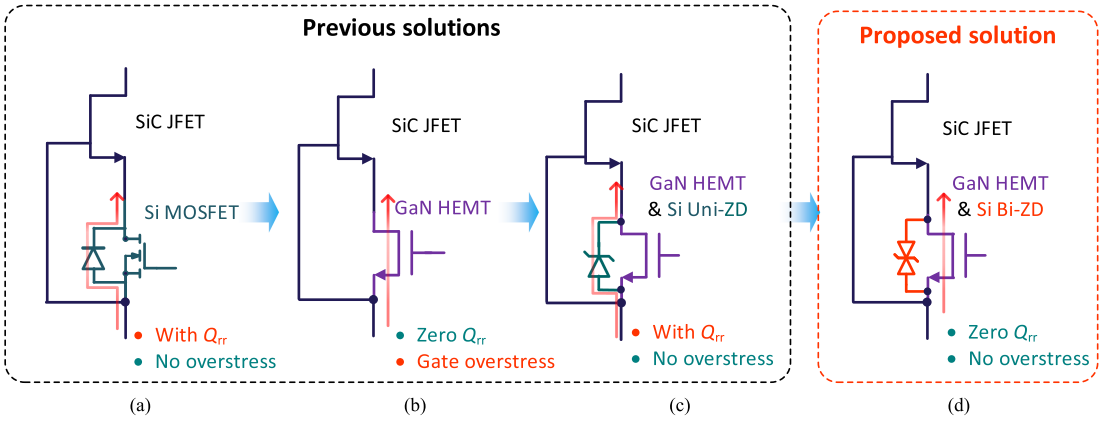

Fig. 1. Configurations of previous solutions and the proposed solution. (a) Cascode Si/SiC device. (b) Cascode GaN/SiC device. (c) Cascode GaN/SiC with a Uni-Zener diode (ZD). (d) Cascode GaN/SiC with a Bi-ZD. The proposed solution based on Bi-ZD provides protection for JFET's gate without introducing Q_{rr}.

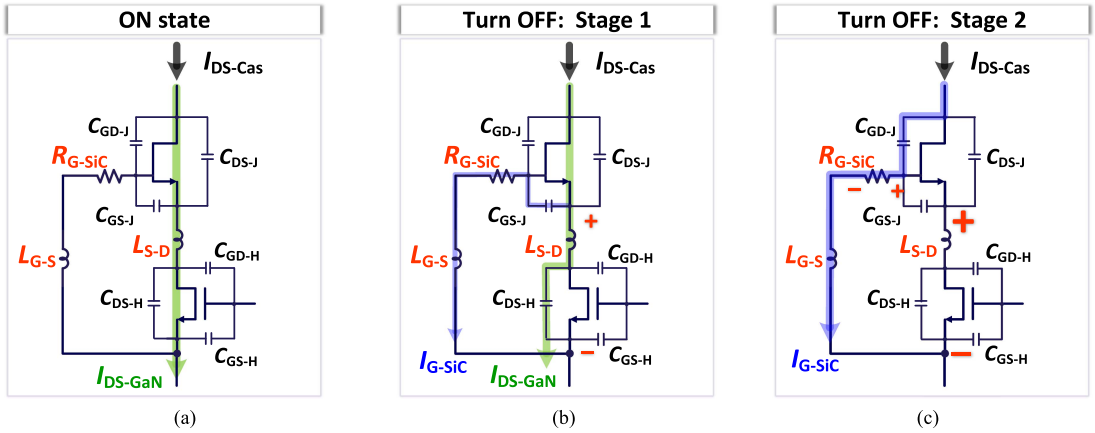

Fig. 2. Turn-OFF process of the GaN/SiC cascode device. (a) ON state. (b) Turn-OFF process, stage 1. (c) Turn-OFF process, stage 2. In stage 2, JFET's gate voltage can be elevated due to the presence of internal gate resistance $R_{\mathrm{G\text{-}SiC}}$. As a result, $V_{\mathrm{DS\text{-}GaN}}$ of HEMT must be increased accordingly to ensure the JFET's channel can be pinched OFF.

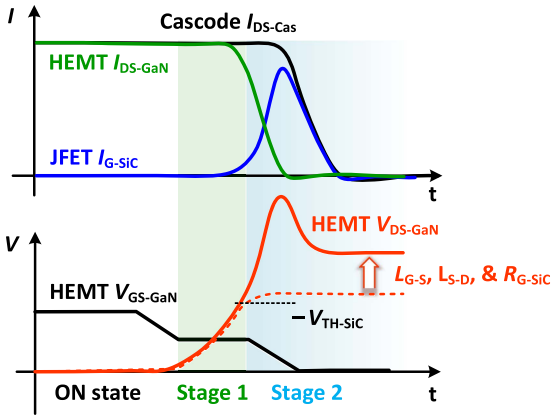

Fig. 3. Schematic voltage and current waveforms of the GaN/SiC cascode device during the turn-OFF process. The parasitic interconnection inductance ($L_{\mathrm{G\text{-}S}}$, and $L_{\mathrm{S\text{-}D}}$) and JFET's gate resistance $R_{\mathrm{G\text{-}SiC}}$ results in $V_{\mathrm{DS\text{-}GaN}}$ overshoot.

$V_{\mathrm{DS\text{-}GaN}}$ overshoot and the consequent gate overstress of JFET. As a result, a ZD is still needed for reliable $V_{\mathrm{DS\text{-}GaN}}$ clamping, and thus protecting the SiC JFET from gate overstress even after copackaging [15], [21], [22]. The previously applied regular uni-directional ZD (Uni-ZD) is a heavily doped Si pn-junction with a forward turn-on voltage of ~0.7 V, which is lower than the reverse-conduction turn-on voltage of a GaN HEMT. Therefore, during the reverse-conduction phase of the GaN/SiC cascode device, current would flow through the forward-biased Si pn-junction of the Uni-ZD, as shown Fig. 1(c). As a result, when the cascode device switches from the reverse-conduction mode to the forward-blocking mode, the Uni-ZD would experience a reverse-recovery process to sweep out the excess minority carriers in the Si pn-junction, leading to a prolonged switching process with exacerbated switching loss [23], [24].

In this article, a new protection design against the gate overstress of the SiC JFET is presented based on the use of a bidirectional Zener diode (Bi-ZD) in parallel with the LV GaN HEMT [see Fig. 1(d)]. With the Bi-ZD, $V_{\mathrm{DS\text{-}GaN}}$ in GaN/SiC cascode device can be effectively clamped, thereby protecting the JFET's gate against overstress during the switching process. Meanwhile, the Bi-ZD also forces the reverse-conduction current to flow through the LV GaN HEMT, which exhibits zero Q_{rr} and high reliability when operated in reverse-conduction mode [25], [26]. As a result, the gate overstress of the HV SiC JFET can be

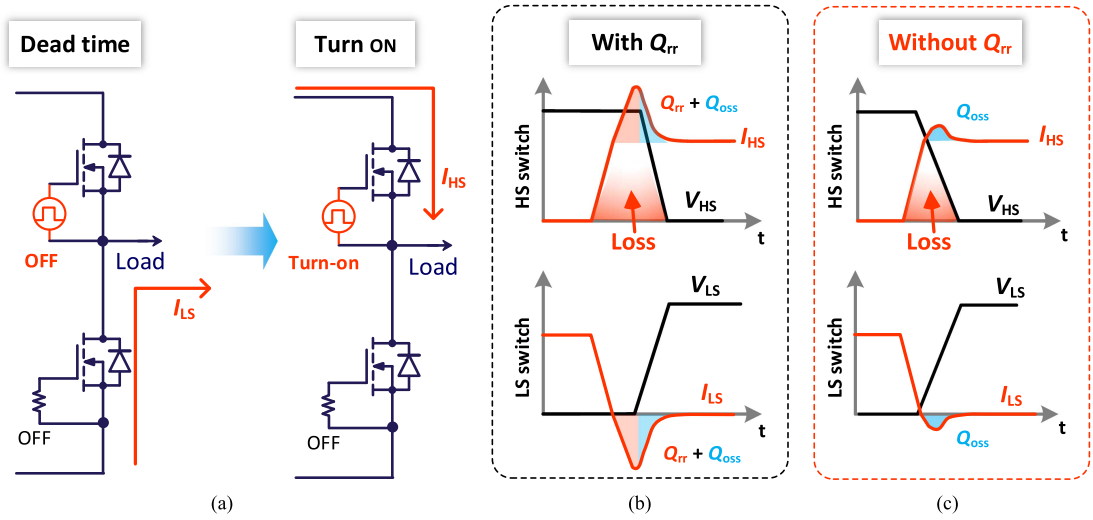

Fig. 4. Half-bridge circuit in hard-switching operation. (a) Schematic description of circuit operation during the turn-ON of the HS switch. (b) Voltage and current waveforms in the HS and LS switch with $Q_{\rm rr}$. (c) Voltage and current waveforms without $Q_{\rm rr}$. Eliminating $Q_{\rm rr}$ reduces switching loss significantly.

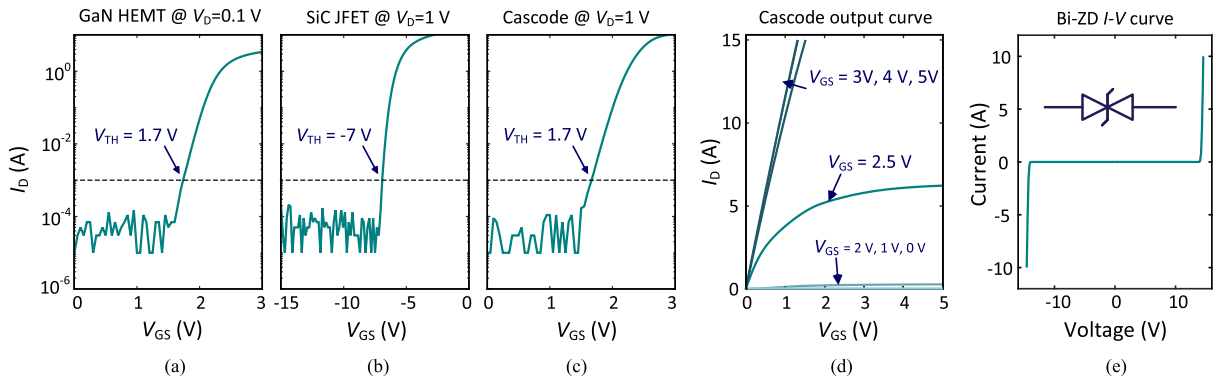

Fig. 5. Transfer and output characteristics of each part and the cascode GaN/SiC device. (a) Transfer curve of the GaN HEMT. (b) Transfer curve of the SiC JFET. (c) Transfer curve of the cascode device. (d) Output curve of the cascode device. (e) I-V curve of the Bi-ZD.

prevented, while the switching performance of the GaN/SiC cascode device is not compromised as no $Q_{\rm rr}$ is introduced.

II. Gate Overstress Issue and the Proposed Protection Solution

A. Gate Overstress Issue of the SiC JFET

Due to the absence of avalanche capability in the LV GaN HEMT, the gate of HV SiC JFET of the GaN/SiC cascode device could be overstressed during the turn-OFF process. Fig. 2 illustrates the turn-OFF transients of the GaN/SiC cascode device, demonstrating the impact of parasitic interconnection inductances ($L_{\rm G\text{-}S}$ and $L_{\rm S\text{-}D}$) and JFET's internal gate resistance $R_{\rm G\text{-}SiC}$. The schematic current and voltage waveforms during the turn-OFF process are depicted in Fig. 3, where $I_{\rm DS\text{-}Cas}$ and $I_{\rm DS\text{-}GaN}$ are the drain-source current of the cascode device and HEMT respectively, and $I_{\rm G\text{-}SiC}$ is the current in the JFET's gate branch.

After HEMT is turned OFF, $V_{\rm DS\text{-}GaN}$ will increase and part of the current is diverted into the gate branch of JFET [see Fig. 2(b), stage 1]. When $V_{\rm DS\text{-}GaN}$ reaches the JFET's threshold voltage $-V_{\rm TH\text{-}SiC}$, JFET's channel is pinched OFF and all the current is redirected into the gate branch of JFET [see Figs. 2(c) and 3]. Due to the presence of parasitic interconnection inductances (i.e., $L_{\rm G\text{-}S}$ and $L_{\rm S\text{-}D}$), the fast turn-off process of HEMT induces oscillations and overshoots on $V_{\rm DS\text{-}GaN}$ in stage 1. Moreover, in stage 2, the high load current can generate a voltage across JFET's internal gate resistance $R_{\rm G\text{-}SiC}$, elevating the JFET's gate voltage [see Fig. 2(c)]. As a result, JFET's channel can be temporarily turned-ON, allowing more charge to leak to the OFF-state GaN HEMT, thereby raising the HEMT's voltage $V_{\rm DS\text{-}GaN}$. The increased $V_{\rm DS\text{-}GaN}$, in turn, pinches off the JFET's channel again quickly, as shown in Fig. 2(c). Due to the absence of avalanche capability in LV GaN HEMT, $V_{\rm DS\text{-}GaN}$ cannot be clamped during the turn-OFF process (see Fig. 3), exposing the gate of SiC JFET to the potential overstress.

B. Proposed Protection Solution

The GaN/SiC cascode device with a protection Bi-ZD is illustrated in Fig. 1(d). Current cannot flow through the Bi-ZD in either direction until the applied voltage is higher than its

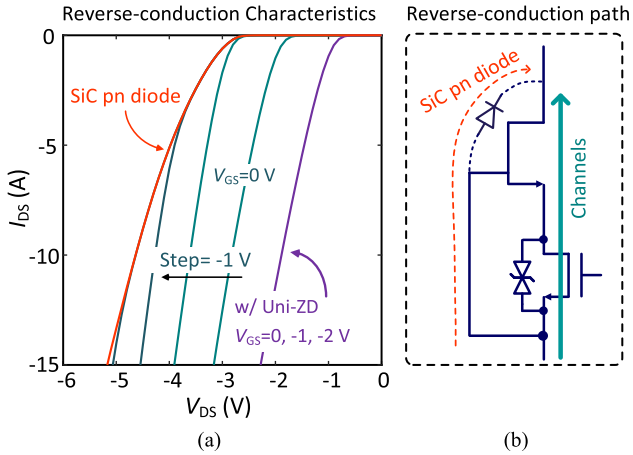

Fig. 6. (a) Reverse-conduction characteristics of the GaN/SiC cascode device with Bi-ZD and Uni-ZD at different V_{GS}. (b) Reverse-conduction current path of the cascode GaN/SiC device with a protection Bi-ZD.

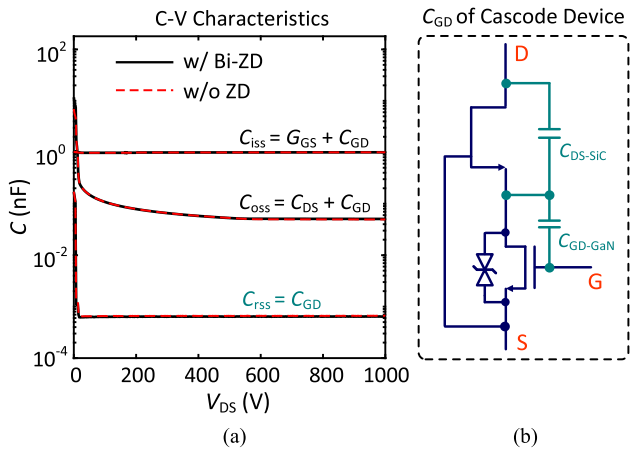

Fig. 7. (a) C-V characteristics of the GaN/SiC cascode device (measured at $V_{AC} = 25$ mV, $f = 100$ kHz). (b) C_{GD} of the cascode GaN/SiC device.

clamping (breakdown) voltage. Therefore, during the switching process, $V_{DS\text{-}GaN}$ can be clamped by the Bi-ZD to prevent the gate of the HV SiC JFET from being overstressed with respect to its source. Meanwhile, during the reverse-conduction phase of the cascode device, current cannot flow through the Bi-ZD due to its bi-directional current blocking capability. Thus, the reverse-conduction current is forced to flow through the LV GaN HEMT [see Fig. 1(d)], and no minority carrier charges are injected into the Bi-ZD during the reverse-conduction process. One of the benefits of the GaN/SiC cascode device, i.e., zero Q_{rr}, is retained.

Without the burden of Q_{rr} introduced by the unidirectional Zener diode, the LV GaN HEMT can be quickly turned OFF to enable the desired voltage blocking. As a result, the turn-OFF process of the cascode device does not need to be compromised and low switching loss in the GaN/SiC cascode device can be obtained [23], [24]. The representative turn-ON processes for the HS switch in a half-bridge configuration with and without Q_{rr} are described in Fig. 4, where Q_{oss} is the output-capacitance charge. With Q_{rr}, the low-side (LS) device needs time to recover

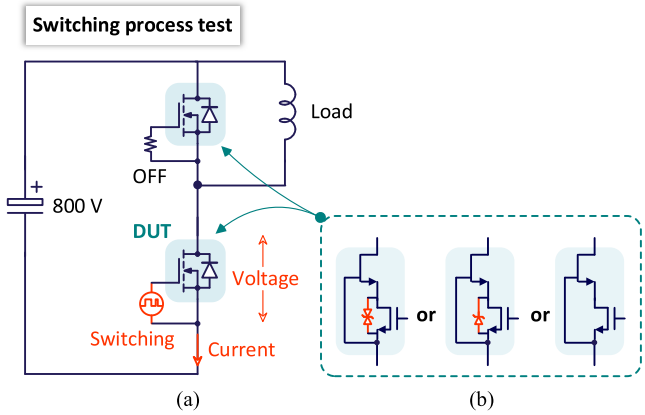

Fig. 8. (a) Half-bridge test set-up. (b) Two devices in the half-bridge are both GaN/SiC cascode devices with the same protection solution.

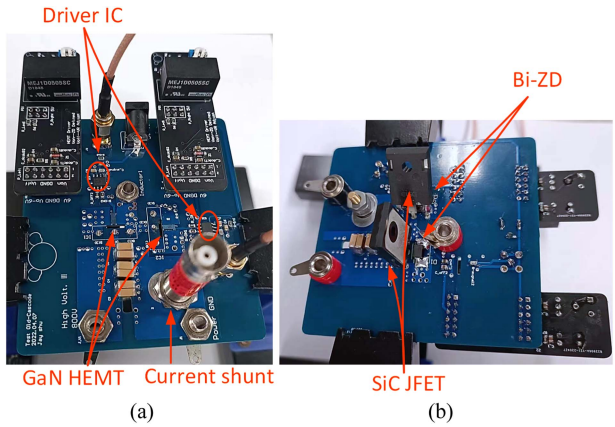

Fig. 9. (a) Front-side and (b) back-side of the test board.

the extra charge (i.e., Q_{rr}) before it can switch from the reverse-conduction mode to the forward-blocking mode, leading to a prolonged switching process and exacerbated switching loss [see Fig. 4(b)]. In comparison, without Q_{rr}, the LS switch does not need additional time to recover after reverse conduction. Hence, the current flowing through the LS device would charge up the C_{oss} of the LS device immediately [see Fig. 4(c)]. A shorter switching process would be achieved with the implementation of Bi-ZD, and the turn-on current overshoot of the HS switch can be significantly suppressed with the benefit of a reduced switching loss, as depicted in Fig. 4(b) and (c).

III. Static Characteristics

A 1.2-kV/30-A GaN/SiC cascode device is demonstrated with a 1.2-kV D-mode SiC JFET (66 mΩ/34 A) [27] and a 40-V E-mode GaN HEMT (3.2 mΩ/53 A) [28]. The clamping voltage of the Bi-ZD should be selected with considerations. First, the clamping voltage should be greater than the magnitude of the SiC JFET's V_{TH}, i.e., 7 V, to ensure the cascode device can be turned OFF during the switching process. Second, the clamping voltage should be lower than the reverse gate voltage limit of the SiC JFET, i.e., 20 V, to protect JFET from negative gate overstress. Therefore, a Bi-ZD of 12-V blocking voltage is chosen to demonstrate the clamping solution [29]. In the following

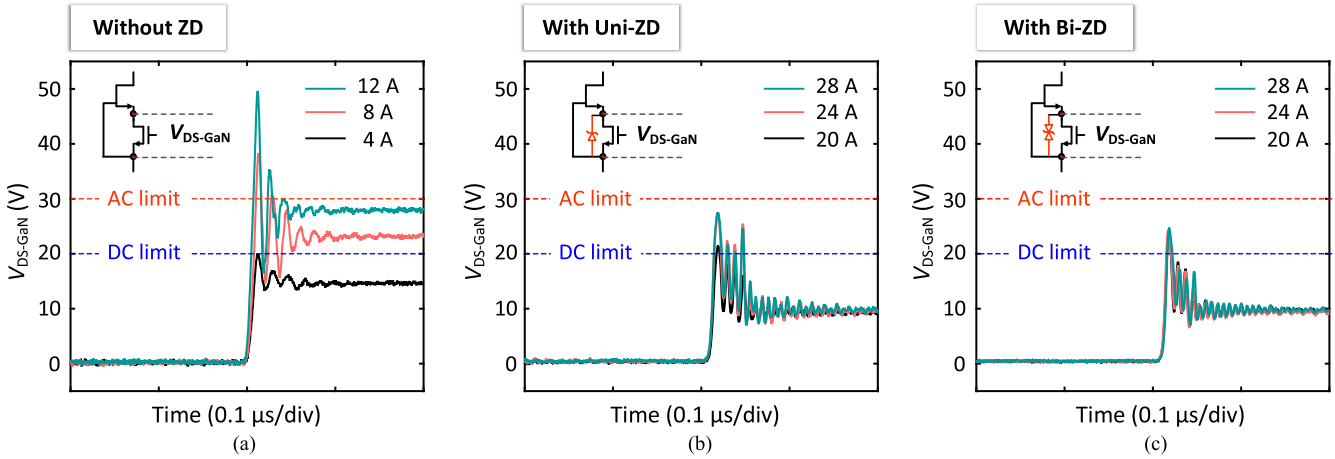

Fig. 10. DUT's $V_{\mathrm{DS\text{-}GaN}}$ waveforms during the turn-OFF process. (a) Without ZD. (b) With a Uni-ZD. (c) With a Bi-ZD. Both Uni-ZD and Bi-ZD can provide sufficient protection for the HV SiC JFET against gate overstress.

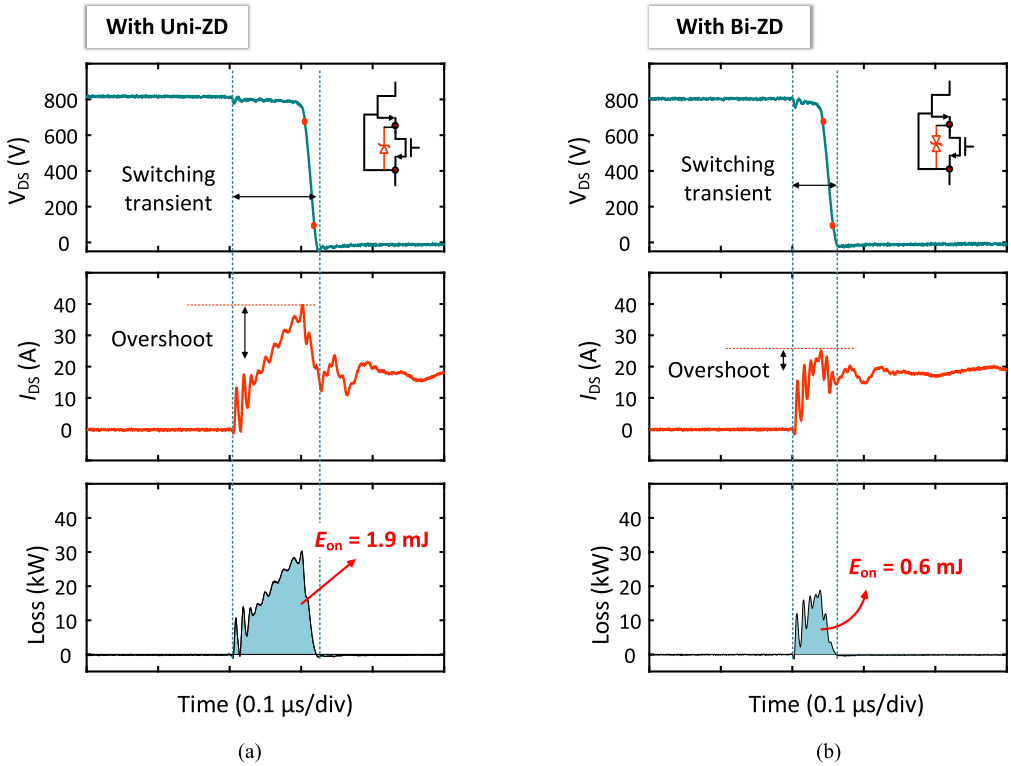

Fig. 11. DUT's waveforms during the turn-ON process of 20-A load current. (a) With a Uni-ZD. (b) With a Bi-ZD. Compared with the Bi-ZD protection solution, the turn-ON process of the cascode device with a protection Uni-ZD is significantly longer, leading to a much higher switching loss.

experiments, a regular Uni-ZD of the same series (i.e., with the same breakdown voltage) is also applied to clamp $V_{\mathrm{DS\text{-}GaN}}$ for comparison.

The transfer and output characteristics of each part and the cascode device are shown in Fig. 5. The V_{TH} of the cascode device equals to that of the HEMT, suggesting HEMT's gate is the control gate for the GaN/SiC cascode device. Owing to the bi-directional current-blocking capability of the Bi-ZD [see Fig. 5(e)], the reverse-conduction current is forced to flow through HEMT, such an operation mode of the cascode device during reverse conduction is verified in Fig. 6. With a Bi-ZD, the reverse-conduction turn-ON voltage of the cascode device can be tuned by the V_{GS} applied to HEMT, suggesting the reverse-conduction current is flowing through the HEMT's channel [see Fig. 6(b)]. In comparison, with a Uni-ZD, the reverse-conduction voltage is independent of the V_{GS} applied to HEMT, and the reverse-conduction turn-ON voltage is ∼0.7 V [see Fig. 6(a)], both suggesting the reverse-conduction current is flowing through the Si Uni-ZD [see Fig. 1(c)], which introduces considerable Q_{rr} after reverse conduction.

However, the zero-Q_{rr} feature of the GaN/SiC cascode device can be impaired when a negative OFF-state V_{GS} is applied to

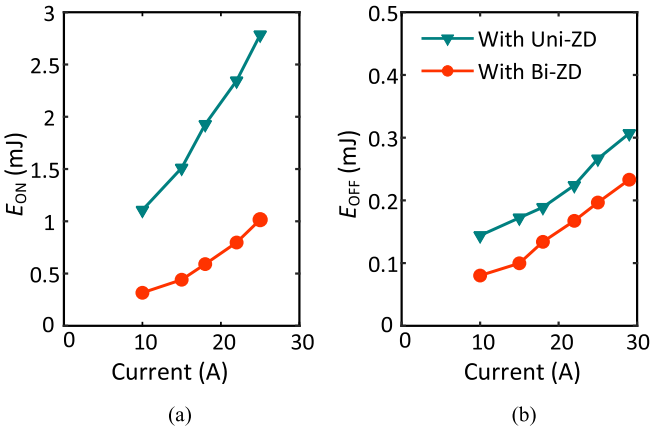

Fig. 12. Switching loss of GaN/SiC cascode device with a Bi-ZD and a Uni-ZD. (a) Turn-ON loss E_{ON}. (b) Turn-OFF loss E_{OFF}. The ON-state and OFF-state gate voltages are 5 and 0 V, and turn-ON and turn-OFF gate resistances are 5.1 and 2 Ω, respectively.

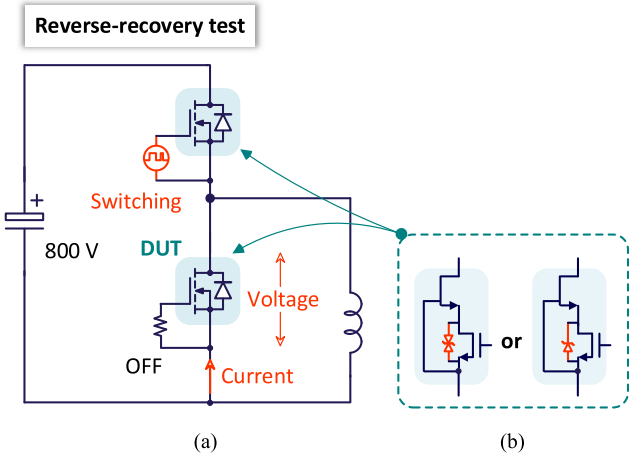

Fig. 13. (a) Half-bridge test circuit used to characterize the reverse-recovery performance of the GaN/SiC cascode device with different protection solutions. (b) Two cascode devices in the half-bridge are protected with the same unit, either both the Uni-ZD or both the Bi-ZD.

HEMT. As shown in Fig. 6, when a negative V_{GS} lower than −2 V is applied, part of the reverse-conduction current of the GaN/SiC cascode device is diverted into the gate-drain SiC pn diode of the HV SiC JFET [see Fig. 6(b)], resulting in certain Q_{rr} and the associated additional switching loss.

Fortunately, the negative V_{GS}, usually used for false turn-on suppression [30], is unnecessary for the GaN/SiC cascode device, which features false turn-on immunity due to the extremely small C_{GD} (i.e., C_{rss}). The C-V characteristics of the GaN/SiC cascode device are shown in Fig. 7. The C_{GD} of the cascode device is the series connection of JFET's drain-source capacitance ($C_{DS\text{-}SiC}$) and HEMT's gate-drain capacitance ($C_{GD\text{-}GaN}$) [see Fig. 7(b)], both are very small, leading to a very small C_{GD} of the cascode device [see Fig. 7(a)]. With such a small C_{GD}, the Miller ratio of the cascode device can be calculated to be $M = Q_{GD}/Q_{GS(TH)} = 0.86$, where $Q_{GS(TH)}$ is the device's gate charge at threshold voltage (i.e., 1.7 V) [31]. The Miller ratio is less than 1, so the GaN/SiC cascode device is completely immune to the false turn-on issue induced by the crosstalk [12], [32]. Therefore, a simple single-polarity gate driver with 0-V OFF-state V_{GS} can be used to drive the GaN/SiC cascode device reliably.

Moreover, the C-V characteristics of the cascode devices with and without Bi-ZD are almost identical, indicating that adding a Bi-ZD will not affect the switching performance of the GaN/SiC cascode device noticeably.

IV. Switching Performance

A. Test Set-Up

The switching process of the cascode device is evaluated on an 800-V half-bridge test set-up [see Figs. 8 and 9] featuring a high-side (HS) inductive load and two identical GaN/SiC cascode devices. The two cascode devices are embedded with the same protection solution, which can be the Bi-ZD, Uni-ZD, or no protection [see Fig. 8(b)]. The current and voltages of the LS device under test (DUT) are measured with current shunt and passive voltage probes with the bandwidth of 2 GHz and 500 MHz.

B. Gate Protection Performance

First, the necessity of $V_{DS\text{-}GaN}$ clamping in the GaN/SiC cascode device is verified. The $V_{DS\text{-}GaN}$ waveforms during the turn-OFF process of the cascode device with different protection solutions are plotted in Fig. 10. Without gate protection ZD, when the load current is increased to just 8 A, $V_{DS\text{-}GaN}$ exceeds both the static limit (dc limit) and transient limit (ac limit) of the SiC JFET's gate voltage, overstressing JFET's gate [see Fig. 10(a)]. In comparison, both the Bi-ZD and the Uni-ZD can clamp the $V_{DS\text{-}GaN}$ within the safe range even at a very high load current (i.e., 28 A for the 1.2-kV/30-A device), providing effective protection for JFET against gate overstress [see Fig. 10(b) and (c)]. The noticeable $V_{DS\text{-}GaN}$ overshoot and oscillation can be attributed to the parasitic power-loop inductance and parasitic interconnection inductance of the cascode device, which can be suppressed after copackaging.

C. Switching Performance

Although both the Uni-ZD and Bi-ZD can provide sufficient protection for JFET's gate, their effects on the switching performance of the cascode device are different. The turn-ON processes of the cascode device with Bi-ZD and Uni-ZD are plotted in Fig. 11. Compared with the Bi-ZD protection solution, the cascode device with a protection Uni-ZD exhibits a significantly longer switching transient with more severe current overshoot, leading to a nearly three times higher switching loss. Fig. 12 summarizes the GaN/SiC cascode device's switching loss with Bi-ZD and Uni-ZD protection solutions under different load currents. Compared with the protection solution with a Uni-ZD, the Bi-ZD protection solution delivers a significant reduction in the switching loss at all current levels. The substantial switching loss reduction of the proposed solution can significantly outweigh the compromise made in deadtime loss. For example, in typical 100-kHz switching applications with a load current of 15 A and a deadtime of 100 ns, the Bi-ZD protection results in an increase

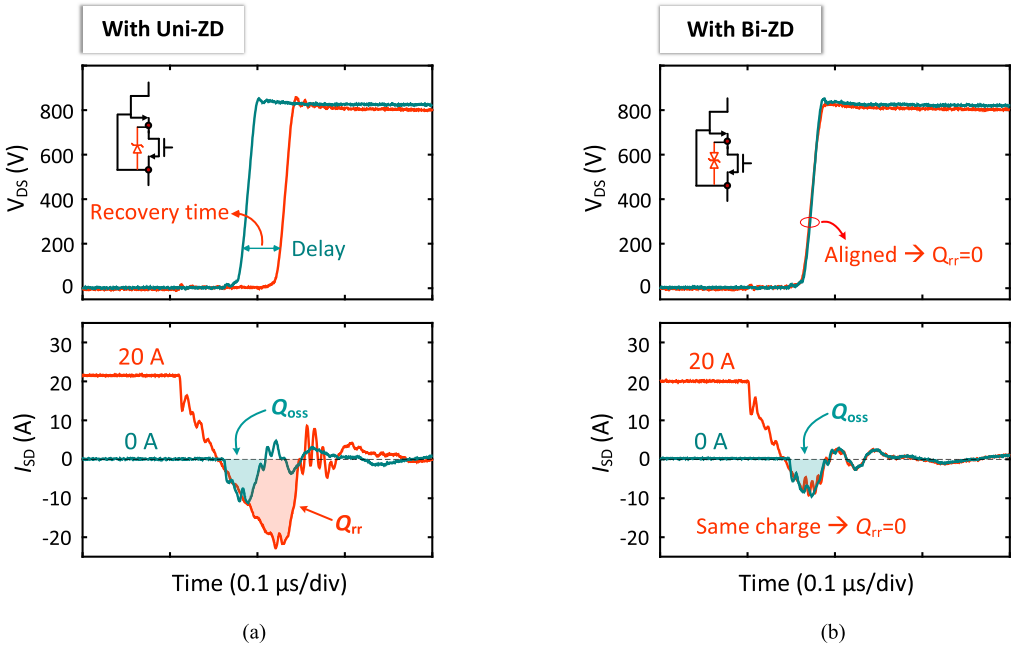

Fig. 14. DUT's voltage and current waveforms during the reverse-recovery process. (a) With Uni-ZD protection solution. (b) With Bi-ZD protection solution. Uni-ZD protection solution introduces significant Q_{rr} while the Bi-ZD solution exhibits zero Q_{rr}.

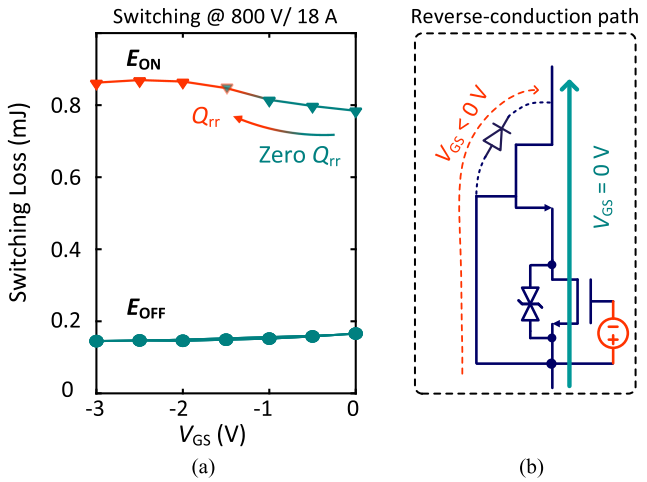

Fig. 15. Switching loss of Bi-ZD-protected GaN/SiC cascode device with various V_{GS}. (a) Switching loss E_{ON} and E_{OFF}. (b) Reverse-conduction current path in the GaN/SiC cascode device. Negative V_{GS} diverts the cascode device's reverse-conduction current into the JFET's gate-drain SiC pn diode, impairing the zero-Q_{rr} feature of the cascode device, leading to exacerbated switching loss.

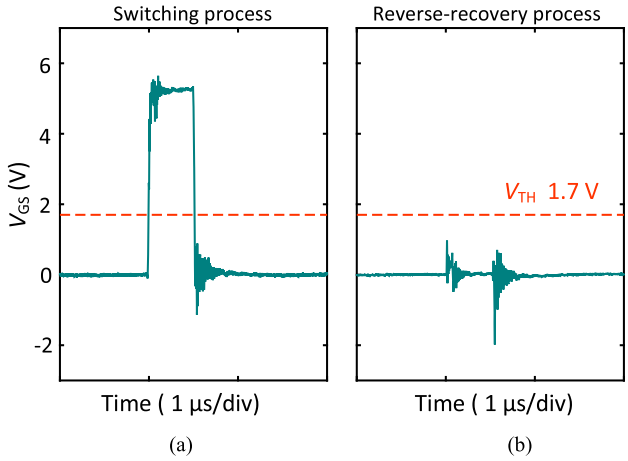

Fig. 16. Gate voltage waveforms of the GaN/SiC cascode device with single-polarity gate driver, i.e., OFF-state $V_{GS} = 0$ V. (a) During the switching process [measured in the test set-up shown in Fig. 6(a)]. (b) During the reverse-recovery process [measured in the test set-up shown in Fig. 11(a)].

of ~6.5 μJ in deadtime loss (assuming a negative V_{GS} of -3 V). However, the switching loss reduction is more than 1 mJ, much higher than the compromise made in the deadtime loss.

The significantly higher switching loss of the cascode device with the Uni-ZD protection solution can be attributed to the revere-recovery process of the Uni-ZD. During the turn-ON process of the LS DUT, the HS device switches from the reverse-conduction mode to the forward-blocking mode [see Fig. 8(a)]. With the Uni-ZD, the HS GaN/SiC cascode device needs to experience a reverse-recovery process to recover the extra charge (i.e., Q_{rr}) in the pn-junction of the Uni-ZD. As a result, the switching process is prolonged, and the switching loss is increased significantly. In comparison, with the Bi-ZD protection solution, the cascode device with zero Q_{rr} does not need additional time to recover after reverse conduction. Therefore, the switching process is much faster, and the switching loss is also significantly lower.

D. Reverse-Recovery Performance

The half-bridge test set-up featuring an LS inductive load and two identical cascode devices (Fig. 13) is used to evaluate the reverse-recovery performance of the cascode device with different protection solutions. For accuracy consideration, the reverse-recovery process of the LS DUT is monitored with

high-bandwidth passive voltage probes and current shunt. Two cascode devices in the half-bridge are embedded with the same protection solution, which can be the Bi-ZD or Uni-ZD [see Fig. 13(b)].

Fig. 14 compares the LS DUT's reverse-recovery process waveforms of 0-A and 20-A reverse-conduction current. When the reverse-conduction current is 0 A, during the HS device's turn-ON process, the LS DUT does not need to recover regardless of the protection design. The LS DUT's current comprises only the DUT's $C_{\rm oss}$-charging current, and thus integrating the DUT's current yields the DUT's $Q_{\rm oss}$, i.e., the green area in Fig. 14(a) and (b).

With the Uni-ZD protection unit, when the reverse-conduction current is increased to 20 A, the LS DUT experiences a reverse-recovery process during the turn-ON process of the HS device. The LS DUT's current comprises both the reverse-recovery current and the $C_{\rm oss}$-charging current, thereby integrating DUT's current yields the sum of DUT's $Q_{\rm rr}$ [i.e., the orange area in Fig. 14(a)] and $Q_{\rm oss}$. The high $Q_{\rm rr}$ of the Uni-ZD leads to a prolonged switching process with an obvious time delay on the $V_{\rm DS}$ rising edge, i.e., the recovery time, as shown in Fig. 14(a).

In comparison, with the Bi-ZD, when the reverse-conduction current is increased to 20 A, the total charge that flows into the cascode device during the reverse-recovery process is not increased, indicating the $Q_{\rm rr}$ of the cascode device is zero [see Fig. 14(b)]. Moreover, the perfect alignment of the $V_{\rm DS}$ rising edge also indicates the $Q_{\rm rr}$ of the cascode device is zero, as the device does not need additional time to recover at a higher reverse-conduction current.

E. Gate Driving Scheme

A simple single-polarity gate driver with a 0-V OFF-state $V_{\rm GS}$ is recommended for the cascode device. For WBG power devices, applying a negative OFF-state $V_{\rm GS}$ to turn OFF the device can suppress false turn-ON, so that the switching loss can be decreased [33], [34], [35]. For the GaN/SiC cascode device, however, the switching loss is increased slightly when a negative OFF-state $V_{\rm GS}$ is used to drive the device [see Fig. 15(a)]. This is because the GaN/SiC cascode device already features false turn-ON immunity due to its extremely small $C_{\rm GD}$ (see Fig. 7), so the negative $V_{\rm GS}$ is no longer effective. Instead, a negative $V_{\rm GS}$ diverts part of the reverse-conduction current into the SiC pn-junction, leading to certain $Q_{\rm rr}$ and the associated additional switching loss [see Fig. 15(b)]. As a result, a simple single-polarity gate driver with a 0-V OFF-state $V_{\rm GS}$ is sufficient and recommended to drive the GaN/SiC cascode device reliably without the false turn-ON issue, as verified by the gate voltage waveforms shown in Fig. 16.

IV. Conclusion

For GaN-HEMT/SiC-JFET cascode power devices, a new voltage clamping solution based on a Bi-ZD has been developed to provide protection against the gate overstress for the high-voltage SiC JFET without compromising the switching performance. Compared to the protection solution based on a unidirectional Zener diode, the bidirectional Zener diode protection solution is free of reverse recovery and the related penalty on switching loss, as verified by experimental results.

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