Paralleled H-Bridge Multilevel Switching-Cell Current Source Inverter

Faramarz Faraji, *Student Member, IEEE*, and Honnyong Cha, *Senior Member, IEEE*

***Abstract*—The paralleled H-bridge multilevel current source inverter (PHB-MLCSI) is widely used in industry, especially for high-power and medium-voltage applications. Even so, the risk of an open-circuit fault (OCF), which is the most common and destructive failure among all conventional CSIs also jeopardizes the reliability of the standard PHB-MLCSI. To overcome this major shortcoming, a new topology called paralleled H-bridge multilevel switching-cell current source inverter is introduced in this article. Thus, OCF is no longer an issue in the proposed topology, even if it occurs frequently or is caused by switch turn ON mismatch/delay among all complementary switches in every switching cycle. The phase-shifted pulsewidth modulation (PS-PWM) method is used to control the proposed topology due to the following two reasons: 1) other PWM schemes, such as level shifted and low/fundamental frequency or half-cycle PWMs cannot overcome OCF if it occurs frequently; 2) mismatches in gating signals, tolerance in parameters of the input dc smoothing inductors (chokes), and unequal input dc voltage values are other concerns in the PHB-MLCSI that may deteriorate the performance of the converter. The PS-PWM method with redundant switching states is a proper modulation technique to handle all the aforementioned mismatch issues to an acceptable level. A variety of experimental tests are conducted to validate the feasibility of the proposed solution. Finally, a comparison is drawn between the proposed circuit and three other existing MLCSIs, further highlighting its distinctive features.**

***Index Terms*—Current source inverter, multilevel converter, overlap-time, phase-shifted pulsewidth modulation (PS-PWM), reliability.**

I. Introduction

MULTILEVEL voltage/current source power converters are widely used in medium-voltage (MV) and high-power (HP) applications [1], [2], [3], [4], [5]. Until recently several multilevel voltage source converters (MLVSCs) including cascaded H-bridge (CHB), modular multilevel converter, neutral-point-clamped (NPC), or diode-clamped, and flying capacitor (FC) also called capacitor-clamped have been commercialized and used in industry [1]. Using the duality principle, the current source version of NPC, FC, and CHB converters are also derived, named single-rating multilevel current source inverter (SR-MLCSI) [see Fig. 1(a)], multirating multilevel current source inverter (MR-MLCSI) [see Fig. 1(b)] and paralleled H-bridge multilevel current source inverter (PHB-MLCSI) [see Fig. 1(c)], respectively [4]. The SR-MLCSI and MR-MLCSI topologies are not attractive for industrial applications due to possessing high numbers of inductors in their structures. In contrast, PHB-MLCSI is widely employed in the industry, especially for HP applications [3]. As reported in [3] an overwhelming majority of MLCSCs used in industry are for HP applications and it is also estimated that at least 700 units of these converters are being manufactured globally. To obtain such a large rating power, it is indispensable to configure two or more CSCs in a parallel manner [3]. This is one of the main reasons that make the PHB-MLCSI preferable for HP applications as several identical H-bridge cells can readily be connected in parallel to increase the output power. Moreover, this modular feature not only does reduce manufacturing costs but also offers a quick and easy replacement in case of a fault/damage in each of these cells [6]. The PHB-MLCSI is also attractive in other area e.g., grid-connected photovoltaic (PV) applications [7]. Notwithstanding several advantages of the PHB-MLCSI and other CSIs including voltage boosting capability, immunity to short-circuit, motor-friendly waveforms to name but a few [3], [5]; no immense explorations and studies have been conducted to improve their functionality compared with VS-MLI counterpart. There exist some obstacles in the PHB-MLCSI and other conventional CSIs, which may adversely affect their performance.

On the one hand, while the PHB-MLCSI and other CSIs are inherently invulnerable to shoot-through problems, there is a risk of an open-circuit fault (OCF) that imperils their reliability, even if a longer overlap-time is introduced among gating signals, and the potential of this failure is even more severe for MLCs since they possess many semiconductors devices in their circuits. This OCF, which may occur due to the presence of electromagnetic interference (EMI) or gate driver failure, is by far the most destructive and prevalent fault in CSIs [5]. Unlike VSCs, where OCF is not hazardous for a short term and can be diagnosed and mitigated to some extent by control methods, OCF in CSCs can rapidly damage the power devices/converter (within several nanoseconds) [8]. Commercially available voltage limiting devices, such as varistors and Zener diodes can be viable options for protecting CSCs from OCF. However, these remedies necessitate larger devices. In [8], an integration of passive and active protection solution against OCF was introduced. Nevertheless,

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The authors are with the School of Energy Engineering, Kyungpook National University, Daegu 41566, South Korea (e-mail: faraji.u@gmail.com; chahonny@knu.ac.kr).

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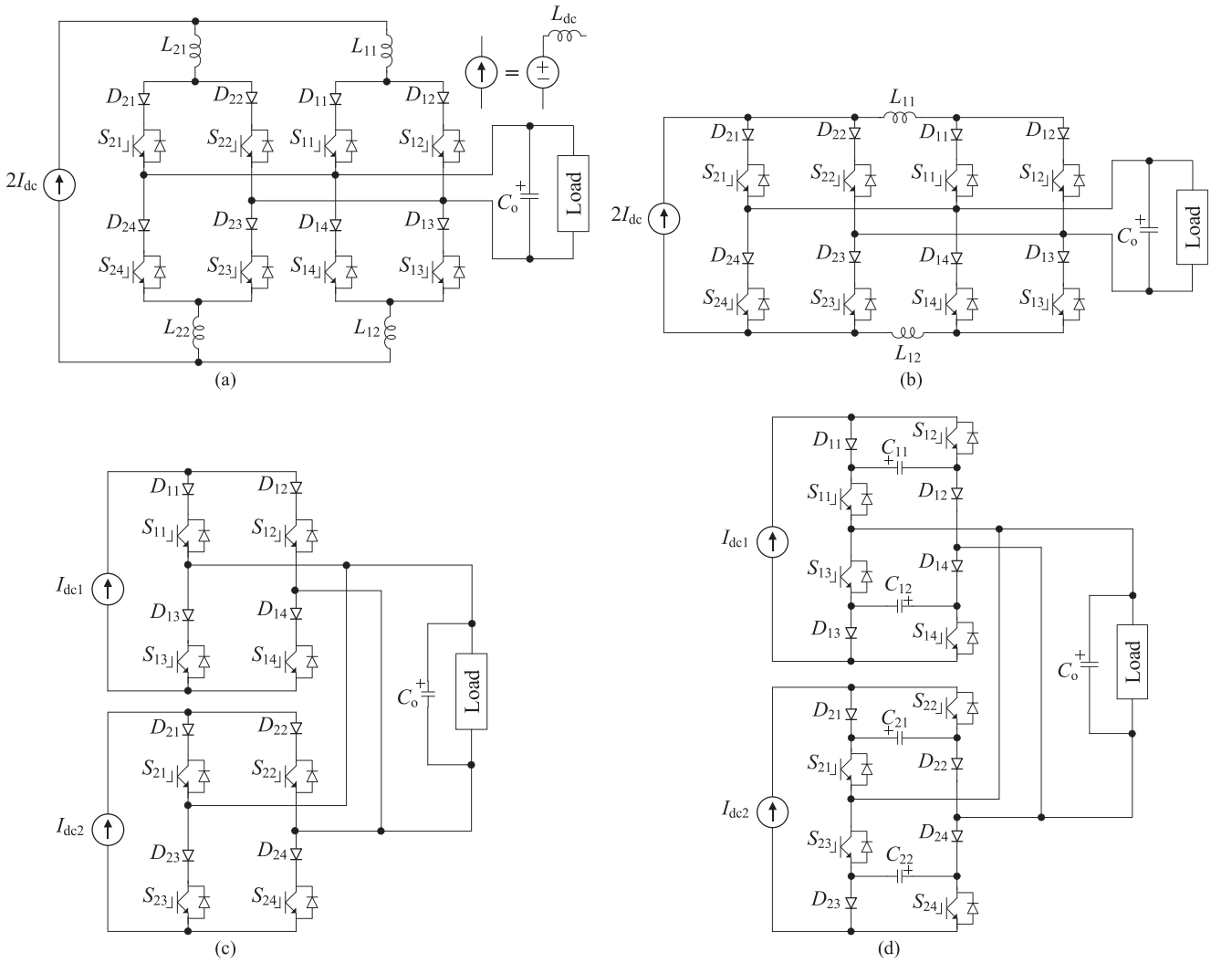


Fig. 1. (a) SR-MLCSI. (b) MR-MLCSI. (c) PHB-MLCSI. (d) Proposed PHB-MLSC^{2}SI.

this scheme makes the system bulky and complicated. An OCF diagnosis and fault-tolerant multilevel CSI was proposed in [9]; however, it fails to protect the circuit if more than one power device encounter OCF.

On the other hand, CSI topologies with separated dc sources and/or with paralleled input smoothing inductors, such as PHB-MLCSI face other designing challenges [3]. As input dc smoothing inductors are generally not available off-the-shelf, they need to be designed and fabricated by the designer/engineer [10]. If not properly designed, a mismatch in parameters value may make the control and balancing of inductors' current more challenging. The uneven value of input dc voltage in separated dc sources is another issue that may occur in PHB-MLCSI particularly in PV application due to partial shading [7]. Once the input voltage/current value of two sources is not identical, the waveform of the output current is deteriorated. In other words, not only does the total harmonic distortion (THD) increase but also the value of output current in positive and negative cycles may not be the same and symmetrical causing dc current injection to the load/grid [11]. The third limitation connected with the PHB-MLCSI is the potential of unbalanced input dc chokes' current induced by the time delay between gating signals, which may degrade the quality of the output waveforms [3].

To deal with the discussed drawbacks, a novel topology called paralleled H-bridge multilevel switching-cell current source inverter (PHB-MLSC^{2}SI) is proposed in this research. The proposed circuit is immune to OCF even if it occurs frequently or is caused by switch turn ON mismatch/delay among all complementary switches in every switching cycle. The solution presented in this research to mitigate OCF is straightforward and relies on the switching-cell (SC) concept to safeguard the proposed topology during such fault conditions, which could arise from EMI noise, gate driver malfunctions, or pulsewidth modulation (PWM) issues. The proposed PHB-MLSC^{2}SI is governed by the phase-shifted PWM (PS-PWM) scheme, which is a prevalent method in industrial applications. This modulation approach offers sufficient switching states to the proposed converter. Hence, the proposed converter can endure nonideal conditions to an acceptable level.

TABLE I
SWITCHING PATTERN OF THE PROPOSED PHB-MLSC^{2}SI

Modes	Switching States								Inverter Current (I_{inv})
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	
1	1	0	0	1	1	0	0	1	$2I_{dc}$
2	1	0	1	0	1	0	0	1	I_{dc}
3	1	0	0	1	0	1	0	1	
4	1	0	0	1	1	0	1	0	
5	0	1	0	1	1	0	0	1	
6	0	1	1	0	1	0	0	1	0
7	1	0	1	0	0	1	0	1	
8	1	0	0	1	0	1	1	0	
9	0	1	0	1	1	0	1	0	
10	0	1	1	0	0	1	0	1	$-I_{dc}$
11	1	0	1	0	0	1	1	0	
12	0	1	0	1	0	1	1	0	
13	0	1	1	0	1	0	1	0	
14	0	1	1	0	0	1	1	0	$-2I_{dc}$

The rest of this article is organized as follows. The PS-PWM approach and the operation principle of the proposed circuit under normal, mismatched, and faulty operating conditions are elaborated in Section II. This section also covers the design guidelines. Section III includes simulation and experimental results, along with a comparison between the proposed and three conventional MLCSIs. Finally, Section IV concludes this article.

II. PROPOSED PHB-MLSC^{2}SI

By incorporating only four small film capacitors known as SC capacitors [12], [13], [14] C_{11}, C_{12}, C_{21}, and C_{22} into the traditional PHB-MCSI [see Fig. 1(c)] and interchanging the position of switches and diodes the proposed topology is derived [see Fig. 1(d)]. The number of power devices between the proposed circuit and conventional PHB-MLCSI is the same. The proposed PHB-MLSC^{2}SI, which is a five-level topology consists of two cells and each cell has four switches connected in series with diodes.

A. Modulation Strategy

The switching states for the proposed PHB-MLSC^{2}SI are illustrated in Table I where "0" indicates the OFF state and "1" represents the ON state of the switches. The switches pair (S_{11}, S_{12}), and (S_{13}, S_{14}) in the upper (first) cell, and switches pairs (S_{21}, S_{22}), and (S_{23}, S_{24}) in the lower (second) cell function in a complementary fashion. In general, the number of total switching combinations/modes for a multilevel converter is defined as [15], [16]

$$N_S = 2^{(n-1)} \tag{1}$$

where N_S is the number of switching combinations/modes. For the proposed topology, which is five-level ($n = 5$), there are 16 possible combinations/modes. Even so, the applicable combinations/modes are 14. The reason is that some redundant switching states (e.g., state [S_{11} S_{12} S_{13} S_{14} S_{21} S_{22} S_{23} S_{24}] = [1 0 1 0 1 0 1 0]) do not have any effective/positive impact on the operation of the proposed circuit. In addition, some switching states are not desirable for the converter. For instance, switching state [S_{11} S_{12} S_{13} S_{14} S_{21} S_{22} S_{23} S_{24}] = [00 00 00 00] creates an OCF for the converter under normal operating condition. Thus, these switching states and their complementary state [S_{11} S_{12} S_{13} S_{14} S_{21} S_{22} S_{23} S_{24}] = [1 1 1 1 1 1 1 1] are avoided in the switching pattern. The switching combinations demonstrated in Table I are applied to the proposed inverter using the PS-PWM strategy. Fig. 2(a) demonstrates the implementation circuit of PS-PWM for the proposed inverter. Overall, a multilevel converter with n number of output current/voltage levels needs $(n-1)$ triangular carrier waves. Thus, for the proposed topology four carrier waves are required. In the PS-PWM approach, all the triangular carrier signals possess identical peak-to-peak magnitude and frequency. Moreover, there is a phase shift (φ_{cr}) between any two neighboring carrier signals, expressed by

$$\varphi_{cr} = \frac{2\pi}{n-1}. \tag{2}$$

Hence, the phase difference (displacement) between any two adjacent carriers' waves is 90° for the proposed five-level structure. Fig. 2(b) shows the gate signals of switches together with the five-level output current generated by the PS-PWM method for the proposed PHB-MLSC^{2}SI. The zoomed view of regions I to IV highlighted in gray color in Fig. 2(b) is shown in Fig. 3. (The numbers 1 to 14 in Fig. 3 are for the operation modes of the proposed topology which is elaborated on next.)

The frequency modulation index m_f for PS-PWM is given by

$$m_f = \frac{f_{cr}}{f_{ref}} \tag{3}$$

where f_{cr} is the carrier frequency and f_{ref} is for modulating waves or fundamental frequency. Then, the semiconductor device switching frequency $f_{sw,dev}$ can be computed by

$$f_{sw,dev} = f_{cr} = f_{ref} m_f \tag{4}$$

The amplitude of the modulation index m; $0 < m \leq 1$ is expressed as

$$m = \frac{W_{ref}}{W_{cr}} \tag{5}$$

in which W_{ref} and W_{cr} are the peak amplitudes of reference and carrier signals, respectively.

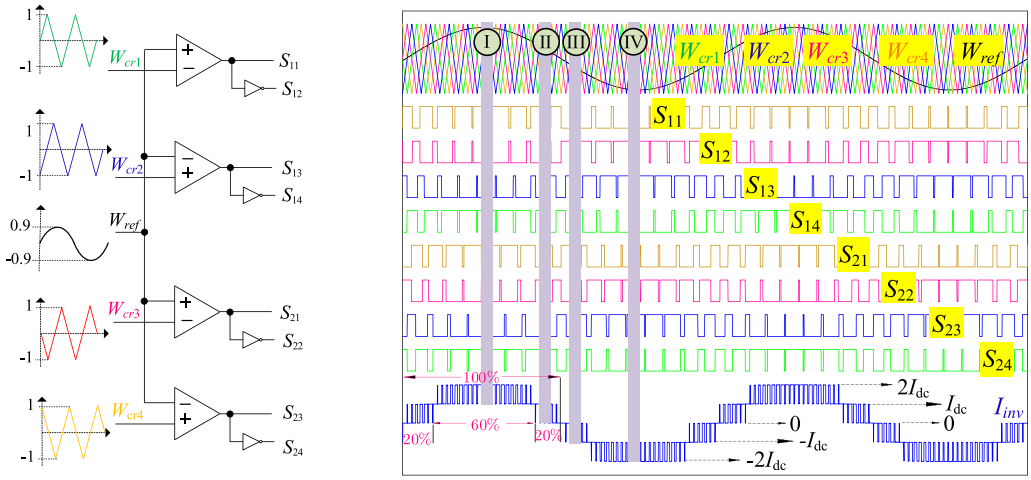
The peak value of the output voltage V_o is found from

$$V_o = m\, H I_{dc}\, R \tag{6}$$

in which H is the number of cells and R indicates the resistive load. As can be observed from Fig. 2(b) (gating signals), all power switches have the same switching pattern. As the stress voltage and current on all power devices in the proposed topology are equal, the mentioned feature of PS-PWM leads to equal power loss distribution among power devices.

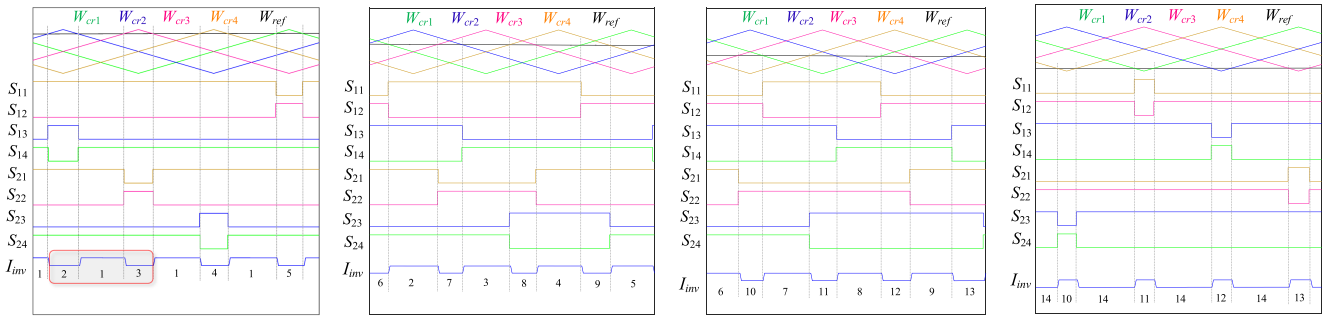
The working/effective/apparent frequency of inverter (the output current) $f_{sw,inv}$ is expressed as

$$f_{sw,inv} = 2H f_{sw,dev} = (n-1)\, f_{sw,dev}. \tag{7}$$



(a) (b)

Fig. 2. (a) Implementation circuit of PS-PWM for the proposed topology. (b) PS-PWM for generating gate signals in the proposed topology.



(a) (b) (c) (d)

Fig. 3. Zoomed view of regions in Fig. 2. (a) Region I. (b) Region II. (c) Region III. (d) Region IV.

As can be seen from Fig. 3, the working frequency of the inverter current I_{inv} for the proposed inverter is four times $(n-1)$ higher than the switching or carrier frequency. In other words, all devices are turned OFF and ON or vice versa only one time in each switching period, whereas the working frequency of the inverter current is four. This desirable feature allows the proposed topology to eliminate more harmonics while a low value of switching frequency helps to decrease the power device switching losses [16].

Regarding Figs. 2(b) and 3, comparing reference wave (W_{ref}) with triangular carrier1 (W_{cr1}) generates the gate signals for switches S_{11} and S_{12}. When W_{ref} is compared with W_{cr2}, the switches S_{13} and S_{14} are driven. The gate signals for the switches S_{21} and S_{22} are created by comparing W_{ref} with W_{cr3}. Finally, the gating signals for switches S_{23} and S_{24} are generated by comparing W_{ref} with W_{cr4}.

B. Operation Principle and Commutation/Transitional Intervals of the Proposed Inverter Under Normal Functioning Condition

Since the proposed circuit has a symmetrical structure, its operation in the positive and negative half cycles is the same. Hence, only three operation modes (from the positive cycle) out of 14 opted to elaborate herein. Moreover, commutation/transition occurs between two operational states/modes, during which the inverter current (I_{inv}) changes from one level to another. Referring to Fig. 3, there are 22 distinct commutation intervals within one fundamental period for the proposed inverter. For the purpose of explaining the operating principle, two specific commutation intervals are focused: the transition from Mode 1 to Mode 2 in region I and the transition from Mode 2 to Mode 7 in region II. However, it is important to note that the same analysis can be applied to the remaining transitional intervals and operating modes, using Table I, Fig. 3, and [12], [13], [14], and [17].

Mode 1 [Table I, and Figs. 2, 3(a), and 4(a)]: W_{ref} is greater than all carrier signals. Therefore, switches S_{11} and S_{14} in the upper cell (cell) are ON, and their complementary switches S_{12} and S_{13} are OFF. Similarly, in the lower cell, the switches S_{21} and S_{24} are ON, and their complementary switches S_{22} and S_{23} are OFF. The inverter current is the sum of the I_{dc1} and I_{dc2} ($I_{\text{dc1}} = I_{\text{dc2}} = I_{\text{dc}}$) and equal to $2I_{\text{dc}}$. SC capacitors C_{11} and C_{21}, which are in parallel with the output capacitor C_{o} are charged. This mode does not have an impact on the charging or discharging of the SC capacitors C_{12} and C_{22}. It should be noted that the voltage

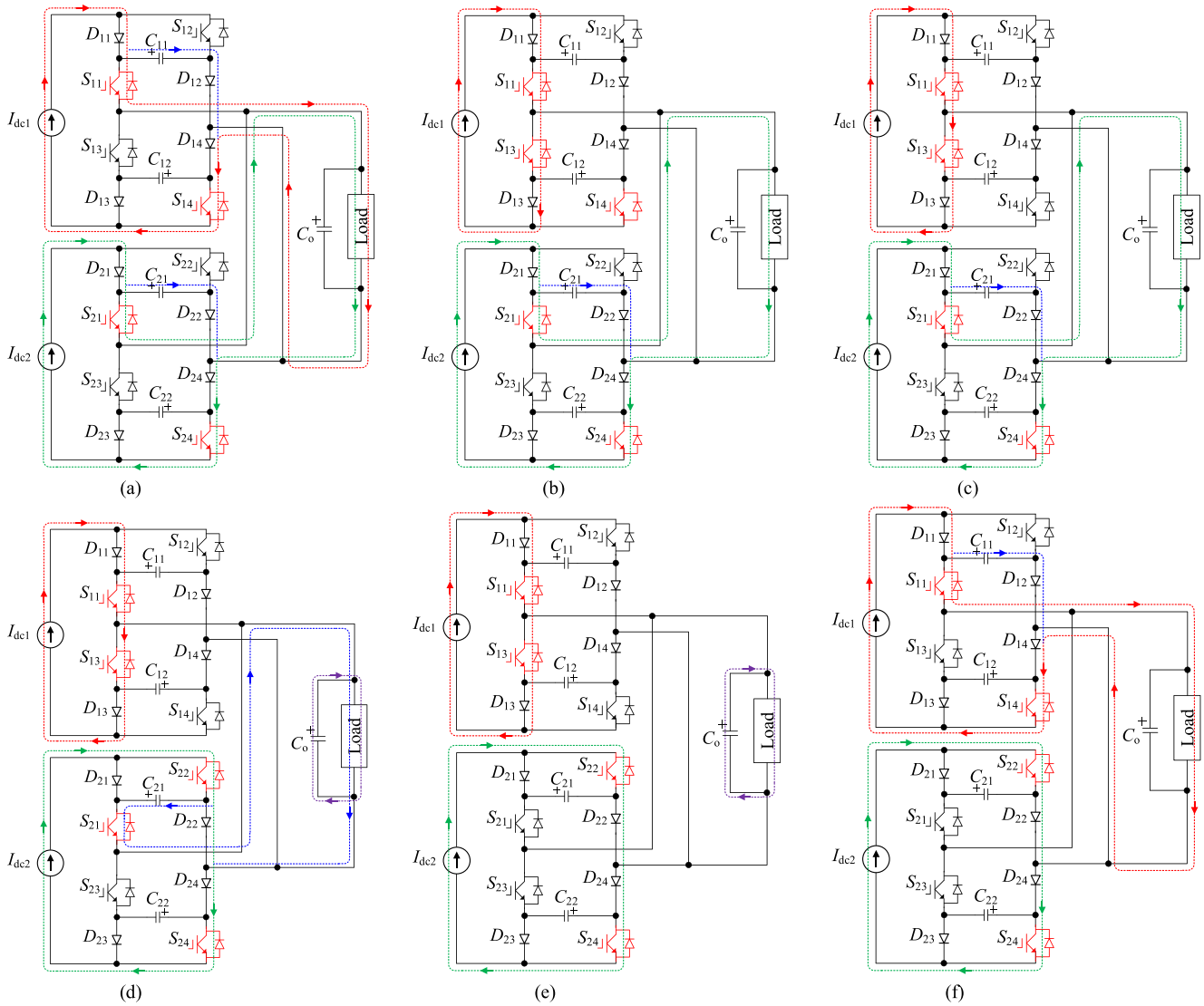


Fig. 4. Operation modes of the proposed topology. (a) Mode 1. (b) Commutation from Mode 1 to Mode 2. (c) Mode 2. (d) Commutation from Mode 2 to Mode 7. (e) Mode 7. (f) Mode 3.

of capacitors C_{12} and C_{22} remain at zero level throughout the positive half cycle.

Commutation from Mode 1 to Mode 2 in Region I [Table I, and Figs. 2, 3(a), and 4(b)]: The transitional/commutation process begins by turning ON switch S_{13}, while the remaining switches maintain their ON/OFF position [see Fig. 4(b)]. In other words, switches S_{11}, S_{13}, and S_{14} in the upper cell, along with S_{21} and S_{24} in the bottom cell are ON, while the switches S_{22} and S_{23} are OFF. As soon as S_{13} is switched ON, diode D_{14} is reversed-biased and D_{13} becomes forward-biased because the voltage of C_{12} is zero. Then, the current $I_{\rm dc1}$ shifts from D_{14} to D_{13} and S_{13}. The capacitor C_{12} is neither charged nor discharged and remains at zero volt. C_{12} and D_{13} appear in parallel and the voltage across diode D_{13} is zero volt when it is forward biased. Both switch pairs (complementary switches) S_{13} and S_{14} remain ON until the commutation/overlap-time is finished. During this transitional period, the inverter current remains equal to $I_{\rm dc2} = I_{\rm dc}$. C_{21} continues its charge while C_{11} and C_{22} do not experience the charge or discharge condition. Once the overlap-time is completed, only switch S_{14} is turned OFF, and the operational mode of the proposed inverter transitions from Mode 1 to Mode 2 [see Fig. 4(c)].

Mode 2 [Table I, and Figs. 2, 3(a), and 4(c)]: $W_{\rm ref}$ is greater than all carrier signals except for $W_{\rm cr2}$. Consequently, in the upper cell, S_{13} is turned ON and its complementary switch S_{14} is turned OFF. The remaining switches do not change their switching states. In other words, S_{11}, S_{21}, and S_{24} are ON and switches S_{12}, S_{22}, and S_{23} are OFF. The inverter current is equal to $I_{\rm dc2} = I_{\rm dc}$. Only capacitor C_{21} is charged.

Commutation from Mode 2 to Mode 7 in Region II [Table I, and Figs. 2, 3(b), and 4(d)]: Before the transition from Mode 2 to Mode 7, switches S_{11} and S_{13} in the upper cell, along with S_{21} and S_{24} in the lower cell, are ON, while their complementary switches, S_{12}, S_{14}, S_{22}, and S_{23} are OFF [see Fig. 4(c)]. The commutation interval process begins by turning ON switch S_{22} in the lower cell, while the remaining switches maintain their

ON/OFF position [see Fig. 4(d)]. As soon as the S_{22} is turned ON, diode D_{21} becomes reversed-biased. The main current shifts from S_{21} to S_{22} and diode D_{22}. The voltage of C_{21} is equal to the output voltage, and a small current flow through the C_{21}, whereas the load is mainly fed by $C_{\rm o}$. In this transitional mode, the inverter current is almost zero. The other SC capacitors do not experience charge or discharge conditions. Once the overlap-time is completed, only switch S_{21} is turned OFF and the proposed topology transitions into Mode 7.

Mode 7 [Table I, and Figs. 2, 3(b), and 4(e)]: Switches S_{11}, S_{13}, S_{22}, and S_{24} are ON, and their complementary switches S_{12}, S_{14}, S_{21}, and S_{23} are OFF. The PS-PWM produces zero current level. This mode does not influence the charging or discharge of SC capacitors.

C. Operation of the Proposed Inverter Under Mismatch Functioning Condition

For the mismatch analysis, it is assumed that there is a $\pm 10\%$ difference in current between the upper and lower cell due to a mismatch condition. In other words, $I_{\rm dc1} = 1.1I_{\rm dc}$ and $I_{\rm dc2} = 0.9I_{\rm dc}$. Furthermore, because of the symmetry of the suggested circuit, the impact of mismatch is only detailed in the positive half cycle. The mismatch condition does not impact the load current/voltage at the $2I_{\rm dc}$ and zero levels. For example, in the normal operating condition of Mode 1 [see Fig. 4(a)], $I_{\rm inv} = I_{\rm dc1} + I_{\rm dc2} = 2I_{\rm dc}$. The condition also holds true under mismatch condition in Mode 1, where $I_{\rm inv} = 1.1I_{\rm dc1} + 0.9I_{\rm dc2} = 2I_{\rm dc}$. In Mode 7 [see Fig. 4(e)], the input dc smoothing chocks are bypassed to create the zero state. As a result, any mismatch on the dc side in zero state does not have any impact on the load side. As observed in Fig. 2(b), 60% of inverter/output waveform is generated by switching between $2I_{\rm dc}$ and $I_{\rm dc}$ levels, with $2I_{\rm dc}$ accounting for half of this portion. Similarly, 40% of the remaining $I_{\rm inv}$ is generated by switching between $I_{\rm dc}$ and zero levels, where the zero state contributes 20% of this proportion. Consequently, it can be concluded that, during the mismatch condition, 50% of the entire functioning cycle does not affect the inverter/output current, and the load perceives this mismatch situation as a normal condition, thanks to the PS-PWM scheme. Although the $I_{\rm dc}$ level may have some impact on the output waveforms, its effect is not significant. As shown in Fig. 3(a) [highlighted in gray], Fig. 4(a) and (c), when the operation state changes from Mode 1 to Mode 2 under mismatch condition, the inverter current is reduced from its nominal value of $I_{\rm dc}$ to $0.9I_{\rm dc}$ ($I_{\rm inv} = I_{\rm dc2} = 0.9I_{\rm dc}$). However, after Mode 2, Mode 1 is repeated, and the current provided to the load is similar to the normal operating condition ($I_{\rm inv} = 1.1I_{\rm dc1} + 0.9I_{\rm dc2} = 2I_{\rm dc}$). Despite this, the average current supplied to load, which is the sum of states 1 and 2, might be slightly lower than its nominal value. To compensate for this reduction, Mode 3 [see Figs. 3(a) and 4(f)] is selected to produce surplus current ($I_{\rm inv} = I_{\rm dc1} = 1.1I_{\rm dc}$). As a result, the average current experienced by the load after these three switching sequencies ($3/f_{\rm sw}$) remains unchanged. Hence, the PS-PWM strategy mitigates the adverse effects of mismatch conditions on the load side. Although the input dc smoothing inductors' currents may exhibit slight deviations from each other under mismatched operating conditions compared with the perfectly balanced normal condition, these discrepancies are minimal. They do not result in oversizing of the chokes or trigger saturation issues that could arise with unfavorable PWM schemes.

D. Design Guideline

A common approach for designing the input dc smoothing inductor is to confine its current ripple within 10%–20% of its rated current

$$L_{\rm dc} = \frac{V_{\rm in}\sqrt{2}}{4f_{\rm o}\Delta I_{\rm L}} \times 0.1 \tag{8}$$

where $L_{\rm dc}$ is the inductor value, $V_{\rm in}$ represents the input voltage, $f_{\rm o}$ denotes the fundamental frequency, Δ is allowable current ripple on inductor in percent, and $I_{\rm L}$ or $I_{\rm in}$ is the input dc/inductor current.

The output filter capacitor is designed to keep the voltage ripple of the output voltage less than 5% of its peak value

$$C_{\rm f} = \frac{I_{\rm in}}{4 \times 2Hf_{\rm sw}\Delta_{uC{\rm f}}}. \tag{9}$$

In (9), $\Delta_{uC{\rm f}}$ represents the maximum allowable voltage fluctuation across the filter capacitor.

The design of SC capacitors is detailed in the next subsection under faulty operating condition.

E. Selection of SC Capacitors and Operation of the Proposed Topology Under Faulty Condition

Under healthy/normal operating conditions, the stress voltage on SC capacitors and power devices is the same and equal to the peak value of output. In this situation, the root mean square (rms) value of SC capacitor's current is defined as [17]

$$\begin{aligned} I_{C11} = I_{C12} = I_{C21} = I_{C22} = I_C \\ = \sqrt{\frac{1}{T_{\rm o}}\left[\frac{(\pi C V_{\rm o})^2}{2T_{\rm o}} + I_{\rm dc}CV_{\rm o}\right]} \end{aligned} \tag{10}$$

in which $T_{\rm o}$ is the output period. Even so, under OCF functioning conditions, as illustrated in Fig. 5, the current of SC capacitors becomes equal to the input dc current, as the fault time induced by EMI or gate driver error is typically short and cannot change the value of the input current. During the faulty condition, $I_{\rm dc}$ charges the SC capacitors, causing an increase in their voltage. As a result, the SC capacitors should be designed based on the increase in their voltage during the faulty operating condition and the fault duration time. Therefore, by assuming that $C_{11} = C_{12} = C_{21} = C_{22} = C$, the capacitance value of SC capacitor can be computed as

$$C = \frac{I_{\rm dc}}{\Delta V_C}\Delta t_{\rm d} \tag{11}$$

in which $\Delta V_C = \Delta V_{C11} = \Delta V_{C12} = \Delta V_{C21} = \Delta V_{C22}$ represents the increase in SC capacitor voltage during the faulty operating condition, and $\Delta t_{\rm d}$ is the fault duration time.

The allowable increase in SC capacitor voltage (ΔV_C) to protect the power devices under faulty functioning conditions

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED PHB-MLC2SI UNDER OCF ON ALL SWITCHES IN MODE 1

FS	CP-OCF	MVS_S-H	MVS_S-OCF	MVS_C-H	MVS_C-OCF
All switches	D_{11}, D_{12}, D_{13}, D_{14}, C_{11}, C_{12} D_{21}, D_{22}, D_{23}, D_{24}, C_{21}, C_{22}	$S_{11} = S_{14} = S_{21} = S_{24} = 0$ $S_{12} = S_{13} = S_{22} = S_{23} = V_o$	$S_{11} = S_{14} = S_{21} = S_{24} = \Delta V_C$ $S_{12} = S_{13} = S_{22} = S_{23} = \Delta V_C + V_o$	$V_{C11} = V_{C21} = V_o$ $V_{C12} = V_{C22} = 0$	$V_{C11} = C_{21} = \Delta V_C + V_o$ $V_{C12} = C_{22} = \Delta V_C$

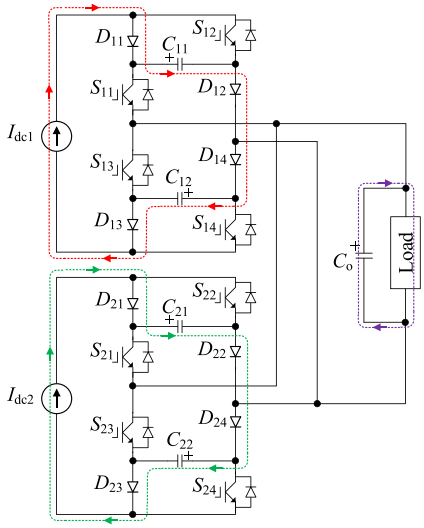


Fig. 5. Operation of the proposed PHB-MLSC^{2}SI under OCF.

can be determined based on the theoretical/actual voltage stress on the power semiconductor device (V_{SA}), which is equal to V_o in the proposed topology, and the voltage rating of the selected device (V_{SWR}) as

$$\Delta V_C \leq V_{SWR} - V_{SA}. \tag{12}$$

Generally, for safety margin purposes, the voltage rating of power devices is selected to be $V_{SWR} = 150\%–180\%\ V_{SA}$. However, it is possible that due to the availability of power devices in the market, this mentioned margin might be exceeded. By considering, $V_{SWR} = 170\% V_{SA}$ and $V_o = V_{SA} \approx 170$ V, the increase in SC capacitor voltage can be obtained from (12), which should be $\Delta V_C \leq 120$ V. Then, the value of SC capacitors with $\Delta t_d = 2.5\ \mu$s (according to the application, switching frequency, etc.) and $I_{dc1} = I_{dc2} = I_{dc} = 10$ A, can be defined from (11) as 0.22 μF.

There are 10 different OCF possibilities for each of the 14 operation modes, 24 for each of the 22 commutation/overlap-time intervals, and one OCF potential affecting all switches at the same time. Consequently, there are 669 possibilities of OCF in one fundamental period. Note that, none of these OCFs influence the functionality of PS-PWM. In other words, PS-PWM operates independently and does not need to change switching states under faulty events.

The most extreme faulty condition (OFC on all switches) is selected for analysis (see Fig. 5). Table II outlines the performance of the proposed inverter under OCF on all switches in Mode 1 and its impact on the voltage of power devices and SC capacitors. From Fig. 4(a) and Table II, under normal condition, the voltage stress on S_{11}, S_{14}, S_{21}, and S_{24} is zero as they are ON, while the remaining OFF switches experience voltage equal to V_o. Once OCF occurs on all switches simultaneously, the input dc current is not interrupted. As seen from Fig. 5, under this faulty condition, I_{dc1} flows through D_{11}, D_{12}, D_{13}, D_{14}, C_{11}, and C_{12} in the upper cell, while I_{dc2} flows via D_{21}, D_{22}, D_{23}, D_{24}, C_{21}, and C_{22} in the lower cell. In this duration, the output filter capacitor C_o supplies the load. Nevertheless, under this circumstance, the voltage of SC capacitors is charged by

$$\Delta V_C = \frac{I_{dc}}{C} \Delta t_d. \tag{13}$$

During the faulty condition (see Fig. 5 and Table II), V_{C11} and V_{C21} increase from V_o to $\Delta V_C + V_o$, and V_{C12} and V_{C22} are increase from 0 to ΔV_C. In addition, ΔV_C is transferred to the power devices, causing V_{S11}, V_{S14}, V_{S21}, and V_{S24} to increase from 0 to ΔV_C, and V_{S12}, V_{S13}, V_{S22}, and V_{S23} to change from V_o to $\Delta V_C + V_o$. However, since ΔV_C was predefined (12) to not exceed V_{SWR}, no harm jeopardizes the power devices. Hence, the proposed topology is protected against OCF. On the other hand, in traditional MLCSIs, even if the OCF occurs on a single switch for a very short time (nanoseconds), a huge overvoltage appears on power devices and damages the converter as the current of input dc current is interrupted.

F. Potential Application of the Proposed Topology

One of the potential applications for the proposed converter is in three-phase/multiphase MV and HP motor drives with a back-to-back configuration. In this setup, even if all switches encounter an OCF, the inductor currents remain connected. Remarkably, as the number of phases increases, the count of SC capacitors does not rise, rendering the suggested protective solution appealing for multiphase motor drives. However, conventional modulation techniques might not be suitable for back-to-back setups, warranting the exploration of modified or new modulation/control strategies.

G. Extension of the Proposed Topology for n Level

Theoretically, MLCs can be extended to any number of levels. Even so, in practice due to technical limitations, the number of levels is limited. Fig. 6 shows the configuration of the proposed inverter for n level. The output current level in the proposed topology is always an odd number similar to the voltage levels in the conventional CHB-MLVSI. However, in other MLVSCs, such as the FC or NPC topologies, the output voltage can be either an odd or even number. The number of H-bridge cells (H), input smoothing inductors (NL_{dc}), and input dc sources (NDC_S) for n level version of the proposed topology can be computed as

$$H = NL_{dc} = NDC_S = \frac{n-1}{2}. \tag{14}$$

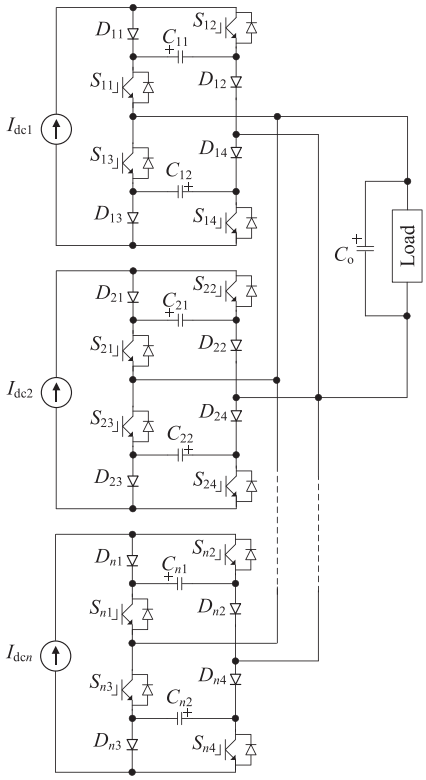


Fig. 6. Configuration of the proposed topology for n level.

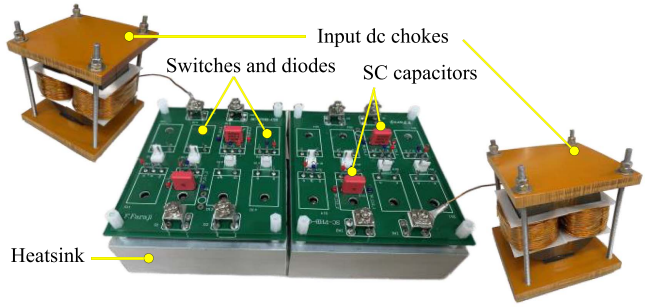


Fig. 7. Photograph of the prototype.

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

Variable	Description	Values
P_o	Output power (kW)	1.4
$L_{dc1} = L_{dc2}$	Input smoothing inductors (mH)	26
v_o	Output ac voltage (V_{RMS})	120
f_{sw}	Switching frequency (kHz)	20
f_o	Output frequency (Hz)	60
C_{11} to C_{21}	SC capacitors (μF)	0.22
C_o	Output capacitor (μF)	30
R, L	Load (Ω, mH)	10, 7.5
m	Modulation index	0.9
δ	Overlap-time (μs)	0.3

The total number of switches and diodes Nsw,diode used in the n level configuration of the proposed inverter can be found from

$$N_{\text{sw,diode}} = 2(n-1). \tag{15}$$

The total number of SC capacitors NSC can be calculated as

$$N_{\text{SC}} = n-1. \tag{16}$$

III. Simulation/Experimental Validation and Comparison

To justify the feasibility and performance of the proposed solution, a 1.4 kW prototype was built with MOSFETs IPW60R040C7 in series with diodes APT30D60BG, and SC capacitors MKS4G032203G in the laboratory, shown in Fig. 7. The PS-PWM strategy together with the overlap-time and OCF were programmed in DSP TMS320F28335 using the code composer studio and then generated gating signals transferred to the gate driver.

In the waveforms, I_{dc1} and I_{dc2} represent the current of upper cell and lower cell inductors' currents, respectively; i_o is output current; v_o denotes output voltage; I_{inv} is inverter's five-level current (before filter); V_{C11} to V_{C22} demonstrate stress voltages on SC capacitors C_{11} to C_{22}, respectively; and finally, V_{S11} to V_{S24} are stress voltages on switches S_{11} to S_{24}, respectively. The simulation and experimental specifications are the same as listed in Table III. It should be noted that all Figs. 8 to 18 are experimental waveforms, except for Figs. 9(e) and (f), and 18, which depict simulation waveforms.

A. Under Normal Operating Condition

Fig. 8(a) and (b) shows the input dc currents (input inductors' currents) labeled as I_{dc1} and I_{dc2}, output current and voltage, and the five-level current of the proposed inverter at the nominal operating condition, in which the power factor (PF) is about 0.96 i.e., the load is $RL = 10\ \Omega$, 7.5 mH. Although the proposed inverters' five-level current is noisy [see Fig. 8(b)], the proposed topology can provide almost purely sinusoidal voltage and current waveforms to the load. Furthermore, the currents of input inductors (chokes) are perfectly balanced thanks to the PS-PWM strategy.

B. Under Faulty Operating Condition

1) Occurrence of OCF on All Switches Only Once: The performance of the proposed and traditional PHB-MLCSI topologies is tested under OCF conditions, named Test #1, and outcomes are depicted in Fig. 9. To create the OCF, a 2.5 μs dead-time is introduced among all switching signals. Fig. 9(a) displays the stress voltage on SC capacitors in the proposed structure. Initially, the proposed topology operates under normal operating condition, and the voltage stress on SC capacitors is equal to the peak value of the output voltage [compare Fig. 8(a) and v_o in Fig. 9(a)]. At 25 ms, the OCF occurs on all switches, and the SC capacitors are charged through input dc currents [see Fig. 9(a)] by the value of ΔV_C discussed in the previous section. As can be observed from Fig. 9(b), when OCF occurs

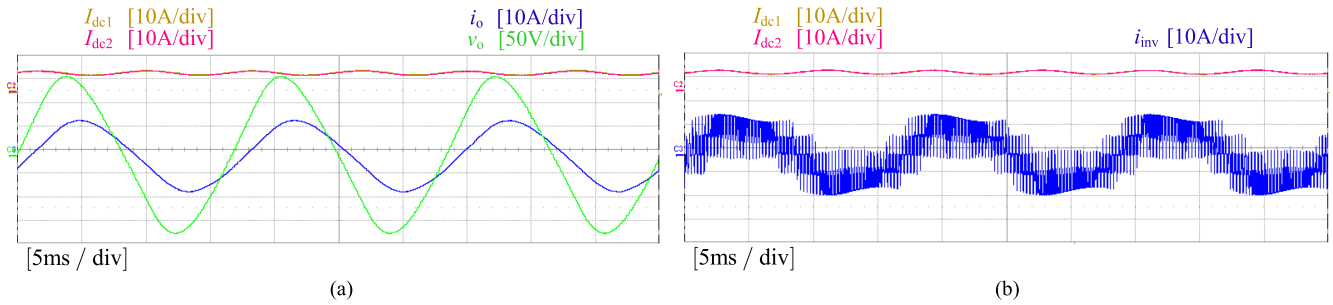


Fig. 8. Experimental results of the proposed PHB-MLSC^{2}SI under normal operating conditions: input dc currents, output current, output voltage, and the inverter's current. (a) and (b) PF = 0.96.

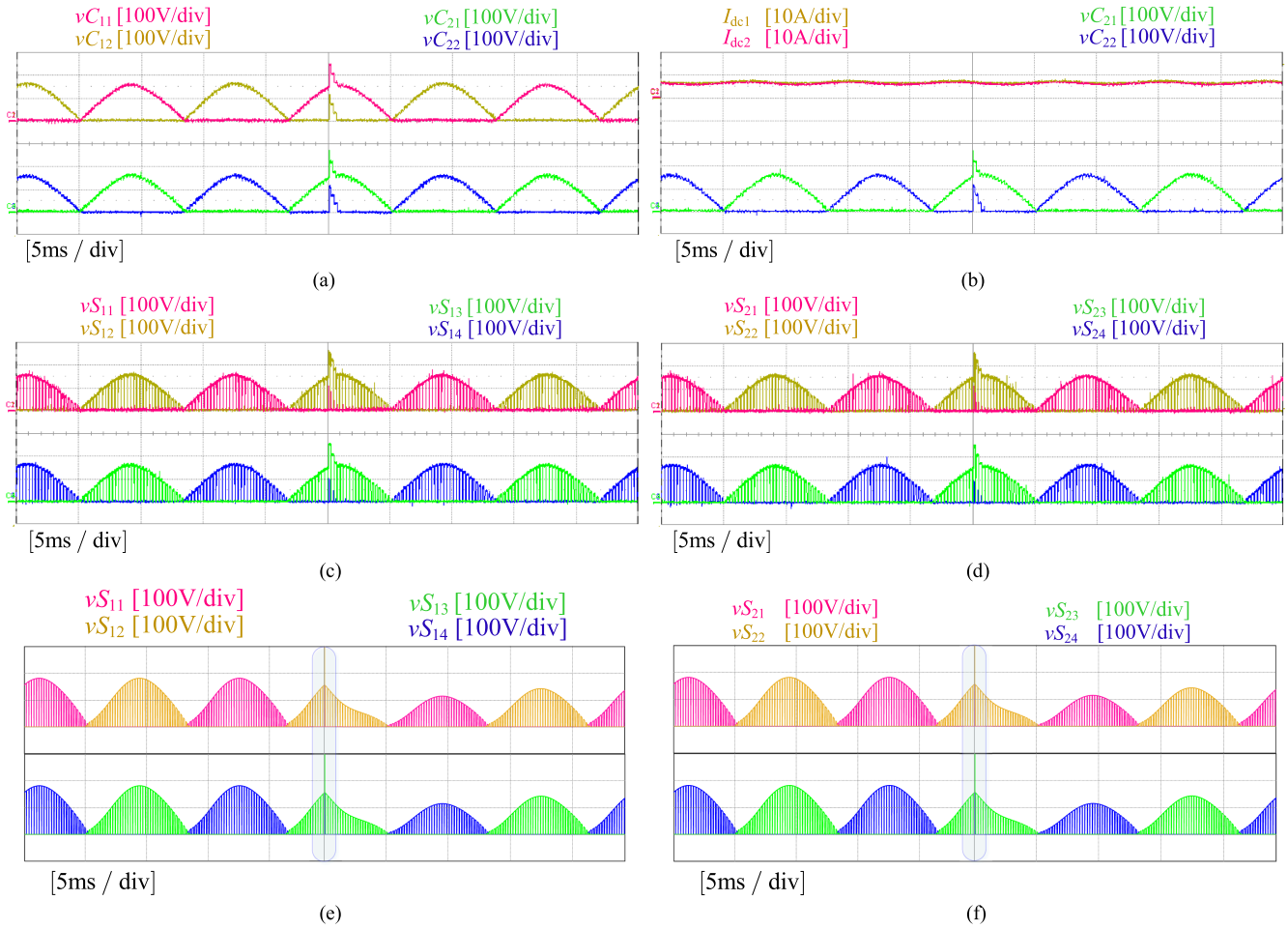


Fig. 9. Experimental results of the proposed PHB-MLSC^{2}SI under faulty condition (Test #1). (a) Stress voltage on SC capacitors. (b) Stress voltage on SC capacitors together with the input dc inductor currents. (c) and (d) Stress voltage on switches. Simulation results of the conventional PHB-MLCSI: (e) and (f) Stress voltage on switches.

on all power switches in the proposed circuit, the input dc choke currents (I_{dc1} and I_{dc2}) are not interrupted as SC capacitors (C_{11}, C_{12}, C_{21}, and C_{22}) provide paths for them. Fig. 9(c) and (d) demonstrates the stress voltage on power switches in the proposed PHB-MLSC^{2}SI. As seen from these figures, under the normal operating condition, the power devices withstand the voltage equal to the peak value of v_o as SC capacitors do. As soon as the fault happens, some extra voltages (spikes) are imposed on switches. V_{S11}, V_{S14}, V_{S21}, and V_{S24} are increased from 0 to Δ_{VC}, and V_{S12}, V_{S13}, V_{S22}, and V_{S23} from V_o to $\Delta V_C + V_o$. To shed further light on the effectiveness of the proposed solution, the same test is conducted on the traditional PHB-MCSI with a ten times smaller dead-time (0.25 μs). Since the OCF test would result in damage to the conventional configuration, this fault is only studied through simulation in MATLAB/Simulink environment. Fig. 9(e) and (f) shows the simulation results of

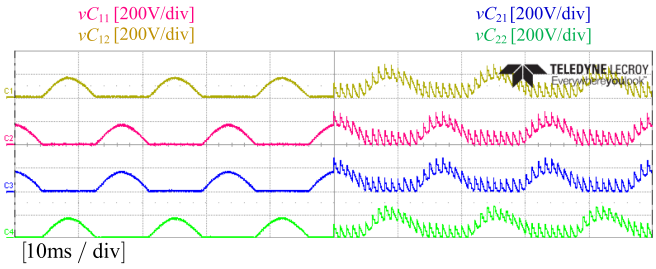


Fig. 10. Experimental results of the proposed PHB-MLSC^{2}SI under faulty (Test #2): stress voltage on SC capacitors.

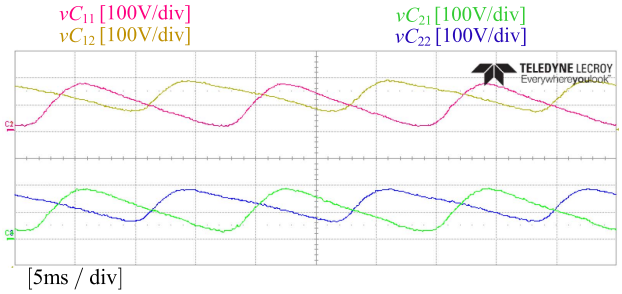


Fig. 11. Experimental results of the proposed PHB-MLSC^{2}SI under faulty condition (Test #3): stress voltage on SC capacitors.

the traditional PHB-MCSI under the mentioned fault operating conditions. As can be noticed from these figures, as soon as the OCF occurs, a huge overvoltage is imposed on all switches. It is indispensable to mention that the traditional PHB-MCSI will be drastically damaged even if the OCF occurs on a single switch, as it would interrupt the current of the input inductor.

2) Frequent Occurrence of OCF on All Switches: To validate the effectiveness of PS-PWM approach for the proposed converter, the second test (Test #2) is conducted. Fig. 10 illustrates the stress voltage on SC capacitors. Initially, the proposed topology operates under normal conditions. At 50 ms, frequent OCF occurs on all switches in the proposed circuit, with a time duration of 1.5 μs, leading to the charge of ΔV_C on SC capacitors. Similar to the previous faulty conditions, these additional voltages are reflected in the power devices. As observed from Fig. 10, the proposed converter can effectively handle this extreme faulty condition. It should be noted that several other PWM strategies, such as level shifted PWMs [e.g., phase disposition, alternative phase opposite disposition (POD), and POD] and low-frequency or half-cycle PWM are also applied to the proposed topology; however, none of them can handle this severe faulty condition.

3) OCF Occurrence on All Power Devices Due to Turn on Delay/Mismatch Among Complementary Switches: In the third test (Test #3), it is assumed that 0.5 μs is the minimum required value for overlap-time, and less than this value may cause OCF due to mismatch/delay in turning ON the complementary switches. Therefore, a 0.2 μs dead-time, instead of overlap-time, is intentionally inserted among all gating signals in the proposed converter to create OCF in every switching action. The outcome of this extreme faulty test is depicted in Figs. 11 and 12. As observed in these figures, the stress voltage pattern on SC capacitors and power devices differs from the previously observed faulty conditions. Switches S_{11}, S_{13}, S_{21}, and S_{23} closely track the stress voltage of C_{11} and C_{21} while the remaining switches exhibit different waveforms. Unlike the previous OCF (Tests #1 and #2) conditions, where all SC capacitors and power devices experience an extra voltage by the value of ΔV_C during the faulty situation, in the mismatch/delay in turning ON fault, only S_{12}, and S_{22} experience this value, while the stress voltage on remaining switches and SC capacitors are almost unaffected.

C. Under Dynamic Operating Condition

The stress on converters induced by transient conditions (e.g., sudden change in load/PF) influences their reliability as well [18]. To this end, the dynamic performance of the proposed PHB-MLSC^{2}SI is experimentally tested. According to Fig. 13(a), the load is suddenly changed from PF $= 0.99$ ($RL =$ 20 Ω, 7.5 mH) to PF $= 0.65$ ($RL = 20\ \Omega$, 62.5 mH) at around 38 ms and then returns from PF $= 0.65$ to PF $= 0.99$ again at almost 42 ms, as exhibited in Fig. 13(b). From Fig. 13, it can be observed that the proposed topology responds smoothly and robustly to this severe change, with the input inductors' currents remaining well-balanced.

D. Under Mismatch Operating Condition

1) Input dc Sources Mismatch: Various nonideal operating conditions are examined for the proposed topology. In the first test, a deliberate 4% mismatch is introduced between the voltage values of two input dc sources. In this scenario, the voltage of the upper input dc source is decreased from 73 to 70 V, while the voltage of the other source remains at its reference value. During this mismatched operating condition (see Fig. 14), the input dc currents deviate from their reference values. Despite the unbalanced currents in the input dc inductors, no degradation is observed in the output current and voltage waveforms. Under this mismatch condition, the current THD (i_{THD}) is equal to 2.31%.

Although PS-PWM can successfully handle this mismatch condition, if the difference in input dc voltage is significant (e.g., in PV applications caused by partial shading), there is a possibility of waveform deviation and, consequently, an increase in THD of output waveforms, as I_{dc} will be synthesized by significantly different I_{dc1} and I_{dc2}. Thus, additional considerations, such as exploring modified/new PWM/control methods or utilizing H-bridge cells with unequal dc voltage [16], can be pursued. This is recommended as future work for the proposed topology.

2) Input dc Chocks/Inductors Mismatch: Fig. 15 shows the performance of the proposed topology under input dc chokes mismatch, where 3 mH is added to the second inductor to create a 10% difference in inductors' value ($L_{\mathrm{dc1}} = 26$ mH and $L_{\mathrm{dc2}} =$ 29 mH). Despite the slight deviation in the inductors' currents from each other, the output current and voltage waveforms are not affected. The i_{THD} is 2.18% under this mismatch operating condition.

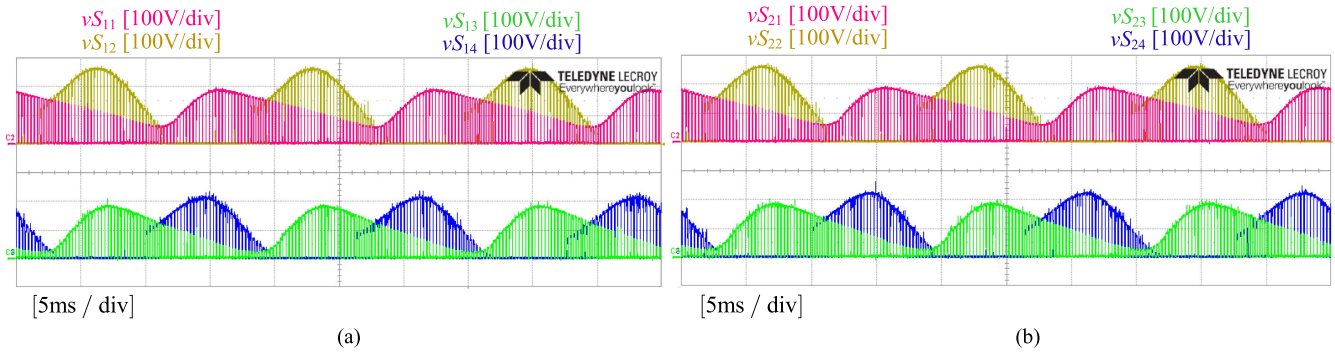


Fig. 12. Experimental results of the proposed PHB-MLSC^{2}SI under faulty condition (Test #3): stress voltage on switches.

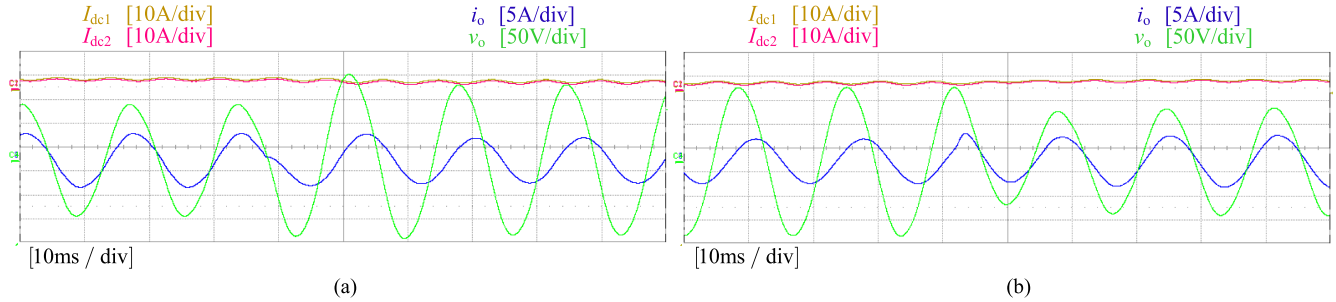


Fig. 13. Experimental results of the proposed PHB-MLSC^{2}SI under dynamic performance: input dc currents, output current, and output voltage. (a) From PF = 0.99 to PF = 0.65. (b) From PF = 0.65 to PF = 0.99.

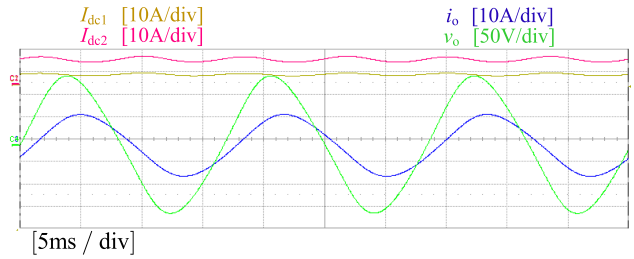


Fig. 14. Experimental results of the proposed PHB-MLSC2SI under input DC sources mismatch: input DC currents, output current, and output voltage.

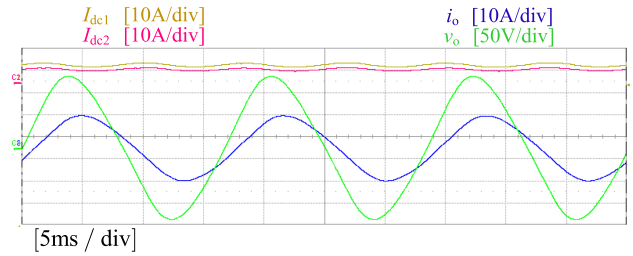


Fig. 15. Experimental results of the proposed PHB-MLSC^{2}SI under input DC inductors mismatch: input DC currents, output current, and output voltage.

3) Overlap-Time Mismatch: Fig. 16 depicts the waveforms of the proposed inverter, in which the value of overlap-time in switches S_{11}, S_{12}, S_{23}, and S_{24} is increased twenty times (δ = 6 μs), while overlap-time in switches S_{13}, S_{14}, S_{21}, and S_{22} is kept at $\delta = 0.3$ μs to make the effect of this mismatch condition

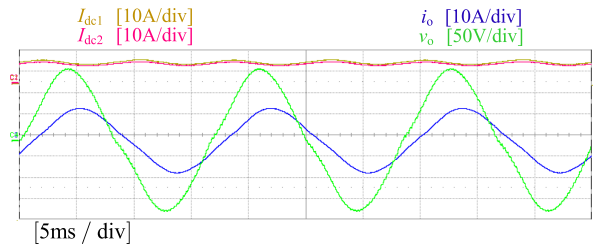


Fig. 16. Experimental results of the proposed PHB-MLSC^{2}SI under overlap-time -mismatch: input DC currents, output current, and output voltage.

visible. As the value of overlap-time among switches is extreme (twenty times), the input dc currents fail to distribute evenly, leading to deviation in the waveforms. Moreover, since the adverse effect of large overlap-time majorly contributes to the zero-cross condition, the deterioration of waveforms in this area is more visible [19], [20]. A significant overlap-time mismatch has a substantial impact on the load side, increasing the THD of the output current to 4.36%, while having an ignorable influence of dc currents.

4) Input dc Sources, Input dc Chocks, and Overlap-Time Mismatches At the Same Time: Finally, the most severe mismatch condition is examined in the proposed topology, where a 3% mismatch is created between the values of input dc voltage (V_{dc1} = 71 V and V_{dc2} = 73 V); 10% mismatch in input inductors' values (L_{dc1} = 26 mH, and L_{dc2} = 29 mH), and 300% mismatch in the overlap-times values ($\delta = 1$ μs in switches S_{11}, S_{12}, S_{23}, and S_{24} and $\delta = 0.3$ μs in switches S_{13}, S_{14}, S_{21}, and S_{22}) at the

TABLE IV
COMPARISON BETWEEN THE PROPOSED AND THREE OTHERS EXISTING FIVE-LEVEL CSIS

Topologies	S	D	In	C	MVS_S	MVS_D	MCS_S	MCS_D	MCS_L	MCS_{IMI}	δ	OCF_h	Di
SR-MLCSI	8	8	4	-	V_o	V_o	I_{dc}	I_{dc}	$2I_{dc}$	I_{dc}	Large	No	Large
MR-MLCSI	8	8	2	-	V_o	V_o	I_{dc}	I_{dc}	$2I_{dc}$	I_{dc}	Large	No	Large
PHB-MLCSI	8	8	-	-	V_o	V_o	I_{dc}	I_{dc}	I_{dc}	-	Large	No	Medi
Proposed inverter	8	8	-	4	V_o	V_o	I_{dc}	I_{dc}	I_{dc}	-	Smaller	Yes	Medi

Note: S: number of (No.) switches. D: No. diodes. In: No. inductors. C: No. capacitors. MVSS: maximum voltage stress on switch. MVSD: maximum voltage stress on diode. MCSS: maximum current stress on switch. MCSD: maximum current stress on diode. MCSL: maximum current stress on input inductor. MCSIMI: maximum current stress on intermediate inductors (IMI). δ: overlap-time. OCFh: OCF handling capability. Di: Dimension.

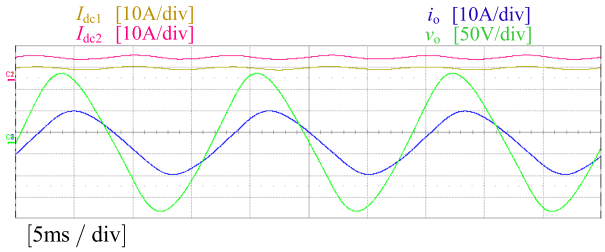


Fig. 17. Experimental results of the proposed PHB-MLSC^{2}SI under the mismatches of the values of input dc voltages, inductors' values, and overlap-time: input DC currents, output current, and output voltage.

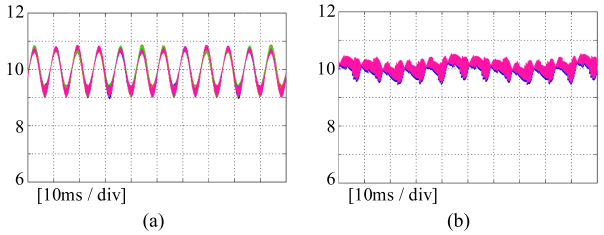


Fig. 18. (a) $i_{L11\text{-}22}$ [A] in SR-MLCSI. (b) $i_{L11\&12}$ [A] in MR-MLCSI.

same time. As evident from Fig. 17, the output waveforms are not influenced even under such a severe mismatch condition. During this mismatch situation, $i_{\mathrm{THD}} = 2.1\%$. By comparing Figs. 16 and 17, it can be concluded that even with three different mismatches (mismatch in input dc source values, mismatch in the value of the input dc inductors, and 1 μs mismatch in overlap-time) simultaneously, the quality of waveforms is much better than with just a larger overlap-time mismatch among switches.

A comparison is made between the proposed and three conventional MLCS to highlight the merits and demerits of the proposed circuit. To ensure a fair comparison, all topologies (see Fig. 1) are simulated using the same specifications (see Table III) and modulation method in the MATLAB/Simulink environment. The value of sharing/intermediate inductors (IMI), L_{11}, L_{12}, L_{21}, and L_{22} in SR-MLCSI, and MR-MLCSI was set at 2.5 mH to maintain their current ripple within 10%–20%

$$L_{11\sim22} = \frac{V_o\sqrt{3}}{4f_{sw}\Delta I_L}. \tag{17}$$

Fig. 18(a) and (b) displays the IMIs' currents in SR-MLCSI and MR-MLCSI, respectively. All IMIs in both converters carry half of the input dc current (10 A) and exhibit good balance thanks to the PS-PWM method. However, the IMIs in SR-MLCSI endure two times higher current ripple compared to ML-MLCSI, as it possesses both low and high frequency ripples. Table IV outlines the key features of the compared converters. The acronyms are defined at the bottom of Table IV. The number of switches and diodes is the same among the topologies. The SR-MLCSI has the highest number of inductors, followed by MR-MLCSI. Although the proposed topology possesses four extra capacitors in its structure, these SC capacitors bring several remarkable merits. Moreover, the footprint of these small SC capacitors is much smaller compared to the IMI inductors employed in SR-MLCSI and MR-MLCSI. In addition, in high-level configuration (e.g., nine-level) the number of IMIs is doubled in SR-MLCSI and MR-MLCSI, making the current balancing of inductors more complicated. In contrast, SC capacitors in the proposed inverter not do not require any voltage balancing controller, even in higher number of level configurations. However, a limitation of the proposed circuit is the requirement for additional input sources, similar to those in conventional PHB-MLCSI.

The stress voltage/current is similar among all configurations. To compare the total input dc current, $2I_{dc}$ is considered as a reference value for the total dc input current. Input inductors in SR-MLCSI and MR-MLCSI withstand two times higher currant than those in PHB-MLCSI and the suggested structure due to possessing a single dc source. IMIs are responsible for half of the input dc current in SR-MLCSI and MR-MLCSI.

As verified in the previous sections, even a tiny mismatch among gating signals (OCF) can create a serious problem in the system. However, the proposed PHB-MLSC^{2}SI is a structure that can effectively overcome this issue. Thus, it can be concluded that the proposed topology is a highly reliable structure from a system performance point of view.

The measured efficiency (using YOKOGAWA WT1800 power analyzer) of the proposed PHB-MLCSI configuration is depicted in Fig. 19, covering a wide range of output power. The lowest efficiency of the proposed inverter is at 20% of full load with a value of 92.8%, reaching the highest efficiency at 66% of full load with 94.9%, and experiencing a slight reduction at full load, which is 94.82%.

From the perspective of power density (dimension), the SR-MLCSI and MR-MLCSI have a higher footprint if the dc-link inductors are not considered, followed by the proposed inverter and traditional PHB-MLCSI. However, when considering the dc-link inductors, the footprint of the proposed inverter might be larger than that of other topologies.

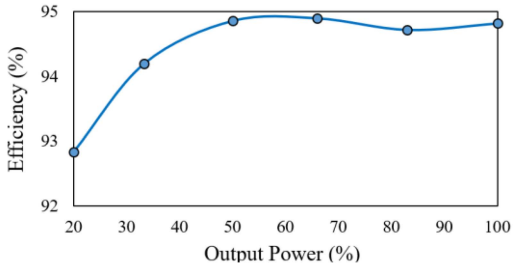


Fig. 19. Measured efficiency of the proposed topology.

IV. Conclusion

The conventional PHB-MLCSI is vulnerable to OCF, which is the major issue among traditional CSIs. To address this obstacle, a novel topology has been suggested in this work which also possesses all benefits of the conventional configuration, such as voltage boosting capability, the possibility to extend to a higher number of levels readily, and short circuit protection ability. Several PWM schemes have been applied to the proposed topology to investigate the efficacy of these control methods for the proposed circuit. The results have revealed that only the PS-PWM method can effectively address different OCF occurrences. Detailed theoretical analysis together with the experimental results have been provided to justify the effectiveness of the proposed solution. Moreover, additional experimental tests have been conducted under dynamic load change, and nonideal operating conditions to highlight the feasibility of the proposed topology. In the end, the proposed topology has been compared with three conventional counterparts from different perspectives to further highlight the effectiveness of the suggested solution.

References

[1] J. Rodríguez, S. Bernet, J. O. P. BinWu, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] N. R. Zargari et al., "A new current-source converter using a symmetric gate-commutated thyristor (SGCT)," *IEEE Trans. Ind. Appl.*, vol. 37, no. 3, pp. 896–903, May/Jun. 2001.

[3] B. Wu, J. Pontt, J. Rodríguez, S. Bernet, and S. Kouro, "Current-source converter and cycloconverter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2786–2727, Jul. 2008.

[4] Z. H. Bai and Z. C. Zhang, "Conformation of multilevel current source converter topologies using the duality principle," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2260–2267, Sep. 2008.

[5] E. P. Wiechmann, P. Aqueveque, R. Burgos, and J. Rodríguez, "On the efficiency of voltage source and current source inverters for high-power drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1771–1782, Apr. 2008.

[6] M.. R. Islam, A. M. Mahfuz-Ur-Rahman, K. M. Muttaqi, and D. Sutanto, "State of the art of the medium-voltage power converter technologies for grid integration of solar photovoltaic power plants," *IEEE Trans. Energy. Conv.*, vol. 34, no. 1, pp. 372–384, Mar. 2019.

[7] K. Gnanasambandam, A. K. Rathore, A. Edpuganti, D. Srinivasan, and J. Rodriguez, "Current-fed multilevel converters: An overview of circuit topologies, modulation techniques, and applications," *IEEE Trans. Power. Electron.*, vol. 32, no. 5, pp. 3382–3401, May 2017.

[8] M. Haberberger and F. W. Fuchs, "Novel protection strategy for current interruption in IGBT current source inverters," in *Proc. 35th Power Electrons. Spec. Conf.*, 2004, pp. 558–564.

[9] M. T. Fard, J. He, and Z. Wang, "Fault diagnosis and fault-tolerant operation of current source inverter for safety-critical applications," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2020, pp. 925–929.

[10] N. Mohan, *Power Electronics*. Hoboken, NJ, USA: Wiley, 2012.

[11] H. Patel and V. Agarwal, "A single-stage single-phase transformer-less doubly grounded grid-connected PV interface," *IEEE Trans. Energy. Conv.*, vol. 24, no. 1, pp. 93–101, Mar. 2009.

[12] D.-T. Do and H. Cha, "High-reliability and reduced switch count single-phase dual-output current source inverter using switching-cell structure," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6513–6524, Jun. 2017.

[13] F. Akbar, H. Cha, and D.-T. Do, "CSI7: Novel three-phase current-source inverter with improved reliability," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9170–9182, Aug. 2021.

[14] T.-T. Nguyen, H. Cha, D.-T. Do, and F. Akbar, "Modified SVPWM for three-phase six-switch switching-cell current source inverter," *IEEE Trans. Power. Electron.*, vol. 37, no. 12, pp. 14820–14830, Dec. 2022.

[15] F. L. M. Antunes, H. A. C. Braga, and I. Barbi, "Application of a generalized current multilevel cell to current-source inverters," *IEEE Trans. Ind. Electron.*, vol. 46, no. 1, pp. 31–38, Feb. 1999.

[16] B. Wu and M. Narimani, *High-Power Converters and AC Drives*. Hoboken, NJ, USA: Wiley, Jan. 2017.

[17] T.-T. Nguyen and H. Cha, "Five-level current source inverter with inductor cell using switching-cell structure," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6859–6869, Jul. 2022.

[18] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.

[19] Y. Geng et al., "An overlap-time compensation method for current-source space-vector PWM inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3192–3203, Apr. 2018.

[20] W. Suroso and T. Noguchi, "Overlap-time compensation technique for current-source power inverter," *IET Power Electron.*, vol. 13, no. 4, pp. 854–862, 2020.

Faramarz Faraji (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the Pooyesh Institute of Higher Education, Qom, Iran, in 2013, and the M.Sc. degree in electrical engineering from Islamic Azad University, Tehran, Iran, in 2016. He is currently working toward the Ph.D. degree in the field of power electronics with the School of Energy Engineering, Kyungpook National University, Daegu, South Korea.

From 2005 to 2009, he was a Train Diesel Generator Technician with Tehran Railway Company, Tehran. From 2009 to 2022, he was an Electrical Engineer with Tehran Regional Electric Company, Tehran. His current research interests include multilevel converters, fault tolerant converters, and modulation/control techniques.

Mr. Faraji was the recipient of the Best IEEE Conference Paper Award in 2022.

Honnyong Cha (Senior Member, IEEE) received the B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree in electrical engineering from Michigan State University, East Lansing, MI, USA, in 2009.

From 2001 to 2003, he was a Research Engineer with the Power System Technology Company, Ansan, South Korea. From 2010 to 2011, he was a Senior Researcher with the Korea Electrotechnology Research Institute, Changwon, South Korea. In 2011, he was with the School of Energy Engineering, Kyungpook National University. In 2017, he was a Visiting Scholar with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His current research interests include high-power dc–dc converters, dc–ac inverters, Z-source inverters, and power conversion for electric vehicles and wind power generation.