Output Capacitance Loss of GaN HEMTs in Steady-State Switching

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***Abstract*—The output capacitance (C_{OSS}) loss, a loss produced when the device's output capacitor is charged and discharged, has become a concern for GaN high electron mobility transistors (HEMTs) in high-frequency applications. This work presents a new, easy-to-implement method for the C_{OSS} loss characterization based on the unclamped inductive switching setup. As compared with prior approaches, this method involves the device's ON-state conduction and could measure the C_{OSS} loss in a single pulse and the steady-state switching. The C_{OSS} loss of three types of the mainstream commercial GaN HEMTs is characterized, which exhibit some common dependencies including a nonmonotonic relation with the *dv/dt* (or resonance frequency), a linear relation with the ON-state current, a power-law relation with the peak blocking voltage, and a little temperature dependence. In addition, their C_{OSS} losses all show minimal distinctions in a single pulse and the steady-state switching, despite the increased ON-resistance in the steady-state switching. This suggests that the traps accounting for the C_{OSS} loss possess different detrapping time constants as compared with the traps governing the dynamic ON-resistance. Finally, a unified model is established to describe the C_{OSS} loss of all three types of GaN HEMTs. These results provide important references for the high-frequency application of GaN HEMTs and new insights into the physical origin of their C_{OSS} loss.**

***Index Terms*—Gallium nitride, high electron mobility transistor (HEMT), high frequency, modeling, output capacitance loss, resonant converters, simulation, unclamped inductive switching (UIS).**

I. Introduction

BENEFITTING from the high mobility of the two-dimensional electron gas (2DEG) channel and the high critical field of GaN, GaN high electron mobility transistors (HEMTs) open the door for high-frequency, more efficient power electronics [1], [2], [3], [4]. Currently, the GaN HEMT has been commercialized from 15 to 900 V and is one of the most promising device solutions for high-frequency power electronics in wireless charging, fast charger, data centers, and electric vehicles [5], [6], [7].

Despite the promise, the dynamic loss induced by the trapped charges in GaN HEMTs is a bottleneck for further adoption of these devices, particularly at very high frequencies up to the megahertz level [2]. A well-known issue is the dynamic drain-to-source ON-resistance ($R_{DS,ON}$), which makes HEMTs suffer from an increased conduction loss during switching [8], [9], [10].

The other dynamic loss issue associated with the switching loss is the output capacitance (C_{OSS}) loss [11], [12], [13]. This loss is the dissipated energy (E_{DISS}) that occurs when the device C_{OSS} is charged and discharged once per switching cycle during the device's OFF-state. For an ideal capacitor, this process should be lossless in theory. However, recent studies have revealed considerable E_{DISS} in some power devices, e.g., Si superjunction, SiC MOSFETs, and GaN HEMTs [5], [14], [15], [16], [17], [18], [19]. Among them, GaN HEMTs generally show higher E_{DISS} than Si and SiC devices [20]. This loss was found to increase with frequency and could dominate the device's total losses in soft-switching converters at the megahertz frequency [11], [12].

The accurate E_{DISS} measurement is of paramount importance but very challenging. Several approaches have been proposed to characterize the E_{DISS} of GaN HEMTs, as summarized in Table I. In the Sawyer-Tower circuit [11] and calorimetric method [12], the device under test (DUT) is in the OFF-state with its gate and source shorted, functioning as a passive C_{OSS} in the converter. Hence, these methods have the limited capability to study the E_{DISS}'s possible dependence on the DUT's ON-state operation. On the other hand, key learning from the dynamic $R_{DS,ON}$ study is the critical roles of the ON-state current and switching locus in determining the trapping state in GaN HEMTs [9]. As traps have been reported to be a possible origin of E_{DISS}

TABLE I
Comparison of Previously Reported Approaches With the Current One to Characterize C_{OSS} Losses of GaN HEMTs

Method	Steady State	DUT ON-state	Extraction of C_{OSS} Losses
Sawyer-Tower [11]	Yes	No	Relatively Simple
Calorimetric [12]	Yes	No	Complicated
Nonlinear Resonance [22]	No	Yes	Relatively Simple
UIS (this work)	Yes	Yes	Simple

Manuscript received 17 January 2023; revised 11 April 2023; accepted 16 May 2023. Date of publication 23 May 2023; date of current version 20 March 2024. This work was supported in part by PowerAmerica Member-Initiated Project through the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, under Award DE-EE0006521, and in part by Virginia Tech Center for Power Electronics Systems Industry Consortium. Recommended for publication by Associate Editor M. Nawaz. *(Corresponding authors: Qihao Song; Yuhao Zhang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3279308.

Digital Object Identifier 10.1109/TPEL.2023.3279308

[11], E_{DISS} could depend on the ON-state current. However, this possible dependence has been rarely studied previously and remains a knowledge gap.

Another knowledge gap is the E_{DISS}'s possible distinction in a single switching pulse and steady-state switching. In [21] and [22], a nonlinear resonance method is proposed for E_{DISS} characterization. This method involves the DUT's ON-state operation before the OFF-state C_{OSS} resonance, but the E_{DISS} characterization is performed in a single pulse. However, the trapping state of GaN HEMTs may differ in a single pulse and steady-state switching [23]. For instance, the dynamic $R_{DS,ON}$ [8], [10] and dynamic breakdown voltage [24], [25], [26], the two well-known dynamic phenomena of GaN HEMTs, both show a large distinction in a single pulse and steady-state switching due to the time-dependent carrier trapping/detrapping behaviors in the device structure.

To address these two gaps, we propose a new, accurate, easy-to-implement C_{OSS} loss measurement approach, which enables studies of the E_{DISS}'s dependence on ON-current, OFF-state blocking voltage, *dv/dt* or resonance frequency (f_R), and temperature. In addition, this approach allows for the E_{DISS} measurement in a single pulse and the steady-state switching, and can, thus, probe the E_{DISS}'s dependence on the steady-state switching frequency (f_{SW}). Based on a unified setup, this approach was applied to measure the E_{DISS} of three mainstream commercial GaN HEMTs. Despite the significant distinction in the device structure, their E_{DISS} shows common dependences, which allows for developing a unified model for device users and sheds light on understanding the physical origin of the C_{OSS} loss in GaN HEMTs. Note that a part of these results is presented at a conference [27]. This article includes extensively more experimental results as well as the models and physical origin discussion that were not present in [27].

The rest of this article is organized as follows. Section II describes the new approach for the C_{OSS} loss measurement, covering the basic principle, mathematical model, hardware setup, and error analysis. Sections III and IV present the C_{OSS} loss measurement in a single pulse and steady-state switching, respectively, as well as the relevant measurement results for all three DUT's. Section V establishes an empirical E_{DISS} model for all DUT's. Section VI probes the physical origin of C_{OSS} loss and provides simulation verifications. Finally, Section VII concludes this article.

II. C_{OSS} Loss Measurement Methodology

A. DUT and Test Setup

The proposed new E_{DISS} characterization method is based on the unclamped inductive switching (UIS) circuit, as shown in Fig. 1(a). The UIS test consists of a power supply in series with a load inductor (L_{load}) and the DUT. Benefitted from the capability to produce fast, high-voltage overshoot under a small bus voltage (V_{bus}), the UIS test has been widely utilized to characterize the overvoltage, surge energy, and avalanche capabilities of power devices [25], [26], [28], [29], [30], [31].

A UIS test mainly contains three stages [25], [28]: in stage I, the DUT is ON, L_{load} is charged by V_{bus}; in stage II, the DUT is turned OFF, and L_{load} resonates with the DUT's C_{OSS} for about a half resonance cycle, which mimics the device operation in resonant converters; in stage III, the DUT conducts reversely, and the resonance gradually dies down. A small V_{bus} of 5 V is used to minimize the hard turn-OFF loss, preventing the DUT from overheating in the steady-state characterization. A capacitor bank (C_{bus}) with large capacitance is in parallel with the power supply to stabilize the bus voltage. Fig. 1(b) shows a photograph of the prototyped test system for TO-247 packaged devices. Air-core Litz-wire-based inductors, which can be modeled as a serial connection of an equivalent resistor and an ideal inductor, are used in the setup for L_{load}, as they are known to produce low and computable losses at high frequencies [22]. A commercial screw-in coaxial shunt resistor with resistance (R_{SHUNT}) of 0.1 Ω measures the DUT drain-to-source current (I_{DS}) with a marginal insertion inductance [32]. The DUT's drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}) are measured by the Tektronix P5100A and TPP1000 probes, respectively. The UIS testing waveform is captured with a Tektronix MSO64 oscilloscope with up to 8 GHz analog bandwidth and 12-bit analog-to-digital converter (ADC) for high horizontal and vertical resolutions. A fresh DUT is used in each measurement to eliminate the possible impact of the DUT's historical operation on E_{DISS}. Over 100 devices from each type of the DUT are meaurered, and good statistical significance is observed.

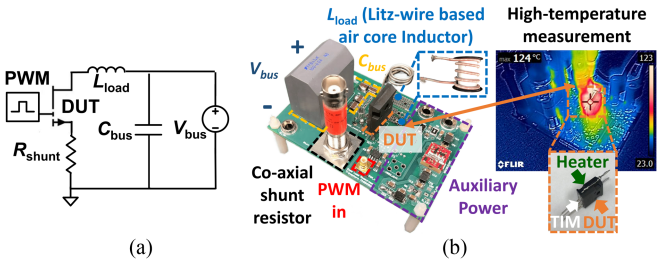

Fig. 1. (a) Schematic of the UIS circuit. (b) Photograph of the test system for TO-247 packaged devices. A power resistor that functions as a heater is stacked onto the DUT's heat slug for high-temperature measurement.

TABLE II
Main Characteristics of the Tested GaN HEMTs

Technology	Part Number	V_{DS} (V)	I_{DS} (A)	C_{OSS} (pF)	E_{OSS} at 400 V (μJ)
P-gate	GS66508T	650	30	65	7
HD-GIT	IGOT60R070D	600	31	72	6.4
Direct-drive	LMG3410R050	600	34	89	9.52

Table II summarizes the three types of DUT's in this work. They are commercial, similarly rated (600/650-V, 30-A) GaN HEMTs with different technologies: P-gate GaN HEMT, hybrid-drain gate injection transistor (HD-GIT), and direct-drive GaN HEMT [3]. The device case temperature is monitored with a Flir E5 thermal camera. Thermal analysis using the datasheet thermal resistance reveals a very small difference (<1 °C) between the junction temperature and case temperature under the UIS

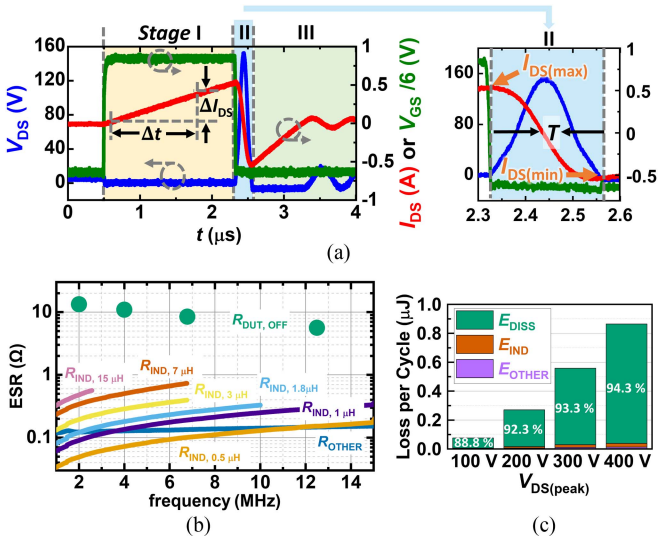

Fig. 2. (a) Typical UIS waveform and zoom-in of stage II from which the E_{DISS} is extracted. (b) Comparison of the ESR of passive components (various inductors, capacitors, and PCB) and the effective ESR of the DUT at various frequencies. (c) Loss breakdown of in the half-cycle resonance of the UIS test; the P-gate GaN HEMT is the DUT, and the UIS is at $V_{\mathrm{DS(peak)}}$ of 100–400 V and L_{load} of 15 μH.

operation. For high-temperature measurements, a power resistor, functioning as a heat source, is stacked onto the DUT's heat slugs and isolated with the TIM.

B. C_{OSS} Loss Extraction

Fig. 2(a) shows an examplar UIS waveform and illustrates the E_{DISS} extraction from the resonance portion of the UIS waveform in stage II. The total loss (E_{TOTAL}) in the half-cycle resonance can be calculated from the I_{DS}, which is equal to the inductor current (I_L) at the start and end of this resonance, i.e., $I_{\mathrm{DS(min)}}$ and $I_{\mathrm{DS(max)}}$

$$E_{\mathrm{TOTAL}} = 0.5\, L \left(I_{\mathrm{DS(max)}}^2 - I_{\mathrm{DS(min)}}^2\right) \tag{1}$$

where L is the L_{load}'s inductance; $I_{\mathrm{DS(max)}}$ and $I_{\mathrm{DS(min)}}$ can be obtained from the peak and valley points of the DUT's' I_{DS}, respectively, as shown in the zoom-in of stage II waveform in Fig. 2(a). L is measured using a Keysight E4990A impedence analyzer at the frequency of the stage II resonace. L can also be directly approximated from stage I waveform, where L_{load} is charged by V_{bus}, considering that $R_{\mathrm{DS,ON}}$ and R_{SHUNT} are small

$$L = \left[V_{\mathrm{bus}} - \left(I_{\mathrm{DS(max)}}/2\right)\left(R_{\mathrm{DS,\ ON}} + R_{\mathrm{SHUNT}}\right)\right] \Delta t/\Delta I_{\mathrm{DS}} \tag{2}$$

where $R_{\mathrm{DS,ON}}$ is the ON-resistance of the DUT; and $\Delta t/\Delta I_{\mathrm{DS}}$ is the reciprocal of the current slew rate extracted from the waveform.

The DUT's C_{OSS} loss can then be derived by subtracting other losses from E_{TOTAL} that occur in the half-cycle resonance. These losses mainly include the winding losses of the L_{load} (E_{IND}) and other conduction losses (E_{OTHER}) containing the losses of the shunt resistor (E_{SHUNT}), the printed circuit board (PCB) parasitics (E_{PCB}), and C_{bus} (E_{CAP}). E_{IND} and E_{OTHER} can be calculated by

$$E_{\mathrm{IND}} = \left(I_{\mathrm{DS(max)}}/2\right)^2 R_{\mathrm{IND}}\, T \tag{3}$$

$$E_{\mathrm{OTHER}} = E_{\mathrm{SHUNT}} + E_{\mathrm{PCB}} + E_{\mathrm{CAP}} = \left(I_{\mathrm{DS(max)}}/2\right)^2 \left(R_{\mathrm{SHUNT}} + R_{\mathrm{PCB}} + R_{\mathrm{CAP}}\right) T \tag{4}$$

where $I_{\mathrm{DS(max)}}/2$ is the rms value of I_{DS} over the half resonance cycle; R_{IND}, R_{SHUNT}, R_{PCB}, and R_{CAP} are the equivalent serial resistance (ESR) of the L_{load}, shunt, PCB, and C_{bus}. T is the time of the half resonance cycle. These ESRs are measured at different frequencies in the range of 1–15 MHz on a Keysight E4990A impedance analyzer.

Based on (1)–(4), E_{DISS} can be then expressed as follows:

$$E_{\mathrm{DISS}} = E_{\mathrm{TOTAL}} - E_{\mathrm{IND}} - E_{\mathrm{OTHER}} \tag{5}$$

The ESR-associated losses, i.e., E_{IND} and E_{OTHER}, are small compared with E_{DISS}, which ensures measurement accuracy. Here, we present two angles to validate this comparison.

First, if we model the OFF-state device as an ESR in series with a lossless C_{OSS}, the effective DUT ESR ($R_{\mathrm{DUT,OFF}}$) can be calculated by

$$E_{\mathrm{DISS}} = \left(I_{\mathrm{DS(max)}}/2\right)^2 R_{\mathrm{DUT,\ OFF}}\, T \tag{6}$$

Fig. 2(b) shows a comparison of the ESRs of various components over frequency, revealing that the DUT's $R_{\mathrm{DUT,OFF}}$ is much higher than the passive components. This validates the dominance of E_{DISS} in E_{TOTAL}.

Second, we calculate the loss breakdown for E_{TOTAL} with the DUT's peak voltage ($V_{\mathrm{DS(peak)}}$) of 100–400 V. As shown in Fig. 2(c), the DUT's E_{DISS} accounts for 88.8%–94.3% of E_{TOTAL}. Note that, in theory, the DUT's turn-OFF switching loss is not included in E_{TOTAL}. When I_{DS} reaches $I_{\mathrm{DS(max)}}$, the DUT's V_{DS} equals V_{bus} and the switching transition should be complete. However, the circuit parasitics may couple this loss with E_{TOTAL}. Even in this case, from the loss calculation standpoint, by using the very low V_{bus} (5 V), the DUT's hard-switching turn-OFF loss is marginal as compared with E_{TOTAL}, leading to minimal impact on the E_{DISS} extraction.

Finally, we performed a sanity check by replacing the DUT with a composite device with a similar capacitance in the UIS test. The composite device comprises a low-C_{OSS} Si MOSFET in parallel with several low-ESR capacitors (Mica and C0G ceramic), which is expected to have minimal E_{DISS}. The UIS test results of this composite device exhibited very small E_{TOTAL} and E_{DISS} as compared with the counterparts for the DUT, which is consistent with the expectation and further validates the overall test setup and method.

C. Error Analysis

Since the L_{load}–C_{OSS} resonance frequency is above MHz, the repeatability and variability of the measurement results need to be carefully examined. This is particularly critical for high-voltage, high-frequency E_{DISS} measurements considering the equipment's finite bandwidth and sampling rate. As an examination, ten UIS measurements are made straight with minutes of relaxation before each for all types of DUT's in this work.

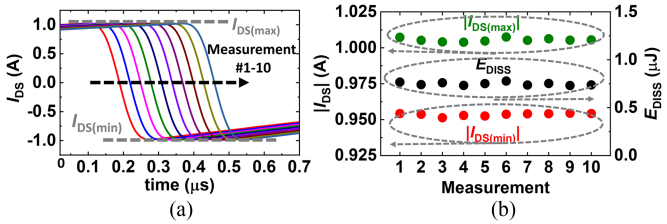

Fig. 3. (a) I_{DS} waveforms of ten successive measurements, illustrating good consistency. (b) Measured $I_{DS(max)}$ and $I_{DS(min)}$ and calculated E_{DISS} from the ten measurements, indicating a maximum ±3% variation in E_{DISS}.

Fig. 3(a) shows a set of ten lined-up I_{DS} waveforms of a P-gate GaN HEMT with a $V_{DS(peak)}$ of 400 V. The waveforms illustrate good consistency with no observable variability. Fig. 3(b) shows the values for $I_{DS(max)}$, $I_{DS(min)}$, and the derived E_{DISS} from these ten measurements, revealing the statistical variation below ±3% for all these parameters. Similar variability checks are performed for all types of DUT's under all test conditions, and a ±3% error range is found to hold for all these tests.

III. Single-Pulse C_{OSS} Loss Measurement

A. General Impacts of Frequency, Current, and Voltage

The potential impact factors for E_{DISS} in a single UIS pulse include the f_R (and *dv/dt*), $V_{DS(peak)}$, $I_{DS(max)}$, and temperature. Besides the temperature, the other four parameters are interdependent. In this section, their modulation methods and relations are illustrated.

The f_R in each UIS cycle can be modulated by tuning L of the load inductor

$$f_R = 1/(2\pi\sqrt{LC_{OSS}}). \tag{7}$$

Under the same L (and f_R), $V_{DS(peak)}$ is determined by $I_{DS(max)}$, and $I_{DS(max)}$ is modulated by the charging time in phase I (t_C)

$$V_{DS(peak)} = I_{DS(max)}\sqrt{L/C_{OSS}} \tag{8}$$

$$I_{DS(max)} = \left[V_{bus} - \left(I_{DS(max)}/2\right)\left(R_{DS,\,ON} + R_{SHUNT}\right)\right]/L \cdot t_C \tag{9}$$

The average *dv/dt* in resonance scales with $V_{DS(peak)}$ and f_R

$$(dv/dt)_{avg} = 2V_{DS(peak)}/\left(\pi\sqrt{LC_{OSS}}\right) = 4V_{DS(peak)}f_R \tag{10}$$

Fig. 4(a) shows the experimental UIS waveforms under the same load inductor but different t_C, illustrating the concurrent modulation of $V_{DS(peak)}$ and $I_{DS(max)}$. Note the UIS period (and f_R) also shows variation, which is due to the nonlinear relation between C_{OSS} and V_{DS} (i.e., for higher $V_{DS(peak)}$, the average C_{OSS} is lower).

As prior methods on E_{DISS} of GaN HEMTs all studied the impact of f_R and $V_{DS(peak)}$ through changing the loop inductance and resonant current, respectively; we follow a similar test procedure based on the UIS method. For all three DUT's, air-core inductors with L of 0.5–15 μH are employed to enable an f_R range from 2 to 12.5 MHz, and under each L, $V_{DS(peak)}$ is modulated by t_C up to 600 V [see Fig. 4(b)–(d)].

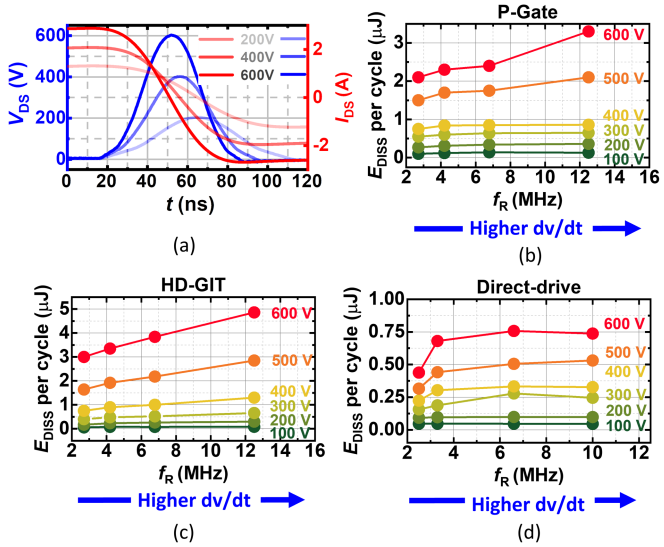

Fig. 4. (a) Set of UIS waveforms under the same load inductor and various charging time, showing the concurrent modulation of $V_{DS(peak)}$ and $I_{DS(max)}$. E_{DISS} as a function of f_R for (b) P-gate HEMT, (c) HD-GIT, and (d) direct-drive HEMT at various $V_{DS(peak)}$.

In general, all three DUT's show higher E_{DISS} as f_R increases, but the magnitude of the increase depends on $V_{DS(peak)}$. When $V_{DS(peak)}$ is below 400 V, the P-gate GaN HEMT and direct drive have little E_{DISS} increase with f_R, while the HD-GIT shows a more pronounced increase. When $V_{DS(peak)}$ is above 400 V, all three DUT's show the E_{DISS} increase with f_R.

One may find that these data cannot strictly reveal the E_{DISS}'s dependence on f_R or $V_{DS(peak)}$ due to the concurrent variation in $I_{DS(max)}$. For example, under the same f_R, the E_{DISS} dependence on $V_{DS(peak)}$, as shown in Fig. 4, could also originate from the $I_{DS(max)}$ variation. As mentioned in Section I, the impact of ON-current on E_{DISS} remains a knowledge gap in the literature. Some reports [16] even found a considerable impact of the capacitive current on the E_{DISS} of the always-OFF DUT.

The above discussion suggests that the non-separate modulation of L and conductive/capacitive current, which is used in most prior literature, has unignorable limitations. In the following sections, we present new approaches for the relevant modulation. In addition, due to the nonmonotonic relation between E_{DISS} and f_R, in the remaining characterizations to be presented in this article, we select two f_R of 2 and 6.78 MHz, which is of great interest for high-frequency resonant converter [33] and wireless power transfer [34], [35] applications, respectively.

B. Dependence on ON-State Conduction Current

To probe the E_{DISS}'s dependence on $I_{DS(max)}$, other variables, e.g., $V_{DS(peak)}$ and f_R, must be kept unchanged. This can be achieved in the UIS setup by paralleling external C0G ceramic capacitors to the DUT's C_{OSS}, as illustrated in Fig. 5(a). In each test set, multiple surface-mounted capacitors are placed in parallel to achieve a marginal ESR, leading to a negligible loss addition for the system. In this modified UIS circuit, f_R can

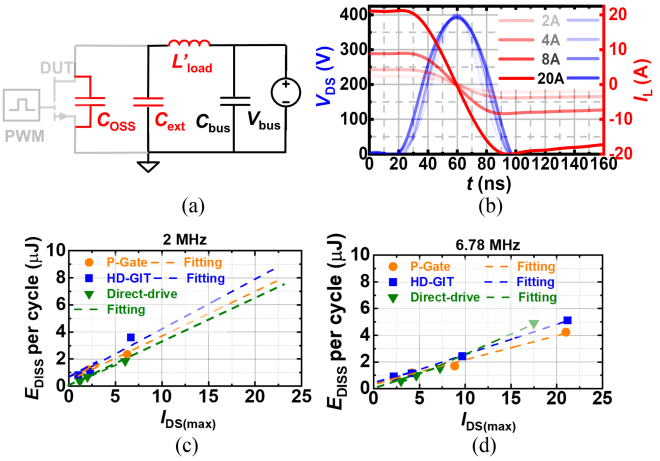

Fig. 5. (a) Schematic of the modified UIS circuit to achieve various $I_{DS(max)}$ keeping $V_{DS(peak)}$ and f_R constant. (b) UIS waveforms with various currents from 2 to 20 A under the same $V_{DS(peak)}$ of 400 V and f_R of 6.78 MHz. E_{DISS} of P-gate HEMT, HD-GIT, and direct-drive HEMT as a function of $I_{DS(max)}$ at $V_{DS(peak)}$ of 400 V and f_R of (c) 2 MHz and (d) 6.78 MHz.

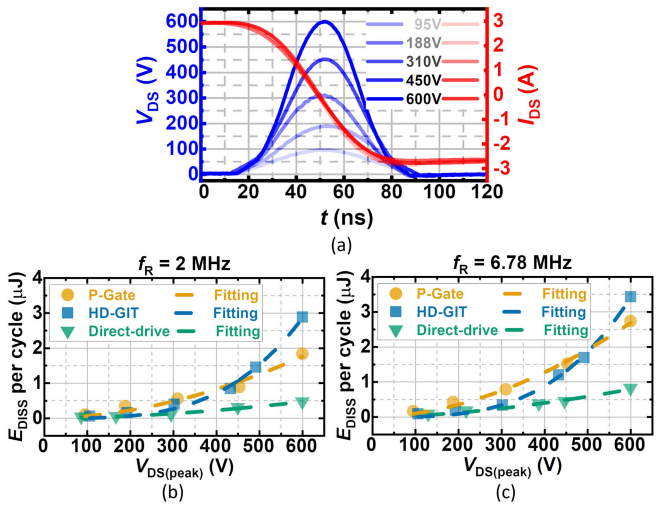

Fig. 6. (a) UIS waveforms with various $V_{DS(max)}$ from ~100 to 600 V under the same $I_{DS(max)}$ of 3 A and f_R of 6.78 MHz. E_{DISS} of P-gate, HD-GIT, and direct-drive HEMTs as a function of $V_{DS(peak)}$ under the same $I_{DS(max)}$ and at f_R of (b) 2 MHz and (c) 6.78 MHz.

be derived similarly to (1)

$$f_R = 1 / \left[2\pi\sqrt{L'(C_{OSS} + C_{ext})}\right] \tag{11}$$

where C_{ext} is the external capacitance, and L' is the adjusted inductance as required to maintain the constant f_R after C_{ext} is added to the system.

Similar to (10), $I_{DS(max)}$ can be expressed as follows:

$$I_{DS(max)} = V_{DS(peak)} \sqrt{(C_{OSS} + C_{ext})/L'} \tag{12}$$

According to (8), $I_{DS(max)}$ can be increased by increasing C_{ext} and reducing L' at the same time while optimizing the C_{ext} and L' based on (11) to maintain the f_R unchanged. Fig. 5(b) shows a series of UIS waveforms with various $I_{DS(max)}$ but the constant $V_{DS(peak)}$ and f_R. Note that C_{ext} and L' are carefully selected to also compensate for the impact of C_{OSS}'s voltage nonlinearity, enabling a superior f_R consistency (<3 ns variation in the half-cycle resonance duration) over the fixed L case [see Fig. 4(a)].

Fig. 5(c) and (d) show the E_{DISS} of three DUT's as a function of $I_{DS(max)}$ at f_R of 2 MHz and 6 MHz, respectively. All the measurements are performed at $V_{DS(peak)}$ of 400 V. All three DUT's show the increased E_{DISS} with $I_{DS(max)}$, and their relation can be well fitted by a linear relation.

C. Dependence on Peak Blocking Voltage

For a selected f_R, using the circuit in Fig. 5(a), the $V_{DS(peak)}$ can be tuned similarly by adjusting L' and C_{ext} without affecting $I_{DS(max)}$ and f_R

$$V_{DS(peak)} = I_{DS(max)} \sqrt{L'/(C_{OSS} + C_{ext})} \tag{13}$$

Fig. 6(a) shows the UIS waveforms with various $V_{DS(peak)}$ while keeping I_{DS} and f_R constant. At the two f_R of 2–6.78 MHz, the E_{DISS} of all three DUT's are characterized for the $V_{DS(peak)}$ ranging from 100 to 600 V, as shown in Fig. 6(b) and (c). For all three DUT's, the E_{DISS}–$V_{DS(peak)}$ dependence can be generally fitted by a power-law relation with a characteristic power-law coefficient specific to the DUT and f_R.

D. Dependence on Temperatures

Using the simple modulation method in Section III-A and the setup shown in Fig. 1(b), the E_{DISS} of three DUT's are measured at 25 °C, 75 °C, and 125 °C under various $V_{DS(peak)}$–$I_{DS(max)}$ conditions. Fig. 7(a)–(c) show the E_{DISS} of the three DUT's at the two f_R and various temperatures, revealing nearly no dependence of E_{DISS} on temperature for all three DUT's under varying f_R, $V_{DS(peak)}$, and $I_{DS(max)}$ conditions. As far as we know, this E_{DISS}'s temperature independence is revealed for the first time for GaN HEMTs.

IV. Steady-State C_{OSS} Loss Measurement

As mentioned in Section I, since the historical operation could impact the trapping state in the device [8], [24], the E_{DISS} measured in the steady-state switching could be different from that in a single pulse. From the device standpoint, exploration of this possible difference is very useful to understand the dominant trapping/detrapping time constant that is related to the C_{OSS} loss.

As shown in Fig. 8, the E_{DISS} in the steady-state switching can be extracted from the repetitive UIS test: the DUT is first put in the continuous UIS switching for over 10 min to reach the steady state, followed by the E_{DISS} extraction from the last UIS switching cycle. In addition to the f_R that describes the resonance pulse duration and *dv/dt*, another parameter f_{SW} is also relevant in the C_{OSS} loss measurement under the steady-state switching. From the application standpoint, the extracted E_{DISS} provides a reference for generic switching operations with the same f_{SW} (beyond the resonant converters with a frequency f_R), as the device C_{OSS} is charged and discharged once in a generic switching cycle. Although the device turn-ON and turn-OFF switching locus are usually different from the resonant locus

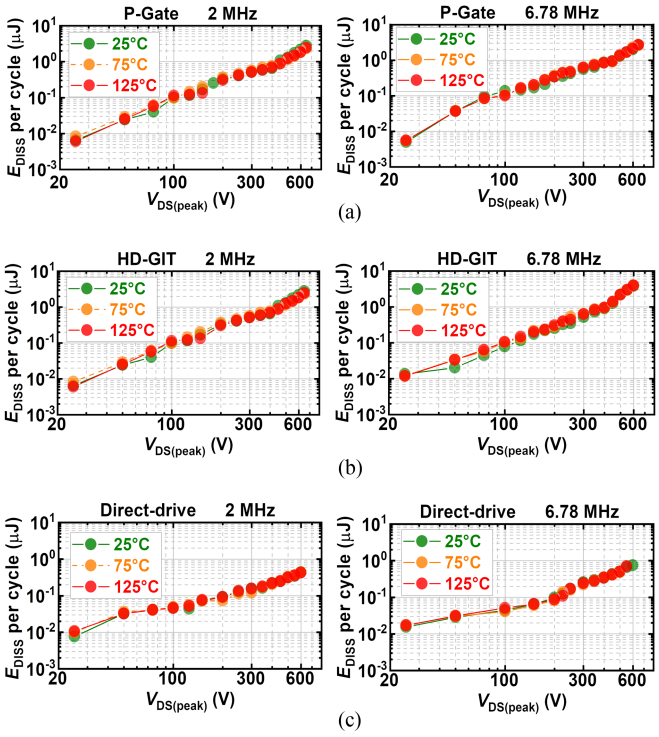

Fig. 7. E_{DISS} of (a) P-gate HEMT, (b) HD-GIT, and (c) direct-drive HEMT under various $V_{DS(peak)}$–$I_{DS(max)}$ conditions (as represented by $V_{DS(peak)}$) at 25 °C, 75 °C, and 125 °C as well as at f_R of 2 and 6.78 MHz.

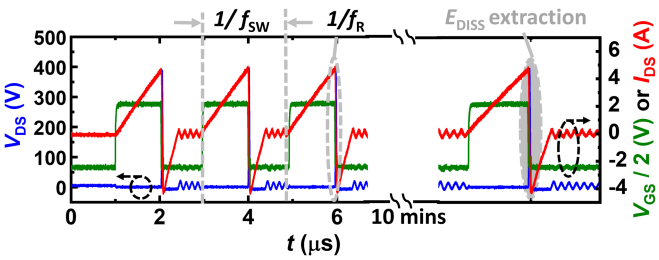

Fig. 8. Waveform for steady-state E_{DISS} extraction. The steady-state E_{DISS} is extracted in the last switching cycle during the 10-min switching.

in the UIS test, the revealed E_{DISS} dependence on *dv/dt*, f_{SW}, $V_{DS(peak)}$, $I_{DS(max)}$, and temperature are expected to hold for these more generic switching applications.

Fig. 9 shows the E_{DISS} as a function of $V_{DS(peak)}$ in a single pulse and the steady-state switching at f_{SW} of 50, 200, and 500 kHz. For all these measurements, f_R, $I_{DS(max)}$, and temperature are 6.78 MHz, 3 A, and 25 °C, respectively. Interestingly, the E_{DISS} in the steady-state switching of all three DUT's are nearly identical to their counterpart in the single pulse. The difference is generally within 3%, i.e., the error range of the test setup. The only exception is found for the P-gate HEMT at $V_{DS(peak)}$ over 600 V, where a slightly larger difference (up to 15%) is present in the E_{DISS} under the steady-state switching and a single pulse.

Since the DUT is turned ON and OFF in each UIS cycle, the trapping-induced (dynamic) $R_{DS,ON}$ increase is expected; it is also known that, at high f_{SW}, the $R_{DS,ON}$ recovery takes

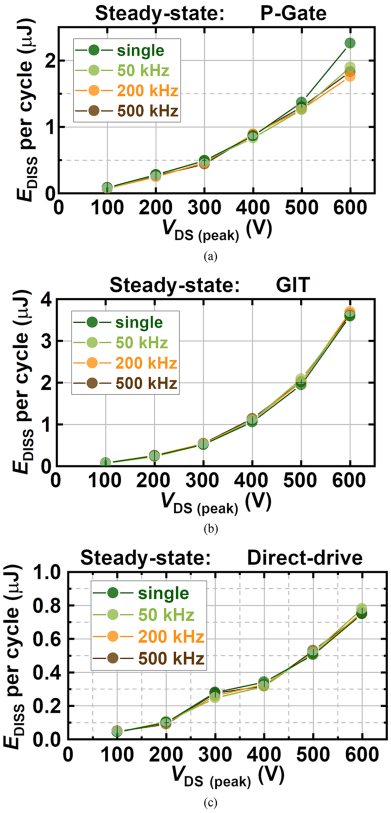

Fig. 9. Comparison of E_{DISS} of (a) P-gate HEMT, (b) HD-GIT, and (c) direct-drive HEMT, extracted at a single pulse and steady-state switching with f_{SW} of 50, 200, and 500 kHz. The f_R, $I_{DS(max)}$, and temperature are 6.78 MHz, 3 A, and 25 °C, respectively.

a longer time (at least several minutes) [9], [25]. Hence, the DUT's right after the repetitive UIS tests are characterized on a Keysight B1505A power device analyzer (the transition time from taking the DUT's from the circuit board to B1505A is about 1.5 min), followed by another set of characterizations after an additional 6-min relaxation. Fig. 10(a)–(d) show the I_{DS}–V_{DS} setup and characteristics of three DUT's before and right after the repetitive UIS tests (f_{SW} = 500 kHz, $V_{DS(peak)}$ = 400 V, and $I_{DS(max)}$ = 3 A) and after the relaxation. An increase in $R_{DS,ON}$ is shown in P-gate HEMT and HD-GIT after the steady-state switching, which is not fully recovered after the 6-min relaxation, suggesting a long detrapping time and deep-level trapping energy.

This $R_{DS,ON}$ increase is also confirmed by the last UIS waveform for E_{DISS} extraction in which $V_{DS(peak)}$ is slightly lower than that in the initial UIS cycles due to the smaller $I_{DS(max)}$ for the same DUT ON-time in stage I of the UIS cycle. For a fair comparison, the single-pulse E_{DISS}, as shown in Fig. 9, is extracted under the $V_{DS(peak)}$ that has been adjusted to be the same as that in the last UIS cycle.

The unchanged C_{OSS} loss albeit the increased $R_{DS,ON}$ suggests the different detrapping time constants of the traps that govern the dynamic $R_{DS,ON}$ and C_{OSS} loss phenomena. This new learning will be further discussed in Section VI for probing the physical causes of the C_{OSS} loss.

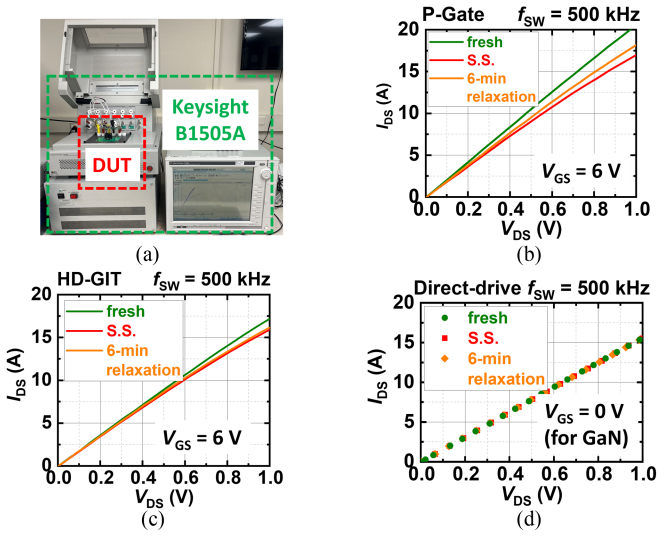

Fig. 10. (a) Setup for $R_{DS,ON}$ characterization. $R_{DS(ON)}$ measured with a fresh device, right after the UIS steady-state switching (f_{SW} = 500 kHz, $V_{DS(peak)}$ = 400 V, and $I_{DS(max)}$ = 3 A), and after 6-min relaxation time after the stressing for (b) P-gate HEMT, (c) HD-GIT, and (d) direct-drive HEMT. I_{DS}–V_{DS} characteristics of direct drive are plotted in dots as the shift is minimal. The $R_{DS,ON}$ of P-gate HEMT and HD-GIT shows long-time recoverable shifts after the continuous switching.

V. C_{OSS} Loss Models

In this section, we develop empirical models for the C_{OSS} loss of all three DUT's based on our experimental testing results. In the literature, Zulauf et al. [11], [13], [36] have modeled the E_{DISS} dependences on V_{DS} and f_R without capturing the E_{DISS} dependence on the ON-state current (as the DUT is kept OFF in those tests and I_{DS} is not constant during V_{DS} modulation). Here, we develop the C_{OSS} loss model capturing its dependences with the ON-state current ($I_{DS(max)}$), $V_{DS(peak)}$, and f_{SW}.

As illustrated in prior sections, our experimental results for all three DUT's can be commonly fitted by the E_{DISS}'s power-law relation with $V_{DS(peak)}$ and its linear relation with $I_{DS(max)}$; also, E_{DISS} is nearly independent of temperature. In addition, since the E_{DISS} is independent of f_{SW}, the E_{DISS}-induced power loss (P_{OSS}) in generic switching equals $E_{DISS} \cdot f_{SW}$. The P_{OSS} model can be expressed as follows:

$$P_{OSS} = f_{SW}\, k \left[\alpha + \beta I_{DS(max)}\right] V_{DS(peak)}^{\gamma} \tag{14}$$

where k, α, β, and γ are the device- and f_R-specific fitting parameters. Unfortunately, since E_{DISS} shows complex dependences on f_R, the above model does not contain analytical relation with f_R but has to be numerically calibrated at each f_R.

Table III summarizes the fitting parameters for three DUT's at f_R of 2 and 6.78 MHz. Note that the linear fitting for the E_{DISS}–$I_{DS(max)}$ relation and the power-law fitting for the E_{DISS}–$V_{DS(peak)}$ relation have been shown in Figs. 5(c) and (d) and 6(b) and (c), respectively. Fig. 11 shows the fitted E_{DISS} at various $V_{DS(peak)}$ and $I_{DS(max)}$ for all three DUT's at the two f_R of 6.78 MHz. A good agreement is shown between the modeled and experimental E_{DISS} results.

TABLE III
Fitting Parameters for Three DUT's

f_R	DUT	k	α	β	γ
2 MHz	P-gate	1.45×10^{-11}	0.42	0.33	1.86
	HD-GIT	0.95×10^{-15}	0.54	0.37	3.42
	Direct-drive	4.12×10^{-10}	0.03	0.30	1.20
6.78 MHz	P-Gate	1.81×10^{-11}	0.36	0.18	1.84
	HD-GIT	2.51×10^{-15}	0.29	0.22	3.32
	Direct-drive	2.58×10^{-11}	0.01	0.20	1.69

VI. Physical Origins and Simulation

The physical origin of the C_{OSS} loss in GaN HEMTs is still controversial [11], [12], [13], [37], [38], [39], while a consensus has been reached that the carrier trapping/detrapping and the resulting large-signal C_{OSS} hysteresis are the indispensable root cause. However, the characteristics of the dominant traps, including their energy level, detrapping time constant, and energy level (or activation energy E_A), remain not fully understood. In this work, our experiments have revealed new dependences of E_{DISS} that hold for various types of GaN HEMTs, including the strong impact of the ON-state current, nearly independence with temperature and f_{SW}, as well as the distinction from the traps accounting for the dynamic $R_{DS,ON}$. These newly found impact and nonimpact factors provide new insights into the physical characteristics of the governing traps for C_{OSS} loss. In this section, we first discuss the new insights that are related to the detrapping time constant and then those related to the possible trap locations.

As a recap, active traps are generally present at three major locations in a GaN HEMT structure (see Fig. 12), the device surface (i.e., the AlGaN/passivation interface), the GaN layer near the 2DEG channel, and the GaN buffer layer (usually doped with additional impurities, such as carbon) [3], [40]. In any of these locations, the traps rarely form a single E_A and cross section. Instead, they are characterized by a distribution of E_A and capture cross sections; as a result, the detrapping of the traps at each location is characterized by a spread time-constant spectrum instead of a single time constant [41].

In a UIS cycle, electron trapping/detrapping mainly occurs during the hard-switched turn-OFF as well as the OFF-state V_{DS} charging/discharging, as illustrated in Fig. 13. The hard-switched turn-OFF process is expected to inject "hot" electrons into the GaN HEMT structure and the amount of "hot" electrons is positively proportional to the $I_{DS(max)}$ [42]. In the OFF-state resonance, more electrons will be introduced by the leakage current, and the high electric field would push electrons toward the drain side at the surface, GaN channel, and buffer (see Fig. 12). At high V_{DS}, electrons are expected to possess a higher kinetic energy, which favors the trapping in various locations. This can explain the E_{DISS}'s positive dependence on $I_{DS(max)}$ and $V_{DS(peak)}$. While the trapping is usually very fast in these

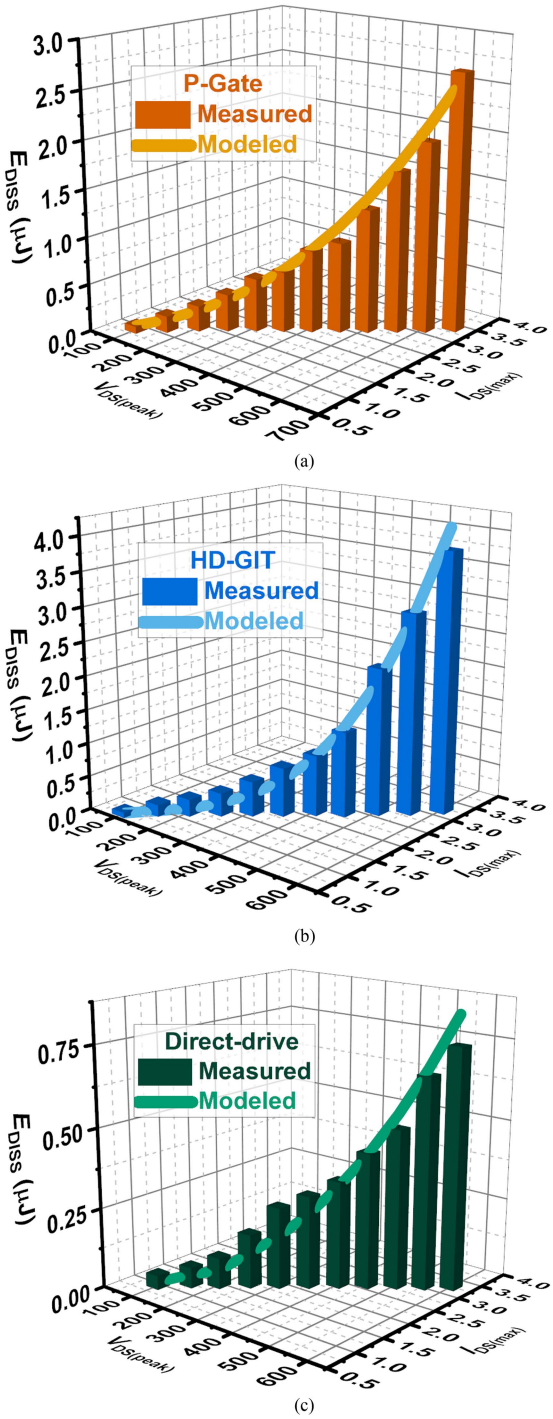

Fig. 11. Experimental data and model fitting of P_{OSS} as a function of $V_{DS(peak)}$ and $I_{DS(max)}$ for (a) P-gate HEMT, (b) HD-GIT, and (c) direct-drive HEMT at f_R of 6.78 MHz.

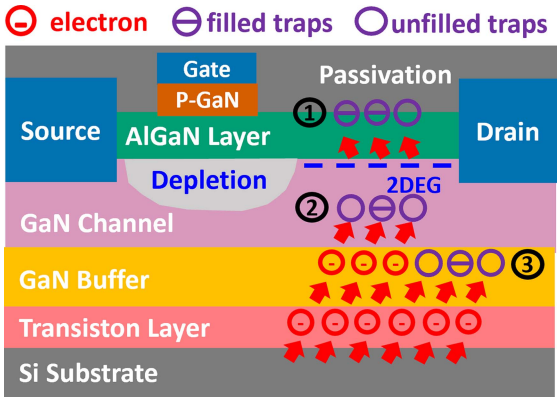

Fig. 12. Illustration of the usual trap locations in the GaN HEMT, i.e., AlGaN/passivation interface, GaN channel layer, and buffer layer.

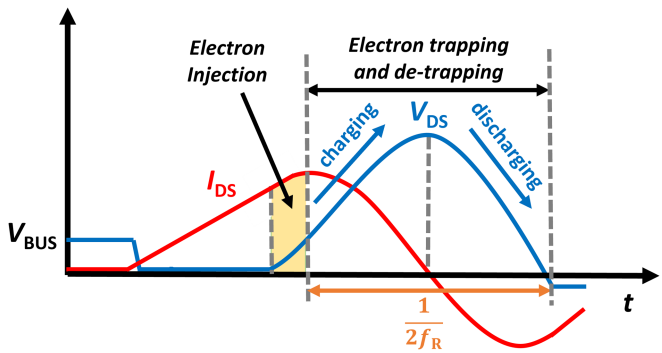

Fig. 13. Illustration of the electron trapping/detrapping in a typical UIS process.

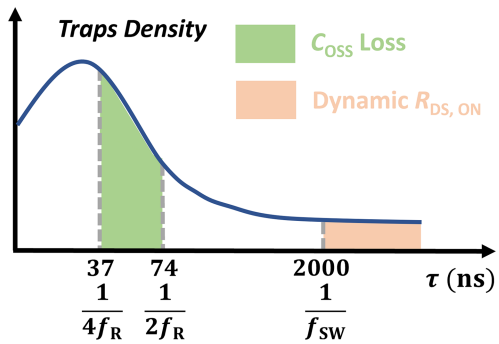

Fig. 14. Illustration of distinct detrapping time constant (τ) range for the traps accounting for the C_{OSS} loss and the dynamic $R_{DS,ON}$.

processes, the detrapping occurs simultaneously governed by the time-constant spectrum [41].

The C_{OSS} loss is known to be related to the large-signal C_{OSS}–V_{DS} hysteresis [11]. This hysteresis is because the trapped carriers alter the depletion boundary in the GaN HEMT at a certain V_{DS} [21]. Hence, in a UIS waveform, the traps relevant to the C_{OSS} loss should have a distinct trapping state during the charging and discharging process (otherwise, they would not result in the C_{OSS}–V_{DS} hysteresis). This suggests that the detrapping time constants of these relevant traps are approximately in the range between $1/4f_R$ and $1/2f_R$. In comparison, the traps that contribute to the dynamic $R_{DS,ON}$ issue should have the detrapping time constant larger than $1/f_{SW}$ (otherwise, traps will be detrapped before the next cycle and would not increase $R_{DS,ON}$). Fig. 14 shows an exemplar illustration with f_R = 6.78 MHz and f_{SW} = 500 kHz. The detrapping time constants

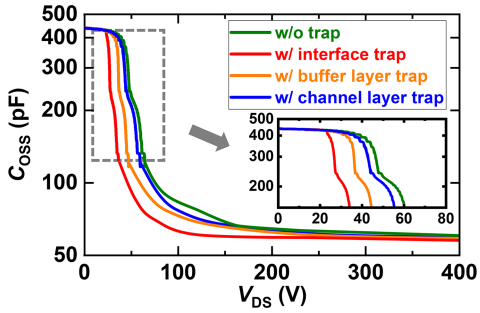

Fig. 15. Simulated C_{OSS}–V_{DS} characteristic with different trap locations.

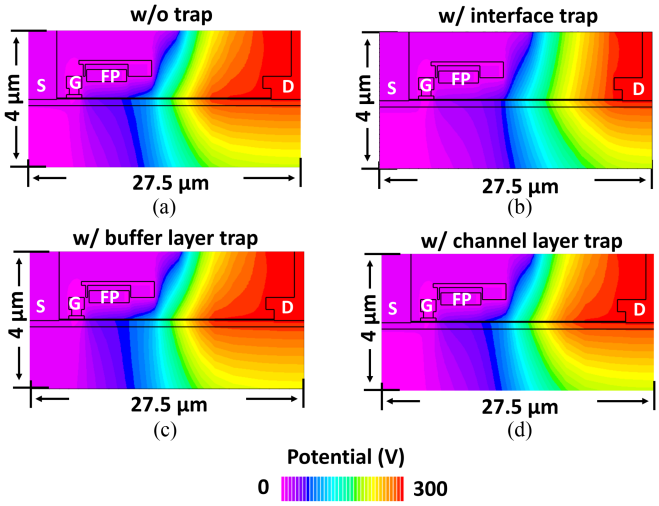

Fig. 16. TCAD simulation of the electronstatic potential contour in GaN HEMTs at an exemplar $V_{DS(peak)}$ of 300 V with (a) no trap, (b) GaN interface trap, (c) buffer layer trap, and (d) channel trap. FP stands for field plate.

for the traps accounting for the C_{OSS} loss and dynamic $R_{DS,ON}$ are estimated to be 37–74 ns and >2000 ns, respectively.

Since $f_{SW} < f_R$, the traps accounting for the C_{OSS} loss and the dynamic $R_{DS,ON}$ have no overlap in the detrapping time constant spectrum. This explains the experimental observations that the E_{DISS} is unchanged for GaN HEMTs with an $R_{DS,ON}$ increase. On the other hand, for different f_R, the traps accounting for the C_{OSS} loss are different in terms of the detrapping time constant range. Hence, the E_{DISS} at different f_R highly depends on the trap densities in the specific time constant range, which explains the nonmonotonic E_{DISS} dependence on f_R.

Up to now, we have discussed the time constant of the relevant traps, which is trap location agnostic. Here, we show that the traps in all three major locations can result in the C_{OSS}–V_{DS} hysteresis, which implies that, with an appropriate detrapping time constant, all these traps can contribute to the device C_{OSS} loss. For this study, we utilize a physics-based TCAD simulation model that has been well-calibrated with a commercial P-gate GaN HEMT [24], [26], [28], [43]. Four device simulations are performed without traps in the device and with the traps in the GaN channel region, GaN buffer region (both with a density of 1.6×10^{16} cm^{-3} [21]), and at the AlGaN/passivation interface (with a sheet density of 2×10^{12} cm^{-2} [42]). Fig. 15 shows the simulated C_{OSS}–V_{DS} characteristics for these four conditions, revealing that the traps in all three locations can induce C_{OSS} shifts. Fig. 16 shows the simulated electrostatic potential contour in the four device structures with an exemplar V_{DS} of 300 V, revealing distinct depletion boundaries in four structures. This illustrates that the traps in all three locations could alter the depletion boundaries (and result in large-signal C_{OSS}–V_{DS} hysteresis).

Finally, we would like to note that the surface traps at the AlGaN/passivation interface have been reported as the key source for the dynamic $R_{DS,ON}$, and the associated detrapping behaviors show weak temperature dependence [42], strong dependence on the ON-state current [44], and large spread in E_A [41]. These dependencies are consistent with those related to the C_{OSS} loss observed in this work. This seems to suggest that the surface traps could be an important origin for the C_{OSS} loss. However, more convincing evidence is still needed in future work. The baseline learning from our simulations is the traps with the appropriate detrapping time constant at various locations that can, in theory, all contribute to the C_{OSS} loss.

VII. Conclusion

This work comprehensively characterizes the E_{DISS} of three mainstream commercial GaN HEMTs using a new, easy-to-implement, accurate approach based on the UIS test. For the first time, we reveal the E_{DISS}'s strong relation with the ON-state conduction current, independence with temperature, and the minimal difference in a single pulse and the steady-state switching (up to 500 kHz). The traps accounting for the C_{OSS} loss in GaN HEMTs are believed to possess different detrapping time constants as compared with those governing the dynamic $R_{DS,ON}$. In addition, a unified model is developed to describe the E_{DISS}'s dependence on $I_{DS(max)}$ and $V_{DS(peak)}$ for all three DUT's at two relevant f_R. These results provide a good reference for device users to characterize and model the GaN HEMT loss in high-frequency applications and unveil new insights into the physical origin of the C_{OSS} loss of GaN HEMTs.

Acknowledgment

The authors would like to thank the collaboration with Silvaco Inc. for device simulations.

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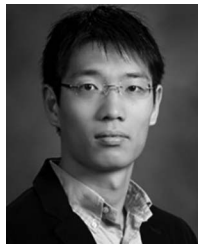

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