Nonisolated Ultra-High Step-Up Quadratic Converter With ZVS Operation and Low Switch Voltage Stress

Maryam Hajilou and Hosein Farzanehfard, *Member, IEEE*

***Abstract*—This article proposes a nonisolated quadratic converter with ultra-high voltage conversion ratio. In the presented structure, an auxiliary circuit containing coupled inductors (CIs) and a voltage multiplier cell is integrated with the quadratic converter to obtain higher voltage gain. As a result, voltage stress over switches is reduced significantly and MOSFETs with low ON-resistance can be used to lower the conduction losses. In addition, soft switching performance is achieved by the auxiliary circuit and all switches are turned ON and turned OFF under zero voltage conditions to eliminate the switching and capacitive turn-ON losses. Furthermore, the soft switching is load independent and is performed over the entire load variation. Moreover, due to leakage inductances of the CIs, the reverse recovery problem of the output diodes is alleviated. Due to the abovementioned advantages, the converter efficiency is enhanced notably. Also, the converter benefits from continuous input current and common ground between the input and output, which removes any limitation on the converter applications. In this article, the converter operation is investigated comprehensively and in order to validate the theoretical analysis, the experimental results of a 150 W prototype are provided.**

***Index Terms*—Low switch voltage stress, quadratic converter, soft switching, ultra high step-up, zero voltage switching (ZVS) operation.**

I. Introduction

NOWADAYS, high step-up converters are ever more employed in various applications including, dc motors, three-phase motor drive systems, dc microgrids, hybrid electric vehicles (HEVs), uninterruptible power supplies (UPSs), piezoelectric element drives, and high-intensity discharge (HID) ballasts [1]. Among the high voltage gain converters, where isolation is not necessary, the nonisolated structure is preferred over isolated topologies due to lower volume, simpler configuration, and higher efficiency [2], [3].

The conventional boost converter has a simple and low-cost step-up structure but for higher voltage gains the duty cycle is over extended, which leads to low efficiency, also the voltage stress of the switch and diode is equal to the output voltage. Numerous technics are employed in converters to achieve high voltage gain, such as switched capacitors (SCs), switched inductors, coupled inductors (CIs), voltage multiplier cells (VMCs), and a combination of these procedures [4], [5], [6], [7], [8], [9]. However, the mentioned methods produce some challenges like high number of elements, volume, cost, and complexity of the converter [10]. Also, the leakage inductance of the CIs produces voltage spike on the switch. The high step-up converters presented in [11] and [12] suffer from the lack of common ground between the input source and the output load that limits the converter applications. The converter presented in [11] uses VMC to boost the voltage gain, while a passive clamp circuit absorbs the leakage inductance energy and recycles to the load. The high step-up converter introduced in [12] reduces the switch voltage stress to half the output voltage, but the duty cycle is confined to 0.35.

Quadratic boost converters have attractive properties including high voltage gain at the lower duty cycles with fewer components and common ground between input and output, although the imposed switch voltage is still high. In [13], an ultrahigh step-up quadratic structure is introduced that uses CIs with a voltage doubler cell to improve the conversion ratio and reduce the switch voltage stress. But this converter utilizes separate switches for each boost stage that increases the circuit cost. In [14], to obtain ultrahigh voltage gain, the quadratic structure is combined with SC cells. But in this converter, the common ground between the input and output is lost and has a high input current ripple. The converters in [11], [12], [13], [14] despite having two power switches in their structures operate at hard switching conditions which at high output powers diminishes efficiency.

Enhancing switching frequency decreases the power converters volume and cost, but leads to more switching losses. Hence various technics are employed to create soft switching performance [15], [16], [17]. With a combination of two boost converter stages, CI, and VMC, an ultrahigh step-up structure with low switch voltage stress is introduced in [18]. In this converter, the switches are turned ON under zero current switching (ZCS) due to the leakage inductance and the leakage inductance energy is absorbed by a passive clamp circuit. High input current ripple, capacitive turn-ON losses and switching losses at turn-OFF are the main drawbacks of this converter. High step-up converters in [19] and [20] use CIs in such a way to increase the voltage gain and provide ZCS condition at turn-ON for the switch. In these converters, a passive clamp circuit limits the switch current spike but suffers from turn-OFF switching loss and capacitive turn-ON loss. In [21], [22], [23], an

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The authors are with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan 84156-83111, Iran (e-mail: hajilou.m@ec.iut.ac.ir; hosein@iut.ac.ir).

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active clamp circuit recycles the leakage inductance energy and provides zero voltage switching (ZVS) operation for the main and auxiliary MOSFETs. The converter in [21] attains high voltage gain by applying CI and a built-in transformer (BIT), but has high input current ripple. In [22] and [24], the voltage gain and the semiconductors voltage stress can be controlled by the CIs turns ratio and the extendable number of diode–capacitor voltage multiplier stages. However, this structure has resulted in a large number of passive and active elements, high cost, and circuit volume. In [25], an auxiliary winding with a diode is employed to provide ZVS condition for two of the power switches while an active clamp circuit is utilized to realize soft switching for other switches. Although, the switching losses are eliminated in the converters of [24] and [25], but excessive number of switches is utilized, which increases the converter cost and control circuit complexity. Moreover, both converters have high input current ripple.

This article introduces a new soft-switched ultra-high step-up converter based on the quadratic structure. In order to significantly increase the voltage gain, an auxiliary circuit containing CIs and a VMC is used. Moreover, ZVS soft switching condition is obtained by the auxiliary circuit for all switches which is independent of the load variation. The proposed structure has considerable advantages such as very high voltage gain, extremely low switches voltage stress, soft switching performance, no capacitive turn-ON loss, no reverse recovery problem of output diodes, common ground between the input and output, continuous input current, low input current ripple, absorbing the leakage inductance energy and recycling to the load, simple structure, low cost, and high efficiency. The mentioned advantages make the converters suitable for various applications and superior to other counterpart converters.

The proposed converter operating principles are discussed in Section II. Comprehensive steady-state analysis and components design along with the soft switching conditions are provided in Section III. Experimental results are presented in Section IV and comparison with other counterpart topologies and efficiency evaluation are depicted in Section V. Finally, Section VI concludes this article.

II. Presented Converter Operating Principles

The proposed ultra-high step-up quadratic converter and its equivalent circuit are shown in Fig. 1. In the proposed converter, the input inductor L_{in}, the input side diodes D_1 and D_2, the main switch M_1, the output diode D_O, the magnetizing inductance L_{m1} and the output capacitor C_O form the basic quadratic converter. The auxiliary switch M_a, the capacitor C_4, and the magnetizing inductance L_{m2} form the soft switching cell. Also, the capacitor C_3 and the auxiliary switch constitute the active clamp circuit, which prevents the main switch current spike by absorbing the leakage inductance energy at turn-OFF. The middle inductor of the quadratic structure and the inductor used in the soft switching cell are coupled and in conjunction with the diode D_3 and the capacitor C_2 increase the voltage gain. N_{P1} and N_{P2} are the number of primary side windings of the first and second CIs, and their secondary side number of windings are

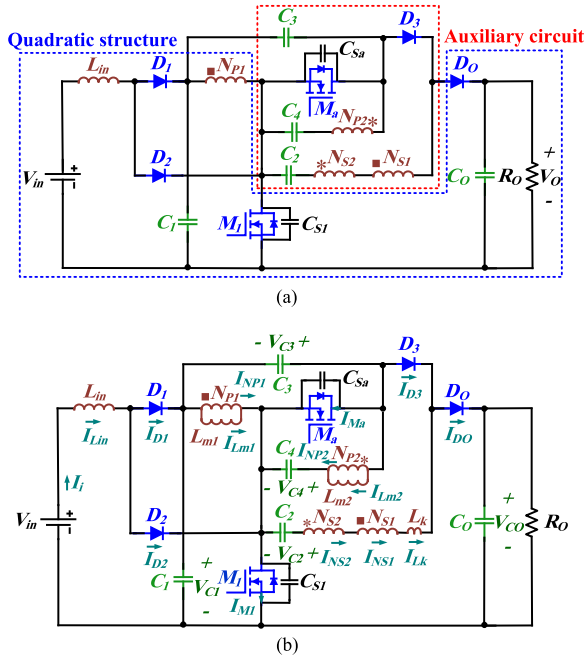

Fig. 1. (a) Proposed converter and (b) its equivalent circuit.

N_{S1} and N_{S2}, respectively. The turns ratios of the CIs are defined as $n = \frac{N_{S1}}{N_{P1}}$ and $m = \frac{N_{S2}}{N_{P2}}$, and L_k is the sum of the leakage inductances of the CIs, which is modeled on the secondary side of CIs. C_{S1} and C_{Sa} are the switches snubber capacitors, which provide soft switching at turn-OFF. To simplify the converter analysis, all semiconductor devices are presumed ideal and all capacitors except the snubber capacitors are large enough so that their voltages are constant. Different operational states and key waveforms of the proposed converter are illustrated in Figs. 2 and 3, respectively. The converter steady-state operation is described in six states in one switching cycle as follows:

State 1 (t_0–t_1): At t_0, the main switch M_1 begins conducting and since its body diode is conducting, the switch is turned ON at zero voltage and zero current switching (ZVZCS) and capacitive turn-ON loss is eliminated. Switch M_a is OFF and diodes D_1 and D_O are reverse biased. In this state, L_{in} is charged by V_{in} through D_2, and its current increases linearly. Also, D_3 is conducting, and the leakage inductance current is increasing in the negative direction while the currents of magnetizing inductances (L_{m1} and L_{m2}) are rising

$$I_{L_k}(t) = \frac{-2I_O f_{\text{sw}}}{D^2}(t - t_0) \tag{1}$$

where D is the main switch duty cycle, f_{sw} is the switching frequency, and I_O is the average output current.

State 2 (t_1–t_2): At t_1, the switch M_1 is turned OFF at ZVS and C_{S1} starts charging from zero to $V_{C1} + V_{C3}$ and simultaneously C_{Sa} is discharging until its voltage becomes zero and the current flows through M_a body diode. In this state, D_2 is reverse biased and the input current flows via D_1. The leakage inductance current reduces to zero at t_2 and D_3 turns OFF at ZCS without

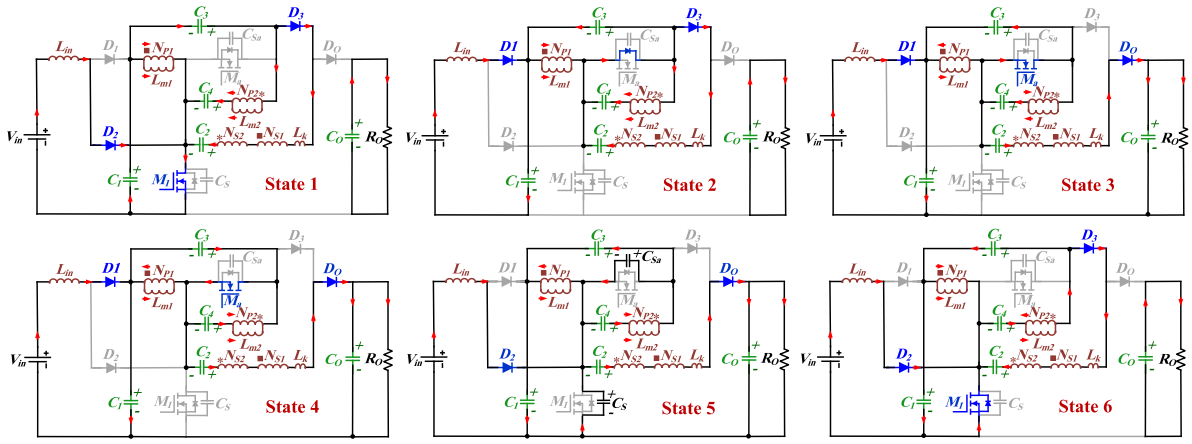

Fig. 2. Equivalent circuit of each operating state.

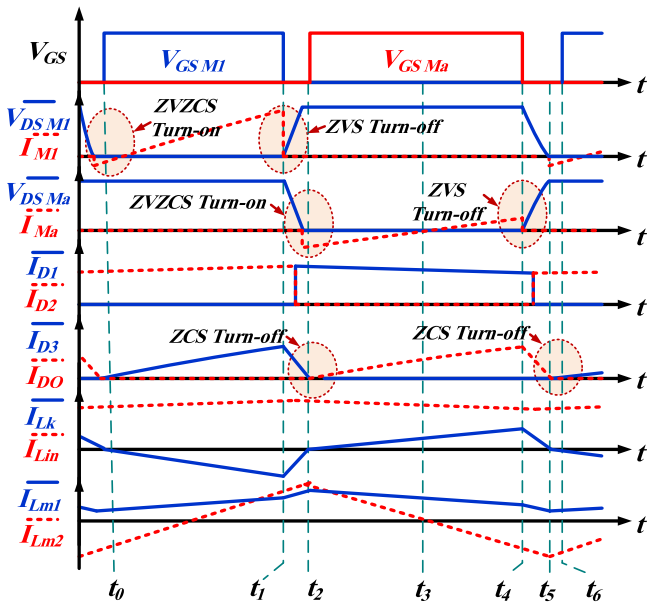

Fig. 3. Theoretical key waveforms of the proposed topology.

the reverse recovery problem

$$I_{Lk}(t) = I_{Lk}(t_1) + \frac{1}{L_k}[(V_{C2} - (1+n+m)V_{C1} - V_{C3})(t-t_1) + \frac{(1+n+m)}{2C_{S1}}((2-D)I_i + \frac{\Delta I_{Lm2}}{2})(t-t_1)^2] \tag{2}$$

where ΔI_{Lm2} is L_{m2} current ripple.

State 3 (t_2–t_3): Due to the M_a body diode conduction in the previous state, this switch can be turned ON under ZVZCS and the capacitive turn-ON loss is removed. D_1 and D_O are forward biased while D_2 and D_3 are reverse-biased. The energy stored in L_{in} is transferred to C_1 through D_1 while C_4 is charged by L_{M2}. C_1 and C_2 are connected in series with N_{P1} and through the secondary winding deliver energy to the load

$$I_{Lk}(t) = \frac{2I_O f_{\text{sw}}}{(1-D)^2}(t-t_2) \tag{3}$$

State 4 (t_3–t_4): At t_3, the L_{m2} current changes direction and thus, the M_a switch current becomes positive. The other circuit conditions and the leakage inductance current variation are like the previous state.

State 5 (t_4–t_5): This state starts by turning OFF M_a at ZVS. The snubber capacitor C_{Sa} begins charging until its voltage clamps to $V_{C1} + V_{C3}$ and at the same time C_{S1} is fully discharged. Then, D_1 turns OFF and D_2 begins to conduct while the leakage inductance current is falling until reaches zero at t_5 and D_O turns OFF at ZCS, which eliminates the reverse recovery problem.

$$I_{Lk}(t) = I_{Lk}(t_4) - \frac{1}{L_k}[((-V_{C2} + (n+m)V_{C1} + V_O)(t-t_4) + \frac{(n+m+1)}{2C_{S1}}(\frac{(n+m)I_O}{(1-D)} + \frac{\Delta I_{Lm2}}{2})(t-t_4)^2]. \tag{4}$$

State 6 (t_5–t_6): At t_5, the C_{S1} voltage reaches zero, and the M_1 body diode turns ON, so M_1 can be turned on at ZVZCS. Also, D_3 begins to conduct, and the input inductor and the magnetizing inductances (L_{m1} and L_{m2}) are being charged. Moreover, I_{Lk} is increasing like the first state.

III. Steady-State Analysis

A. Voltage Gain

Due to short duration of states 2, 5, and 6, only states 1, 3, and 4 are considered in steady-state analysis. At the end of this section, the leakage inductance effect on the voltage gain is investigated, which shows a very small effect on the voltage gain and thus, the leakage inductance is neglected here.

By applying the volt–second balance principle on the input inductor, and the magnetizing inductances, the capacitors C_1, C_3, and C_4 voltages are achieved as

$$V_{C1} = \frac{V_{\text{in}}}{1-D}, V_{C3} = V_{C4} = \frac{D}{(1-D)^2}V_{\text{in}}. \tag{5}$$

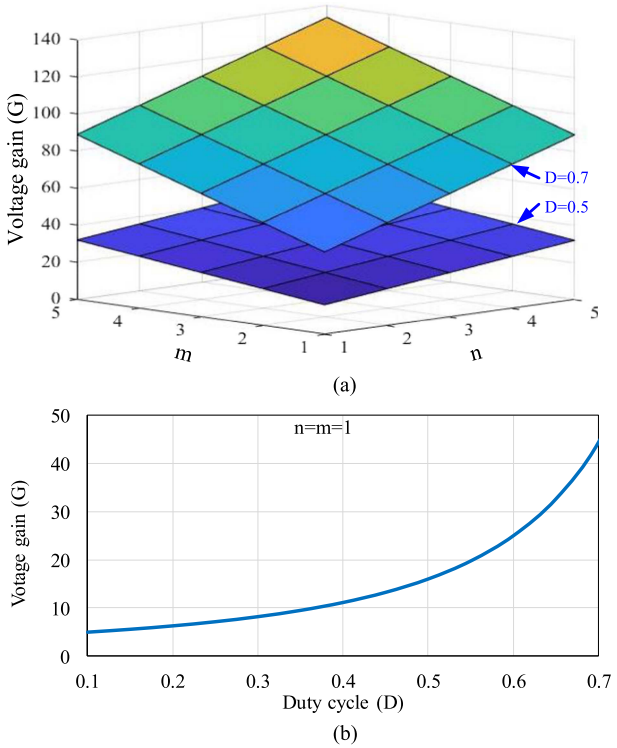

Fig. 4. Voltage gain versus (a) turns ratios and (b) duty cycle.

By applying Kirchhoff Voltage Law (KVL) in state 1, the voltage relationship of capacitor C_2 is achieved as

$$V_{C2} = \frac{1+n+m-D(n+m)}{(1-D)^2} V_{\text{in}}. \tag{6}$$

In the main switch OFF-state, the power is being transferred to the load, and the output voltage is the summation of V_{C1}, V_{C2}, V_{C3}, and the voltage of secondary side CIs thus, the ideal converter voltage gain is expressed as

$$G = \frac{V_O}{V_{\text{in}}} = \frac{2+n+m}{(1-D)^2}. \tag{7}$$

The voltage gain versus n and m for various D is illustrated in Fig. 4(a) and the voltage gain versus duty cycle for $m = n = 1$ is shown in Fig. 4(b). As observed, the presented converter has ultra-high voltage gain without high turns ratio or extreme duty cycle.

B. Semiconductors Voltage and Current Stress

In state 3 and state 1, the voltage stress of the main and auxiliary switches is clamped to $V_{C1} + V_{C3}$ as

$$V_{M1} = V_{Ma} = \frac{V_O}{2+n+m}. \tag{8}$$

According to (7) and (8), increasing the turns ratios, enhances the voltage gain and greatly improves the switches voltage stress. Low switch voltage stress leads to utilization of low cost MOSFETs with low ON-resistance, which diminishes the conduction loss. The voltage stress of D_1 is clamped to V_{C1} in state 1 while V_{C3} is applied on D_2 in state 3. Also, according to the proposed converter equivalent circuit in state 3 and state 1, the voltage stress of D_3 and D_O are $V_O - (V_{C1} + V_{C3})$. Thus, using (5)–(8) the diodes voltage stresses are as follows:

$$V_{D1} = \frac{1-D}{2+n+m} V_O, V_{D2} = \frac{D}{2+n+m} V_O \tag{9}$$

$$V_{D3} = V_{DO} = \frac{1+n+m}{2+n+m} V_O. \tag{10}$$

The input current flows through D_2 when M_1 is ON and then flows via D_1 when M_1 is OFF. Thus, the average currents of D_2 and D_1 are equal to DI_i and $(1-D)I_i$, respectively. Also, the current stress of both diodes is equal to $I_i + \frac{\Delta I_{\text{Lin}}}{2}$. Assuming ideal components, the input average current is GI_O and the diodes current stress is as follows:

$$I_{D1} = I_{D2} = \left(G + \frac{DR_O}{2f_{\text{sw}} L_{\text{in}} G} \right) I_O. \tag{11}$$

Considering the capacitors ampere–second balance, the capacitors average current is zero. Thus, the average current of D_3 and D_O is equal to I_O. So, according to these diodes current waveforms in Fig. 3, their peak currents are given by the following:

$$I_{D3} = \frac{2}{D} I_O \tag{12}$$

$$I_{\text{DO}} = \frac{2}{1-D} I_O. \tag{13}$$

Based on the general inductor relation $\Delta I = V_L \Delta t / L$, I_{Lk} at t_1 and t_4 are obtained as (14) and (15), respectively.

$$\frac{D((n+m+1)V_{C1} - V_{C2} + (m+1)V_{C3} - mV_{C4})}{f_{\text{sw}} L_k} \tag{14}$$

$$\frac{(1-D)(V_{C1} + V_{C2} + (n+1)V_{C3} + mV_{C4} - V_O)}{f_{\text{sw}} L_k}. \tag{15}$$

By equating (16) with (14), (17) with (15) and summing them, simplifying, and replacing capacitors voltages from (5) to (7), the voltage gain relationship by considering L_k is derived as

$$G = \frac{V_O}{V_{\text{in}}} = \frac{2+n+m}{(1-D)^2} \left(\frac{1}{1 + \frac{2L_k f_{\text{sw}}}{R_O} \left(\frac{1}{D^2} + \frac{1}{(1-D)^2} \right)} \right). \tag{16}$$

According to (16), the proposed converter conversion ratio for different leakage inductances is illustrated in Fig. 5. As observed, L_k has a very small effect on the voltage gain and thus, the ideal voltage gain of (7) is accurate. By writing the Kirchhoff Current Law (KCL) in the proposed converter, the average current of L_{m1} is obtained as $(1-D)I_i$ and the average current of L_{m2} is zero. By applying KCL at t_1 and t_4, considering the current variation of the magnetizing inductances, and using (12) and (13), the main and auxiliary switch maximum currents are obtained by the following:

$$I_{M1} = \left((2-D)G + \frac{2(1+n+m)}{D} \right) I_O + \frac{(1-D)V_{C3}}{2f_{\text{sw}}} \left(\frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right) \tag{17}$$

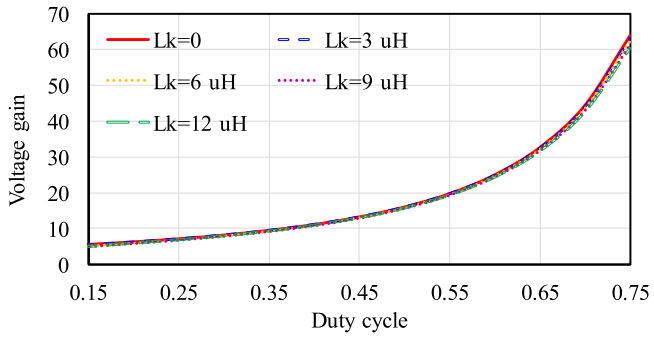

Fig. 5. Leakage inductance effect on voltage gain.

$$I_{\text{Ma}} = \frac{m+n}{1-D} I_O + \frac{(1-D)V_{C3}}{2f_{\text{sw}}} \left(\frac{1}{L_{m1}} + \frac{1}{L_{m2}} \right). \quad (18)$$

IV. Design Considerations and Soft-Switching Conditions

A. Elements Design

The input inductor is charged by the input voltage in state 1 and for CCM operation at light load (10% full load), it is designed as follows:

$$L_{\text{in}} \geq \frac{DV_{\text{in}}}{0.2GI_O f_{\text{sw}}}. \quad (19)$$

For applications where the current ripple is not very important, higher current ripple for L_{in} can be considered, which leads to smaller L_{in}. The capacitor C_1 charges L_{m1} during the main switch ON-state and to avoid power reprocessing, it is preferred to keep I_{Lm1} positive for improved converter efficiency. Therefore, L_{m1} current ripple can be considered 20% of L_{m1} average current to prevent the current from returning to C_1 at light loads, but this increases the converter volume and the conduction losses. Therefore, since there is a tradeoff for L_{m1} design, the ripple is considered twice the L_{m1} average current at half load. Based on the L_{m1} average current given in the previous section, L_{m1} is derived as

$$L_{m1} \geq \frac{DV_{C1}}{(1-D)GI_O f_{\text{sw}}}. \quad (20)$$

In the main switch OFF-state, C_1 is charged and C_2 is discharged by $I_i - I_{\text{DO}}$ and I_{DO}, respectively. By considering (13) and I_{DO} waveform in Fig. 3, these capacitors equations can be expressed as follows:

$$C_1 \geq \frac{(1+m+n+D)I_O}{(1-D)f_{\text{sw}}\Delta V_{C1}}, C_2 \geq \frac{I_O}{f_{\text{sw}}\Delta V_{C2}}. \quad (21)$$

The capacitor C_3 is discharged in the second half duration of state 1 by $(m+1)I_{D3} + I_{\text{LM2}}$. Also, C_4 is charged at the same time by $I_{\text{Lm2}} + mI_{D3}$ and in state 3 by $I_{\text{Lm2}} - mI_{\text{DO}}$. Thus, capacitors are obtained as follows:

$$C_3 \geq \frac{1}{4\Delta V_{C3} f_{\text{sw}}} \left(3(m+1)I_O + \frac{\Delta I_{\text{Lm2}} D}{2} \right) \quad (22)$$

$$C_4 \geq \frac{1}{2\Delta V_{C4} f_{\text{sw}}} \left(mI_O + \frac{\Delta I_{\text{Lm2}}}{4} \right) \quad (23)$$

$$C_O \geq \frac{DI_O}{f_{\text{sw}}\Delta V_O}, \Delta I_{\text{Lm2}} = \frac{(1-D)V_{C4}}{L_{m2} f_{\text{sw}}}. \quad (24)$$

where ΔV_{C1-4} are C_{1-4} voltage ripples, and the C_O voltage ripple is equal to the output voltage ripple.

B. Soft Switching Conditions

When the main switch is turned OFF, C_{S1} begins to charge and limits the switch voltage slop to provide ZVS condition at turn-OFF. Simultaneously, the auxiliary switch snubber capacitor is discharged, and M_a body diode starts conducting. Therefore, M_a can be turned ON under ZVZCS condition. At the same time, the leakage inductance current decreases in the negative direction until reaches zero. As a result, D_3 is reverse biased at ZCS. Before switch M_1 is turned ON, M_a is turned OFF under ZVS due the snubber capacitor C_{Sa} across it. The voltage summation of both snubber capacitors ($V_{\text{CS1}} + V_{\text{CSa}}$) is clamped to $V_{C1} + V_{C3}$ hence when C_{Sa} is fully charged, C_{S1} is completely discharged, and the main switch body diode conducts. Then, M_1 can be turned ON under ZVZCS without capacitive turn-ON loss. Also, D_O turns OFF at ZCS since the leakage inductance current smoothly declines to zero. In order to realize the ZVZCS operation for M_1 at turn-ON, $I_{\text{CSa}} - I_{\text{CS1}}$ at t_4 must be higher than zero and also to turn-ON the main switch body diode at t_5, I_{M1} at the end of state 5 must be lower than zero. Moreover, the inductive energy available must be enough to completely discharge and charge the snubber capacitors. So, soft switching conditions are as follows:

$$(n+m+1)I_{\text{DO}}(t_4) - I_{\text{Lm2}}(t_4) - I_{\text{Lm1}}(t_4) \geq 0 \quad (25)$$

$$I_{D2}(t_5) + I_{\text{Lm1}}(t_5) + I_{\text{Lm2}}(t_5) \leq 0 \quad (26)$$

$$\frac{1}{2} L_{m2} I_{Lm2}(t_4)^2 \geq \frac{1}{2}(C_{S1} + C_{\text{Sa}})(V_{C1} + V_{C3})^2. \quad (27)$$

In the above equations, $I_{\text{DO}}(t_4)$ is obtained from (13) and $I_{D2}(t_5)$ is almost equal to I_i. $I_{Lm2}(t_5)$ is $\frac{\Delta I_{Lm2}}{2}$ and since the duration of state 5 is very small, $I_{Lm2}(t_4)$ is the same as $I_{Lm2}(t_5)$. Also, I_{Lm1} at both times is approximately $\frac{(1-D)I_i}{2}$. Thus, (25) and (26) are written as (28) and (29), respectively.

$$\frac{2+3(m+n)}{1-D} I_O + \Delta I_{Lm2} \geq 0 \quad (28)$$

$$(3-D)GI_O - \Delta I_{Lm2} \leq 0. \quad (29)$$

As observed, the first condition is always established. According to (24), $\frac{\Delta I_{Lm2}}{2}$ is independent of load variation, thus the worst condition for (29) is at full load and L_{m2} should be designed at I_O maximum. Therefore, from the second condition, L_{m2} is derived as follows:

$$L_{m2} \leq \frac{(1-D)V_{C4}}{(3-D)GI_O f_{\text{sw}}}. \quad (30)$$

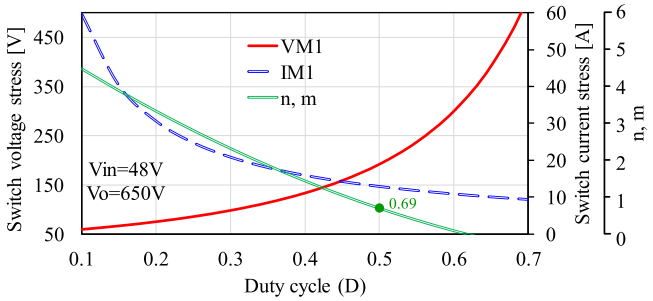

Fig. 6. Main switch voltage and current stress and turns ratios versus duty cycle for a constant voltage gain.

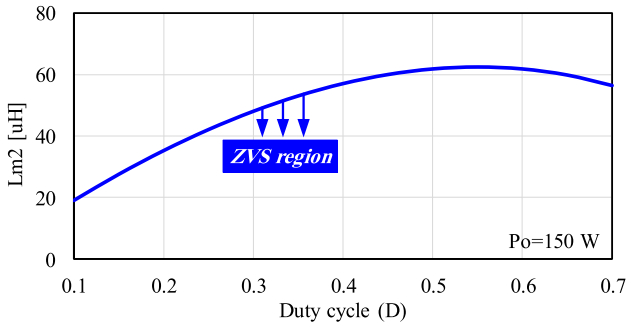

Fig. 7. Soft switching region versus duty cycle.

By substituting (5) in (27) which is the third condition for soft switching, the following is obtained:

$$L_{m2} \le \frac{D^2(1-D)^2}{4(C_{S1}+C_{\rm Sa})f_{\rm sw}{}^2}. \tag{31}$$

The relation (27) is obtained by assuming that L_{m2} energy has the significant contribution to charge and discharge the snubber capacitors and the energy of L_{m1} and the CIs approximately cancel each other.

C. Design Procedure

The converter numerical design for $V_{\rm in} = 48\,V$ and $V_O = 650\,{\rm V}$ at 150 W is performed. Based on the voltage gain, the switches voltage stress equation in (8) can be written as follows:

$$V_{M1} = V_{\rm Ma} = \frac{V_O}{G(1-D)^2}. \tag{32}$$

Using (7), (17), and (32), the main switch voltage and current stress along with the turns ratios versus duty cycle are shown in Fig. 6. As seen, for a certain voltage gain, the switch voltage and current stresses are appropriate at low duty cycles and high duty cycles, respectively. Thus, to operate the converter at a suitable duty cycle and use low voltage MOSFETs to reduce the conduction loss and cost, duty cycles between 0.3 and 0.5 is appropriate. At $D = 0.5$, the switch voltage stress is equal to 200 V and 250 V MOSFET can be selected while higher D improves the efficiency. At $D = 0.5$, n and m are equal to 0.69 and the input inductor and L_{m1} are designed from (19) and (20). Also, the capacitors are designed from (21) to (24) for less than 2% voltage ripple. Moreover, the snubber capacitors are selected like any snubber capacitor [26]. Then, to provide ZVZCS at turn-ON for M_1, L_{m2} is designed from (30) and (31), which ZVS region versus D is indicated in Fig. 7. The components values according to this design procedure are provided in Table I.

TABLE I
PROPOSED CONVERTER PROTOTYPE SPECIFICATIONS

Symbol	Parameter	Specification
$V_{\rm in}$,V_O	Input and output voltages	48 V, 650 V
P	Output power	150 W
$f_{\rm sw}$	Switching frequency	100 kHz
M_1, M_a	main and auxiliary switches	IRF250P224
D_1, D_2	Quadratic diodes	VS-20CTQ150-M3
D_3, D_O	Diodes	DSEP15-06B
C_1, C_3	input and clamp capacitors	10 μF
C_2, C_4	capacitors	4.7 μF, 10 μF
C_O	Output capacitor	10 μF
C_{S1}, C_{Sa}	Snubber capacitors	4.7 nF
L_{in}	Input inductor	400 μH
L_{m1}, L_{m2}	Magnetizing inductances	350 μH, 35 μH
N_{S1}:N_{P1}	Number of turns	24:34
N_{S2}:N_{P2}	Number of turns	14:20
Core$L_{\rm in}$	Magnetic core of L_{in}	EI 35/21/9
Core1	Magnetic core of L_{m1}	EI 35/21/9
Core2	Magnetic core of L_{m2}	EI 25/13/11
$R_{\rm Lin}$	Windings Resistance	64 $m\Omega$
R_{NP1}, R_{NS1}	Windings Resistances	63, 89 $m\Omega$
R_{NP2}, R_{NS2}	Windings Resistances	14, 43 $m\Omega$
k_{Lin}	Litz wires number for $L_{\rm in}$	7
k_{NP1}, k_{NS1}	Number of litz wires N_{P1}, N_{S1}	4, 2
k_{NP2}, k_{NS2}	Number of litz wires N_{P2}, N_{S2}	9, 2

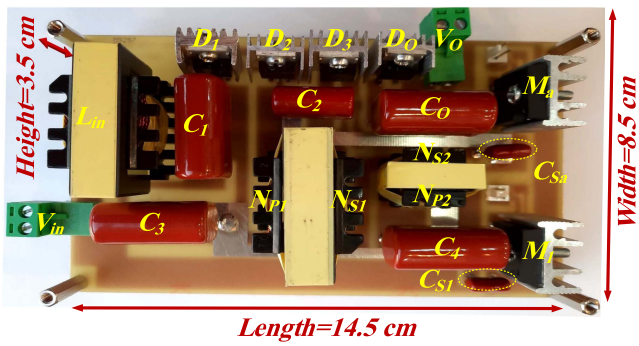

Fig. 8. Implemented prototype converter.

V. EXPERIMENTAL RESULTS AND EFFICIENCY

To evaluate the theoretical analysis, a 150 W converter laboratory prototype is implemented as shown in Fig. 8. The prototype specifications are illustrated in Table I and the experimental results are illustrated in Fig. 9. It is notable that the proposed converter due to has ultra-high voltage gain, is a good selection for dc motors. The switches M_1 and M_a voltage and current waveforms at full load are presented in Fig. 9(a) and 9(b), respectively. As observed, the switches are turned ON at ZVZCS condition and turned OFF under ZVS condition. Therefore, the switching and capacitive turn-ON losses are eliminated, while the switches voltage stress is reduced significantly. The main and auxiliary switches waveforms at light load (15 W) are depicted in Fig. 9(c) and 9(d) indicating ZVZCS turn-ON condition is

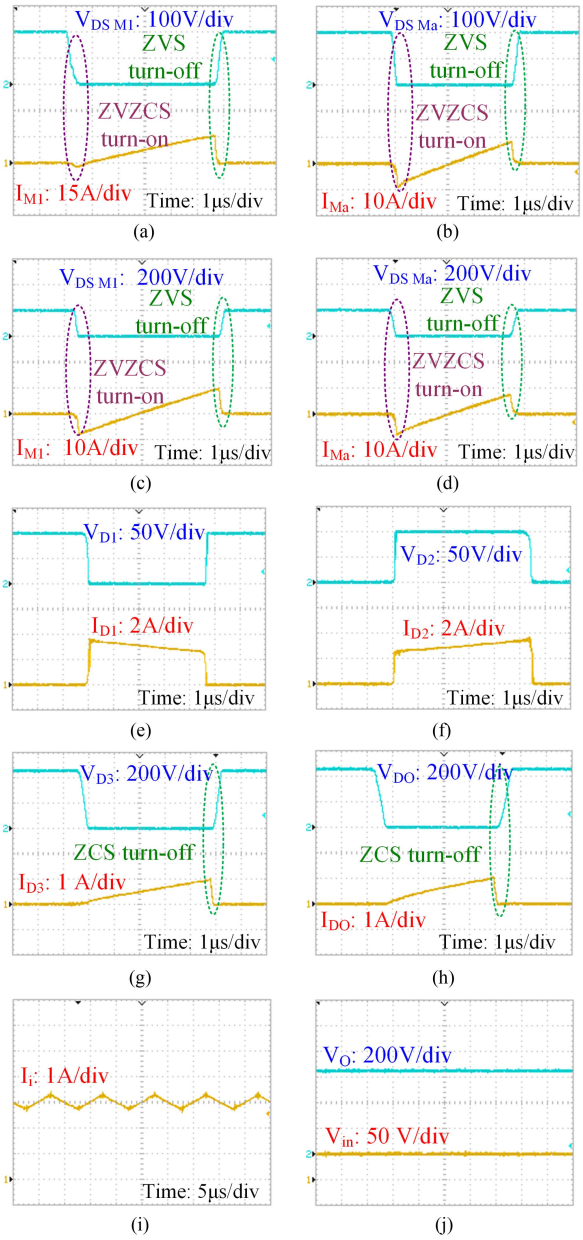

Fig. 9. Experimental waveforms of (a) M_1 at full load, (b) M_a at full load, (c) M_1 at light load, (d) M_a at light load, (e) D_1, (f) D_2, (g) D_3, (h) D_O (i) Input current, and (j) Input and output voltages.

established for both switches. Fig 9(e)–9(h) shows the voltage and current waveforms of all diodes. According to Fig. 9(g) and 9(h), diodes D_3 and D_O turn-OFF at ZCS condition eliminating these diodes reverse recovery losses. The low ripple continuous input current waveform is depicted in Fig. 9(i) while the input and output voltages are provided in Fig. 9(j). Also, the converter dynamic load performance is achieved by changing the load from full load to half load and vice versa as shown in Fig. 10.

The converter control circuit schematic and waveforms are shown in Fig. 11. A basic PI voltage controller, which is realized by IC TL494 produces the gate-source signal of M_1. Also, the gate-source signal of M_a is generated by IC CD4098, IC 7404,

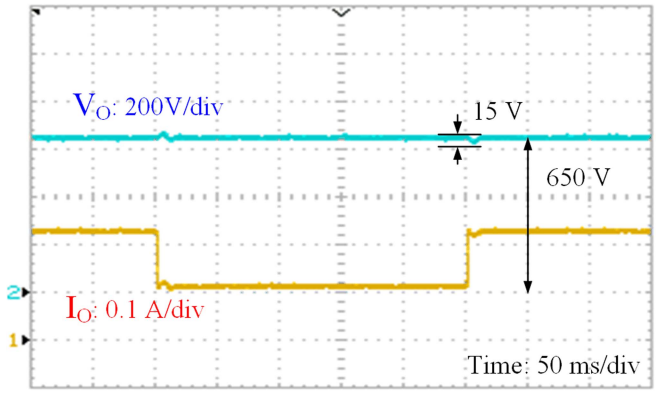

Fig. 10. Step load transient response.

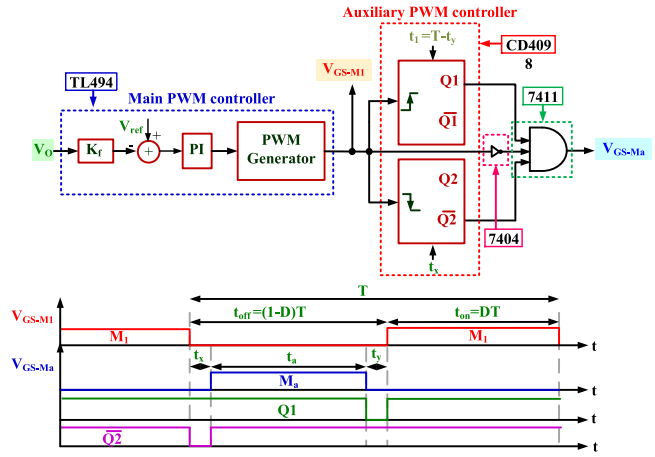

Fig. 11. Control circuit schematic and waveforms.

and IC 7410. IC CD4098 contains two monostable blocks, IC 7404 is a NOT gate, and IC 7411 is an AND gate and all of them provide suitable pulse signals from the main control block for the auxiliary switch. The pulse width of the first and second monostable is adjusted by $t_1 = T - t_y$ and t_x, respectively. In this control circuit schematic, t_x is the time interval to discharge the auxiliary switch snubber capacitor (C_{Sa}) and charge the main switch snubber capacitor (C_{S1}), simultaneously. Also, t_y is the time interval to discharge C_{S1} and charge CSa simultaneously.

$$t_x \geq \frac{(V_{C1}+V_{C3})(C_{S1}+C_{\mathrm{Sa}})}{\frac{2(n+m+1)I_O}{D}+\frac{(1-D)V_{C4}}{2L_{m2}f_{\mathrm{sw}}}+(2-D)GI_O}, \tag{33}$$

$$t_y \geq \frac{(V_{C1}+V_{C3})(C_{S1}+C_{\mathrm{Sa}})}{\frac{(n+m+1)I_O}{1-D}+\frac{(1-D)V_{C4}}{2L_{m2}f_{\mathrm{sw}}}-(1-D)GI_O}. \tag{34}$$

The integrated circuits used for the control circuit are illustrated in Fig. 12. To create the delay time for M_a turn-ON, the gate signal of M_1 is employed for the leading edge triggering of the first monostable (+TR1) and the trailing edge triggering of the second monostable (-TR2) in CD4098. The pulsewidth of the first and second monostable is obtained by the external resistor and capacitor (RX1 and CX, and RX2 and CX2, respectively). Then, the output pulsewidth of two monostable terminals ($\overline{Q_2}$

TABLE II
PERFORMANCE COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER COUNTERPART CONVERTERS

Con.	Number of S/D/BC/C,W/T.C[1]	Voltage gain (G)	Maximum normalized switches voltage stress (V_M/V_O)	Normalized sum of the diodes voltage stresses $\sum(V_D/V_O)$	At $D=0.65$ and $n=m=1$ G	At $D=0.65$ and $n=m=1$ (V_M/V_O)	Switching condition on/off	CG[2]	LICR[3]	Reported f_{sw}/P/E[4]
[11]	2/5/4/2,3/13	$\frac{n(2-D)}{(1-D)^2}$	$\frac{(1-D)}{n(2-D)}$	$\frac{2+3n-2D}{n(2-D)}$	11	0.26	Hard/Hard	no	yes	50/500/91
[12]	2/4/4/2,2/12	$\frac{2(1-D)}{(1-D)^2-D}$	$\frac{1}{2}$	$\frac{4-3D}{2(1-D)}$	–	–	Hard/Hard	no	yes	30/250/92.2
[13]	2/5/5/2,3/14	$\frac{1+2n+D}{(1-D)^2}$	$\frac{(1+D)}{1+2n+D}$	$\frac{4+4n-2D}{1+2n+D}$	29.8	0.45	Hard/Hard	yes	yes	50/280/94.3
[14]	2/5/5/3,3/15	$\frac{2+D}{(1-D)^2}$	$\frac{1}{2+D}$	$\frac{8G-1+(1+12G)^{0.5}}{6G+1-(1+12G)^{0.5}}$	21.6	0.37	Hard/Hard	no	no	33/250/93.5
[18]	2/5/5/2,3/14	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{1}{G(1-D)^2}$	$\frac{5+4n-2nD-3D}{G(1-D)^2}$	23	0.35	ZCS/Hard	yes	no	50/130/96.3
[21]	2/3/5/2,4/12	$\frac{m(n+1)(1+D)+2}{(1-D)}$	$\frac{1}{m(n+1)(1+D)+2}$	$\frac{3m(n+1)+3}{G(1-D)}$	15.1	0.19	ZVS/ZVS	yes	no	100/400/95.3
[22]	2/4/6/2,3/14	$\frac{1+2n}{(1-D)}$	$\frac{1}{1+2n}$	$\frac{4n}{1+2n}$	8.5	0.33	ZVS/ZVS	yes	yes	95/500/98
[23]	2/6/6/2,3/16	$\frac{1+2n}{(1-D)^2}$	$\frac{1}{1+2n}$	$\frac{1+4n}{1+2n}$	24.5	0.33	ZVS/ZVS	yes	yes	50/175/92.8
[24]	3/4/5/2,4/14	$\frac{(2-D)(n+m(1-D))+1-D}{(1-D)^2}$	$\frac{1}{G(1-D)^2}$	$\frac{3n(2-D)+1-D}{G(1-D)^2}$	17.7	0.3	ZVS/ZVS	yes	no	100/500/96.8
[25]	4/4/5/2,4/15	$\frac{n(2-D)+(1-D)^2}{(1-D)^2}$	$\frac{1}{G(1-D)^2}$	*	12	0.68	ZVS/ZVS	yes	no	100/1k/94.8
pro.	2/4/5/3,5/14	$\frac{2+n+m}{(1-D)^2}$	$\frac{1}{2+n+m}$	$\frac{3+n+m}{2+n+m}$	32.6	0.25	ZVS/ZVS	yes	yes	100/150/96.7

1. Switch/Diode/Bulky capacitor (all the capacitors except the snubber capacitors)/Core,Winding/Total components (S+D+BC+C)
2. Common ground 3. Low input current ripple 4. fs/P/E: Switching frequency [kHz]/ Power [W]/ Efficiency [%] *. $(\frac{3n+(1-D)}{n(2-D)+(1-D)^2}+\frac{L_1}{M})\frac{M}{L_1}$

TABLE III
GATE DRIVE COMPLEXITY AND LOSS COMPARISON BETWEEN THE CONVERTERS IN TABLE II

Converter	Number of switches	Gate drive complexity and loss	Gate drive requirements
[11]–[14], [18]	2	Low	Two switches are signaled simultaneously and one switch has a floating source.
[21]–[23], proposed	2	Low	Switches are signaled complementary and one switch has a floating source.
[24]	3	Medium-High	Two switches are signaled simultaneously and one switch is signaled complementary. Two switches have floating sources.
[25]	4	High	Two switches are signaled simultaneously and the other two switches are signaled complementary. Three switches have floating sources.

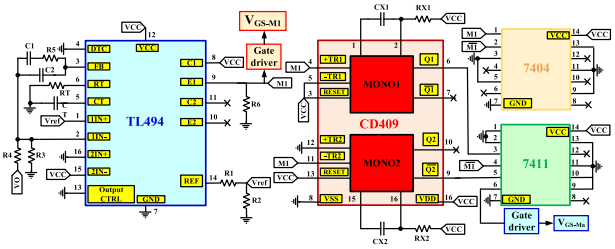

Fig. 12. Details of the proposed converter control circuit.

and Q_1), and the NOT gate signal of M_1 are applied to the AND gate IC 7411.

VI. COMPARISON

To demonstrate the advantages of the proposed converter, a comprehensive comparison is performed with other counterpart structures in Table II. Moreover, a comparison in terms of gate drive complexity and loss, between the proposed converter and the converters in Table II, is performed in Table III. Also, the principal characteristics of the converters in [11], [12], [13], [14], [18], [21], [22], [23], [24], [25] versus duty cycle are compared in Fig. 13. As observed, the proposed structure with an acceptable number of elements has the highest voltage gain and low voltage stress across the switches (a quarter of output voltage at $n=m=1$) while the summation of voltage stresses on diodes is minimum. Moreover, soft-switching operation at ZVS is provided by the proposed converter and capacitive turn-ON losses are eliminated. Besides, the converter benefits from the common ground between the input and output and has low input current ripple.

According to Fig. 13(b), the switch voltage stress is decreased by enhancing duty cycle in [11] but this converter and the converters in [12] and [14] have no common ground between the input and output and they are hard switched. Moreover, the converter in [14] has higher number of elements compared to the proposed converter and high input current ripple, which limits the converter applications. The converters in [13] and [18], have high voltage gain with the same number of elements as the proposed converter, but suffer from hard switching operation while the input current ripple is high in the converter of [18]. The converters of [21], [22], [23], [24], [25] operate under ZVS condition however, the voltage gain is low in [21] and [22] and the converters in [21], [24], and [25] have high input current ripple. The converter in [22] has a high efficiency with the same number of elements as the proposed converter, but it has lower voltage gain. To increase the voltage gain, the number of elements must be increased, which reduces the efficiency. The converter of [23] has lower voltage gain with higher number of the elements than the proposed converter. The voltage stress over the power switches and the sum of diodes voltage stresses in the converter of [25] is extremely higher than the presented converter. Also, this converter has two extra switches while the converter in [24] has one additional switch in their structures which increase the converters size, cost, and control complexity.

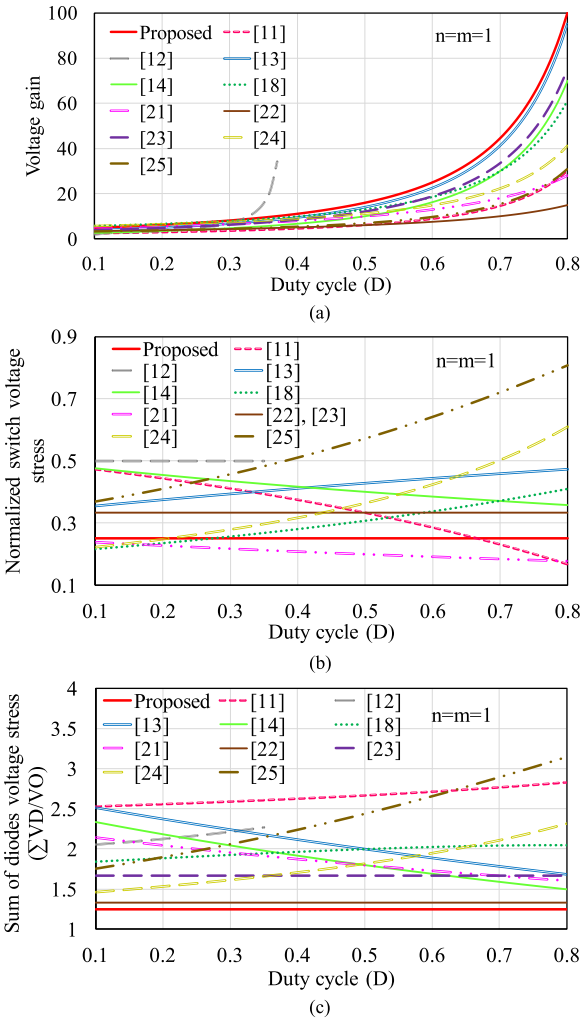

Fig. 13. Comparison among the converters in Table II in terms of (a) Voltage gain, (b) Normalized switches voltage stress, and (c) Normalized sum of diodes voltage stresses.

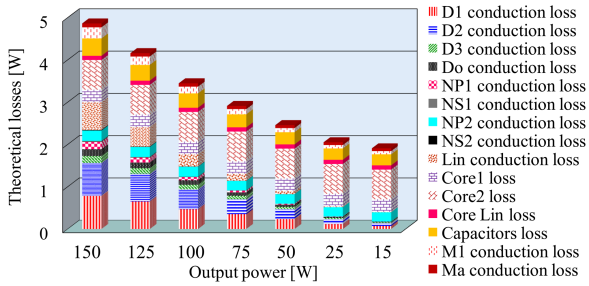

Fig. 14. Proposed converter loss breakdown analysis.

The proposed converter loss distribution at various output powers is achieved as shown in Fig. 14. Due to soft switching operation, switching losses are eliminated and efficiency is improved. The efficiency diagram versus the output power for the proposed converter and some of the quadratic converters in Table II that have two switches is presented in Fig. 15, which indicates 96.7% efficiency for the proposed converter at full

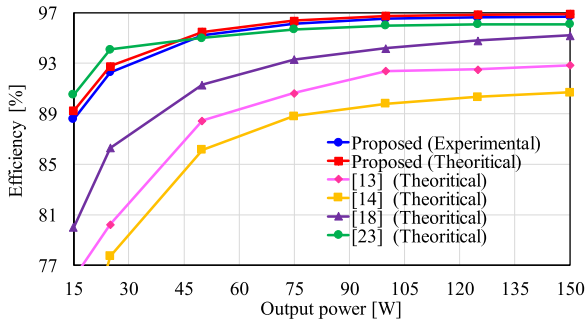

Fig. 15. Efficiency versus output power of the proposed converter and other counterpart converters.

load and 96% over in a wide output power range. To obtain the compared converters efficiencies at the same operating condition as the proposed converter, these converters are designed for the specifications reported in Table I before computer simulation. Then, the converters theoretical efficiencies are attained by performing loss breakdown analysis, which requires data to be obtained from simulation results, theoretical calculations, and datasheet parameters. It is notable that the same switches and diodes as the proposed converter are used for all these converters, only due to the higher voltage stress of the auxiliary switch in the converters of [13], [14], switch APT84M50 L is employed which is the same category switch. Also, the same magnetic cores as the proposed converter are used for other converters.

In the loss breakdown analysis of the proposed converter, due to ZVS operation of switches, the switching losses and capacitive turn-ON losses are assumed approximately zero. The conduction losses of switches and diodes are approximated by $R_{\rm DS}({\rm on}){I_M}^2({\rm rms})$, and $V_F I_D({\rm ave})$, respectively, where $R_{\rm DS}({\rm on})$ is the switches ON-state resistance, $I_M({\rm rms})$ is the root mean square (rms) value of switches ON-state current, V_F is the diodes forward bias voltage drop and $I_D({\rm ave})$ is the average current of diodes. Litz wires are used for windings, and the windings conduction loss is obtained from $R_W {I_W}^2({\rm rms})$ which R_W is the windings electric resistance and $I_W({\rm rms})$ is the rms value of windings current. Also, the ESR loss of capacitors is obtained from ESR${I_C}^2({\rm rms})$, where ESR is the equivalent series resistance and $I_C({\rm rms})$ is the rms current of capacitors. Moreover, the core loss is approximated by the Steinmetz equation as $P_C = a{f_{\rm sw}}^x (B_{pk})^y$ where P_C is the core loss density in mW/cm^3, $B_{pk} = \frac{L\Delta I}{2nA_e}$ is the flux density peak in Tesla while, a, x, and y are the Steinmetz coefficients and reported by the manufacturer. L is the inductor value, ΔI is the inductor current swing, n is the number of turns and A_e is the core effective cross-sectional area.

VII. Conclusion

This article has proposed a new ultra-high step-up converter based on the quadratic structure. The presented converter has taken advantage of integrating CIs, a VMC, and an active clamp circuit to increase the voltage gain and reduce the switch voltage stress significantly. Moreover, soft switching operation under

ZVS at turn-ON and turn-OFF for all switches is established which is independent of load variation. As a result, switching losses and capacitive turn-ON losses are eliminated. Also, the leakage inductance energy is absorbed and recycled to the output while the output diodes turn OFF at ZCS, which eliminate the reverse recovery problem. Furthermore, the proposed converter has continuous input current and common ground between the input source and load which are necessary factors for various applications. The performance comparison shows that the introduced converter is superiority to other counterpart structures in terms of voltage gain, switch voltage stress, and providing soft switching operation. The results of an implemented converter prototype and loss breakdown analysis confirm the converter performance.

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Maryam Hajilou received the B.S. and M.Sc. degrees in electrical engineering from Isfahan University of Technology, Isfahan, Iran, in 2018 and 2020, respectively. She is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran.

Her current research interests include high step-up dc–dc converters, resonant converters, and soft switching techniques.

Hosein Farzanehfard (Member, IEEE) was born in Isfahan, Iran, in 1961. He received the B.Sc. and M.Sc. degrees from the University of Missouri, Columbia, MO, USA, in 1983 and 1985, respectively, and the Ph.D. degree from Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 1992, all in electrical engineering.

Since 1993, he has been a Faculty Member with the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran. He is the author or coauthor of more than 300 technical papers published in journals and conference proceedings. His current research interests include high-frequency soft-switching converters, power factor correction, bidirectional converters, and renewable energy interface converters.