Nonisolated Integrated Boost Featured (NIIBF) Multi-Input Ultrahigh Gain DC–DC Converter

Obulapathi Balapanuru, *Member, IEEE*, Makarand M. Lokhande, *Senior Member, IEEE*, and Mohan V. Aware, *Senior Member, IEEE*

***Abstract*—The nonisolated multi-input topologies are restricted to low voltage gain relative to single-input topologies. To achieve high voltage gain, coupled inductor, and various voltage-boosting techniques (such as switched inductors/capacitors) are used in the literature. The voltage-boosting structures increase the total component count, size, and cost of the converter. The operational limitations are observed in coupled-inductor-based converters due to peak current at a source side. This work proposes a nonisolated integrated boost featured converter without using a coupled inductor and voltage-boosting techniques. It achieves ultrahigh voltage gain with three basic boost cells, over other reported converters in a two-input category, with less component count and low average normalized voltage stress. It also facilitates flexible operating possibilities such as single-input, multi-input, and energy transfer capability among input ports. Furthermore, with equal duty cycle control ($D_1 = D_2 = D_3$), the power management between the energy storage systems is inherently provided by the proposed topological structure. The control complexity is minimized in a modified control algorithm. Hence, the integration of various energy storage systems is simplified. A hardware prototype is developed to validate the functional capability of the proposed converter.**

***Index Terms*—Bidirectional, high gain, hybrid energy storage, inherent current sharing, multi-input, nonisolated.**

I. Introduction

THE multi-input dc–dc converters have a vital role in various applications such as dc/ac microgrid, hybrid electric vehicles (EVs) for integrating the different renewable energy storage resources (PV, wind, etc.), and hybrid energy storage systems (battery, ultracapacitor, fuel cells, etc.). The main advantages of the multi-input converter are less component count, unified controllability, and cost-effectiveness. However, multi-input topologies are restricted to low voltage gain relative to single-input topologies [1]. To achieve high voltage gain, coupled inductor, and various voltage-boosting techniques such as switched capacitor, voltage multiplier, and voltage lift switched inductor are used in the literature [2], [3], [4], [5], [6], [7], [8], [9]. The operational limitations are observed in coupled-inductor-based converters due to the high peak current at a source side. The noncoupled-inductor-based converters achieve high voltage gain by embedding boosting techniques such as a switched capacitor/inductor, voltage multiplier, etc., into the basic dc–dc converter [5], [6], [7], [8], [9]. The coupled inductor, voltage multiplier, and switched capacitor-based high-gain topologies commonly encounter challenges related to increased size or elevated cost. As a result, the nonisolated multi-input converters with an integrated boost feature and without using a coupled inductor (or advanced boosting techniques) are reported in the literature with reduced component count and size of the converter [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20].

In [10], two basic buck–boost converters are used to form a two-input converter. In [11] and [12], two conventional converters, such as boost and buck–boost structures, are integrated to form a multi-input topology. The reported structure facilitates relatively low voltage gain with unidirectional capability. In [13], a half-bridge buck–boost and boost cells are restructured to form a multi-input topology. In [14], a bridge structure is formed with two-input sources and a unidirectional control switch. In [15], an extended version of the converter reported in [14] is formed by adding an additional source across V_1 with relay connectors. In [16], the source cell, along with a switch and diode, are embedded into the two-port conventional buck–boost converter to form a multi-input structure. In [17], a modular multi-input converter with boost cells is reported.

The previously discussed noncoupled-inductor-based converters are suffering from either low voltage gain [5], [6], [7], [8], [11], [13], [17] or high voltage stress [7], [13], [18], [19]. As a matter of fact, the main contribution of this work is to propose a multi-input dc–dc converter with an integrated boost feature having high voltage gain and low voltage stress. The proposed converter is developed with three boost cells integrated together, as shown in Fig. 1. It has ultrahigh voltage gain (14 at $D = 0.5$), low average normalized voltage stress (ANVS), and less component count than other reported converters in a two-input category. Furthermore, it facilitates additional functionalities such as single-input, multi-input, energy transfer capability among input ports, inherent power sharing, and simplified control. Hence, the proposed converter has well-suitable performance characteristics for integrating various renewable energy resources (PV) and hybrid energy storage systems (battery, ultracapacitor, and fuel cell) with simplified control for dc/ac microgrid or hybrid EV applications.

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The authors are with the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur 440010, India (e-mail: obulapathi36@students.vnit.ac.in; makarand.lokhande@gmail.com; mvaware@eee.vnit.ac.in).

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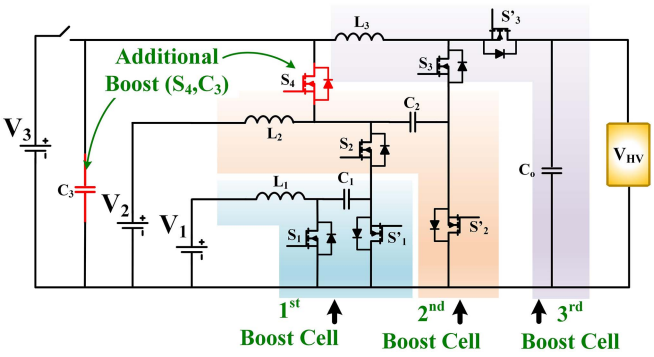

Fig. 1. Proposed NIIBF multi-input converter.

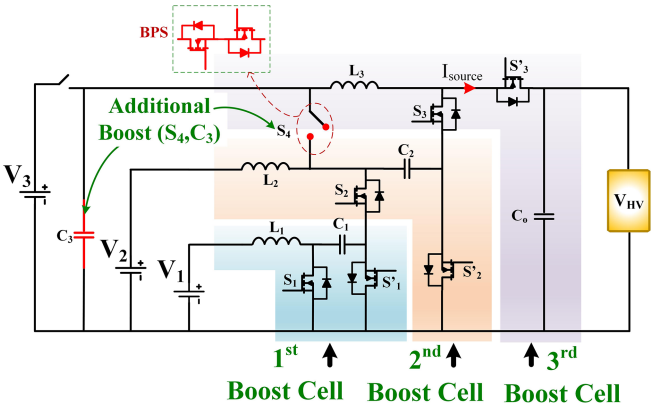

Fig. 2. Topology formation process of the proposed converter.

The main contributions of the work are summarized as follows.

1) Achieving ultrahigh voltage gain by integrating interleaved and semicascaded structures with three basic boost cells.
2) Less component count and low average normalized voltage stress (ANVS).
3) Inherent power management between sources (i.e., during dual-input operation, V_1 and V_2 inherently deliver 65% and 35% of required power at duty cycle (D) = 0.6 without any controller requirement).
4) Current sensorless topology due to the nonexistence of a current loop.
5) Simplified control algorithm to integrate different energy storage systems.

II. Proposed Topology

The proposed converter consists of three main power switches (S_1, S_2, S_3), three complementary power switches (S_1', S_2', S_3'), and one bidirectional power switch (BPS or S_4), three inductors (L_1, L_2, L_3), and four capacitors (C_1, C_2, C_3, and C_o). For simplicity, here onward, the BPS is shown in the circuit diagram with a single switch S_4. The topological formation of the proposed converter is depicted in Fig. 2. It is an integration of three conventional boost cells in a semicascaded manner. Furthermore, the components S_4 and C_3 provide additional boost during single-input and two-input operations of the proposed converter. The BPS facilitates the three-input operation and energy transfer among the sources. The various operating possibilities of the proposed converter are described as follows:

1) single-input operation while V_1 and V_3 sources are unable to deliver the power;
2) two-input operation while V_3 source is unable to deliver the power;
3) bidirectional operation of the proposed converter;
4) three-input operation when V_1, V_2, and V_3 sources are available to deliver the power;
5) energy transfer between the input sources (V_2 charging from V_3).

The operational possibilities of the proposed converter are divided into Sections II-A and II-B. In Section II-A, the operation of the proposed converter using S_4 as a single switch for single-input, two-input, and bidirectional operations is described. In Section II-B, the operation of the proposed converter using S_4 as a BPS switch for three-input and battery charging operations is included. Furthermore, the synchronous switching scheme is implemented to all the operating possibilities of the proposed converter.

A. Operation of Proposed Converter Without BPS Switch

1) Single-Input Operation of Proposed Converter: In single-source operation, sources V_1 and V_3 are inactive. Hence, the first boost cell (S_1, L_1, C_1) is in the OFF state throughout the operation. However, the third boost cell can be connected with the second boost cell, which provides high voltage gain.

Mode-1: In this mode of operation, the main switches S_2 and S_3 are in the ON state. The inductor L_2 stores energy from input source V_2. Inductor L_3 stores energy from capacitors C_2, and C_3 through switch S_1' and S_3. On the load side, the output capacitor C_o alone supplies the load, as shown in Fig. 3(a).

Mode-2: In this mode, the main switches S_2 and S_3 are in the OFF state and complementary switches (S_2', S_3', S_4) are in the ON state. The stored energy in the inductor L_2 charges the capacitors C_2 and C_3. The remaining energy in L_2 and energy stored in L_3 transfer to the output capacitor C_o and load through output switch S_3', as shown in Fig. 3(b).

2) Two-Input Operation of Proposed Converter: In two-source operation, source V_3 is inactive. However, all three boost cells can be utilized together. Consequently, it provides higher voltage gain than single-source operation.

Mode-1: In this mode of operation, the main switches S_1, S_2, and S_3 are in the ON state. The inductor L_1 stores energy from input source V_1. Inductor L_2 stores energy from both output capacitor C_1 and input source V_2. Inductor L_3 stores energy from capacitors C_1, C_2, and C_3. On the load side, the output capacitor C_o alone supplies the load, as shown in Fig. 4(a).

Mode-2: It is a part of mode-1. In the $D_2 \neq D_1$ case, one of the source inductors discharges, and other source inductor charges through the path provided by the complementary switches. for instance, if $D_2 > D_1$, as shown in Fig. 4(b), in that case, inductor L_2 stores energy from capacitor C_1 for D_1 duration and from

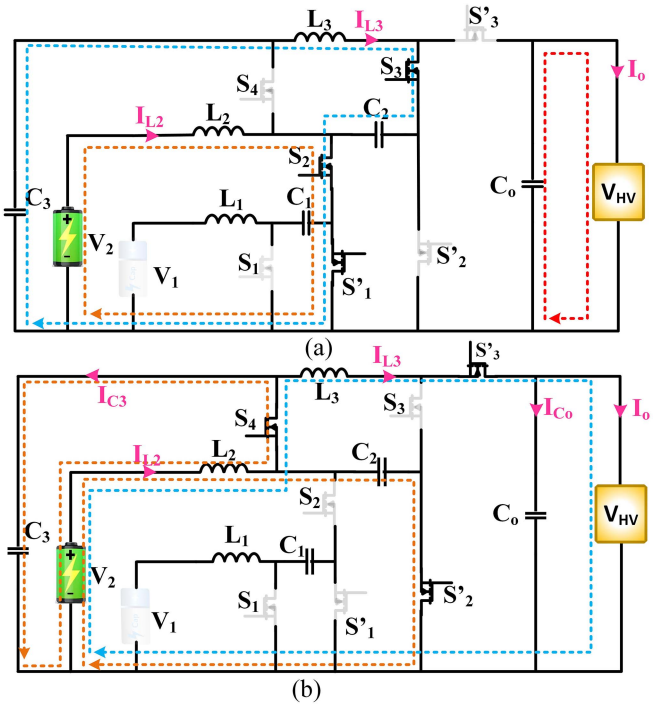

Fig. 3. Single-input operation of the proposed converter with synchronous switching scheme. (a) Mode-1. (b) Mode-2.

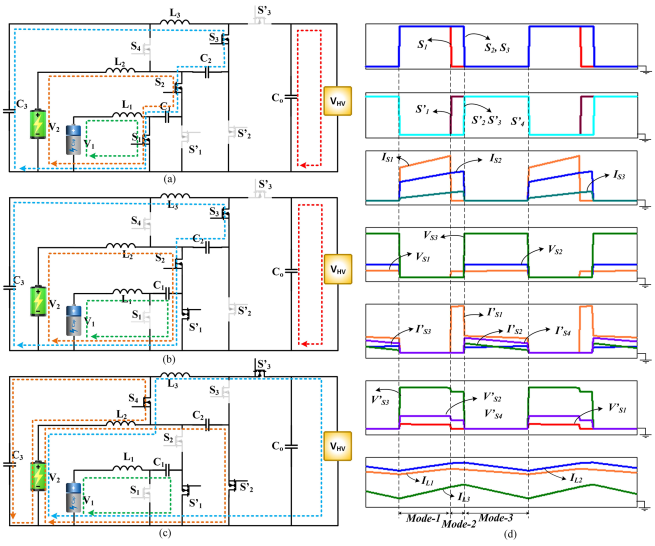

Fig. 4. Representation of the two-input operation of the proposed work with synchronous switching. (a) Mode-1. (b) Mode-2. (c) Mode-3. (d) Switching waveforms with mode-1, mode-2, and mode-3.

source V_2 alone for D_2 duration. Similarly, inductor L_3 stores energy from capacitor C_1 for D_1 duration and from capacitors C_1 and C_2 for D_2 duration. In the inductor L_1 case, it transfers energy to C_1 through switch S_1'.

Mode-3: In this mode, the main switches S_1, S_2, and S_3 are in the OFF state, and the complementary switches (S_1', S_2', S_3', S_4) are in the ON state. The stored energy in the inductor L_1 charges the capacitor C_1. Furthermore, inductor L_2 gives energy to the

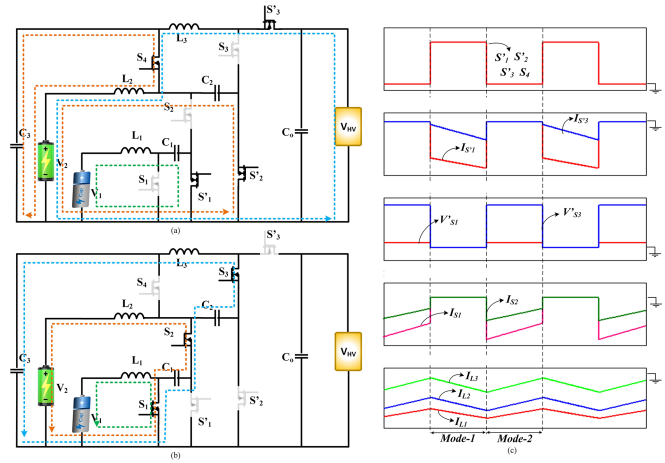

Fig. 5. Representation of bidirectional capability of the proposed converter. (a) Mode-1. (b) Mode-2. (c) Switching waveforms with mode-1 and mode-2.

capacitors C_2 and C_3. In addition, the inductors L_2 and L_3 transfer their energies to the capacitor C_o and the load through the output switch S_3', as shown in Fig. 4(c). The steady-state switching waveforms for the two-input operation are shown in Fig. 4(d).

3) Bidirectional Operation of Proposed Converter: In two-source operation, source V_3 is inactive. However, all three boost cells can be utilized together. In this operation, the power flows from high-voltage side (load) to low-voltage side (source-1 and source-2).

Mode-1: In this mode of operation, main switches S_1, S_2, and S_3 are in the OFF state and complementary switches S_1', S_2', S_3', and S_4 are in the ON state. The inductor L_1 stores energy from output capacitor C_1 through source V_1. Inductor L_2 stores energy from both capacitor C_2 and capacitor C_3 through input source V_2. Inductor L_3 stores energy from the high side (V_{HV}) through inductor L_2 and source V_2, as shown in Fig. 5(a).

Mode-2: In this mode, the main switches S_1, S_2, and S_3 are in the ON state, and the complementary switches (S_1', S_2', S_3', S_4) are in the OFF state. The stored energy in the inductor L_1 freewheels with the source V_1 through switch S_1. Similarly, L_2 freewheels with the source V_2 through switch S_2. At the same time, it charges the output capacitor C_1. Furthermore, inductor L_3 gives energy to the capacitors C_1, C_2, and C_3, as shown in Fig. 5(b). The switching waveforms of the proposed converter in the bidirectional operation are depicted in Fig. 5(c).

B. Operation of Proposed Converter With BPS Switch

1) Three-Input Operation of Proposed Converter: In three-source operation, a BPS switch is required as switch S_4 to avoid reverse power flow from V_2 to V_3. So that, all three boost cells can be effectively utilized. It provides higher voltage gain than single-source operation and lower than two-source operation.

Mode-1: In this mode of operation, the main switches S_1, S_2, and S_3 are in the ON state. The inductor L_1 stores energy from input source V_1. Inductor L_2 stores energy from both output capacitor C_1 and input source V_2. Inductor L_3 stores energy

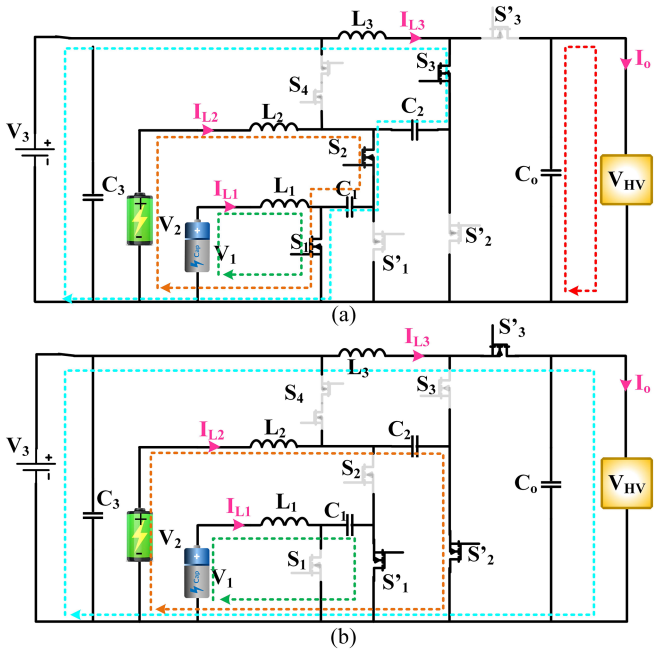

Fig. 6. Three-input operation of the proposed converter with synchronous switching. (a) Mode-1. (b) Mode-2.

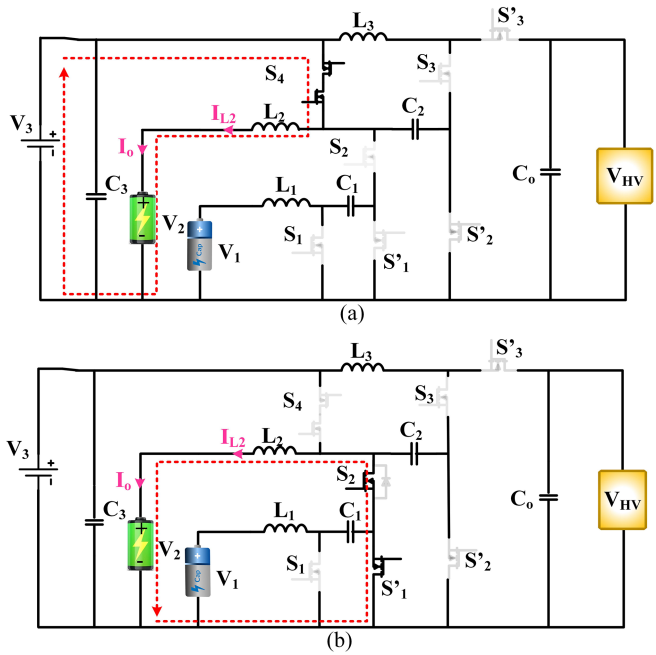

Fig. 7. V_2 source charging from V_3 source operation of the proposed converter. (a) Mode-1. (b) Mode-2.

from capacitors C_1, C_2, and V_3. On the load side, the output capacitors C_o alone supply the load, as shown in Fig. 6(a).

Mode-2: In this mode, the main switches S_1, S_2, and S_3 are in the OFF state, and the complementary switches (S_1', S_2', S_3') are in the ON state. The stored energy in the inductor L_1 charges the capacitor C_1. Furthermore, inductor L_2 gives energy to the capacitor C_2. Meanwhile, the inductor L_3 transfers its energy to the capacitor C_o and the load through the output switch S_3', as shown in Fig. 6(b).

2) V_2 Source Charging From V_3 Source Operation of Proposed Converter. Mode-1: In this mode of operation, all main switches are in the OFF state. Only, the BPS S_4 in the ON state. The inductor L_2 stores energy from input source V_3. Energy is delivered to the V_2 ports, as shown in Fig. 7(a).

Mode-2 In this mode, the main switches S_1, S_2, and S_3 are in the OFF state, and the complementary switch S_1' is in the ON state. The stored energy in the inductor L_1 transfers into the V_2 ports through switches S_1' and S_2, as shown in Fig. 7(b).

In order to obtain the voltage gain (M) expression for each operation of the proposed converter, a volt–second balance law is applied to the inductors L_1, L_2, and L_3 in the following section.

III. Steady-Sate Analysis of the Proposed Converter

A. Single-Input Operation

The volt–second balance applied to inductor L_2 is given by

$$\int_0^{D_2T_s} V_2 + \int_{D_2T_s}^{T_s} (V_2 - V_{c2}) = 0$$

$$V_{c2} = V_{c3} = \frac{V_2}{1 - D_2}. \tag{1}$$

The volt–second balance applied to inductor L_3 is given by

$$\int_0^{D_2T_s} (V_{c2} + V_{c3}) + \int_{D_2T_s}^{T_s} (V_{c3} - V_{co}) = 0$$

$$V_{co} = \frac{V_2(1 + D_2)}{(1 - D_2)^2}. \tag{2}$$

Single-source voltage gain (M_1) is given by

$$M_1 = \frac{V_2}{V_{co}} = \frac{1 + D_2}{(1 - D_2)^2}. \tag{3}$$

Similar to the volt–second balance law, in order to get the average inductor currents for the single-input operation, an ampere-balance law is applied to the inductor L_2. Accordingly, the following equation is obtained:

$$I_{L_2} = \frac{I_o(1 + D)}{(1 - D)^2}. \tag{4}$$

B. Two-Input Operation

The volt–second balance applied to inductor L_1 is given by

$$\int_0^{D_1T_s} V_1 + \int_{D_1T_s}^{T_s} (V_1 - V_{c1}) = 0$$

$$V_{c1} = \frac{V_1}{1 - D_1}. \tag{5}$$

The volt–second balance applied to inductor L_2 is given by

$$\int_0^{D_1T_s} V_{c1} + \int_0^{D_2T_s} V_2 + \int_{D_2T_s}^{T_s} (V_2 - V_{c2}) = 0$$

$$V_{c2} = V_{c3} = \frac{V_2 + V_{c1}D_1}{1 - D_2}. \tag{6}$$

The volt–second balance applied to inductor L_3 is given by

$$\int_0^{D_1T_s} V_{c1} + \int_0^{D_2T_s} (V_{c2}+V_{c3}) \int_{D_2T_s}^{T_s} (V_{c2}-V_{co}) = 0$$

$$V_o = V_{co} = \frac{2-(1-D)^2}{(1-D)^3} V_{\text{in}}; \quad \text{for } D_1 = D_2. \tag{7}$$

The voltage gain (M_2) for equal voltage and duty ratio for the two-input operation is given by

$$M_2 = \frac{V_o}{V} = \frac{2-(1-D)^2}{(1-D)^3}. \tag{8}$$

Similar to the volt–second balance law, in order to get the average inductor currents for the two-input operation, an ampere-balance law is applied to the inductors L_1 and L_2. Accordingly, the following equations are obtained:

$$\left.\begin{aligned} I_{L_1} &= \frac{2I_oD}{(1-D)^3} \\ I_{L_2} &= \frac{I_o(1+D)}{(1-D)^2} \end{aligned}\right\}. \tag{9}$$

C. Three-Input Operation of Proposed Converter

The volt–second balance applied to inductor L_1 is given by

$$\int_0^{D_1T_s} V_1 + \int_{D_1T_s}^{T_s} (V_1 - V_{c1}) = 0$$

$$V_{c1} = \frac{V_1}{1-D_1}. \tag{10}$$

The volt–second balance applied to inductor L_2 is given by

$$\int_0^{D_2T_s} (V_2+V_{c1}) + \int_{D_2T_s}^{T_s} (V_2 - V_{c2}) = 0$$

$$V_{c2} = \frac{V_1D_2 + V_2(1-D_1)}{(1-D_1)(1-D_2)}. \tag{11}$$

The volt–second balance applied to inductor L_3 is obtained as

$$\int_0^{D_3T_s} (V_{c1}+V_{c2}+V_{c3}) + \int_{D_3T_s}^{T_s} (V_{c3}-V_{c0}) = 0$$

$$V_{co} = \frac{V_1D_3 + V_2(1-D_1)D_3 + V_3(1-D_1)(1-D_2)}{(1-D_1)(1-D_2)(1-D_3)}. \tag{12}$$

Three-source voltage gain (M_3) with the conditions $V_1 = V_2 = V_3$ and $D_1 = D_2 = D_3$ is given by

$$M_3 = \frac{V_{co}}{V} = \frac{1}{(1-D)^3}. \tag{13}$$

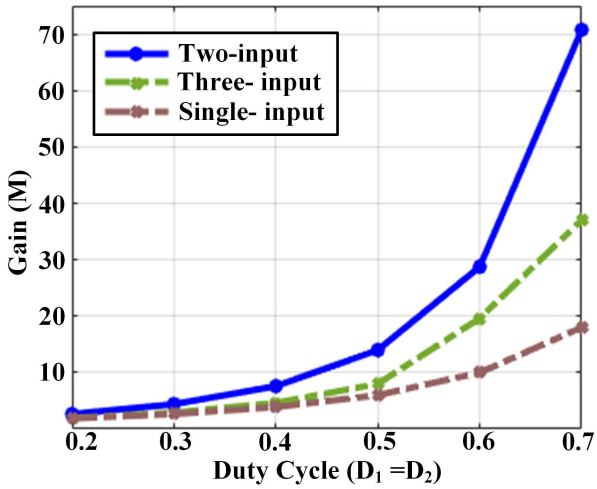

Fig. 8. Analytical voltage gains of the proposed converter for single-input, two-input, and three-input modes of operation.

Similarly to the volt–second balance law, in order to get the average inductor currents for the two-input operation, an ampere-balance law is applied to the inductors L_1, L_2, and L_3. Accordingly, the following equations are obtained:

$$\left.\begin{aligned} I_{L_1} &= \frac{I_oD}{(1-D)^3} \\ I_{L_2} &= \frac{I_oD}{(1-D)^2} \\ I_{L3} &= \frac{I_o}{1-D} \end{aligned}\right\}. \tag{14}$$

The voltage gain of the proposed converter for single-input, two-input, and three-input mode operations is shown in Fig. 8 with $(V_1 = V_2 = V_3)$ and $(D_1 = D_2 = D_3)$.

D. V_2 Charging From V_3 Operation of Proposed Converter

The volt–second balance applied to inductor L_2 is obtained as

$$\int_0^{D_1T_s} (V_3 - V_2) + \int_{D_1T_s}^{T_s} -V_2 = 0 \tag{15}$$

$$V_2 = V_3D_3. \tag{16}$$

IV. Voltage and Current Stress Analysis

During the ON-time switching period, the complementary switches are in the OFF state. Therefore, voltage stress across S_1', S_2', S_3', and S_4 are given by

$$\left.\begin{aligned} V_{S_1'} &= V_{C1} = \frac{V_1}{1-D} \\ V_{S_2'} &= V_{S_4} = V_{c1}+V_{c2} = \frac{(2-D)V_1}{(1-D)^2} \\ V_{S_3'} &= V_{c1}+V_{c2}+V_{co} = \frac{(3-D)V_1}{(1-D)^3} \end{aligned}\right\}. \tag{17}$$

On the other hand, during the OFF-time switching period, the main switches S_1, S_2, and S_3 are in the OFF state. Therefore,

voltage stresses across S_1, S_2, and S_3 are given by

$$\left.\begin{aligned} V_{S_1} &= V_{c1} = \frac{V_1}{1-D} \\ V_{S_2} &= V_{c2} = \frac{V_1}{(1-D)^2} \\ V_{S_3} &= V_{co} = \frac{2-(1-D)^2}{(1-D)^3} V_1 \end{aligned}\right\}. \tag{18}$$

a) Average normalized voltage stress (ANVS): It is the summation of the total voltage stress of all the switches divided by the number of switches and output voltage

$$\text{ANVS} = \frac{\sum V_{Si}}{n * V_o}. \tag{19}$$

The ANVS for different input modes of operations is given by

$$\text{ANVS}_1 = \frac{3-D}{3(1+D)}; \quad \text{for} \quad \text{single-input} \tag{20}$$

$$\text{ANVS}_2 = \frac{11+3D^2-10D}{7(2-(1-D)^2)}; \quad \text{for} \quad \text{two-input} \tag{21}$$

$$\text{ANVS}_3 = \frac{9+3D^2-11D}{6}; \quad \text{for} \quad \text{three-input.} \tag{22}$$

b) Current stress on the converter components: During the ON-time switching period, the main switch S_3 carries inductor current (I_{L3}). Consequently, the maximum current stress on switch S_3 is calculated as follows:

$$I_{S_{3_p}} = I_{L3_p} = I_{L3} + \frac{\Delta i_{L3}}{2} \tag{23}$$

$$= I_{L3} + (V_{C1} + V_{C2} + V_{C3})D/(2L_3 f_{\text{sw}}). \tag{24}$$

Similarly, the maximum current stress on switches S_1 and S_2 are given by

$$I_{S_{2_p}} = I_{S_{3_p}} + I_{L2_p} \tag{25}$$

$$I_{S_{2_p}} = I_{S_{3_p}} + I_{L_2} + (V_{C1} + V_2)D/(2L_2 f_{\text{sw}}) \tag{26}$$

$$I_{S_{1_p}} = I_{S_{2_p}} + I_{L_{1_p}} \tag{27}$$

$$I_{S_{1_p}} = I_{S_{2_p}} + I_{L_1} + V_1 D/(2L_1 f_{\text{sw}}). \tag{28}$$

In addition, during the OFF-time switching period, switch S_1' carries inductor L_1 peak current under the equal duty ratio condition. Whereas, during the unsymmetrical duty ratio condition, the switch S_3 carries inductor current I_{L1}, I_{L2}, and I_{L3} for $D_2 - D_1$ duration. The maximum current stress on switch S_3 for both equal and unsymmetrical duty ratio conditions is given by

$$I'_{S_{1_p}} = I_{L_{1_p}} = I_{L_1} + V_1 D/(2L_1 f_{\text{sw}}). \tag{29}$$

Similarly, the maximum current stress on switches S_2', S_3', and S_4 are given by

$$I'_{S_{2_p}} = I_{S_{4_p}} = (I_{L_{2_p}} - I_{L_{3_p}})/2 \tag{30}$$

$$I'_{S_{3_p}} = I_{L_{3_p}} = I_{L3} + (V_{C1} + V_{C2} + V_{C3})D/(2L_3 f_{\text{sw}}) \tag{31}$$

where I_{L1}, I_{L2}, and I_{L3} are the average inductor currents (9). From the observations, it is clear that the switch S_3' is having least current stress. Meanwhile, the switch S_1 is having high current stress among all the power switches.

V. Design of the Proposed Converter

The critical design conditions of the proposed converter operated in a continuous conduction mode (CCM) are obtained in this section. When the average inductor current exceeds the ripple current flowing through the inductor by more than 50% ($I_L > \Delta i_L/2$), CCM operation is assured.

$$\left.\begin{aligned} L_1 &\geq \frac{(1-D)^6 RT_s}{8-4(1-D)^2} \\ L_2 &\geq \frac{(2-D)(1-D)^4 DRT_s}{2((1+D)(2-(1-D)^2))} \\ L_3 &\geq \frac{(3-D)(1-D)^2 DRT_s}{4-2(1-D)^2} \end{aligned}\right\}. \tag{32}$$

Similarly, the capacitor critical conditions are given by

$$\left.\begin{aligned} C_1 &\geq \frac{I_{L1}(1-D)^2 T_s}{2V_1} \\ (C_2 = C_3) &\geq \frac{I_{L3}(1-D)^2 DT_s}{2V_1} \\ C_0 &\geq \frac{I_o DT_s}{2V_o} \end{aligned}\right\}. \tag{33}$$

The RMS currents of the proposed converter are derived as follows:

$$\left.\begin{aligned} I_{C_1} &= I_o\sqrt{\frac{4D}{(1-D)^5}} \\ I_{C_2} = I_{C_3} &= I_o\sqrt{\frac{D}{(1-D)^3}} \\ I_{C_0} &= I_o\sqrt{\frac{D}{(1-D)}} \end{aligned}\right\} \tag{34}$$

where R is the load resistance and T_s is the converter switching period (T_s=1/f_{sw}).

VI. Small-Signal Analysis of the Proposed Converter

PWM converters are not considered to be a type of linear, time-invariant circuit. It is not possible to perform the dynamic and stability analysis directly. Therefore, small-signal state-space average modeling approach is performed to linearize the nonlinearity of a converter [21]. The state-space representation of a general PWM converter is given by

$$\left.\begin{aligned} \dot{x} &= A_i x + B_i u \\ y &= C_i x + E_i u \end{aligned}\right\} \tag{35}$$

where x is the state variable, u is the input or control variable, and y is the output variable. Furthermore, i=0 represents switch S_1 OFF-state and i=1 for switch S_1 ON-state condition.

Moreover, it is important to note that all the energy storage elements (L_1, L_2, L_3, C_1, C_2, C_o) are considered as state variables. Furthermore, the derivatives of the state variables for ON-time and OFF-time switching periods are listed in Table I. By using the earlier information, the state-space average model of the proposed converter is derived as follows:

TABLE I
DERIVATIVE OF STATE VARIABLES DURING ON STATE AND OFF STATE

Variable	ON state	OFF state
$\frac{di_{L_1}}{dt}$	$\frac{v_1}{L_2}$	$\frac{v_1 - v_{c1}}{L_1}$
$\frac{di_{L_2}}{dt}$	$\frac{v_2 + v_{c1}}{L_2}$	$\frac{v_2 - v_{c2}}{L_2}$
$\frac{di_{L_3}}{dt}$	$\frac{v_{c1} + v_{c2} + v_{c3}}{L_3}$	$\frac{v_{c3} - v_o}{L_3}$
$\frac{dv_{c1}}{dt}$	$\frac{-i_{L2} - i_{L3}}{C_1}$	$\frac{i_{L1}}{C_1}$
$\frac{dv_{c2}}{dt}$	$-\frac{i_{L3}}{C_2}$	$\frac{i_{L2} - I_{L3}}{2C_2}$
$\frac{dv_{c2}}{dt}$	$-\frac{i_{L3}}{C_3}$	$\frac{i_{L2} - I_{L3}}{2C_3}$
$\frac{dv_{co}}{dt}$	$-\frac{v_o}{RC_o}$	$\frac{i_{L3}}{C_o} - \frac{v_o}{RC_o}$

A. STATE-SPACE SMALL SIGNAL MODELING

The state equation of the proposed converter for one complete switching period is given by

$$\dot{x} = d(A_1 x + B_1 u) + \overline{d}(A_0 x + B_0 u). \tag{36}$$

Equation (36) is nonlinear in nature. In a state-space average modeling approach, perturbation and linearization are applied around the steady-state average operating point for getting a linear equation. Hence, the nonlinear equation will split into a steady-state average value and a small signal variable.

$d_1 = D_1 + \widetilde{d_1}$; $\overline{d_1} = \overline{D}_1 - \widetilde{d_1}$; $d_2 = D_2 + \widetilde{d_2}$
$\overline{d}_2 = \overline{D}_2 - \widetilde{d_2}$; $x = X_i + \widetilde{x}$; $\widetilde{d} \ll D$; $\widetilde{x} \ll X_i$. By, applying perturbation and linearization, the small signal state space average linear model of the proposed converter is obtained as

$$\left.\begin{aligned} \dot{\widetilde{x}} &= A\widetilde{x} + B\widetilde{d} \\ \dot{\widetilde{y}} &= C\widetilde{x} \end{aligned}\right\}. \tag{37}$$

$x = [I_{L1}\ \ I_{L2}\ \ I_{L3}\ \ V_{c1}\ \ V_{c2}\ \ V_{co}\ ]^T; y = [I_{L1}\ \ I_{L2}\ \ V_{co}\ ]^T$, A is the average system matrix, B is the average input matrix, and C is the average output matrix

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{-\overline{D}_1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{D_1}{L_2} & \frac{-\overline{D}_2}{L_2} & \frac{-\overline{D}_2}{L_2} \\ 0 & 0 & 0 & \frac{D_1}{L_3} & \frac{(1+D_2)}{L_3} & \frac{-\overline{D}_2}{L_3} \\ \frac{\overline{D}_1}{C_1} & \frac{-D_2}{C_1} & \frac{-\overline{D}_2}{C_1} & 0 & 0 & 0 \\ 0 & \frac{\overline{D}_2}{C_2} & \frac{-(1+D_2)}{C_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{\overline{D}_2}{C_0} & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix}$$

TABLE II
CURRENT SHARING UNDER EQUAL DUTY CYCLE CONTROL FOR TWO-INPUT OPERATION WITH LOAD CURRENT I_o =1 A

D	I_s=$\frac{(2-(1-D)^2)I_o}{(1-D)^3}$	I_{L1}=$\frac{2I_oD}{(1-D)^3}$	I_{L2}=$\frac{(1+D)I_o}{(1-D)^2}$
0.3	4.402 A	1.74 A (39.52%)	2.65 A (60.47%)
0.4	7.592 A	3.703 A (48.73%)	3.89 A (51.26%)
0.5	14 A	8 A (57.14%)	6 A (42.85%)
0.6	28.75 A	18.75 A (65.21%)	10 A (34.78%)

$$B = \begin{bmatrix} \frac{V_{c1}}{L_1} & 0 \\ \frac{V_{c1}}{L_2} & \frac{V_{c2}}{L_2} \\ \frac{V_{c1}}{L_3} & \frac{V_{c2}+V_{co}}{L_3} \\ \frac{-I_{L1}}{C_1} & \frac{-(I_{L2}+I_{L3})}{C_1} \\ o & \frac{-(I_{L2}+I_{L3})}{C_2} \\ 0 & \frac{-I_{L3}}{C_o} \end{bmatrix}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}; \quad \begin{aligned} \widetilde{x} &= [SI - A]^{-1}\widetilde{d} \\ \widetilde{y} &= [SI - A]^{-1}BC\widetilde{d} \end{aligned}$$

$$y = \begin{bmatrix} \widetilde{i}_{L1} \\ \widetilde{i}_{L2} \\ \widetilde{v}_{co} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \\ G_{31} & G_{32} \end{bmatrix} \begin{bmatrix} \widetilde{d}_1 \\ \widetilde{d}_2 \end{bmatrix}. \tag{38}$$

1) *Unequal Duty Cycle Control*

The unequal duty cycle is a conventional control approach, in which a decoupling method [22] is adopted. It transforms cross-coupled two-loop system into independent single-loop system for each input with two control variable. Hence, the controller complexity is increased.

2) *Proposed Equal Duty Cycle Control*

$$\frac{\widetilde{v_o}}{\widetilde{d}} = G_{31} + G_{32}. \tag{39}$$

In the equal duty cycle, duty cycles of two-input sources are equal $(D_1 = D_2 = D)$. Furthermore, due to semicascaded structure of the proposed converter, the current supplied by the two sources are inherently supplied according to the Table II relation. As a result, a single voltage loop is sufficient to control the proposed converter. Hence, the controller complexity is minimized. However, if required, the proposed converter can also be operated in the current control mode. This will work like a conventional control approach that uses the decoupling

method. It requires current sensors as well as a design of the current control loop along with the voltage loop.

VII. Performance Evaluation

A. Inherent Power Management

The inherent power sharing of the proposed converter can be easily understandable in terms of charge balance of the capacitors. According to the power balance principle, the total source current requirement is given by

$$I_{\text{source}} = \frac{(2-(1-D)^2)I_o}{(1-D)^3} \tag{40}$$

The amount of total source current (I_{source}) shared by each source can be understood by the capacitor charge balance principle. The charge balance of capacitor (C_o) is given by

$$-\int_0^{DT_s} I_o + \int_{DT_s}^{T_s} (I_{L3} - I_o) = 0$$

$$I_{L3} = \frac{I_o}{1-D}. \tag{41}$$

The charge balance of capacitors (C_2) and (C_3) is given by

$$-\int_0^{DT_s} I_{L3} + \int_{DT_s}^{T_s} (I_{L2} - I_{L3}) = 0$$

$$I_{L2} = \frac{I_o(1+D)}{(1-D)^2}. \tag{42}$$

The amount current shared by the source V_2 is given by

$$\frac{I_{L2}}{I_{\text{source}}} = \frac{(42)}{(40)} = \frac{(1+D)(1-D)}{2-(1-D)^2}. \tag{43}$$

Similarly, the charge balance of capacitor (C_1) is given by

$$\int_0^{DT_s} -(I_{L2} + I_{L3}) + \int_{DT_s}^{T_s} (I_{L1}) = 0$$

$$I_{L1} = \frac{2DI_o}{(1-D)^3}. \tag{44}$$

The amount current shared by the source V_1 is given by

$$\frac{I_{L1}}{I_{\text{source}}} = \frac{(44)}{(40)} = \frac{2D}{2-(1-D)^2}. \tag{45}$$

The current sharing between the sources (V_1 and V_2) for the two-input operation is provided in Table II. It is noticed that, at $D = 0.6$, the V_1 source is supplying (65.21%) and V_2 source supplying (34.78%) of the required source current (I_{source}) inherently, without any current control requirement. This current sharing occurs inherently without the need for any specific current control requirements. This is one of the main contributions of the proposed topology. As a result, the control design for the proposed converter is simplified. A single voltage loop control is sufficient to regulate and control the converter's operation. By utilizing a single voltage loop control, the proposed converter can effectively manage the current sharing between the two-input sources (V_1 and V_2) at the specified duty cycle, facilitating easier implementation and control of the system.

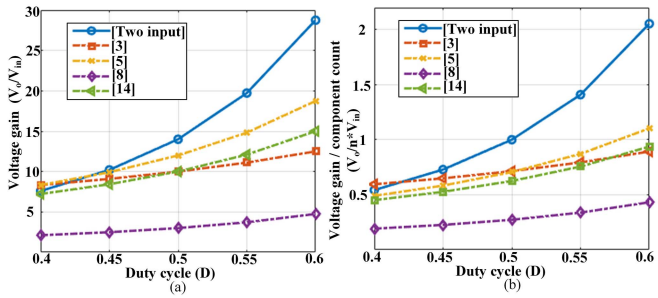

Fig. 9. Comparison of (a) voltage gain and (b) voltage gain per total components count (n) of the proposed converter with reported works.

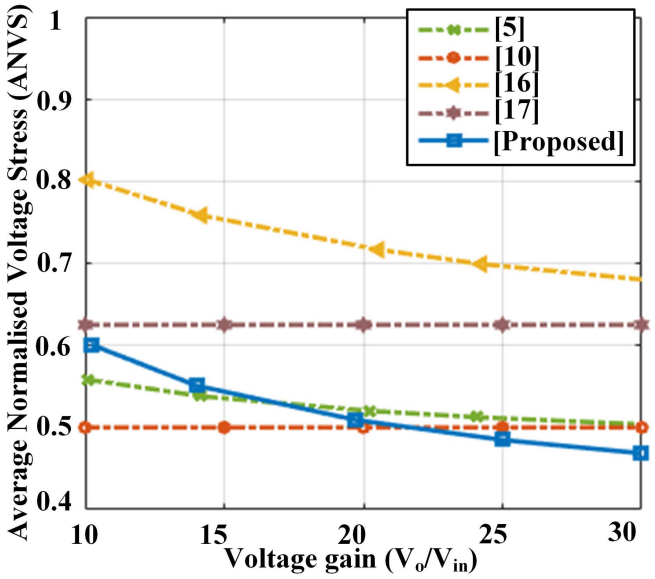

Fig. 10. Comparison of average normalized voltage stress (ANVS) with reported converters.

B. Comparative Analysis With Reported Converters

In order to evaluate the potential capabilities of the proposed converter, a comparative analysis is performed with the reported converters in the literature, as shown in Figs. 9, 10, and Tables III and IV. According to Fig. 9 and Table III, the proposed converter achieved a high voltage gain (28 at $D = 0.6$) with less component count, less cost, and relatively high efficiency than other reported converters in the class of nonisolated integrated boost featured (NIIBF) converters.

In the two-input operation with $D = 0.5$, it is observed that each component of the proposed structure contributes one unit gain, which is almost 45% higher than reported converters, as shown in Fig. 9(b). Furthermore, a comparison is made for average normalized voltage stress (ANVS=($\sum V_{Si}/nV_o$)) for voltage gain of 10–30 times with reported converters, as shown in Fig. 10 and Table IV. It is noticed that the proposed converter has less ANVS than other converters. Consequently, the size and cost of the converter are eventually reduced. This ultrahigh gain is useful for integrating low-voltage renewable

TABLE III
COMPARISON OF PROPOSED CONVERTER WITH OTHER REPORTED CONVERTERS

Interpretations	[Proposed]	[5]	[6]	[7]	[8]	[11]	[17]
Switch* count	7	7	10	9	8	8	8
Inductor count	3	2	4	4	2	2	4
Capacitor count	4	5	5	4	1	2	4
Total count (n)	14	14	19	17	11	12	16
Voltage gain	$\frac{2-(1-d)^2}{(1-d)^3}$	$\frac{5}{1-d}$	$\frac{m}{(1-d)}$	$\frac{3}{(1-d)^2}$	$\frac{[2d_2(1-k)+k(1+d_m)]}{1-d_m}$	$\frac{1+d^2-d}{(1-d)^2}$	$\frac{3-d}{(1-d)^2}$
Cost (USD)	50.22	56.93	60.32	60.56	33.88	38.12	58.32
Efficiency (200 W)	91%	94%	97%	88%	89.5%	86%	88%

* Switch = diode + power switch

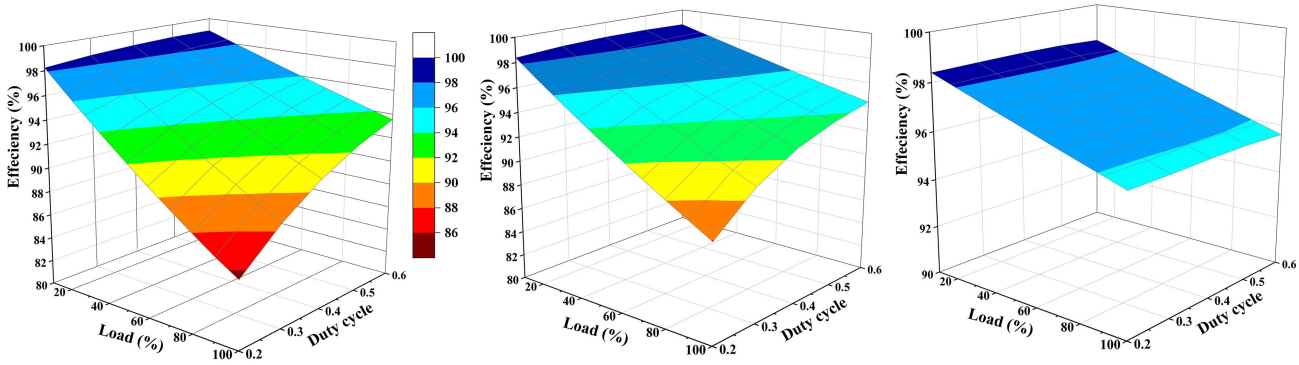

Fig. 11. Analytical efficiency of the proposed converter with load and duty cycle variations for (a) single-input, (b two-input, and (c) three-input operation.

TABLE IV
COMPARISON OF AVERAGE NORMALIZED VOLTAGE STRESS WITH REPORTED CONVERTERS

Reference	Total Voltage stress $V_{TS} = \sum V_{si}$	ANVS $\text{ANVS} = \frac{V_{TS}}{nV_o}$
[5]	$\frac{14-5D}{(1-D)^2}$	$\frac{14-5D}{21}$
[10]	$\frac{4}{1-D}$	0.5
[16]	$\frac{4-2D}{(1-D)^2}$	$\frac{2-D}{2(1+D^2-D)}$
[17]	$\frac{5}{1-D}$	0.625
[Proposed]	$\frac{11-10D+3D^2}{(1-D)^3}$	$\frac{11-10D+3D^2}{7(2-(1-D)^2)}$

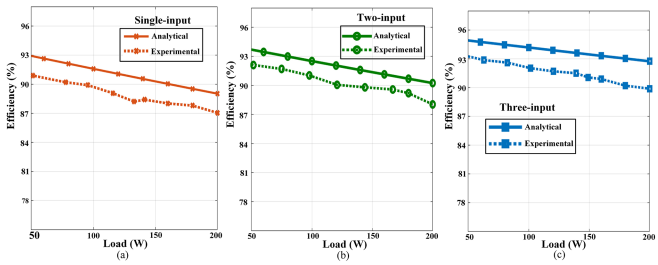

Fig. 12. Comparison of analytical and experimental efficiency of the proposed converter for (a) single-input, (b) two-input, and (c) three-input operation.

energy resources and hybrid energy storage systems. Furthermore, common ground and continuous input current features are applicable for PV integration. The analytical efficiency curves of the proposed converter with load and duty cycle variation are depicted in Fig. 11. It is noticed that the proposed converter has higher efficiency at higher duty cycle and load conditions for all types of inputs. Comparatively, the single-input mode of operation has less efficiency due to the conduction of the switch (S_1) for DT_s switching period, which causes increased conduction losses. The three-input operation has high efficiency because of the absence of a switch (S_4) throughout the operation. The efficiency of the two-input operation lies in between single-input and three-input operations. The experimental plots of efficiency curves at duty cycle (D) = 0.45 conditions are compared with the analytical efficiency, as shown in Fig. 12 . There is a 2%–4% deviation obtained in the efficiency plots due to approximated analytical calculations and the additional circuitry conduction losses in the developed hardware setup.

VIII. EXPERIMENTAL VALIDATION

The functional capabilities of the proposed converter have been evaluated by using a 200-W hardware prototype, as shown in Fig. 13. The rated input voltage of programmable sources is considered 12 V. Furthermore, inductors L_1, L_2, and L_3 are selected to limit the current ripple to less than 20% of the rated input current. The selection of rating of all switches is made by using their respective voltage and current stress expressions

TABLE V
EXPERIMENTAL VALIDATION OF AVERAGE NORMALIZED VOLTAGE STRESS (ANVS) OF THE PROPOSED CONVERTER WITH TWO-INPUT ($V_1 = V_2 = 12$ V)

D	V_o	V_{S1}	V_{S2}	V_{S3}	$V_{S'1}$	$V_{S'3}$	$V_{S'2}$ and V_{S4}	ANVS
0.3	47V	V_{S1} 14V	V_{S2} 20V	V_{S3} 45V	$V_{S'1}$ 14V	$V_{S'3}$ 80V	$V_{S'2}$ V_{S4} 35V	= 0.771
0.5	140V	V_{S1} 20V	V_{S2} 46V	V_{S3} 138V	$V_{S'1}$ 20V	$V_{S'3}$ 190V	$V_{S'2}$ V_{S4} 55V	= 0.542
0.6	275V	V_{S1} 25V	V_{S2} 52V	V_{S3} 270V	$V_{S'1}$ 24V	$V_{S'3}$ 351V	$V_{S'2}$ V_{S4} 82V	= 0.468

* Output voltage gain (M) = 3.75, 11.5, and 22.5 at D = 0.3, 0.5, and 0.6, respectively.

The bold values described in Section-VIII, subsection-A. They are required to calculate the experimental ANVS. So that the claimed low ANVS can be experimentally validated.

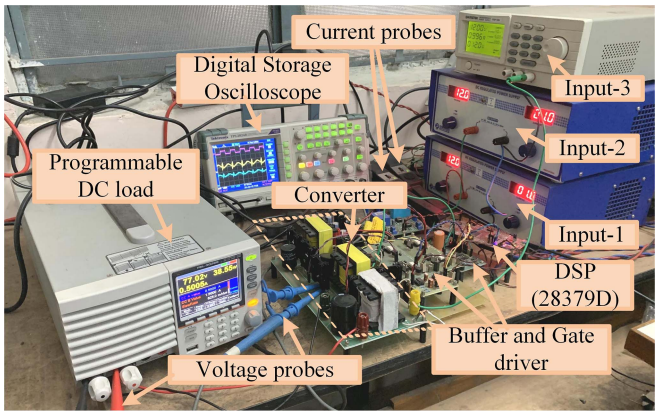

Fig. 13. Hardware setup of the proposed converter.

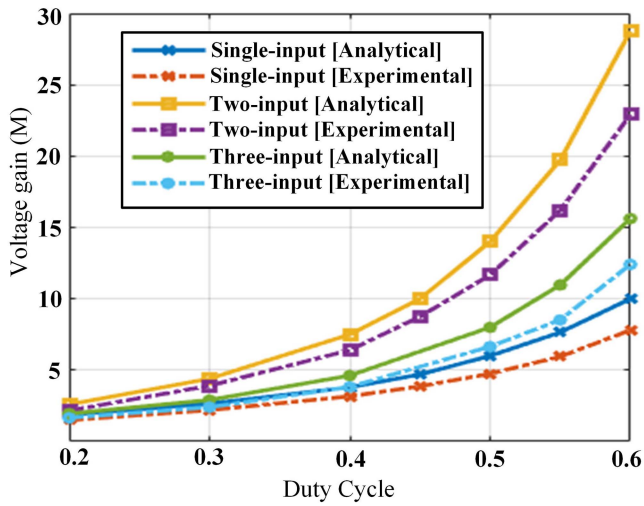

Fig. 14. Comparison of ideal and experimental voltage gain of the proposed converter for different input operations.

(17)–(31). In this section, the experimental validation of various functionalities of the proposed converter is evaluated.

A. Average Normalized Voltage Stress

The experimental validation of ANVS of the proposed converter with the two-input operation is shown in Table V. The analytical AVNS for $D = 0.3$, 0.5, and 0.6 are 0.782, 0.551, and 0.472, respectively. The obtained experimental AVNS for $D = 0.3$, 0.5, and 0.6 are 0.771, 0.542, and 0.468, respectively, which are very close to the analytical values. It is noticed that, nominally, each switch of the proposed converter has less than 50% of the output voltage stress at high voltage gain or at an operating duty cycle (D) of more than 0.5.

B. Output Voltage Gain (M)

The ultrahigh voltage gain capability of the proposed converter is validated with the experimental voltage gain values depicted in Fig. 14. The obtained experimental curves follow the analytical curves. However, there is an increased deviation between analytical and experimental gain curves due to voltage drop across the internal resistance of inductors and additional voltage drop in the developed hardware setup.

C. Steady-State and Dynamic Operation

The designed parameters and selected circuit components for the steady-state and dynamic operation of the proposed converter are listed in Table VI. The control strategy for a proposed dual-input converter is designed with equal duty cycle control ($D_1 = D_2 = D_3$)-based single voltage loop PI compensator ($P = 0.006$, $I = 1$) with the antiwindup feature, as shown in Fig. 15. The functional capabilities of the proposed converter are evaluated at 12 V input and 100 V output for single-, two-, and three-input operations under both open-loop and closed-loop working conditions. The obtained hardware results are classified into various scenarios and they are provided in the following subsequent section.

TABLE VI
PROPOSED CONVERTER PARAMETERS

Parameter	Value/Model number
Input (V_1, V_2, V_3)	12V
Switching frequency (f_{sw})	50kHz
Switch (S_1,S_1',S_2,S_2',S_3)	IRFB4227PbF
Switch (S_3',S_4)	IRFP21N60LPbF
Inductor (L_1, L_2, L_3)	0.25mH, 0.42mH, 1.1mH
Capacitor (C_1, C_2, C_3, C_o)	22 μF, 56 μF, 56μF, 220 μF

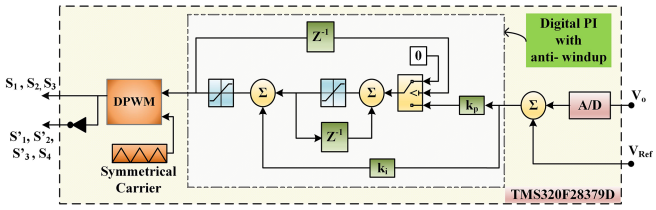

Fig. 15. Equal duty cycle control with single-loop control strategy of the proposed converter.

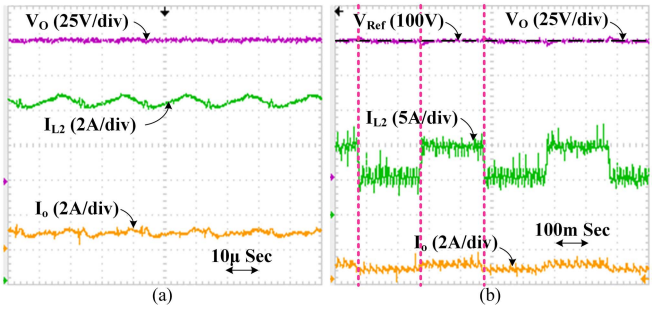

Fig. 16. Experimental results of single-input operation for (a) open-loop steady-state condition and (b) closed loop under dynamic step load condition ($V_1 = 12\,V$).

a) Single-input source operation ($V_1 = 0\,V$, $V_2 = 12\,V$, $V_3 = 0\,V$): The experimental results for single-input voltage (V_2 = 12 V) and equal duty cycle (0.62 for S_2 and S_3) are depicted in Fig. 16. The currents flowing through inductor L_2 and load are labeled as I_{L2} and I_o. In the open-loop case, single-input achieved 100 V output voltage with a duty ratio of 0.62 at 0.8 A load current (I_o), as shown in Fig. 16(a). Furthermore, in the closed-loop case, an output voltage (V_o) of 100 V is maintained for a given input voltage (12 V) under a dynamic step load condition (0.5–1 A), as shown in Fig. 16(b). It is observed that, during load current transition, the output voltage has 4% overshoot and undershoot with a single-input source condition.

b) Two-input source operation ($V_1 = 12\,V, V_2 = 12\,V, V_3 = 0\,V$): The two-input source ($V_1 = V_2 = 12$ V) working of the proposed converter is evaluated with equal duty cycle control, as shown in Fig. 17. The current flowing through inductor L_1 is labeled as I_{L1}. The output voltage of 100 V is obtained with a 0.42 duty cycle at a 0.8 A load current under an open-loop condition, as shown in Fig. 17(a). As listed in Table II, under

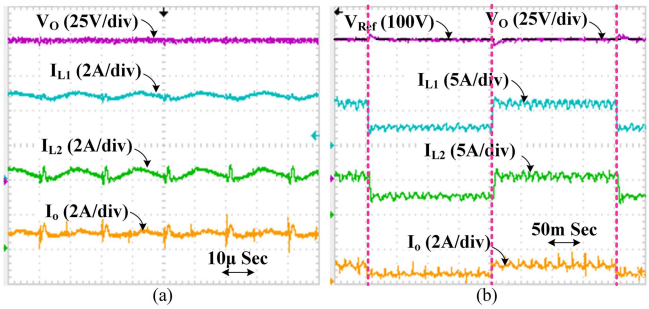

Fig. 17. Experimental results of the two-input operation for (a) open-loop steady-state condition and (b) closed loop under dynamic step load condition with equal duty cycle control ($D_1 = D_2$) and equal input ($V_1 = V_2 = 12$ V).

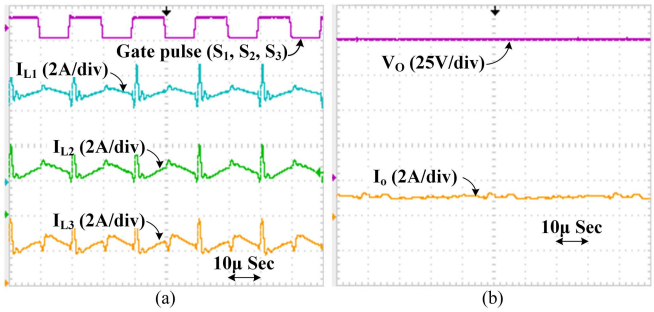

Fig. 18. Experimental results for a steady-state open-loop condition for three-input modes of operation ($V_1 = V_2 = V_3 = 12$ V).

equal duty cycle control, source V_1 is supplying 53%, and source V_2 is supplying 47% of the total input current requirement. Therefore, if the converter is designed at a desired current ratio, the requirement of the inner current loop is minimized, which reduces the controller complexity. Fig. 17(b), describes the two-input closed-loop operation of the proposed converter under a dynamic step load (0.5–1 A) condition. It is noticed that the proposed converter achieved 100 V output voltage with nominal voltage overshoot (4%) and undershoot (4%).

c) Three-input source operation ($V_1 = 12\,V$, $V_2 = 12\,V$, $V_3 = 12\,V$): Three-input mode of operation is depicted in Fig. 18. The current flowing through inductor L_3 is labeled as I_{L3}. The 100 V output is obtained with a 0.53 duty cycle. The dynamic step load condition is shown in Fig. 19. It is noticed that the proposed converter has nominal voltage overshoot (5%) and undershoot (5%) in maintaining 100 V output with three inputs under step load variation (0.5–1 A). Hence, the proposed converter has good transient performance during dynamic load conditions.

d) Energy transfer between the input sources (V_2 charging with V_3 source operation. $V_3 = 24\,V$): It is a special operating mode of the proposed converter, in which the energy between the sources is able to transfer/exchange (from source V_3 to V_2). Its steady-state operating waveforms are depicted in Fig. 20. In this mode, the proposed converter works in the buck-stage operation using the switch S_2. With a 0.53 duty cycle, 24 V of V_3 source input is stepped down to 12 V at the battery ports with

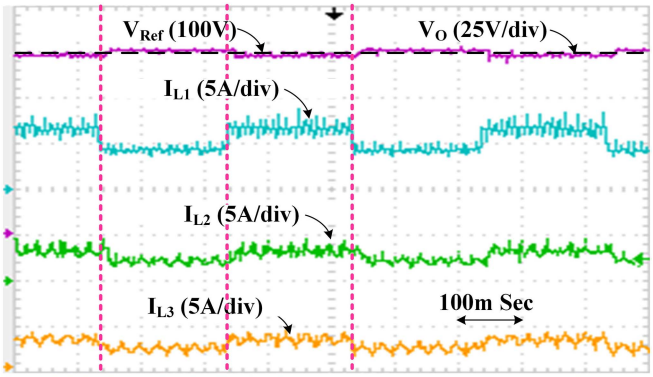

Fig. 19. Experimental results for dynamic step load condition for a three-input mode of operation with equal duty cycle control ($D_1 = D_2 = D_3$) and equal input ($V_1 = V_2 = V_3 = 12$ V).

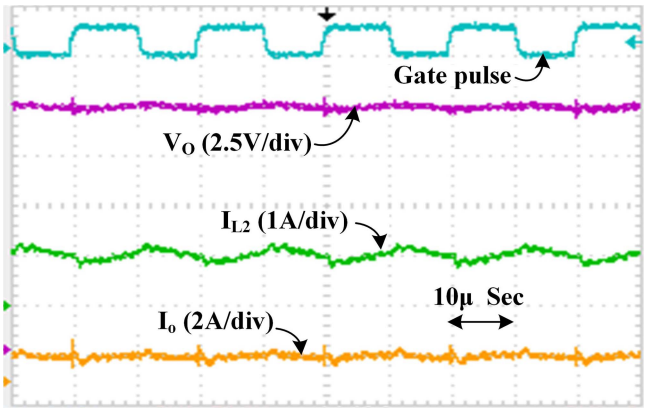

Fig. 20. Experimental results for steady-state operation of energy transfer between the input sources ($V_3 = 24$ V).

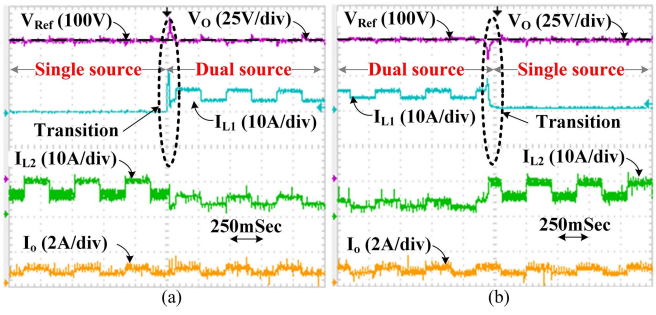

Fig. 21. Experimental results for (a) single-source to dual-source and (b) dual-source to single-source transition operation under dynamic step load with equal duty cycle control ($D_1 = D_2$) and equal input ($V_1 = V_2 = 12$ V).

a load current of 1 A. Therefore, it is validated that the proposed structure is capable of transferring energy between the sources.

e) Input source transition operation: The source transition capability of the proposed converter is evaluated with equal duty cycle control under dynamic load step conditions (0.5–1 A), as shown in Fig. 21. It is noticed that the proposed converter has voltage overshoot (15%) and undershoot (12%) in a single-source to dual-source and dual-source to single-source transition conditions, respectively. Therefore, it is evident that the proposed converter has good transient performance during source transition or change in the mode of operating conditions.

Finally, from the experimental validation and comparative analysis, it is evident that the proposed converter has well-suitable performance characteristics for integrating renewable energy resources and energy storage systems.

IX. Conclusion

In this work, a multi-input nonisolated dc–dc converter with three basic boost cells is proposed, without using a coupled inductor or voltage-boosting techniques (switched capacitor/inductor). From the performance evaluation and hardware results, it is validated that the proposed structure has unique features such as ultrahigh gain, low ANVS, and inherent power management. In the two-input operation with D=0.5, it is observed that each component contributes one unit gain, which is almost 45% higher than reported converters in the literature. Furthermore, because of inherent power management, the current loop (also current sensors) requirement is eliminated. As a result, the integration and control of different energy storage systems are simplified. Finally, experimental results for both open-loop and closed-loop control validate the claimed functionalities of the proposed converter.

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Obulapathi Balapanuru (Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from the Rajeev Gandhi Memorial College of Engineering, Nandyal, India, in 2014, and the M.Tech. degree in electrical power system from the JNTUA College of Engineering, Pulivendula, India, in 2018. He has been working toward the Ph.D. degree in analysis and design of high gain isolated and non-isolated dc-dc converters for hybrid energy storage integration with the Visvesvaraya National Institute of Technology (VNIT), Nagpur, India, since 2019.

Since 2018 to 2019, he was a Junior Research Fellow with Electrical Engineering Department, VNIT. His current research interests include electric vehicles, energy storage systems, digital control, multiport dc–dc converters, and power electronics.

Makarand M. Lokhande (Senior Member, IEEE) received the Bachelor of Engineering degree in electrical and electronics engineering from the G.H. Raisoni College of Engineering, Nagpur University, Nagpur, India, in 2001, the Master of Engineering degree in power system from the University of Pune, Pune, India, in 2003, and the Ph.D. degree in power electronics from Energy Science and Engineering Department, Indian Institute of Technology Bombay, Mumbai, India, in 2010.

From 2009 to 2013, he was with Pandit Deendayal Petroleum University Gandhinagar, Gujarat, India. From 2013 to 2015, he was with Electrical Engineering Department, Sardar Vallabhbhai National Institute of Technology, Surat, India, and since 2015, he has been with the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur where he is currently an Associate Professor. His research interests include electric vehicles, solar photovoltaic, microgrids, power electronics, and electrical machines.

Mohan V. Aware (Senior Member, IEEE) received the B.E. degree in electrical engineering from the College of Engineering, Amravati, India, in 1980, and the M.Tech. degree in power apparatus and system from IIT Bombay, Mumbai, India, in 1982.

From 1982 to 1989, he was a Design Officer with Crompton Greaves, Ltd., Nasik, India. From 1989 to 1991, he was a Development Engineer with Nippon Denro Ispat, Ltd., Nagpur. From 2001 to 2002, he was a Research Fellow with Electrical Engineering Department, Hong Kong Polytechnic University, Hong Kong, China. He is currently a Professor with the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur. He has authored and coauthored more than 200 technical papers in different journals and conference proceedings. His current research interests include multiphase electrical drives, distributed generation, energy storage systems, and power electronics.

Dr. Aware is a Commonwealth Academic Fellow.