Letters

New Gate Control Method of PWM Resonant Converters for Near-Zero-Ripple Fuel Cell Current

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***Abstract*—Various recent research has focused on reducing input current ripple to ease the life span and heat issue of fuel cells. Among various topologies, pulsewidth modulation resonant (PWMR) converters have become promising candidates for fuel cell dc–dc converters, and numerous prior studies have been conducted. However, they still either suffer from input current ripple or complex control and implementation. In this letter, a new gate control method for PWMR converters is proposed. The proposed method not only achieves the near-zero-ripple input current but also can improve power conversion efficiency by reducing the turn-ON switching loss of synchronous rectifiers. The proposed gate control method was verified through 600 W PWMR prototype converters**

***Index Terms*—Fuel cells, gate control method, low input current ripple, pulse width modulation converters, resonant converters.**

I. Introduction

ENVIRONMENTAL pollution and the depletion of fossil fuels have caused a significant interest in renewable energy sources such as photovoltaics, wind energy, and fuel cells. Among them, the fuel cell is gaining interest due to its space-effective, and high energy density characteristics. Fuel cells have been adopted as a new energy source and utilized in various applications, such as fuel cell electric vehicles, dc microgrids, and uninterruptible power supply [1]. Despite superior characteristics, fuel cells suffer from lifespan and heat issues depending on an input current ripple [2]. Moreover, the output voltage of the fuel cell is low, inconstant, and unstable. Therefore, a dc–dc converter is necessary for low input current ripple and stable output voltage.

Various dc–dc converter topologies for fuel cells have been suggested [3], [4], [5], [6], [7], [9], [10]. They mainly focus on high step-up voltage gain and low input current ripple to ease the drawbacks of fuel cells. Most of them are based on the boost converter due to its high step-up voltage gain and continuous input current. Interleaved boost integrated pulsewidth modulation resonant (IBI-PWMR) converter and current-fed push–pull integrated PWMR (CFPPI-PWMR) converter have been proposed in [4] and [5]. Wide voltage gain range and low input current ripple can be achieved, but as the operating point moves from the optimal, input current ripple increases significantly [6].

To achieve near-zero-ripple (NZR) input current, a synchronous rectifier (SR) modulation method (now referred to as conventional control method), which can be applied to both IBI-PWMR and CFPPI-PWMR converter has been proposed in [6]. Primary-side switches operate with a fixed ($0.5 - T_d/T_s$) duty ratio (considering two dead times in one switching period), and the SR duty ratio (D_{sec}) regulates the output. T_d and T_s are the dead time and the switching period, respectively, which are determined at the converters' design stage. The fixed ($0.5 - T_d/T_s$) duty ratio of primary-side switches seems to minimize the input current ripple even up to NZR level. However, the input current ripple remains due to the unsynchronized drain-source voltage (V_{DS}) transition of primary-side switches during dead time. [7].

To overcome the limitation, Lee et al. [7] suggested a CFPPI-PWMR converter with an SR current rebuild-up control. By utilizing additional control variable (D_{BW}), all the primary-side switches achieve zero-voltage-switching (ZVS). Thereby, synchronized V_{DS} results in NZR input current. Determining optimal rebuild-up current (I_{ZVS}) is a key factor in [7]. Without the optimal I_{ZVS}, additional loss or the input current ripple may increase. However, the calculation and realization of the optimal I_{ZVS} requires additional sensing circuits or a look-up table (LUT), which increases overall costs, and complexity of implementation. Moreover, turning on each SR twice in a switching period results in an additional gate driving loss and turn-ON switching loss. Control complexity and additional SR turn-ON for D_{BW} further limits the versatility of [7]. Thereby, Lee et al. [7] may not be a practical solution due to the mentioned drawbacks.

This letter proposes a simple gate control method for PWMR converters that can achieve NZR input current without additional

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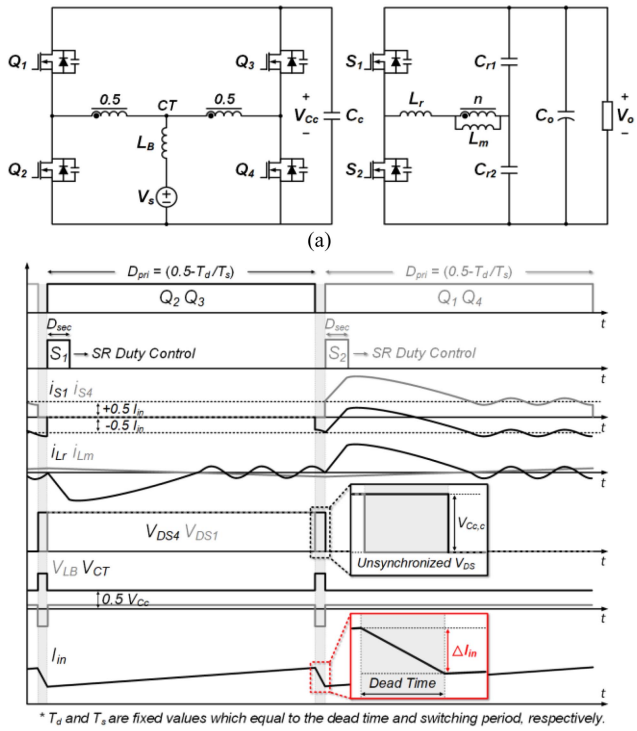


Fig. 1. CFPPI-PMWR converter. (a) Circuit diagram. (b) Key waveforms with the conventional control in [6].

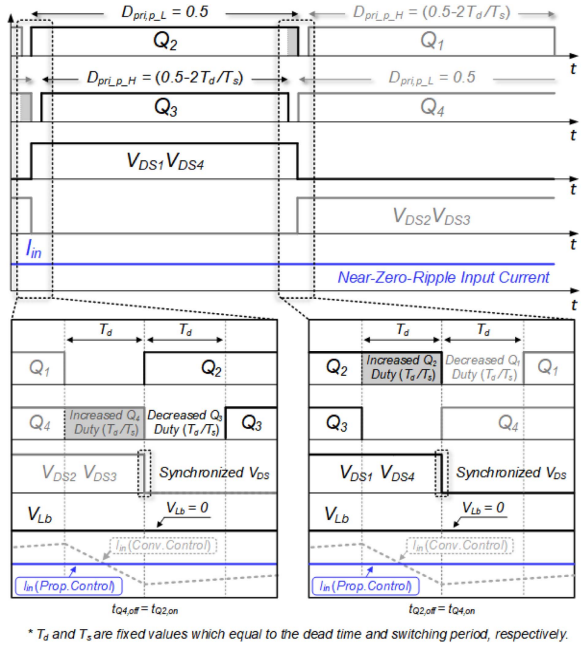


Fig. 2. Key waveforms of the proposed gate control method.

sensing circuits, calculations, or LUT in various structures, including CFPPI and IBI-PWMR converters. Only the fixed duty ratio of the primary-side switches is changed compared to [6]. Furthermore, by removing the steep voltage charging period of synchronous rectifiers (SRs) during dead time, the turn-ON voltage of SRs can be reduced with the proposed method. Therefore, the proposed gate control method can be a simple and practical solution to achieve NZR input current and improved efficiency in the PWMR converters.

II. Proposed Gate Control Method

A. Input Current Ripple in Conventional Control Method

Both CFPPI-PWMR converter and IBI-PWMR converter with the conventional control method [6] suffer from an input current ripple. Since the operation of both structures is similar, only the CFPPI-PWMR converter is analyzed in this letter for simplicity.

Fig. 1 shows the CFPPI-PWMR converter and its key waveform under the conventional control method. Primary-side switches operate with a fixed $(0.5 - T_d/T_s)$ duty ratio, and the SR duty ratio (D_{sec}) regulates the output power. Disregarding the dead time (T_d) and switching characteristics, the voltage across the clamping capacitor $(V_{Cc,c})$ equals twice the input voltage $(2V_s)$. Assuming an ideal center-tap transformer, the voltage on CT node always equals the input voltage (V_s). Therefore, zero voltage on the boost inductor leads to a zero-input current ripple. In actual case, the dead time between the switches in the same leg should be guaranteed to prevent shoot-through. Unsynchronized V_{DS} transition occurs due to the different switching characteristics of the primary-side switches during this dead time

$$V_{Cc,c} = \frac{V_S}{0.5 + (T_d/T_s)} \tag{1}$$

$$\Delta I_{in} = (V_{Cc,c} - V_S) \cdot T_d / L_B. \tag{2}$$

In the boost-integrated structures, not only the powering current but also the input current flows through the primary-side switches. For the CFPPI-PWMR converter, the input current is distributed at the CT node and flows through the switches, resulting in a negative bias current ($-0.5I_{in}$) on the high-side switches (Q_1, Q_3) and a positive bias ($+0.5I_{in}$) current on the low-side switches (Q_2, Q_4). To achieve ZVS, a negative current must be present before the switch turns ON. Due to the different polarity of the bias currents, only the high-side switches achieve ZVS, and the low-side switches turn ON with hard-switching. Thereby, during the dead time, the V_{ds} of the high side switch is 0, and the V_{ds} of the low side switch is $V_{Cc,c}$, as shown in Fig. 1(b).

Regarding the different switching characteristics during dead time, $V_{Cc,c}$ can be obtained by applying a volt-second balance equation on L_B. As in (1), $V_{Cc,c}$ is lower than $2V_S$ due to the unsynchronized V_{DS} during the dead time. Since $V_{Cc,c}$ does not equal to $2V_s$, nonzero voltage is applied to the boost inductor during the switching period, which leads to an input current ripple ($\triangle I_{in}$), as in (2).

B. Proposed Gate Control Method

Key waveforms of the proposed gate control method are shown in Fig. 2. The proposed method regulates the output using the same SR modulation in [6] and only modifies the fixed duty

TABLE I
COMPARISON OF CONVENTIONAL AND PROPOSED GATE CONTROL METHOD

	Conv. Method [6]	Prop. Method
Fixed duty Ratio of Q_2, Q_4	$0.5 - T_d/T_s$	0.5
Fixed duty Ratio of Q_1, Q_3	$0.5 - T_d/T_s$	$0.5 - 2T_d/T_s$
Gate Signal Synchronization	$t_{Q2,on(off)} = t_{Q3,on(off)}$ $t_{Q1,on(off)} = t_{Q4,on(off)}$	$t_{Q2,on} = t_{Q4,off}$ $t_{Q2,off} = t_{Q4,on}$
Output Regulation	SR duty (D_{sec}) modulation in [6]	

* T_d and T_s are fixed values which equals to the dead time and switching period, respectively.

ratio of the primary-side switches to achieve NZR input current. The gate signals of the low-side switches (Q_2, Q_4) are extended by T_d, and gate signals of the high-side switches (Q_1, Q_3) are decreased by T_d, as shown in Fig. 2. Thereby, the fixed duty ratio of the high-side switches and the low-side switches is (0.5-$2T_d/T_s$) and 0.5, respectively. Since the T_d and T_s are determined at the converters' design stage, the duty ratio of the primary-side switches is fixed to a constant value and does not vary upon entire operating conditions. For example, if the switching frequency (f_s) and the dead time (T_d) is selected as 50 kHz and $200n$ s, respectively, the duty ratio of the high-side switches is fixed to 0.48 and the low-side switches is fixed to 0.5. Turn-ON of the Q_2 gate signal ($t_{Q2,\mathrm{ON}}$) is synchronized with the turn-OFF of the Q_4 gate signal ($t_{Q4,\mathrm{OFF}}$) and turn-OFF of the Q_2 gate signal ($t_{Q2,\mathrm{OFF}}$) is synchronized with the turn-ON of the Q_4 gate signal ($t_{Q4,\mathrm{ON}}$). Through the proposed gate control of the primary-side switches, the V_{DS} transition of the primary-side switch is synchronized, as shown in Fig. 2. The clamping capacitor voltage of the proposed method ($V_{Cc,p}$) is as (3) due to the synchronized V_{DS} voltage. Since $V_{Cc,p}$ equals $2V_s$, zero voltage is applied on the boost inductor during the entire switching period, and results in a zero-input current ripple. Comparison between conventional and proposed control methods are summarized in Table I

$$V_{Cc,p} = 2 \cdot V_s \tag{3}$$

$$D_{\mathrm{sec}} = \frac{\cos^{-1}\left(\frac{4nV_{Cc}\cdot(0.5V_{\mathrm{out}}+\Delta V_{Cr})+V_{\mathrm{out}}^2}{2\cdot(nV_{Cc}+0.5V_{\mathrm{out}}+\Delta V_{Cr})\cdot V_{\mathrm{out}}}\right)}{\omega_{r1}\cdot T_s} \tag{4}$$

$$\Delta V_{Cr} = P_{\mathrm{out}} \cdot T_s/(8nV_{Cc} \cdot C_r) \tag{5}$$

$$\omega_{r1} = 1\Big/\sqrt{L_r \cdot 2C_r}. \tag{6}$$

C. Voltage Gain Analysis of the Proposed Control Method

The operation of the CFPPI-PWMR converter with the conventional [6] and the proposed control method is mainly divided into build-up mode and powering mode. In the build-up mode, the voltage of the clamping capacitor (V_{Cc}) and the resonant capacitor build up the resonant inductor current. In the powering mode, power is transferred to the output through the resonance of L_r, C_{r1}, and C_{r2}.

The clamping capacitor voltage (V_{Cc}) of the conventional control method ($V_{Cc,c}$) is as (1). Due to the unsynchronized V_{DS}, $V_{Cc,c}$ is lower than 2 V_s even if the primary-side switches operate with a 0.5 duty ratio. Meanwhile, the V_{Cc} of the proposed method ($V_{Cc,p}$) is as (3), due to the synchronized V_{DS}. Increased voltage in build-up mode will result in increased voltage gain ($M = V_{\mathrm{out}}/V_s$). The SR duty ratio of the conventional method ($D_{sec,c1}$) and the proposed method ($D_{sec,p}$) can be calculated by substituting $V_{Cc,c}$, and $V_{Cc,p}$ to V_{Cc} in (4) and (5), respectively. $\triangle V_{Cr}$ is the maximum deviation of the resonant capacitor voltage (V_{Cr}) with respect to the 0.5 $\mathrm{V_{out}}$.

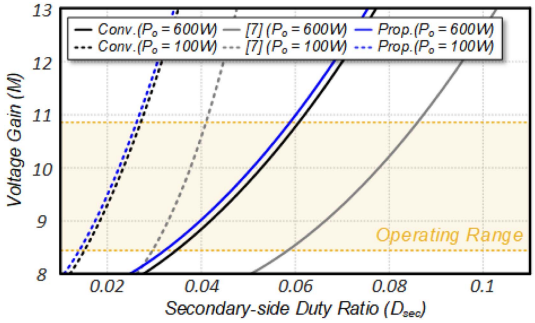


Fig. 3. Voltage gain comparison of the proposed control method.

Fig. 3 shows the voltage gain (M) according to the SR duty ratio of the conventional method ($D_{sec,c1}$), the proposed method ($D_{sec,p}$), and the control method in [7] ($D_{sec,c2}$) under various load conditions ($P_{\mathrm{out}} = 100$ W and $P_{\mathrm{out}} = 600$ W). As shown in the figure, the proposed method has the smallest D_{sec} under the same voltage gain, and the control method in [7] has the largest D_{sec}. The maximum duration of the powering mode in [7] is limited due to the wide duty ratio ($D_{sec,c2}$) range and the additional back-ward duty ratio (D_{BW}). Since the duration of the powering mode mainly depends on the resonant parameters, the limited duration of the powering mode might limit or complex the resonant parameter design. Meanwhile, the narrow duty ratio range of the proposed method, does not affect the resonant parameter design. Thus, the proposed method can be simply applied to the various PWMR converters without the design modifications.

D. Synchronous Rectifier Turn-On Voltage Comparison

Fig. 4 shows the key waveform of the proposed method for SR turn-ON voltage analysis. CFPPI-PWMR converter operates symmetrically under both conventional and proposed control methods. Since both methods operate almost the same during build-up and powering period, minor differences are neglected for simplicity. Thereby, only the drain to source voltage of S_2 ($V_{DS,S2}$) is analyzed during two modes for turn-ON voltage comparison.

Mode 1 [t_a - t_b]: Mode 1 starts after the powering period. The conventional and proposed method can be simplified to an equivalent series LC resonant circuit. As in Fig. 5(a), it consists of an equivalent voltage source ($V_{res,ref1}$), resonant inductor (L_r), and equivalent capacitance ($2C_{oss,\mathrm{SR}}$), which resonates with a resonant frequency of w_{r2}. $C_{oss,\mathrm{SR}}$ is the output capacitance of SRs. The damping effect of parasitic resistance is neglected for simplicity. In the series LC resonant circuit with a dc voltage source, the voltage across the capacitor resonates sinusoidally with respect to the dc source voltage. Thereby, $V_{DS,S2}$ resonates

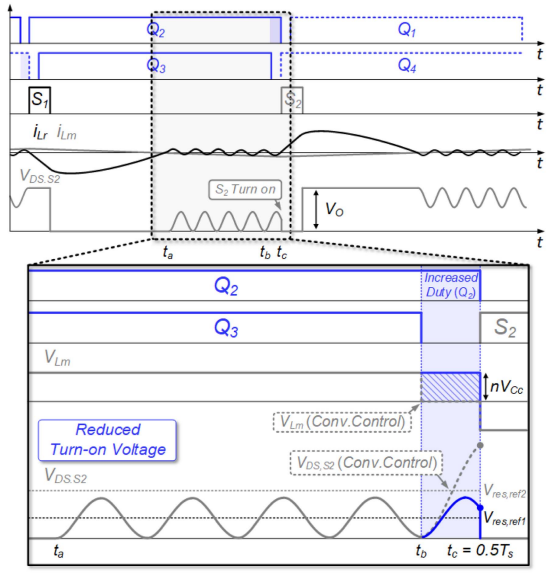


Fig. 4. Key waveforms of proposed control for SR turn-ON voltage comparison.

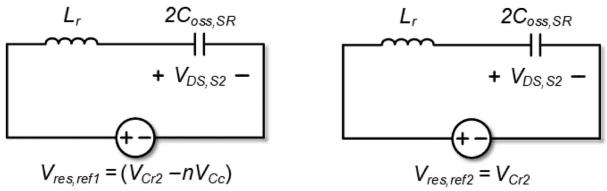


Fig. 5. Equivalent resonant of the operation modes. (a) Conventional control: mode 1, proposed control: mode 1 and mode 2. (b) Conventional control: mode 2.

sinusoidally with respect to the reference dc voltage ($V_{res,ref1}$). The voltage across the SR in the conventional method ($V_{DS,S2,C}$) and the proposed method ($V_{DS,S2,P}$) during mode 1 is as

$$V_{DS,S2,C}(t) = \begin{cases} V_{res,ref1} \cdot (1 - \cos(\omega_r(t - t_a))) \cdots (t_a \le t \le t_b) \\ V_{res,ref2} - (V_{res,ref2} - V_{DS,S2}(t_b)) \\ \cdot \cos(\omega_r t) \cdots (t_b \le t \le 0.5T_s) \end{cases}$$

$$V_{DS,S2,\mathrm{P}}(t) = V_{res,ref1} \cdot (1 - \cos(\omega_r(t - t_a))) \cdots (t_a \le t \le 0.5T_s) \quad (7)$$

$$V_{res,ref1} = V_{Cr2}(0.5T_s - D_{\mathrm{sec}}T_s - T_p - T_d) - nV_{Cc} \quad (8)$$

$$V_{res,ref2} = V_{Cr2}(t_b) = V_{Cr2}(0.5T_s - T_d) \quad (9)$$

$$\omega_{r2} = 1 \Big/ \sqrt{L_r \cdot 2C_{oss,\mathrm{SR}}} \quad (10)$$

$$T_p = \sin^{-1} \times \left(\frac{\sqrt{(\Delta V_{Cr} + V_{\mathrm{out}}) \cdot (\Delta V_{Cr} V_{\mathrm{out}} - 4n^2 V_{Cc}^2 \Delta V_{Cr})}}{V_{\mathrm{out}} \cdot (-nV_{Cc} + 0.5V_{\mathrm{out}} + \Delta V_{Cr})} \right) \Big/ \omega_r \quad (11)$$

$$V_{\mathrm{on},Conv} = V_{DS,S2,C}(0.5T_s) \quad (12)$$

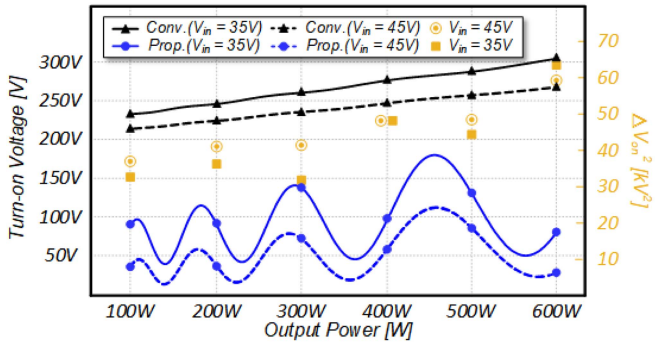


Fig. 6. SR turn-ON voltage comparison of the conventional [6] and the proposed control method under various conditions. (Deadtime = 200 ns).

$$V_{\mathrm{on},Prop} = V_{DS,S2,\mathrm{P}}(0.5T_s) \quad (13)$$

$$\Delta V_{\mathrm{on}}^2 = V_{\mathrm{on},Conv}^2 - V_{\mathrm{on},Prop}^2. \quad (14)$$

Mode 2 [$t_b - 0.5T_s$]: Mode 2 starts after Q_3 turns OFF. The equivalent resonant circuit of the conventional and proposed method differs at mode 2. Fig. 5(b) shows the equivalent resonant circuit of the conventional method during mode 2. Series *LC* resonance occurs between L_r and $2C_{oss,\mathrm{SR}}$ as in mode 1, but the equivalent voltage source ($V_{res,ref2}$) differs in the conventional method. When mode 2 starts, due to unsynchronized V_{DS} transition, as mentioned in Section II-A, the voltage across the magnetizing inductor (V_{Lm}) changes from nV_{Cc} to 0 and increases the equivalent voltage source from ($V_{cr2} - \mathrm{n}V_{Cc}$) to V_{cr2}. Thereby, $V_{DS,S2}$ resonates with respect to higher dc reference voltage ($V_{res,ref2}$). As a result, $V_{DS,S2}$ charge steeply during mode 2 in the conventional method. Steep voltage charging before the turn-ON results in an excessive SR turn-ON voltage. Meanwhile, for the proposed method, the extended turn-ON time of Q_2 maintains V_{Lm} to be clamped to nV_{Cc}. The dc reference voltage of the sinusoidal reference ($V_{res,ref1}$) is maintained the same as in mode 1. Thereby, an equivalent resonant circuit of the proposed method is equal to that of mode 1, and resonance from mode 1 continues in mode 2. $V_{DS,S2,C}$ and $V_{DS,S2,P}$ during mode 2 is as (7). The turn-ON voltage of the conventional ($V_{\mathrm{ON},Conv,}$) and proposed methods ($V_{\mathrm{ON},Prop,}$) is as (12) and (13), respectively.

The main principle of the SR turn-ON voltage reduction feature in the proposed method is based on maintaining the equivalent dc voltage source ($V_{res,ref}$) in the series *LC* resonant circuit to a low value. Thereby, the voltage across the SR resonates sinusoidally with respect to the smaller dc reference voltage. In the proposed method, equivalent voltage source is maintained to the low value through the primary-side gate control, which results in a reduced SR turn-ON voltage.

The left axis of Fig. 6 shows the turn-ON voltage of the conventional and proposed control methods under various input voltage and load conditions. The right axis of the Fig. 6 shows the $\triangle V_{\mathrm{ON}}{}^2$, which is as (14). Since the switch turn-ON loss is proportional to the squared turn-ON voltage, $\triangle V_{\mathrm{ON}}{}^2$ shows the tendency of the reduced SR turn-ON loss. In the conventional

TABLE II
COMPARISON OF THE PROPOSED CONTROL METHOD WITH THE PREVIOUS STUDIES

		Conventional control [6]	[7]	Proposed control
Input Current Ripple		Large	NZR level	NZR level
Control and Implementation Complexity		Simple	Complex (Requires additional sensing circuits or LUT)	Simple
Switching Loss	Primary-side Switches	Large (2 of 4 switches achieve ZVS)	Small (4 of 4 switches achieve ZVS)	Large (2 of 4 switches achieve ZVS)
	Secondary-side SRs	Large	Largest (SR turns-on twice)	Small (Reduced SR turn-on voltage)
Versatility		Wide	Limited	Wide

method, the voltage across the SR charges steeply before the turn-ON due to the increased dc reference voltage of the sinusoidal resonance. Meanwhile, in the proposed method, SR turns ON during the continued sinusoidal resonance of mode 1. SR turn-ON voltage of the proposed method ranges between the minimum to maximum value of the sinusoidal resonance voltage. Thereby, it is inconsistent upon the load variation. However, the SR turn-ON voltage of the proposed method is always lower than that of the conventional method at the entire load condition, as shown in Fig. 6. As a result, the reduced SR turn-ON voltage of the proposed method improves the overall efficiency.

E. Comparison With the Previous Studies

Comparison of the proposed control method with the previous research [6], [7] is summarized in Table II. Implementation of the conventional control method [6] is simple, but significant input current ripple and turn-ON switching loss occurs. Lee et al. [7] achieved NZR input current and ZVS of the primary-side switches through additional backward duty ratio (D_{BW}) of SRs. However, realization of D_{BW} requires additional sensing circuits or LUT, resulting in complex control and increased cost. Complex control and additional turn-ON of SR limits the versatility of [7]. Furthermore, switching loss and gate driving loss of SRs increases. Since the proposed control method only changes the fixed duty ratio of the primary-side switches, it can achieve NZR input current without complex control, thus, no additional sensing circuits or LUT is required. It can be easily applied to PWMR converters with various types of rectifiers [9], [10]. Moreover, the efficiency can be improved through the SR turn-ON voltage reduction feature. Thereby, the proposed control method is the most simple and effective solution for the PMWR converters in fuel cell applications.

III. VERIFICATION

A. Implementation of the Proposed Control Method

Fig. 7 shows the control block diagram of the conventional and the proposed control method. Both methods utilize the fixed primary-side duty ratio (D_1–D_4), and the output power is regulated with the SR duty ratio (D_{sec}). The only difference between the two control methods is the fixed duty ratio of the primary-side switches. Considering the dead time, the conventional method operates all four switches (Q_1–Q_4) with a fixed ($0.5 - T_d/T_s$) duty ratio, Meanwhile, in the proposed method, the low-side switches (Q_2, Q_4) operate with a fixed 0.5 duty ratio, and the high-side switches operate with a fixed ($0.5\text{-}2T_d/T_s$) duty ratio. Since the T_d and T_s are determined at the design stage in prior, the proposed control method does not require additional sensing circuits, calculations, or look-up table for implementation.

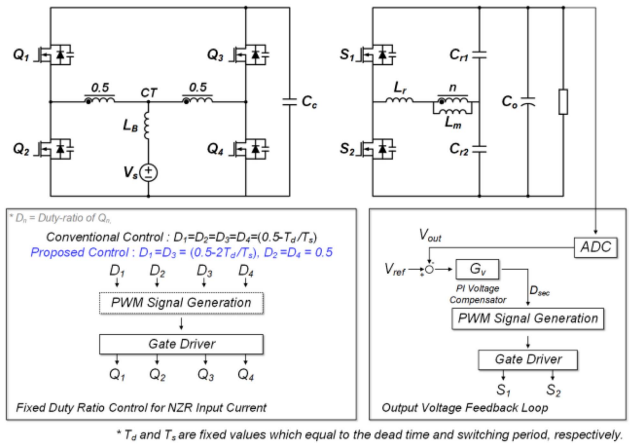


Fig. 7. Control block diagram of the conventional control method [6], and the proposed control method.

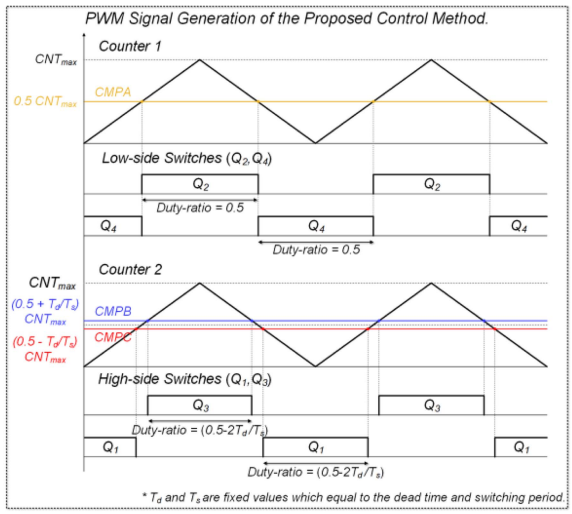


Fig. 8. Primary-side gate signal implementation of the proposed control method.

The primary-side gate signals and the output voltage feedback loop are implemented through the TMS32028069 microcontroller. Fig. 8 shows the detailed implementation method of the primary-side gate signals. Two counters (Counter 1, Counter 2)

TABLE III
PROTOTYPE DESIGN PARAMETERS

	IBI-PWMR Converter	CFPPI-PWMR Converter
Switch (Q_1-Q_4)	Infineon IPP075N15N	
SR Switch (S_1-S_2)	ROHM SCT3060AL	
Boost Inductor	CH330060 (63.04 μH, 64.97 μH)	CH236125 (33.93 μH)
Transformer	PQ4040 (L_m = 787.4 μH, 12:22)	PQ4040 (L_m = 787.4 μH, 6:6:22)
Resonant Inductor (L_r)	PQ2625 (35.96 μH, 16 Turns)	
Resonant Capacitor (C_{r1},C_{r2})	147 nF x 2ea	

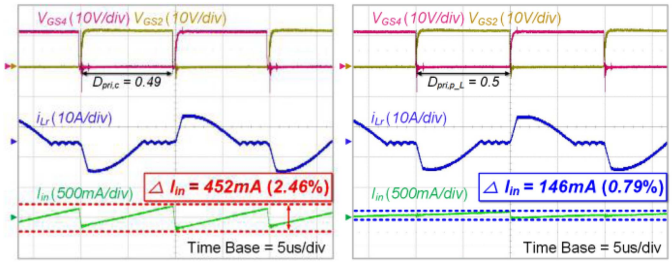


Fig. 9. Experiment key waveforms under 45 V input 600 W condition in CFPPI-PWMR converter. (a) Conventional control [6]. (b) Proposed control.

and three compare values (CMPA, CMPB, CMPC) are utilized. The maximum value of the counter ($CNT_{\max}$) is set to meet the switching frequency (50 kHz) and CMPA, CMPB, and CMPC are set to $0.5CNT_{\max}$, $(0.5 + (T_d/T_s))\cdot CNT_{\max}$ and $(0.5 - (T_d/T_s))\cdot CNT_{\max}$, respectively. Gate signals for the low-side switches are generated by comparing Counter 1 with CMPA, and the gate signals for the high-side switches are generated by comparing Counter 2 with CMPB and CMPC.

B. Experiment Results

To verify the effectiveness of the proposed control method, a 600 W CFPPI-PWMR converter was tested under the conditions of 35–45 V input, 380 V output voltage, 50 kHz switching frequency, and 200 ns deadtime. Since the proposed control method can also be applied to the IBI-PWMR converter [6], it was also verified under the same experiment condition. Conventional [6] and proposed gate control methods are tested under the same prototype design based on Table III.

Fig. 9 shows the experiment waveforms of the conventional and proposed control methods. The fixed duty ratio of the primary-side switches in the conventional method ($D_{pri,c}$) is 0.49. The fixed duty ratio of the high-side switches (D_{pri,p_H}) and the low-side switches (D_{pri,p_L}) in the proposed control method is 0.48 and 0.5, respectively. In both control method, the fixed duty ratio does not vary upon the entire operating conditions. As shown in Fig. 9(a), an input current ripple of conventional method occurs due to an unsynchronized V_{DS} transition during dead time. Under full load condition with 45 V input, 452 mA (2.46%) input current ripple occurs. On the other hand, as shown in Fig. 9(b), the proposed method mitigates the input current ripple and achieves the NZR input current. Under full load condition with 45 V input, the input current ripple is reduced to 146 mA (0.79%). Since high-side switches achieve ZVS and low-side switches turn ON with hard-switching, a slight difference in V_{DS} discharging time results in a remained input current ripple. However, more than 67% of the input current ripple is reduced by the proposed control method.

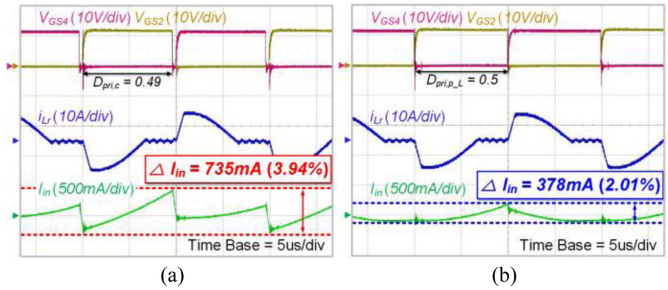


Fig. 10. Experiment key waveforms under 45 V input 600 W condition in IBI-PWMR converter. (a) Conventional control [6]. (b) Proposed control.

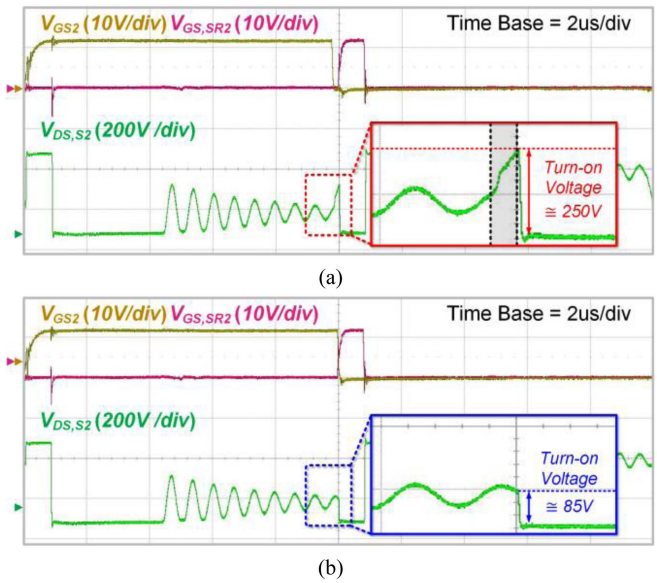
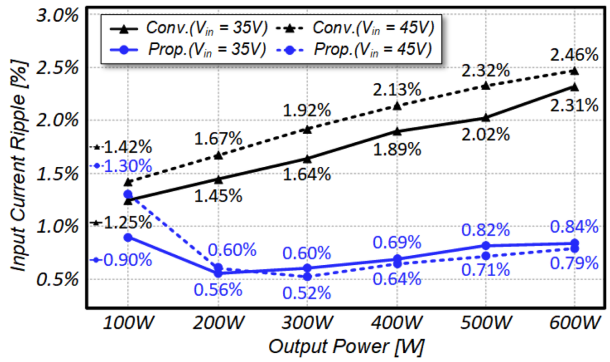


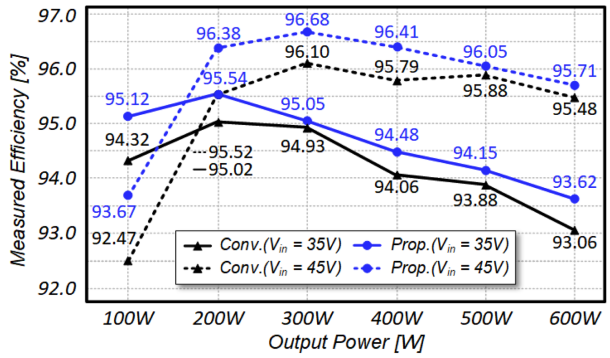
Fig. 11. Experiment key waveforms for SR turn-ON voltage comparison in CFPPI-PWMR converter. (a) Conventional control [6]. (b) Proposed control.

The proposed method was also effective on the IBI-PWMR converter. Under full load conditions with 45 V input, the input current ripple is reduced from 735 mA (3.94%) to 378 mA (2.01%), as shown in Fig. 10(a) and (b). The remained input current ripple is mainly due to the tolerance of the two boost inductors. However, more than 48% of the input current ripple is reduced by mitigating the effect of unsynchronized V_{DS} through the proposed method. Therefore, it was verified that the proposed method can effectively reduce the input current ripple in both PWMR converter structures.

Fig. 11 shows an experiment waveform of a conventional and proposed control method for SR turn-ON voltage comparison. As shown in Fig. 11(a), steep voltage charging occurs during



(a)



(b)

Fig. 12. Experiment results of conventional [6] and proposed control. (a) Measured input current ripple. (b) Measured efficiency.

dead time due to an increase in $V_{res,ref}$. On the other hand, as in Fig. 11(b), in the proposed method, the voltage across SR continues the resonance in the previous state due to maintained $V_{res,ref}$ during the dead time. Under 200 W load condition with 35 V input, the turn-ON voltage of SR in the conventional and proposed methods is 250 and 85 V respectively.

Fig. 12 shows the measured input current ripple and efficiency of the prototypes. The input current ripple of the proposed method peaks at the 100 W operation due to the V_{DS} discharging time difference. The V_{DS} discharging time of the high-side switches is increased, due to the small negative current for the ZVS under light load condition [8]. Nevertheless, as shown in Fig. 12(a), the proposed method was able to reduce significant amount of the input current ripple under the entire load condition.

The proposed method also achieved higher efficiency due to reduced SR turn-ON switching loss under the entire load conditions, as shown in Fig. 12(b). Even though the efficiency improvement is inconsistent due to the variation of the SR turn-ON voltage, the overall efficiency is improved by the proposed method. Consequently, the proposed method achieves lower input current ripple and higher efficiency than that of the conventional method.

IV. Conclusion

A new gate control method of PWMR converters for NZR input current is proposed in this letter. The proposed method only changes the fixed duty ratio of the primary-side switches, thereby no additional sensing circuits or LUT is required. The proposed gate control, which was verified in both the CFPPI-PWMR converter and IBI-PWMR converter, resulted in a significantly reduced input current ripple. The steep voltage charging period of SRs was also removed, which leads to reduced turn-ON loss of SRs and improved efficiency. The proposed method can further be applied to various PWMR converters [9], [10]. This simple and effective control method can be a practical and promising solution for PWMR converters in fuel cell applications.

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